



Design and implementation of the ELIQ Smart-plug system device

Master of Science Thesis in the Master Degree Programme

Embedded Electronic System Design

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CHALMERS UNIVERSITY OF TECHNOLOGY

Göteborg, Sweden, 2014

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Examiner: Per Larsson-Edefors

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[Cover: an explanatory caption for the (possible) cover picture with page reference to detailed information in this essay.]

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Abstract

The company Exibea AB plans to design and implement a new product called ELIQ Smart-plug device to help the households control the energy consumption at home more conveniently and intelligently. The expected function of the ELIQ Smart-plug device is to measure the power consumption value of the connected electrical appliance, send the measured value to the ELIQ Display Unit through RF wireless communication, switch on or switch off the power supply to the connected electrical appliance automatically and repeat the received ELIQ protocol RF message to work as a wireless repeater for other ELIQ devices in the company.

This master thesis explores the design process and the implementation method of the ELIQ Smart-plug system device including both of the hardware part and software part in depth. MSP430AFE233 is chosen to be the microcontroller unit used on the Smart-plug electrical board to control the whole system. In order to calculate the power consumption value, the RMS (Root Mean Square) values of both of the voltage and current on the connected appliance should be measured firstly, then the power consumption value will be obtained easily by multiplying the voltage RMS value and the current RMS value. The calculated power consumption value will be encoded and combined with some other specified bits such as preamble bits and header bits together into a data packet according to the ELIQ protocol. The data packet will be transmitted to the RF module on the Smart-plug electrical board through SPI communication firstly, then the wireless communication between the antenna of this RF module and the antenna of another RF module on the ELIQ Display Unit board will be implemented. The power consumption value will be displayed on the ELIQ Display Unit device to show the households the transient power consumption of the connected electrical appliance. The Smart-plug device can also switch on or switch off the power supply to the appliance automatically according to the measured power consumption value to achieve the aim of energy-saving in a house. In addition, this Smart-plug device system can repeat the received RF message from other ELIQ devices and then send the same RF message to the ELIQ Display Unit or the ELIQ Hub to work as a wireless repeater in order to extend the wireless transmission distance and amplify the power of the signal.

Furthermore, the comparison of selecting components for the Smart-plug electrical board and some important attentions need to be considered in both of the hardware design and software design are discussed in this master thesis.

The ELIQ Smart-Plug Design

Acknowledgement

It is my pleasure to show my gratitude towards everyone who supported me during my master thesis.

Firstly, I would like to thank the company Exibea AB for offering this master thesis opportunity and especially Hakan Ludvigsson who was my supervisor at the company. He is very pleasant to work with. He provided me a good working environment and helped a lot about the component selection and producing the PCB board. Also I would give thanks to Olof Hartelius and Johan Salin at the company who were available for answering my questions and shared many technical knowledge and experience with me together.

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Finally, I also appreciate for the effort that my master thesis opponent, Gongpei Cui made. His criticism and questions opened my eyes for the weak points in my master thesis.

The ELIQ Smart-Plug Design

List of Abbreviations

- AC Alternating Current
- ACLK Auxiliary Clock
- A/D Analog to Digital
- ADC Analog to Digital Converter
- BCSCTLx Basic Clock System Control Register x
- CPU Central Processor Unit
- CS Chip Selection
- DC Direct Current
- DCO Digitally Controlled Oscillator
- EDA Electronic Design Automation
- FIFO First Input First Output
- FSR Full Scale Range
- GDO General Digital Output
- GFSK Gaussian Frequency-Shift Keying
- GIO General Input/Output
- GO General Output
- GUI Graphic User Interface
- I/O Input or Output
- ISR Interrupt Service Routine
- ISM Industrial, Scientific and Medical
- JTAG Joint Test Action Group
- LED Light Emitting Diode
- MCLK Main System Clock
- MCU Microcontroller Unit
- MSP Mixed Signal Processor
- NPN transistor Negative-Positive-Negative Transistor
- OSR Oversampling Ratio
- PCB Printed Circuit Board
- PWM Pulse Width Modulation
- PxDIR Px Direct Register
- PxIE Px Interrupt Enable Register
- PxIES Px Interrupt Edge Select Register
- PxIFG Px Interrupt Flag Register
- PxIN Px Input Register
- PxOUT Px Output Register
- PxREN Px Pullup/Pulldown Resistor Register
- RAM Random Memory
- RF Radio Frequency
- RISC Reduced Instruction Set Computer
- RMS Root Mean Square
- RX Receive, Receive Mode

- SCLK Serial Clock
- SD24_A A/D Converter 24-bit sigma-delta Analog to Digital Converter
- SD24CTL SD24 Control Register
- SD24INTCTLx SD24 Channel x Input Control Register
- SD24CCTLx SD24 Channel x Control Register
- SD24MEMx SD24 Channel x Conversion Memory Register
- SI Serial Input
- SMCLK Sub Main System Clock
- SMD Surface Mounted Device
- SO Serial Output
- SPI Serial Peripheral Interface
- SPST Single Pole Single Throw
- SRAM Static Random Memory
- TACCRx Timer_A Capture/Compare Register x
- TACCTLx Timer_A Capture/Compare Control Register x
- TACTL Timer_A Control Register
- TAR Timer_A Counter Register
- TX Transmit, Transmit Mode
- UART Universal Asynchronous Receiver/Transmitter
- USART Universal Synchronous/Asynchronous Receiver/Transmitter
- USB Universal Serial Bus
- VCO Voltage Controlled Oscillator
- WDT Watchdog Timer
- WWF World Wide Fund for Nature
- XTAL Crystal

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1. Introduction

1.1 Background

Over the last decade, energy saving has been a hot topic across the whole world. Households always find it difficult to plan and handle their energy consumption at home. Unnecessary use of energy is not only an environmental issue but also affects the economy negatively for the consumers.

The company Exibea AB was founded in 2008 in Gothenburg, Sweden, with a focus on providing products to help the consumers to control and reduce their energy consumption. Now the company is planning to design and implement a new product called ELIQ Smart-plug device. This device is expected to detect the energy use and display the measured value on the company's flagship products ELIQ Energy Display Unit or ELIQ Energy Online to provide feedback to the consumers [1][2]. The Smart-plug device will be inserted between the power outlet and any household appliance to measure the energy use and switch on/off the power supply to the connected appliance, which can be also controlled by the user from the ELIQ Energy Online web GUI or the remote mobile phone, allowing the user to set up power on/off scheduling based on the current electricity price, room temperature or other parameters to help facilitating a more energy-conservative lifestyle.

1.2 Problem statement

Energy consumption in the world is on the rise, leading to a non-sustainable society in the long run. Lack of energy is a serious challenge for human beings in the future. Today the government in almost every country formulates a strategy to reduce the energy consumption in every field of the society. It is not only a matter for governments, but also boils down to a matter for every citizen of Earth: We all have the responsibility to save the electric energy in daily life in order to provide an ecological and sustainable society [3] for the coming generations.

Although electricity does not create any pollution where it is used, there may be carbon dioxide emission and other environmentally negative substances coming out at the production site. The WWF (World Wide Fund for Nature) states that if the carbon dioxide emission is kept on the same level as today, the global temperature will increase two degrees Celsius, which will lead to the severe global warming crisis and then a series of natural disasters in the world [4]. Wind power and hydropower almost do not produce any carbon dioxide emission, however, they can still create other negative environmental problems such as the disrupted water flows.

In order to create an ecological society, the electricity energy consumption of households is an important concern. Household energy consumption accounts for about 25% of the total energy consumption in the world [5]. One of the effective ways to decrease electricity energy consumption in households is by increasing consumers' awareness as people at least in the past have been careless about lowering electricity energy consumption even though lowering

electricity energy consumption could reflect well on their household budget.

Taking steps towards achieving the ecological and smart home, the new product ELIQ Smart-plug device which the company Exibea AB plans to develop is expected to manage home electricity energy consumption. This Smart-plug device system can provide functions such as measurement and visualization of the home energy consumption and automatic switch on/off control for home electrical appliances. In addition, it can be also connected to the network of a smart home to achieve efficient ecological operation.

Since the envisioned Smart-plug device is a new concept, this master thesis project work is concerned with conceiving, implementing, integrating and evaluating a Smart-plug device based on the different off-the-shelf subcomponents.

1.3 Specification

The ELIQ Smart-plug device should provide the following functions:

- Measure the power consumption value of the connected appliances and send the value once every 15 seconds to the ELIQ Energy Display Unit or the ELIQ Energy Online web GUI through the ELIQ Hub to display to the households with using the RF-module in 868 MHz ISM band
- Switch on/off power supply to the connected appliances according to the measured power consumption value or by the user from the ELIQ Energy Online web GUI and indicate on/off status
- Repeat received ELIQ protocol RF communication, making the device work as a wireless extender or repeater for other ELIQ devices

1.4 Purpose

With the measurement and visualization of the home energy consumption by using this Smart-plug device system, the households can know the energy consumption value in a room instantly and directly then can manage the energy use of the house easily and conveniently. The automatic switch on/off control for the home appliances can achieve the automatic reduction of the household energy consumption. The hope is that with the help of this Smart-plug device system, household energy consumption can be lowered significantly, leading to not only better household economy but also to a sustainable society.

1.5 Subcomponents

The subcomponents the company has access to in this project are resistors, capacitors, diodes, relay, switching power supply device, ferrite beads, transient voltage suppressor, NPN transistor, crystal, fuse, varistor, LED, MCU, RF module, PCB board, plug and so on. The PCB board will be manufactured by the PCB factory according to the designed circuit drawn by the specified EDA software tool then the electrical subcomponents will be soldered on the PCB board. The Smart-plug board will be connected to a plug to be inserted between the power outlet and the

household appliance. The tools multimeter, soldering iron and soldering tin will be used to implement integrating these different off-the-shelf subcomponents into one testing product.

1.6 Project procedure

The electrical board of the Smart-plug device should be designed and implemented for testing before the products in mass production, including both hardware design and software design. For the hardware part, the electrical circuit design including the prototyping design and the selection of the MCU and other suitable off-the-shelf components should be completed firstly. Then the schematic and the PCB layout will be done by the specialized EDA tool. After the PCB board is produced by the factory, soldering the components on the PCB board will be the following step. The software task is to make programming for the MCU on the Smart-plug board to make the Smart-plug device achieve the expected targets successfully.

1.7 Scope

The knowledge of this master thesis is related to the fields of analog circuit, digital circuit, A/D mixed signal system, microcontroller unit, C code programming and wireless communication.

1.8 Limitations

There are some parts of this master thesis project left out due to the time reason. For instance, the power supply circuit that drives the MCU, the RF module and the relay will not be designed within this master thesis project work. Instead, a switching power supply device which can transfer the 230V AC input from the mains to the 3.3V DC output to be the working supply voltage is bought as the off-the shelf subcomponent. Since this temporary switching power supply device is quite expensive and bulky, the final product in mass production will need a different power solution on the Smart-plug electrical board to reduce cost and size. Secondly, the wireless communication between the Smart-plug board and the ELIQ Energy Unit board or the ELIQ Energy Hub does not need to be considered since this procedure is already done by the company Exibea AB according to the company's own RF protocol. In addition, on the ELIQ Energy Unit board, the procedure of decoding received data packet and displaying the value on the LCD display needs not to be mentioned as it has been also completed by the company.

Furthermore, the size, the exterior, the package, the manufacture, the process technology and the arts and crafts of the final product have also not been considered as the aim of this master thesis project is just designing a prototype.

1.9 Thesis outline

Chapter 2 introduces the theory of the basic design principle firstly, then the selection of the suitable type of MCU and the basic knowledge of the selected MCU are described in detail. That is vital for the readers to understand the following electrical circuits design and configurations in software. Then, chapter 3 introduces the materials used in this project, including both of the

hardware tools and software tools. In chapter 4, the specific methodology of the hardware design is elaborated. The software methodology design including the software design process flowchart, the system setup initiation and the implementation of some special applications are described step by step in chapter 5. Some important graphs such as the schematic of the whole electrical circuits inside the Smart-plug device, the PCB layout of the Smart-plug electrical board and the real photo of this electrical board are presented to be the visual support for this master thesis in chapter 6. Chapter 7 will show the results of this project to the readers. In chapter 8, some issues such as the comparison of suitable selection for the control unit component or some conditions need be considered during the design will be discussed. Finally, in chapter 9, the findings and insights from this project will be reviewed overall.

2. Theory

2.1 Basic design principle

The basic design principle diagram of the Smart-plug device system is shown in Figure 2.1 below.

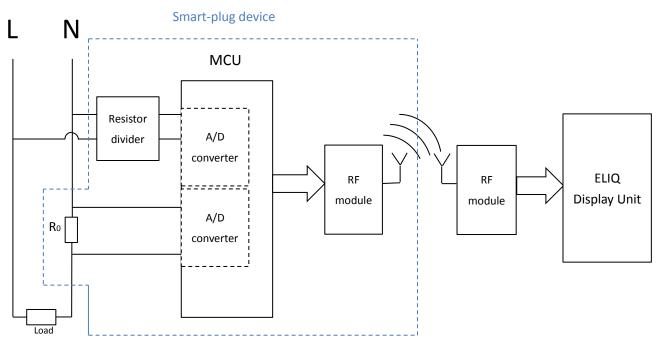


Figure 2.1 The diagram of the basic design of the Smart-plug system

As can be seen from Figure 2.1 above clearly, L means the live wire and N means the neutral wire from the household mains respectively. As the Smart-plug device needs to measure the power consumption value of the electrical appliance, the value of the current on the live wire and neutral wire of the circuit inside the smart-plug can be measured firstly in order to calculate the power consumption. R0 is a resistor with small resistance value set on the neutral wire of the circuit as the sampling resistor. The voltage value on R0 can be measured by connecting both sides of the resistor to the A/D converter module of the MCU. If the voltage on R0 is known, then the current value on the electrical appliance is easy to obtain by dividing the R0 resistance value. Load means the load resistor of the electrical appliance connected to the Smart-plug device. The voltage on the electrical appliance can also be measured by the A/D converter module of the MCU. The resistor divider circuitry needs to be added between Live, neutral wire and the MCU since the A/D converter of the MCU can only be convert small voltage values.

After sampling signal values during a specific time interval, both of the current effective value and voltage effective value on the electrical appliance can be calculated using the sampled value captured from the A/D converter, then the power consumption value can be calculated by multiplying the effective voltage value and the effective current value. The power consumption value will be transmitted to the ELIQ Display Unit via the respective RF module on both of the Smart-plug board and the ELIQ Energy Display Unit board.

In European countries, the voltage from the household mains is 230V AC. Since this Smart-plug device is designed mainly for the market of the European countries, the design of the circuit is based on the mains voltage equals to 230V AC. As the effective voltage value 230V from the mains in European countries is almost highest among that across the world, the hardware circuit design discussed in the later chapters will be also suitable for use in other regions outside Europe.

2.2 Selection of MCU

A series of considerations are necessary to choose the type of MCU. As the product size limitation and thermal regulation needs to be considered, the Texas Instruments MSP430 series ultra-low-power microcontrollers are the first choice for the company since these types of MCU possess the features of small size and ultra-low-power [6].

Initially, the MSP430F21x2 family MCUs, the MSP430G2x33 family MCUs and the MSP430AFE2x3 family MCUs have been considered to be the selections of the control MCU on the Smart-plug electrical board in this project. Since the voltage from the household mains is alternating from outside, the voltage on the sampling resistor is also alternating. The A/D converter in many types of MCU such as the MSP430F21x2 family MCUs and the MSP430G2x33 family MCUs can only detect the positive voltage value and the reference voltage on the A/D module is also positive value as same as the supply voltage. If choosing these types of MCU, the voltage polarity switching circuit need be added between the sampling resistor and MCU in order to do the voltage bipolar-unipolar conversion. The MSP430AFE2x3 family MCUs have the different analog-to-digital converters system can be input a pair of analog values. The differential value of the pair will be processed by the SD24_A A/D converter. Therefore, if choosing the MSP430AFE2x3 family MCUs, the AC signals can be interfaced directly without the need of voltage bipolar-unipolar conversion.

The analog-to-digital converters in the MSP430F21x2 family MCUs and the MSP430G2x33 family MCUs can only transfer the analog decimal data to the 10 bits digital binary data, however, the MSP430AFE2x3 family MCUs with the SD24_A modules can transfer the analog decimal data to the 16 bits digital binary data. That means the MSP430AFE2x3 family MCUs can implement the analog-to-digital conversion much more accurately than the MSP430F21x2 family MCUs and the MSP430G2x33 family MCUs with extremely higher resolution and smaller interval between each adjacent transferred digital binary data.

Thus, the MSP430AFE2x3 family MCUs are the better selections for this project. Among the different types of MCUs in the MSP430AFE2x3 family, in the overall consideration of the price, the size, the power dissipation, the flash memory size, the SRAM memory size, the number of ADC channels and the resolution of the ADC converter, the type MSP430AFE233 is chosen to be the working microcontroller unit on the Smart-plug electrical board.

2.3 Introduction of MSP430AFE233

2.3.1 Description

MSP430AFE233 is a type of mixed signal ultra-low-power microcontroller which consists of several devices featuring different sets of peripherals targeted for various applications [6]. The architecture is optimized to achieve extended battery life in portable measurement applications. The CPU inside this MCU is a 12MHz 16-bit RISC CPU including sixteen 16-bit registers and constant generators that contribute to maximum code efficiency [6]. Three independent 24-bit sigma-delta A/D converters, one 16-bit timer, one 16-bit hardware multiplier, one USART communication interface, one watchdog timer and eleven I/O pins are also integrated in this device.

2.3.2 Features

There are the basic features of MSP430AFE233 [6]:

- Low supply voltage range: 1.8 V to 3.6 V
- Ultra-low power consumption

 -Active mode: 220 μA at 1 MHz, 2.2 V
 -Standby mode: 0.5 μA
 -Off mode (RAM retention): 0.1 μA
- Five power-saving modes
- Ultra-fast wake-up from standby mode in less than 1 μs
- 16-Bit RISC Architecture, up to 12-MHz system clock
- Basic clock module configurations

 Internal frequencies up to 12 MHz
 Internal low-power low-frequency (LF) oscillator
 High-frequency (HF) crystal up to 16 MHz
 Resonator
 - -External digital clock source
- Basic clock module configurations
- Three 24-bit Sigma-Delta Analog-to-Digital (A/D) converters with differential programmable gain amplifier inputs
- 16-bit Timer A with three capture/compare registers
- Serial communication interface (USART), Asynchronous UART or Synchronous SPI selectable by software
- 16-bit hardware multiplier
- Serial onboard programming, no external programming voltage needed programmable code protection by security fuse
- On-chip emulation module

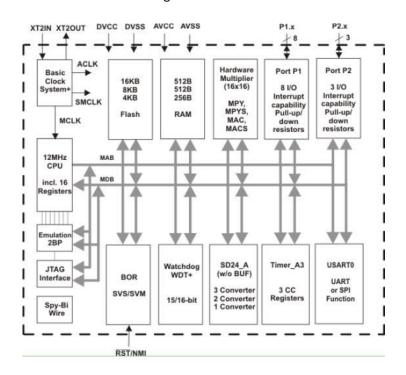


Figure 2.2 below shows the functional diagram of MCU MSP430AFE233.

Figure 2.2 The functional diagram of MSP430AFE233 [7]

Figure 2.3 below shows the pin designation of MCU MSP430AFE233. The MSP430AFE233 has 24 pins totally.

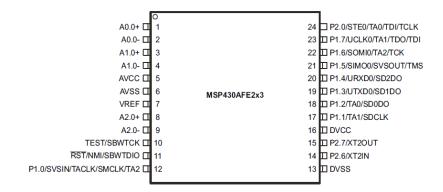


Figure 2.3 The pin designation of MSP430AFE233 [7]

2.3.3 Digital I/O ports

MSP430AFE233 has two I/O ports, P1 and P2. P1 has 8 pins, P1.0 to P1.7, P2 has 3 pins, P2.0, P2.6 and P2.7. Each I/O pin can be individually configured in software for input or output direction and each I/O line can be individually read or written [8].

The digital I/O ports have interrupt capability and each interrupt for the P1 and P2 I/O lines can be enabled individually [8]. The P1 and P2 I/O lines can be configured to be provided an interrupt by the rising edge or falling edge of an input signal [8]. Each I/O port pin contains the independent input and output registers and the individually configurable pullup or pulldown resistors.

2.3.3.1 Digital I/O ports input register PxIN

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function [8]. When the bit is set to be "0", the input signal to the corresponding I/O pin is low; when the bit is set to be "1", the input signal to the corresponding I/O pin is high.

2.3.3.2 Digital I/O ports output register PxOUT

If the pullup/pulldown resistor of the corresponding pin is disabled by the PxREN register, the pin is configured as I/O function, and the bit in each PxOUT register will reflect the value of the output signal at the corresponding I/O [8]. When the bit is set to be "0", the output signal from the corresponding I/O pin is low; when the bit is set to be "1", the output signal from the corresponding I/O pin is high.

If the pullup/pulldown resistor of the corresponding pin is enabled by the PxREN register, the corresponding bit in the PxOUT register will select whether the pullup resistor or pulldown resistor is used [8]. When the bit is set to be "0", the pin is pulled down; when the bit is set to be "1", the pin is pulled up.

2.3.3.3 Digital I/O ports direction register PxDIR

Each bit in each PxDIR register will select the direction of the corresponding I/O pin [8]. When the bit is set to be "0", the corresponding pin is set to be input direction; when the bit is set to be "1", the corresponding pin is set to be output direction.

2.3.3.4 Digital I/O ports pullup/pulldown resistor enable

register PxREN

Each bit in each PxREN register can enable or disable the pullup/pulldown resistor of the corresponding I/O pin [8]. When the bit is set to be "0", the pullup/pulldown resistor of the corresponding I/O pin is disabled; when the bit is set to be "1", the pullup/pulldown resistor of the corresponding I/O pin is enabled, in this case, the corresponding bit in the PxOUT register will select whether the pullup resistor or pulldown resistor is used.

2.3.3.5 Digital I/O ports interrupts

Each pin in ports P1 and P2 have interrupt capability, which is configured with PxIFG, PxIE and PxIES registers individually and independently [8]. PxIFG is the Px interrupt flag register, PxIE is the interrupt enable register and PxIES is the interrupt edge select register. All of the P1 pins source the single interrupt vector and all of the P2 pins source a different single interrupt vector [8].

Each PxIE bit can enable the associated PxIFG bit which is the interrupt flag for its corresponding I/O pin. When one PxIE bit of the corresponding P1 port pin or P2 port pin is set to be "0", that means the I/O interrupt is disabled at thin pin; when one PxIE bit of the corresponding P1 port pin or P2 port pin is set to be "1", that means the I/O interrupt is enabled at thin pin.

Each PxIES bit will select which interrupt edge is used to control the PxIFGx flag of the corresponding I/O port pin. When one PxIES bit of the corresponding P1 port pin or P2 port pin is set to be "0", the associated PxIFGx flag is set with a low-to-high transition; when one PxIES bit of the corresponding P1 port pin or P2 port pin is set to be "1", the associated PxIFGx flag is set with a high-to-low transition [8]. It is important to notice that only transitions, not static levels, cause the interrupts.

Each PxIFGx bit is set when the selected input signal edge occurs at the pin. All of the PxIFGx interrupt flags request an interrupt when their corresponding PxIE bit and the GIE bit are set at the same time [8]. Each PxIFG flag must be reset with software. In addition, software can also set each PxIFG flag to generate a software initiated interrupt [8]. When one PxIFGx bit of the corresponding P1 port pin or P2 port pin is set to be "0", that means there is no interrupt pending at this port pin; when one PxIFGx bit of the corresponding P1 port pin or P2 port pin is set to be "1", that means there is an interrupt pending at this port pin.

2.3.4 Basic clock module

2.3.4.1 Basic clock module structure

Figure 2.4 below shows the internal hardware structure of the basic clock module inside MCU MSP430AFE233.

Design and implementation of the ELIQ Smart-plug device system

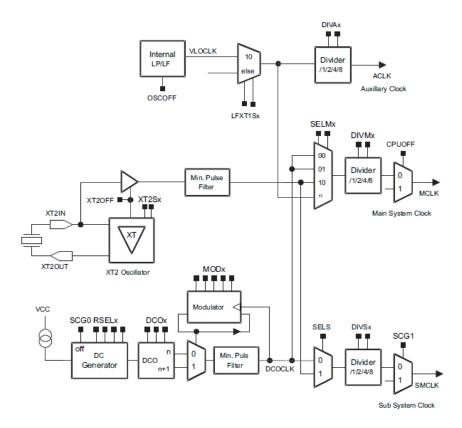


Figure 2.4 The internal structure of the basic clock module in MSP430AFE233 [8]

2.3.4.2 Basic clock module registers

There are a series of registers in the basic clock module. The initial state of the internal circuits of the basic clock module needs to be set by configuring each bit of these registers firstly to determine the working clock for the task executed in the MCU when the system starts working.

In BCSCTL1, the basic clock system register 1, the XT2OFF bit which occupies bit 7 is used to choose whether the XT2 oscillator is turned on or turned off. If XT2OFF bit equals to "0", XT2 oscillator is turned on; if XT2OFF bit equals to "1", XT2 oscillator is turned off. Since XT2CLK needs to be used for MCLK and SMCLK, the XT2 oscillator should be turned on by clearing the XT2OFF bit.

Table 2.1 below shows the function	of each bit in the BCSCTL1 register.
Tuble 2.1 below shows the function	of each bit in the bescret register.

7	6	5	4	3	3 2 1 0				
XT2OFF	XTS	DI\	/Ax	RSELx					

Table 2.1 The function of each bit in the BCSCTL1 register [8]

In BCSCTL2, the basic clock system register 2, the SELMx bits which occupy bit 7 and bit 6 are used to select the clock source for the MCLK. The SELS bit which occupies bit 3 is used to select clock source for the SMCLK. The DIVMx bits which occupy bit 5 and bit 4 will determine the value

of the divider ratio for the MCLK. Similarly, the DIVSx bits which occupy bit 2 and bit 1 will determine the value of the divider ratio for the SMCLK. Table 2.2 below shows the function of each bit in the BCSCTL2 register.

7 6		5	4	3	2	1	0
SELMx		DIV	′Mx	SELS	DIV	/Sx	DCOR

Table 2.2 The function of each bit in the BCSCTL2 register [8]

In BCSCTL3, the basic clock system register 3, the XT2Sx bits which occupy bit 7 and bit 6 are used to select the frequency range for the XT2 clock. Table 2.3 below shows the function of each bit in the BCSCTL3 register.

7	6	5	5 4		3 2		0
	XT2Sx		T1Sx	XCAPx		XT2OF	LFXT1OF

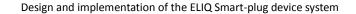
Table 2.3 The function of each bit in the BCSCTL3 register [8]

2.3.5 Timer_A

In the MCU MSP430AFE233, Timer_A is a 16-bit timer/counter with multiple capture/compare registers. The 16-bit timer/counter can be chosen to work in four different operating modes. Timer_A has a selectable clock source and configurable PWM outputs. It also has extensive interrupt capabilities. The interrupts can be generated from the overflow condition of the counter or from the capture/compare registers.

2.3.5.1 Timer_A structure

Figure 2.5 below shows the internal hardware structure of the Timer_A module inside MCU MSP430AFE233.



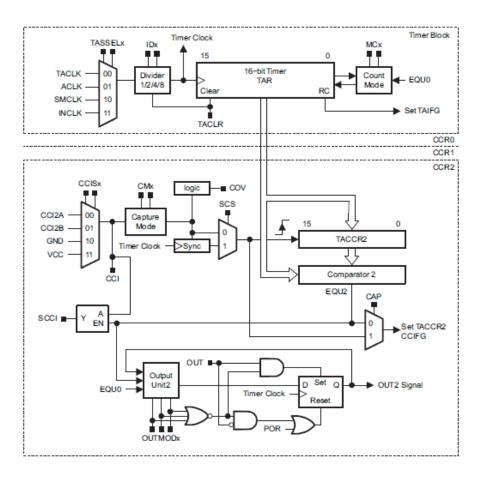


Figure 2.5 The internal structure of Timer_A in MSP430AFE233 [8]

2.3.5.2 Timer_A registers

There are also some registers in the Timer_A module. Each bit of these registers needs to be configured firstly to give the initial state of the circuits inside the Timer_A module when the system starts working.

Table 2.4 below shows the function of each bit in TACTL, the Timer_A control register. The TASSELx bits which occupy bit 9 and bit 8 will select the Timer_A clock source from TACLK, ACLK, SMCLK or INCLK. The IDx bits which occupy bit 7 and bit 6 will select the ratio of the divider to divide the frequency of the input clock signal from the Timer_A clock source. The MCx bits which occupy bit 5 and bit 4 will be used to choose which operating mode for the Timer_A to work with from the up mode, the continuous mode or the up/down mode. The TACLR bit which is bit 2 of the TACTL register is used to clear both of the count value in the TAR register and the ratio value of the timer clock divider. The TAIE bit which is bit 1 of the TACTL register is used to enable the Timer_A interrupt. The TAIFG bit which is bit 0 of the TACTL register is the Timer_A interrupt flag bit.

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15	14	13	12	11	10	9	8		
	unused								

7	6	5	4	3	2	1	0
IDx		М	Сх	unused	TACLR	TAIE	TAIFG

Table 2.4 The function of each bit in the TACTL register [8]

Table 2.5 below shows the function of each bit in TAR, the Timer_A register. The 16-bit count value of Timer_A is stored into the TAR register, which occupies every bit of the TAR register.

TARx	15	14	13	12	11	10	9	8

7	6	5	4	3	2	1	0			
	TARx									

 Table 2.5 The function of each bit in the TAR register [8]

Table 2.6 below shows the function of each bit in TACCRx, the Timer_A capture/compare register x. Whether the compare mode or the capture mode is used can be chosen by the CAP bit in the TACCTLx register. If choosing the compare mode, the data stored into the TACCRx register will be compared with the count value in the Timer_A register. If choosing the copied into the TACCRx register when a capture is performed.

15	14	13	12	11	10	9	8		
TACCRx									
7	6	5	4	3	2	1	0		

TACCRx Table 2.6 The function of each bit in the TACCRx register [8]

Table 2.7 below shows the function of each bit in TACCTLx, the capture/compare control register x. The CAP bit which occupies bit 8 is used to choose whether the compare mode or the capture mode is employed for the TACCRx register. The CCIE bit which occupies bit 4 is to enable the capture/compare mode. The CCIFG bit which is bit 0 is the capture/compare interrupt flag bit.

15	15 14 13			11	10	9	8
CMx		CC	ISx	SCS	SCCI	unused	CAP
7	6	5	4	3	2	1	0
OUTMODx			CCIE	CCI	OUT	COV	CCIFG

 Table 2.7 The function of each bit in the TACCTLx register [8]

2.3.6 SD24_A

2.3.6.1 SD24_A structure

The MSP430AFE233 has three multichannel 24-bit sigma-delta analog-to-digital converters. Figure 2.6 below shows the internal structure of the multichannel SD24_A analog-to-digital converters inside the MCU MSP430AFE233. There are eight fully differential multiplexed analog input pairs in each converter channel. Among the eight fully differential analog input pairs, A0 to A5 are used to accept the external input analog signal. A5 is used to measure the working supply voltage for the MCU with the resistive divider circuitry and A6 is used to measure the room temperature by connecting a temperature sensor inside the MCU. The analog input module is followed by the second-order oversampling sigma-delta modulator and the digital decimation filter. The input analog differential value will be converted to a 1 bit data stream by the single-bit comparator with the modulator frequency fM which can reach 1.1MHz inside the second-order sigma-delta modulator.

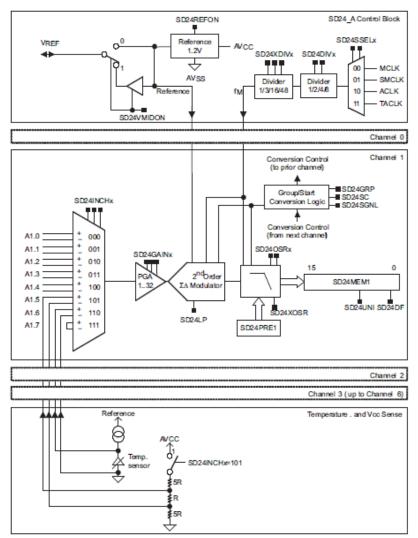


Figure 2.6 The internal structure of the multichannel SD24_A analog-to-digital converters [8]

2.3.6.2 SD24_A registers

There are a series of registers inside the SD24_A module. These registers also need be configured in software before the task starts.

Table 2.8 below shows the function of each bit in SD24CTL, the SD24 control register. The SD24SSELx bits which occupy bit 5 and bit 4 will select the clock source from MCLK, SMCLK, ACLK or external TACLK. Both of the SD24XDIVx bits which occupy bit 11 and bit 10 and the SD24DIVx bits which occupy bit 7 and bit 6 can divide the clock to generate the modulating frequency f_M for the sigma-delta modulator together. The SD24REFON bit which occupies bit 2 is used to select whether the on-chip reference voltage 1.2 V is turned on or turned off for each SD24_A channel by setting SD24REFON = "1" or SD24REFON = "0".

15	14	13	12	11	10	9	8
	rese	rved		SD24XDIVx			SD24LP
							_

7	6	5	4	3	2	1	0
SD24DIVx SD24SSELx			SSELx	SD24VMIDON	SD24REFON	SD24OVIE	reserved

Table 2.8 The function of each bit in the SD24CTL register [8]

Table 2.9 below shows the function of each bit in SD24INTCTLx, the SD24 channel x input control register. The SD24INCHx bits which occupy bit 2, bit 1 and bit 0 will select which differential input pair to be used in the corresponding SD24_A channel. The SD24GAINx bits which occupy bit 5, bit 4 and bit 3 are used to choose the gain value of the preamplifier for the differential input AC signal from 1, 2, 4, 8, 16 or 32 before the differential input AC signal coming into the 2nd sigma-delta modulator. The SD24INTDLYx bits which occupy bit 7 and bit 6 are used to choose how many samples delay for the first interrupt after the analog-to digital conversion starts. The software variable will read the converted value from the SD24MEMx register in the SD24 interrupt service routine every time the SD24_A interrupt triggers. It needs to consume some time to get the digital result from the analog-to-digital conversion, when the first interrupt generates immediately just after the analog-to-digital conversion starts, the software variable will read the conversion. Thus, adding this interrupt delay between the analog-to digital conversion and make the software work more stably.

7	6	5	4	3	2	1	0
SD24II	NTDLYx		SD24GAINx			SD24INCHx	

Table 2.9 The function of each bit in the SD24INTCTLx register [8]

Table 2.10 below shows the function of each bit in SD24CCTLx, the SD24 channel x control register. The SD24UNI bit which occupies bit 12 is to select whether the bipolar mode or unipolar

mode is used to accept the input AC signal. If choosing the unipolar mode, the analog input pair in the SD24 A can only be entered into the positive signal, while the bipolar mode can deal with both of the positive signal and negative signal. The SD24XOSR bit which occupies bit 11 and the SD24OSRx bits which occupy bit 9 and bit 8 will decide the oversampling ratio together to get the sampling frequency f_s from the modulating frequency f_M for the decimation digital filter. The SD24LSBACC bit which occupies bit 6 is used to choose whether the 16 most significant bits or the 16 least significant bits of the output conversion value from the decimation digital filter will come into the SD24MEMx register. The SD24LSBTOG bit which occupies bit 7 is used to choose whether the SD24LSBACC bit will be toggled or not be toggled each time the SD24MEMx register is read by software. The SD24IFG bit which occupies bit 2 is the SD24_A interrupt flag bit, which is set every time the new conversion result data is written into the SD24MEMx register, that means the SD24_A interrupt will be triggered every time the converted data from the digital filter output is stored into the SD24MEMx register. This bit will be cleared automatically after the data in the SD24MEMx register is read by the CPU. Nevertheless, it is better that SD24IFG is cleared by using the software code every time the SD24MEMx register is read by the CPU to avoid the data confusion conflict in the small time interval. The SD24GRP bit which occupies bit 0 is used to choose whether the corresponding channel works independently in single channel mode or the corresponding channel is grouped with higher channel to work together. The SD24SNGL bit which occupies bit 10 is used to select whether the single data conversion mode or the continuous data conversion mode is selected. If choosing single conversion mode, the SD24SC bit will be cleared automatically after one analog-to-digital conversion is completed then the conversion procedure will be stopped immediately, while the conversion will continue until the SD24SC bit is cleared by software in the continuous conversion mode. After the analog-to-digital conversion in the channel is stopped, the channel will be powered down and the corresponding digital filter will be turned off. Since the value in the SD24MEMx register can change when the analog-to-digital conversion is stopped, it is better that the conversion data is read by the SD24MEMx before the SD24SC bit is cleared to avoid reading an invalid result. The SD24BUFx bits which occupy bit 14 and bit 13 are used to choose whether the high impedance input buffer is enabled or disabled in the SD24_A analog-to-digital converter. The SD24OVIFG bit which occupies bit 5 is the SD24_A overflow interrupt flag to indicate whether the SD24 A overflow interrupt is pending or not pending in the channel. The SD24DF bit which is bit 4 will choose whether the SD24_A conversion data is in offset binary format or in two's complement format by setting SD24DF = 0 or SD24DF = 1. The SD24IE bit which is bit 3 will enable the SD24_A interrupt. The SD24SC bit which is bit 1 will start the analog-to-digital conversion.

15	14	13	12	11	10	9	8
reserved	SD24	BUFx	SD24UNI	SD24XOSR	SD24SNGL	SD24	OSRx

7	6	5	4	3	2	1	0
SD24LSBTOG	SD24LSBACC	SD240VIFG	SD24DF	SD24IE	SD24IFG	SD24SC	SD24GRP

Table 2.10 The function of each bit in the SD24CCTLx register [8]

Figure 2.7 below shows the single channel operation by using the continuous conversion mode. It can be seen clearly that the conversion will continue until the SD24SC bit is cleared by software.

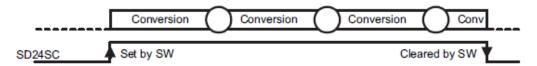


Figure 2.7 The diagram of the single channel operation using the continuous conversion mode [8]

Table 2.11 below shows the function of each bit in the SD24MEMx, the SD24_A channel x conversion memory register. This register will store the 16-bit converted digital data result from output of the digital filter. According to the value of the SD24LSBACC bit in the SD24CCTLx register, the 16 most significant bits or the 16 least significant bits of the conversion result data from the decimation digital filter output will be stored in the SD24MEMx register.

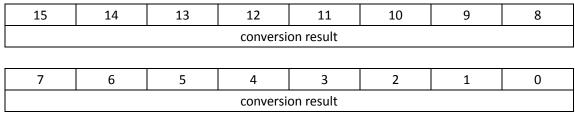


Table 2.11 The function of each bit in the SD24MEMx register [8]

2.3.6.3 Analog-to-digital conversion in SD24_A

According to the different oversampling ratios set in the decimation filter, the output value from the filter ranges from 15 bits to 30 bits. When setting the oversampling ratio equal to 256 and SD24LSBACC = "1", the output value of the digital decimation filter is 24 bits and the 16 most significant bits will come into the SD24_A conversion memory register. In the programmable gain amplifier, the value of gain can be selected from 1, 2, 4, 8, 16 or 32. The relation of the full scale input voltage range and the reference voltage is:

$$V_{FSR} = \frac{V_{REF/2}}{GAIN_{PGA}}$$
(2.1)

The resolution is :

resolution
$$\Delta = \frac{V_{FSR}}{2^{n-1}}$$
 (2.2)

Figure 2.8 below shows the relationship of the digital output value and the input analog voltage value using the bipolar mode and 2's complement data conversion mode.

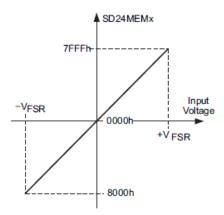


Figure 2.8 The relationship of the digital output value and the input analog voltage value

The converted digital value is:

converted digital value =
$$\frac{\text{differential value of analog input pair}}{\text{resolution }\Delta}$$
 = (calculated analog value)₂ (2.3)

2.3.6.4 Digital filter in SD24_A

The digital filter will process the digital 1 bit data stream from the second-order sigma-delta modulator with using a $SINC^3$ comb filter.

The transfer function in the Z-Domain is:

$$H(z) = \left(\frac{1}{OSR} \times \frac{1 - Z^{-OSR}}{1 - Z^{-1}}\right)^3$$
(2.4)

The transfer function in the frequency domain is:

$$H(f) = \left[\frac{\operatorname{sinc}\left(\operatorname{OSR}\times\pi\times\frac{f}{f_{M}}\right)}{\operatorname{sinc}\left(\pi\times\frac{f}{f_{M}}\right)}\right]^{3} = \left[\frac{1}{\operatorname{OSR}}\times\frac{\operatorname{sin}\left(\operatorname{OSR}\times\pi\times\frac{f}{f_{M}}\right)}{\operatorname{sin}\left(\pi\times\frac{f}{f_{M}}\right)}\right]^{3}$$
(2.5)

The oversampling ratio (OSR) is the ratio of the modulator frequency f_M to the sampling frequency f_S , thus $OSR = \frac{f_M}{f_S}$. Figure 2.9 below shows the frequency response of the digital filter in the SD24 A/D converter. The first filter notch is at $f_S = \frac{f_M}{OSR}$, as can be seen from Figure 2.9 below, every notch frequency is a multiple of the modulator frequency f_M .

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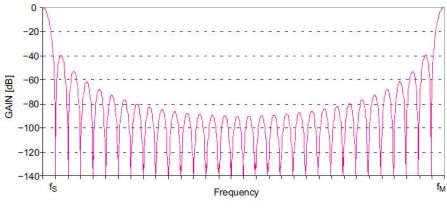


Figure 2.9 The frequency response of the digital filter in the SD24_A A/D converter [8]

The decimation of the digital bit-stream is completed in the digital filter in each enabled SD24_A analog-to-digital channel. Then the digital filter can output the new conversion results to the corresponding SD24MEMx register at the sampling frequency f_S .

3. Materials

3.1 Hardware components

3.1.1 MCU

MSP430AFE233 is selected as the microcontroller unit to be used in the Smart-plug electrical board. MSP430AFE233 has been described in detail in chapter 2.

3.1.2 RF module

The RF module with the chip CC1101 is chosen to transmit and receive the RF message in this Smart-plug system as a series of advantageous the chip CC1101 possesses, such as small package size, just 4×4 mm QFN and cheap price. The chip CC1101 is a low-cost sub-1 GHz transceiver designed for low-power wireless applications [9]. The circuit inside the chip CC1101 is mainly intended for the ISM (Industrial, Scientific and Medical) frequency bands at 315MHz, 433MHz, 868MHz and 915MHz. In this project, the 868MHz ISM band is used for the wireless communication between the antennas of the RF modules in different ELIQ devices. Figure 3.1 below shows a photo of the RF module used in this project.

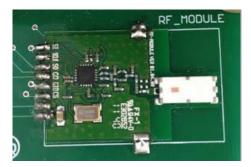


Figure 3.1 The photo of the RF module used in this project

This RF transceiver is integrated with a highly configurable baseband modem. The modem supports various modulation formats and has a configurable data rate up to 600 kbps [9]. The chip CC1101 can provide extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication and wake-on-radio [9].

The main operating parameters and the 64-byte transmit/receive FIFOs of CC1101 can be controlled via an SPI interface [9]. In a typical system, the CC1101 will be used together with a microcontroller and some other passive components.

Figure 3.2 below shows the schematic of the chip CC1101 and the peripherals circuits comprised with the additional passive components such as resistors, inductors, capacitors and the crystal using the 868MHz ISM band.

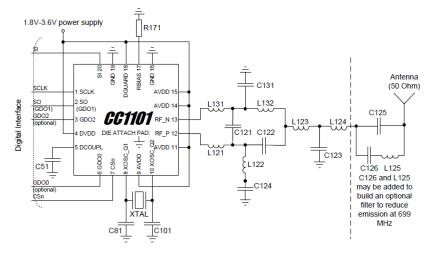


Figure 3.2 The schematic of the chip CC1101 and peripheral circuits on the RF module [9]

Figure 3.3 below shows the top view of the pin-out of the chip CC1101.

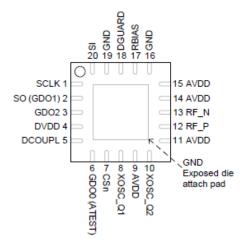


Figure 3.3 The top view of the pin-out of the chip CC1101 [9]

Table 3.1 below shows the fund	ctional description of	each pin of the chip CC1101.

Image: style Image: style<	Pin #	Pin Name	Pin type	Description
Defension Optional general output pin when CSn is high 3 GDO2 Digital Output Digital output pin for general use: Test signals FIFO status signals Clear channel indicator Clock output, down-divided from XOSC Serial output RX data 4 DVDD Power (Digital) 1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator 5 DCOUPL Power (Digital) 1.6 - 2.0 V digital power supply output for decoupling NOTE: This pin is intended for use with the <i>BETINI</i> only. It can not be use to provide supply voltage to other devices 6 GDO0 Digital I/O Digital output pin for general use: Test signals Clear channel indicator Clock output X data Serial output RX data Serial output RX data Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital input Serial configuration interface, chip select 8 XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 10 XOSC_Q2 Analog I/O Crystal oscillator pin 2 11 AVDD Power (Analog) 1	1	SCLK	Digital Input	Serial configuration interface, clock input
3 GDO2 Digital Output Digital output pin for general use: Test signals FIFO status signals Clear channel indicator Clock output, down-divided from XOSC Serial output RX data 4 DVDD Power (Digital) 1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator 5 DCOUPL Power (Digital) 1.6 - 2.0 V digital power supply output for decoupling NOTE: This pin is intended for use with the <i>Bettell</i> only. It can not be use to provide supply voltage to other devices 6 GDO0 Digital I/O Digital output pin for general use: (ATEST) Visital VO Digital output pin for general use: (ATEST) Visital output RX data • Test signals • FIFO status signals • Clear channel indicator • Clock output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial output RX data • Serial configuration interface, chip select 8 XOSC_Q1 Analog	2	SO (GDO1)	Digital Output	Serial configuration interface, data output
Image: Section of Sectio				Optional general output pin when CSn is high
9 AVDD Power (Digital) 1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator 5 DCOUPL Power (Digital) 1.8 - 3.6 V digital power supply output for decoupling NOTE: This pin is intended for use with the <i>definition</i> only. It can not be use to provide supply voltage to other devices 6 GDO0 Digital I/O Digital output pin for general use: Test signals Clear channel indicator Clock output, down-divided from XOSC Serial output pin for general use: Clear channel indicator Clear channel indicator Clear channel indicator Clock output, down-divided from XOSC Serial output RX data Serial output RX data Serial output X data Serial output TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select XOSC_Q2 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 11 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 12 RF_P RF I/O Negative RF input signal to LNA in receive mode Positive RF input signal from PA in transmit mode 13 RF_N RF I/O Negative RF output signal from PA in t	3	GDO2	Digital Output	Digital output pin for general use:
Image: Second				Test signals
Image: Second				FIFO status signals
Image: space of the system				Clear channel indicator
4 DVDD Power (Digital) 1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator 5 DCOUPL Power (Digital) 1.6 - 2.0 V digital power supply output for decoupling NOTE: This pin is intended for use with the <i>Bettient</i> only. It can not be use to provide supply voltage to other devices 6 GDO0 Digital I/O Digital output pin for general use: Test signals FIFO status signals Clear channel indicator Clock output, down-divided from XOSC Serial output RX data Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input Socc_Q2 9 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 12 RF_P RF I/O Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode 13 RF_N RF I/O Negative RF input signal for PA in transmit mode 14 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 15 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 15 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 15 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connectio				Clock output, down-divided from XOSC
Solution Voltage regulator Voltage regulator Notes and solution of the solutis solution of the solutis solution of the solutis solution of the				Serial output RX data
NOTE: This pin is intended for use with the <i>GETTOT</i> only. It can not be use to provide supply voltage to other devices 6 GDO0 (ATEST) Digital I/O Digital output pin for general use: • Test signals • FIFO status signals • Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select 8 XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 11 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 12 RF_P RF I/O Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode 13 RF_N RF I/O Negative RF input signal from PA in transmit mode 14 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection	4	DVDD	Power (Digital)	
6 GD00 (ATEST) Digital I/O Digital output pin for general use: • Test signals • FIFO status signals • Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select 8 XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 10 XOSC_Q2 Analog I/O Crystal oscillator pin 2 11 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 12 RF_P RF I/O Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode 13 RF_N RF I/O Negative RF input signal from PA in transmit mode 14 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 15 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection	5	DCOUPL	Power (Digital)	1.6 - 2.0 V digital power supply output for decoupling
ATEST) Test signals Test signals FIFO status signals Clear channel indicator Clear channel indicator Clock output, down-divided from XOSC Serial output RX data Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection XOSC_Q2 Analog I/O Crystal oscillator pin 2 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection XOSC_Q2 Analog I/O Crystal oscillator pin 2 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection RF_P RF I/O Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode RF_N RF I/O Negative RF output signal from PA in transmit mode Negative RF output signal from PA in transmit mode AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection				NOTE: This pin is intended for use with the CC1101 only. It can not be used to provide supply voltage to other devices
FIFO status signals Clear channel indicator Clear channel indicator Clock output, down-divided from XOSC Serial output RX data Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select 8 XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD 9 AVDD 9 AVDD 9 AVDD 10 XOSC_Q2 11 AVDD 12 RF_P RF_P RF I/O Positive RF input signal to LNA in receive mode Positive RF input signal from PA in transmit mode 13 RF_N RF I/O Negative RF output signal from PA in transmit mode 14 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 15 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection	6	GDO0	Digital I/O	Digital output pin for general use:
• Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select 8 XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD 9 Power (Analog) 1.8 - 3.6 V analog power supply connection 10 XOSC_Q2 11 AVDD 12 RF_P 8 I/O 9 Negative RF input signal fom PA in transmit mode 13 RF_N		(ATEST)		Test signals
Image: Second				FIFO status signals
Image: Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing 7 CSn Digital Input Serial configuration interface, chip select 8 XOSC_Q1 Analog I/O Crystal oscillator pin 1, or external clock input 9 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 10 XOSC_Q2 Analog I/O Crystal oscillator pin 2 11 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 12 RF_P RF I/O Positive RF input signal to LNA in receive mode 13 RF_N RF I/O Negative RF input signal from PA in transmit mode 14 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection 15 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection				Clear channel indicator
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15 AVDD Power (Analog) 1.8 - 3.6 V analog power supply connection		_		
	14	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
	15	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
16 GND Ground (Analog) Analog ground connection	16	GND	Ground (Analog)	Analog ground connection
17 RBIAS Analog I/O External bias resistor for reference current	17	RBIAS	Analog I/O	External bias resistor for reference current
18 DGUARD Power (Digital) Power supply connection for digital noise isolation	18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19 GND Ground (Digital) Ground connection for digital noise isolation	19	GND	Ground (Digital)	Ground connection for digital noise isolation
20 SI Digital Input Serial configuration interface, data input	20	SI	Digital Input	Serial configuration interface, data input

Table 3.1 The functional description of each pin of the chip CC1101 [9]

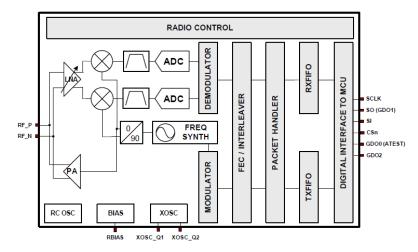


Figure 3.4 below shows the internal hardware structure inside the chip CC1101.

Figure 3.4 The internal hardware structure inside the chip CC1101 [9]

The digital interface of this type of RF module has 6 port pins—SCLK, SO (GDO1), SI, CS, GDO0 and GDO2. These port pins will connect to the corresponding pins on the MCU respectively. The CSn pin is the serial configuration interface to be used for the chip selection. The SCLK pin is the serial configuration interface to be used for the clock input. The SI pin is the serial configuration interface to be used for the clock input. The SI pin is the serial configuration interface to be used for the data input. The chip CC1101 has two dedicated configurable pins, the GDO0 pin and the GDO2 pin and one shared pin, the GDO1/SO pin that can output internal status for the software [9]. All of these pins can be used to generate interrupts of the MCU. The GDO1 pin is shared with the SO pin together. By selecting any other of the programming options, the GDO1/SO pin will become a generic pin [9]. But when the CSn pin is low, the GDO1/SO pin will always work as a normal SO pin which is the serial configuration interface to be used for the digital output pin for general use such as to be the test signal interface, the FIFO status signal interface, the indicator of clearing channel, the clock output, the serial output of RX data and the serial input of TX data [9]. The GDO2 pin except one difference that the GDO2 pin can only be the serial output of RX data but not the serial input of TX data.

When the RF module is used to transmit the data to another device through the wireless communication, the data input from the SI pin of the RF module will go into the TX FIFO firstly. Then after processing the data in the packet handler and interleaver, the data will be modulated in the modulator followed by the frequency systhesizer. The frequency synthesizer includes a complete on-chip LC VCO and a 90 degree phase shifter for generating the signal to the PA (power amplifier). Then after amplifying the power of the signal in the PA, the signal will go to the positive RF output port pin and negative RF output port pin to the antenna for the wireless communication.

When the RF module is used to receive the RF signals from another device through the wireless communication, the received positive RF signal and negative RF signal from the wireless communication will be amplified by the LNA (low noise amplifier) firstly. Then the positive RF signal and negative RF signal will be down-converted in quadrature (I and Q) with the

intermediate frequency in the down-conversion mixers. At intermediate frequency, the I/Q signals will be transferred to the digital signal by the analog-to-digital converters inside the chip CC1101. Then after the demodulation in the demodulator and the bit synchronization in the packet handler, the data will go to the digital interface to be transmitted to the MCU through the SPI communication.

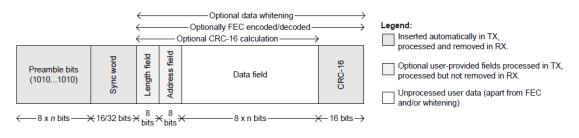


Figure 3.5 below shows the format of the data packet for the chip CC1101.

Figure 3.5 The format of the data packet for the chip CC1101 [9]

The preamble pattern is an alternating sequence of ones and zeros (10101010...) [9]. When enabling TX, the modulator will start transmitting the preamble bytes firstly. After a number of preamble bytes have been transmitted, the modulator will send the sync word and then the data from the TX FIFO if the data is available. If the TX FIFO is empty, the modulator will continue to send the preamble bytes until the first byte is written to the TX FIFO, then the modulator will send the sync word and the data [9].

3.1.3 AC/DC Converter

In this project, the switching power device RECOM RAC02-3.3SC is chosen as the AC/DC converter to transfer the high voltage AC signal to the low voltage DC signal to give the low working supply voltage for both of the MCU and the RF module. It has a wide input voltage ranges from 80V AC to 264V AC and a stable output voltage 3.3V DC [10]. The output rated power is 2 Watt so the maximum output current is 600 mA. The use of this component is to convert 230 VAC from live wire and neutral wire to 3.3V DC for the MCU and RF module. The RECOM RAC02-3.3SC has 4 pins, two of which are input pins connected to the live wire and neutral wire respectively, while the other two pins are output pins connected to the pins DVCC and VDD on both of the MCU and the RF module.

3.1.4 Relay

The electromagnetic relay HKE V6-S-DC3V is used to control the switch on or switch off status of the electrical appliance. The structure inside this type of relay is SPST, single pole single throw, which can be seen clearly in Figure 3.6 below, the pole is either normally open or normally closed. Figure 3.7 shows the footprint of the relay HKE V6-S-DC3V. The coil rated voltage is 3V and the coil resistance is 45 Ω so the rated coil power is 200mW. The relay HKE V6-S-DC3V has four terminals, two of which will be connected in the live wire, there is a mechanical switch device which is set between these two terminals to operate the large current via the live wire. The small

current goes through the coil resistor which is set between the other two terminals will generate the electromagnetic force to operate the latch on the mechanical switch device. When the voltage on the coil achieves at the coil pick-up voltage 2.25V, the mechanical switch device will be closed under the electromagnetic force from the coil then the electrical appliance will be connected to the household mains; when the voltage on the coil decreases below 0.3V, the mechanical switch device will be opened then the electrical appliance will be isolated from the household mains.

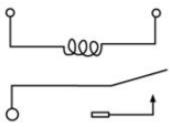


Figure 3.6 The internal hardware connection diagram of the relay HKE V6-S-DC3V [10]

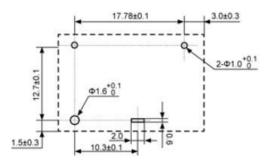


Figure 3.7 The footprint of the relay HKE V6-S-DC3V [10]

3.1.5 NPN transistor

The transistor BC847C is chosen as a control component in the control unit circuit to switch on or switch off the power supply to the electrical appliance. It is a 3-pin NPN transistor whose termination type is SMD and the footprint is SOT-23. The collector-emitter breakdown voltage is 45V and the collector-emitter saturation voltage is 200mV. The maximum value of the continuous collector current I_c is 100mA. The power dissipation of the NPN transistor BC847C is 250mW [11].

3.1.6 Crystal

All of the I/O ports in the MSP430AFE233 MCU have multiplex functions besides general purpose input or output pins function. P2.6 and P2.7 can be interfaced with the external crystal oscillator. P2.6 is the input terminal of external crystal and P2.7 is the output terminal of external crystal. The MULTICOMP-HC49U-3.2768-20-30-60-12-ATF-CRYSTAL is used as the external crystal to connect P2.6 and P2.7 of the MCU in this project. The frequency of this type crystal is 3.2768MHz. It can output 3.2768MHz frequency with extremely high stability for the MCU to be selected as the clock source for the ACLK, MCLK or SMCLK inside the MCU. The number of pins of the MULTICOMP-HC49U-3.2768-20-30-60-12-ATF-CRYSTAL is 2 and the crystal mounting type of it is

through hole [12].

3.1.7 Other components

Table 3.2 below shows the other components used in this Smart-plug device system.

Name of the component	Туре	Termination type	Footprint	Quantity
Ferrite beads	BLM21BD121SN1D	SMD	0805	2
Varistor	B72214S0271K101 (275VAC , 4500A)	Axial Leaded		1
TVS (Transient voltage suppressor)	SMAJ6.0CA	SMD	0805	1
Fuse	SCHURTER – FUSE (250VAC, 1A)	SMD		1
LED	MULTICOMP - LED, HIGH RED	SMD	0805	1
Resistors (330kΩ)		SMD	1206	3
Resistor (2.7kΩ)		SMD	0805	1
Resistor (1.5kΩ)		SMD	0805	1
Resistors (200Ω)		SMD	0805	1
Resistors (100Ω)		SMD	0805	1
Resistors (20Ω)		SMD	0805	2
Resistors (10Ω)		SMD	0805	1
Resistor (6.8Ω)		SMD	1206	1
Metal film Resistor (0.01Ω)	LOB5 R010 FLF	Axial Leaded		1
Capacitor (330uF)		SMD	7243	1
Capacitors (10uF)		SMD	0805	2
Capacitors (0.1uF)		SMD	0805	3
Capacitors (15nF)		SMD	1206	2
Capacitors (47pF)		SMD	0805	4
Capacitors (12pF)		SMD	0805	2
Diodes	IN4148	SMD	0805	5

Table 3.2 The overview of the other components used in this project

3.2 Software tools

3.2.1 Altium Designer 6

Altium Designer 6 is an electronic design automation tool to plot the printed circuit board with related libraries [13]. This EDA tool is developed by the company Altium Limited in Australia. It has two major parts: schematic design and PCB design. In the schematic design part, the electrical circuit schematic is drawn by setting design rules, search and selection of the electrical components from the component library, placement of components and connecting the components [13]. In the PCB design part, the printed circuit board graph file will be completed by drawing footprints of the components, choosing footprints of the components from the component of placement of the components from the component footprint library, placement of neuronatic trace routing in different layers, signal integrity analysis and manufacturing files generation with support for Gerber formats [13].

3.2.2 Switcher CAD III

Switcher CAD III is a computer aid design software produced by the company Linear Technology Corporation [14]. It is a suitable simulation tool to implement the circuit feasibility analysis. The simulation of the designed electrical circuit is executed in software by the simulator with a schematic module and waveform viewer [14]. The data results can be seen clearly in the waveform viewer after running the schematic design.

3.2.3 IAR Embedded Workbench

IAR Embedded Workbench is a high performance C/C++ compiler and debugger tool suite for the 8 bits, 16 bits or 32 bits microcontrollers [15]. It has an integrated development environment including a compiler, an assembler, a linker and a debugger with user-friendly interface [16]. In addition, IAR Embedded Workbench provides an uninterrupted workflow and a single toolbox in which all of the components can integrate seamlessly. The objective code can be generated fast and the execution time for developing low power applications is short in this advanced and powerful software tool.

IAR Embedded Workbench supports a large number of different processors including MSP430 microcontroller families. In this project, IAR Embedded Workbench for TI MSP430 Kickstart evaluation edition is used to debug and compile the C programming code for MSP430AFE233.

3.2.4 Lite Fet-Pro430 MSP430 flash programmer

The Lite Fet-Pro430 MSP430 flash programmer which is developed by Elprotronic Inc is used to download the program into the MCU via JTAG interface. It is a software package to operate with

existing programming adapters such as MSP430-FET (using parallel port), MSP-FET430UIF (using USB port) or Olimex' MSP430-JTAG [17]. In this project, MSP-FET430UIF using USB port is chosen as the programming adapter.

4. Hardware design

As outlined in the basic design principles in chapter 2, both of the voltage and current on the electrical appliance need be measured firstly in order to calculate the power consumption of the appliance. If selecting unipolar mode in the SD24CCTLx register, the input voltage can only be the positive value. Since the basic prototype is designed without the need of level shifter circuitry to do the bipolar-unipolar conversion, the bipolar mode need be selected by setting SD24UNI = "0" in the SD24CCTLx register. The on-chip reference voltage 1.2V is turned on by setting SD24REFON = "1" in the SD24CTL register to implement the analog-to-digital conversion.

4.1 Power supply circuit design

Figure 4.1 below shows the schematic of the power supply circuit inside the Smart-plug device.

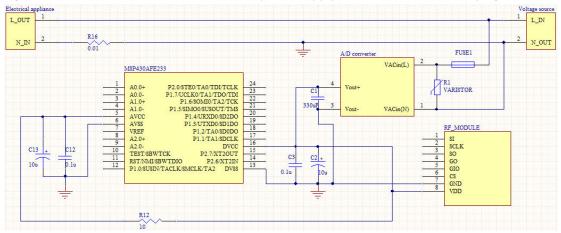


Figure 4.1 The schematic of the power supply circuit of the Smart-plug system

Since the working voltage of the MCU ranges from 1.8V to 3.6V but the voltage from the mains between live wire and neutral wire is 230V AC. An AC/DC converter needs to be added to transfer the high AC voltage to the low DC voltage for both of the MCU and RF module. RECOM RAC02-3.3SC is chosen as the AC/DC converter to supply low DC voltage. It has a wide input voltage ranges from 80 V AC to 264V AC and a stable output voltage 3.3V DC. The output power is 2 Watt so the output current can reach 600 mA to give enough drive current for normal operation of both of the MCU and the RF module. The RECOM RAC02-3.3SC has 4 pins, two of which are input pins VACin(L) and VACin(N) connected to the live wire and neutral wire respectively, other two pins are output pins Vout+ and Vout-.

There is a fuse SCHURTER – FUSE (250V AC, 1A) whose rated current is 1A set between the live wire and the VACin(L) pin of the AC/DC converter before the 230V AC signal on the live wire going into the AC/DC converter. When the current through the fuse from the mains to the VACin(L) pin exceeds 1A, the metal wire inside this fuse will melt to prevent the input ports of the AC/DC converter from being broken by the large current resulted from the short circuits, overloading, mismatched loads, or device failure.

In addition, there is a varistor B72214S0271K101 (275V AC, 4500A) set between the VACin(L) pin and the VACin(N) pin of the AC/DC converter as equivalent as between the live wire and neutral wire from the mains outside. The varistor is an electronic component with a nonlinear current– voltage characteristic as similar as a diode. The feature of the varistor is to conduct significantly increased current when voltage is excessive. When the voltage on the varistor increases more than a specific value, the resistance of the varistor will decrease a lot to be similar as the conductive state to shunt the current which is created by the high voltage away. In this case, the varistor can protect the AC/DC converter against excessive transient surge voltage.

The Vout+ pin is connected to the DVCC pin on the MCU and the VDD pin on the RF module. It is also connected to the AVCC pin on the other side of the MCU via a 10Ω resistor. The Vout- pin is connected to the DVSS pin, the AVSS pin on the MCU, the GND pin on the RF module and also the board ground. In this design, the supply voltage for both of the MCU and the RF module is 3.3V DC. The polarity capacitor C2 and the common capacitor C3 are set in parallel between the DVCC and the board ground to remove the possible residual AC noise waves from the output pins of the AC/DC converter. As similar as C2 and C3, the polarity capacitor C13 and the common capacitor C12 are also set in parallel between the AVCC and the board ground to remove the possible residual AC noise waves from the output pins of the AC/DC converter.

4.2 Voltage sampling circuit design

Since the effective value of the voltage from the household mains is not stable 230V AC consistently but can fluctuate between 210V and 250V, it is necessary to measure the real voltage value on the electrical appliance at the moment. Figure 4.2 below shows the schematic of the designed voltage sampling circuit which is used to measure the effective voltage value on the electrical appliance inside the Smart-plug device.

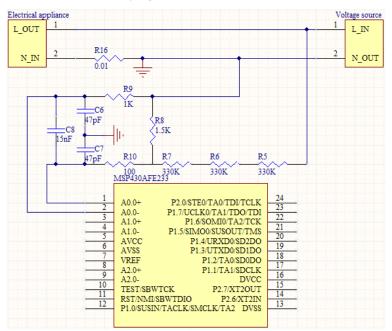


Figure 4.2 The schematic of the voltage sampling circuit of the Smart-plug system

As can be seen from Figure 4.2 above, the channel 0 of the SD24_A converters system is used as input for the instantaneous voltage samples which is divided by the dividing resistor circuit, the board ground is set to connect the neutral wire. The bipolar mode is selected and the internal reference voltage is 1.2V, thus the full scale input voltage is $\pm 0.6V$. Since the A/D converter of the MCU can only convert a small voltage value, the resistor divider circuitry needs to be added between live neutral wire and the MCU. For the resistors, there should be 10% of maximum voltage as margin. In order to verify the input voltage value does not exceed the critical value of the A/D converter module to break the MCU, the input voltage should range from -0.54V to 0.54V. Since the AC signal from the household mains may reach 250V AC, which triggers the peak value is $250 \times \sqrt{2} = 353.55V$, the divisor value of the voltage dividing circuit should satisfy that:

Divisor
$$\ge \frac{353.55V}{0.54V} \approx 655$$
 (4.1)

That means the divisor value of the voltage dividing circuit should be at least 655. According to this analysis, three identical $330k\Omega$ resistors and one $1.5k\Omega$ resistor are chosen to comprise the dividing circuitry as Figure 4.2 above shows. The more resistors are deployed, the lower voltage each resistor bears. In view of the thermal noise of resistors with high resistance, three identical resistors R5, R6 and R7 are employed. Thus, the divisor value in the design is:

Divisor =
$$\frac{330k+330k+330k+1.5k}{1.5k} = 661$$
 (4.2)

With this voltage dividing circuit, the input voltage to the A/D converter module of the MCU can be kept between -0.54V and 0.54V to verify ensure a safe operation range for the MCU chip.

The resistor R9 and capacitor C6, as similar as the resistor R10 and the capacitor C7, constitute the RC low pass filter circuit. Since there may be some high frequency flooding waves left combined with the DC voltage signal together, the aliasing may occur in the circuit. The RC low pass filter can remove the interrupts from these high frequency flooding waves.

4.3 Current sampling circuit design

Figure 4.3 below shows the schematic of the designed current sampling circuit which is used to measure the effective current value on the electrical appliance inside the Smart-plug device.

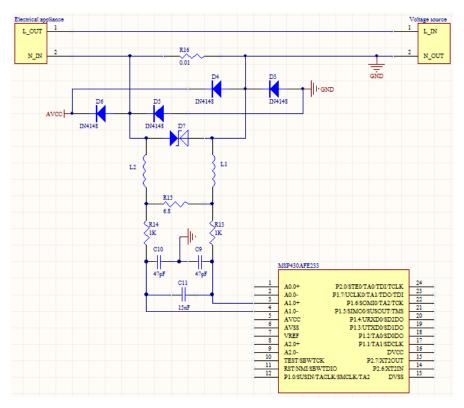


Figure 4.3 The schematic of the current sampling circuit of the Smart-plug system

As can be seen from Figure 4.3 above, channel 1, another channel of the SD24_A analog-to-digital converters system in MSP430AFE233, is used to capture the current value on the instantaneous electrical appliance. R16 is the sampling resistor with extremely small resistance value set in the main circuit. Since the current value on the electrical appliance needs to be measured in order to calculate the power consumption, the voltage value on the sampling resistor can be measured firstly. The Smart-plug device is designed to measure the electrical appliance with the power consumption range from 2W to 3000W, that means the maximum effective current value on the live wire and neutral wire can reach:

$$\frac{3000W}{230V} \approx 13A \tag{4.3}$$

As the input voltage to the SD24_A analog-to-digital converter should range from -0.54V to 0.54V, so the maximum resistance value of the sampling resistor is:

$$\frac{0.54V}{\sqrt{2} \times 13A} \approx 0.029 \,\Omega \tag{4.4}$$

If choosing the sampling resistor as 0.029Ω , the power consumption on the sampling resistor is: $13^2 \times 0.029 \approx 4.9 W$ (4.5)

This power consumption value is quite large, which will make the Smart-plug device too hot, thus a resistor with smaller resistance value should be chosen here as the sampling resistor. In order to simplify the power value calculation, the resistor with a resistance value 0.01Ω is selected to be the sampling resistor. In this case, if the 3000w electrical appliance is connected to the Smart-plug device, the power consumption value on the sampling resistor is:

Design and implementation of the ELIQ Smart-plug device system

$$13^2 \times 0.01 = 1.69 \,\mathrm{W}$$
 (4.6)

This power consumption value is suitable for the product.

The maximum voltage value on the sampling resistor can reach:

$$13 \times \sqrt{2} \times 0.01 \approx 0.184 \, V$$
(4.7)

This voltage value is inside the safe range as the input voltage value to the SD24_A analog-to-digital converter module of MSP430AFE233.

Considering the thermal margin for the application, LOB5 R010 FLF, the 0.01Ω current sense resistor, with the rated power 5W, resistor tolerance ±1% and the metal film resistor element type is chosen to be the sampling resistor in the Smart-plug device.

As can be seen in Figure 4.3 above, there are four IN4148 diodes set before the voltage signal on the sampling resistor going to the MCU. Two of the four diodes are set in parallel with the sampling resistor and the other two of the four diodes are set in the same way. The use of these four IN4148 diodes is to clamp the input voltage to the analog inputs of the A/D converter inside the MCU in a small voltage range. There may be some large spikes or surges in the live wire and neutral wire from the mains, triggering the voltage value on the sampling resistor to exceed the safe range of the analog inputs largely to break the MCU. Since the minimum threshold forward voltage of the diode IN4148 is about 0.6V DC, if connecting the four diodes as Figure 4.3 above shows, the voltage value of the two points on both of the two sides of the sampling resistor will be clamped in a range from -0.6V to 3.9V. If the voltage value on either point of two sides of the sampling resistor exceeds this range, one of the four diodes will face a breakdown to make the current flow through the diode instantly in order to prevent the MCU from being damaged.

There are also a transient voltage suppressor SMAJ6.0CA which is called D7 in the figure 4.3 and a burden resistor R15 set in parallel with the sampling resistor. The transient voltage suppressor can protect the MCU from being damaged by the transient overvoltage in the circuit. Although the 0.01 Ω resistor is chosen as the sampling resistor and the maximum input voltage value to the SD24 A analog-to-digital converter module of the MCU is 0.184V less than the full scale input voltage 0.6V, there still exist some voltage spikes which may exceed the safe voltage range of the MCU in the signal. The SMAJ6.0CA is a type of bidirectional transient voltage suppressor to deal with the AC overvoltage signal. The circuit inside the bidirectional transient voltage suppressor can be equivalent to two mutually opposing avalanche diodes in series with one another. When the voltage on the device is lower than the avalanche breakdown voltage, the device will represents high impedance. When the voltage on the device exceeds the avalanche breakdown voltage, the impedance will decrease a lot instantly then the excess current will be shunted by the device. In addition, all of the overvoltages above the breakdown voltage will be suppressed less than the value of clamping voltage. The transient voltage suppression diode can respond to the overvoltages much faster than other common over-voltage protection components such as the varistor and absorb a large amount of the transient energy internally. When the overvoltage goes away, the transient voltage suppressor can reset automatically.

There are two ferrite beads BLM21BD121SN1D in series with the anti-aliasing resistors R20 and R21 respectively. When the signal through the ferrite bead BLM21BD121SN1D is low frequency, there is almost not any impedance. However, if the ferrite bead BLM21BD121SN1D encounters with high frequency signal, the resistance element of the ferrite bead will become dominant. As this characteristic, it can be used to remove the high frequency noise and some spike disturbance from the 50Hz AC signal.

As similar as the voltage sampling circuit, two RC low pass filter circuitries made up of the resistor R13 and the capacitor C9, the resistor R14 and the capacitor C10 are also added before the signal going into the analog input pairs of the MCU to avoid the signal aliasing in the current sampling circuit.

4.4 Switching on/off control unit circuit design

The schematic of the control unit circuit which is used to switch on or off the power supply to the connected appliance is shown in Figure 4.4 below.

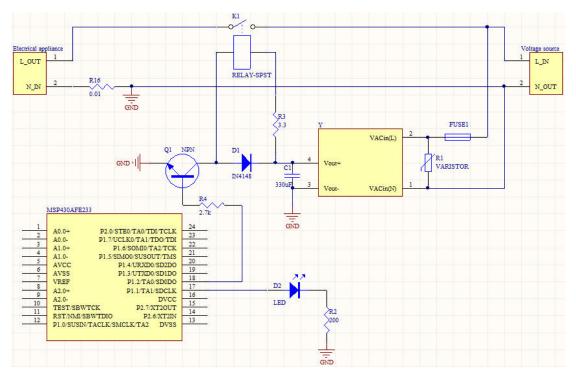


Figure 4.4 The schematic of the control unit circuit

The electromagnetic relay HKE V6-S-DC3V is set in the live wire. As described in section 3.1.2, there is a mechanical switch device to operate the large current via the live wire inside the internal structure of this type of relay. The current goes through the coil resistor will generate the electromagnetic force to operate the latch on the mechanical switch device. If the voltage on the coil reaches the coil pick-up voltage 2.25V, the mechanical switch device will be closed under the electromagnetic force from the coil then the electrical appliance will be connected to the household mains; however, if the voltage on the coil decreases below 0.3V, the mechanical

switch device will be opened then the electrical appliance will be isolated from the household mains. The I/O port pin P1.2 in the MCU is connected to the base pin of the NPN transistor. When the P1.2 output is set to be "1" in software, the output voltage of the P1.2 is near 3.3V DC since the power supply to the MCU is 3.3V DC. In this case, the voltage between the base pin and the emitter pin will exceed the base-emitter saturation voltage of the BC847C. Then the circuit between the collector pin and the emitter pin will conduct. Since the emitter pin is connected to the board ground, the electric potential of the collector will be also near the board ground in this case. Then there will be the electric potential difference between the point Vout+ of the A/D converter and the collector of the BC847C, the current on the coil of the relay will increase significantly. From the simulation waveform by using the software tool Switcher CAD III, it can be seen that the current on the coil is 64.8mA at this moment, so the voltage on the coil is:

$$64.8 \text{mA} \times 45 \,\Omega \approx 2.916 \,\text{V} \tag{4.8}$$

Now the voltage on the coil is more than the pick-up voltage 2.25V, thus the mechanical switch device will be closed under the electromagnetic force from the coil, the electrical appliance will be conducted as it is in the switch on status connected to the household mains.

When the P1.2 output is set to be "0" in software, the output voltage of the P1.2 is almost 0 as the board ground. The circuit between the collector and the emitter will be isolated. There is no voltage potential difference between the point Vout+ of the A/D converter and the collector of the BC847C, so the current on the coil will be extremely small, almost 0, then the voltage on the coil decreases below 0.3V, the mechanical switch device will be opened and the electrical appliance will be isolated from the household mains.

P1.1 is connected to a LED and a 200 Ω resistor. This pin is used to turn on or shut off the LED to indicate the switch on or switch off status of the electrical appliance. When the electrical appliance is switched off from the power supply by the relay, the output of P1.1 is "1", that means then the output voltage from this pin is close to 3.3V DC as the VCC and the LED will be turned on. When the electrical appliance is switched on, the output of P1.1 is "0", that means the output voltage from this pin is close to 0 as the VDD, triggering the LED be shut off.

The diode IN4148 is set in parallel with the relay to prevent electric spark when the P1.2 output value is toggled from "1" to "0". As Figure 4.4 above shows, the positive pole of the IN4148 is connected to the collector pin of the NPN transistor and the negative pole of the IN4148 is connected to the Vout+ of the A/D converter. When the P1.2 output value is toggled from "1" to "0", the NPN transistor will be toggled to the cutoff status from the saturation status instantaneously, the circuit link between the collector pin and the emitter pin will be isolated. As the coil is similar as a inductor and the effect of an inductor in a circuit is to oppose changes in current through it by developing a voltage across it proportional to the rate of change of the current, the instantaneous change of the current on the coil will generate the electromotive force to make the coil work as a voltage source. There will still exist the voltage differential between the point Vout+ of the A/D converter and the point collector pin of the NPN transistor, the residual current will not disappear soon, so the electric spark may be generated on the coil. If setting the diode IN4148 here, the coil and the diode IN4148 can compose a circuit loop, the

residual current can flow away through the diode IN4148 to prevent the coil from being damaged by the electric spark.

4.5 Communication between MCU and RF module

Figure 4.5 below shows the schematic of the designed circuit of the connection between the MCU and the RF module.

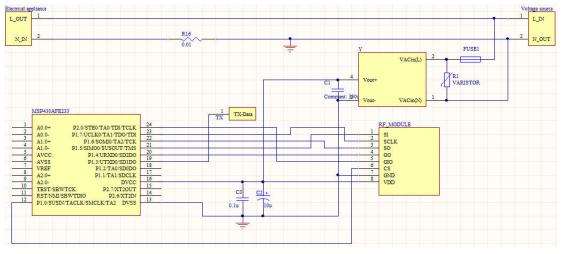


Figure 4.5 The schematic of the communication circuit between MCU and RF module

The RF module has 8 port pins, 6 of them consist of the digital interface to connect the MCU and other 2 port pins are VDD and GND connected to the Vout+ pin of the AC/DC converter and the board ground respectively. During the 6 port pins of the digital interface, SI pin is connected to the P1.5 (SIMO) pin of the MCU, SO pin is connected to the P1.6 (SOMI) pin of the MCU, SCLK pin is connected to the P1.7 (UCLK) pin of the MCU, CS pin is connected to the P1.0 pin of the MCU, these 4 pins will implement the 4-wire SPI communication together. The SCLK pin is the serial configuration interface to be used for the clock input, the SI pin is the serial configuration interface to be used for the serial configuration interface to be used for the clock input, the serial configuration interface to be used for the clock input, the serial configuration interface to be used for the clock input, the serial configuration interface to be used for the clock input, the serial configuration interface to be used for the clock input, the serial configuration interface to be used for the clock input.

The GO pin is connected to the P1.4 (URXD) pin of the MCU, the GIO pin is connected to the P2.0 pin of the MCU, meanwhile, the GO pin is connected to the GDO2 pin of the chip CC1101 and the GIO pin is connected to the GDO0 pin of the chip CC1101 on the RF module. Both of the GDO2 pin and the GDO0 pin are the digital output pins for general use such as to be the test signal interface, the FIFO status signal interface, the indicator of clearing channel and the clock output. However, the GDO0 pin can be used as both of the serial output of RX data and the serial input of TX data while the GDO2 pin can only be used as the serial output of RX data. From Figure 4.5 above, it can be noticed that there is a small empty pad outside the MCU on the PCB board connected to the port pin P1.3 (UTXD) of the MCU. This small empty pad can be used to detect

whether the software code of the communication between the MCU and the RF module is running successfully or not by writing some test code in software and using an oscilloscope as the detection tool.

5. Software design methodology

Figure 5.1 below shows the flowchart of the software process. The details of the software execution process will be explained specifically in the following sub chapters.

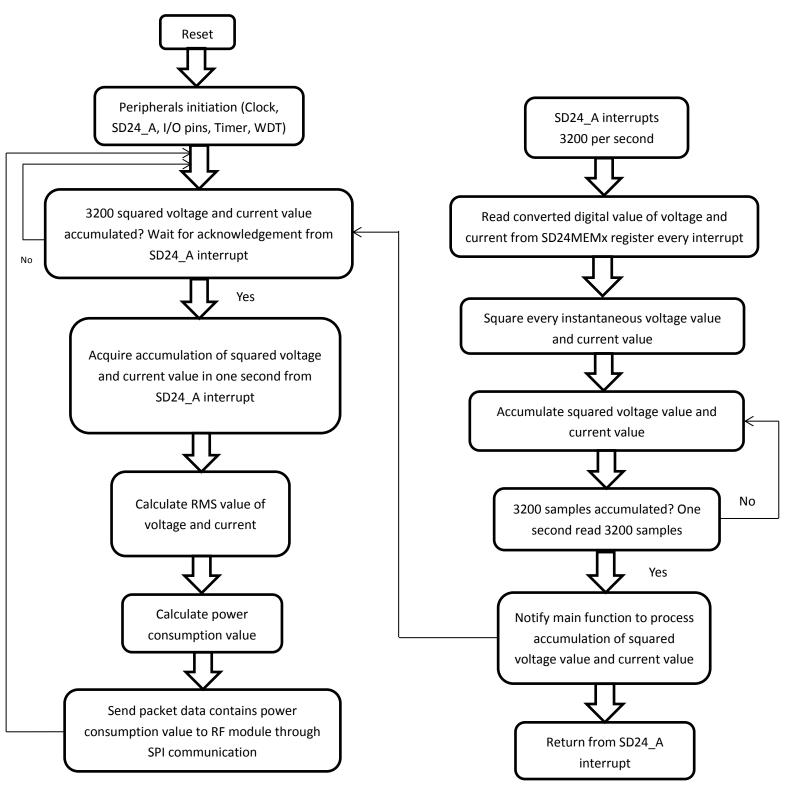


Figure 5.1 The flowchart of the implemented software

5.1 Power consumption value calculation

5.1.1 Peripherals initiation in MSP430AFE233

In the MCU MSP430AFE233, the major peripherals are the SD24_A A/D converters, the clock system, the timer and the watchdog timer. After a device RESET, the initial setup of these major peripherals will be implemented in software firstly. The initialization routines include the setup of the SD24_A analog-to-digital converters, clock system, general purpose input/output port pins, timer and watchdog timer.

5.1.1.1 Clock system initiation

In the BCSCTL1 register, the XT2OFF bit is used to choose whether the XT2 oscillator is turned on or turned off. Since XT2CLK needs to be used for MCLK and SMCLK, the XT2 oscillator should be turned on by clearing the XT2OFF bit.

7	6	5	4	3	2	1	0
XT2OFF	XTS	DI\	/Ax		RS	ELx	

Table 5.1 The function of each bit in the BCSCTL1 register [8]

In software, the code to initialize the BCSCTL1 register is:

#define XT2OFF (0x80)

BCSCTL1 &= ~XT2OFF;

In the BCSCTL2 register, the SELMx bits will be used to select the clock source for the MCLK and the SELS bit will be used to select clock source for the SMCLK. XT2CLK is used as the clock source for MCLK and SMCLK and the XT2 oscillator has already been set present on chip, so the SELMx bits = "1 0" and the SELS bit = "1". Neither the MCLK nor the SMCLK needs to be divided, so the DIVMx bits are equal to "0 0" to make the divider ratio for MCLK is 1. Similarly, the DIVSx bits are equal to "0 0" to make the divider ratio for SMCLK is 1.

7	6	5	4	3	2	1	0
SEL	.Mx	DIV	′Mx	SELS	DIV	/Sx	DCOR

Table 5.2 The function of each bit in the BCSCTL2 register [8]

In software, the code to initialize the BCSCTL2 register is:

#define SELS (0x08)
#define SELM_2 (0x80)

BCSCTL2 |= SELS+SELM_2;

In the BCSCTL3 register, the XT2Sx bits are used to select the frequency range for the XT2 clock. Since the frequency of the external crystal connected to the XT2 ports is 3.2768MHz, the XT2Sx

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bits are equal to "1 0" to make the external crystal used on the electrical board is suitable for the selected frequency range from 3MHz to 16MHz.

7	6	5	4	3	2	1	0
XT	2Sx	LFX1	Г1Sx	XCA	APx	XT2OF	LFXT1OF

Table 5.3 The function of each bit in the BCSCTL3 register [8]

In software, the code to initialize the BCSCTL3 register is:

#define XT2S_2 (0x80) #define LFXT1S_2 (0x20)

BCSCTL3 |= XT2S_2+LFXT1S_2;

5.1.1.2 I/O ports initiation

P1.0 is connected to the CS pin on the RF module. This pin is used to control the chip selection for the Radio Frequency module. The chip selection is activated when the CS pin is low. In the P1DIR register, bit 0 is set to be "1" since controlling the chip selection of the RF module is in the output direction for the MCU. In the P1REN register, bit 0 is set to be "0" then the pullup/pulldown resistor for this pin is disabled. Since the chip selection is activated when the CS pin is low, bit 0 is set to be "1" in the P1OUT register to make the initial state of the chip selection function is disabled.

As described in section 4.4, the port pin P1.1 is used to turn on or shut off the LED to indicate the switch on or switch off status of the electrical appliance. In the P1DIR register, bit 0 is set to be "1" since controlling the LED is in the output direction for the MCU. In the P1REN register, bit 1 is set to be "0" then the pullup/pulldown resistor for this pin is disabled. In the P1OUT register, bit 1 is set to be "0" to shut off the LED in the beginning.

The port pin P1.2 is used to control the relay to switch on or switch off the power supply to the electrical appliance, which has also been described in section 4.4 in detail. In the P1DIR register, bit 2 is set to be "1" since controlling the NPN transistor is in the output direction for the MCU. In the P1REN register, bit 2 is set to be "0" then the pullup/pulldown resistor for this pin is disabled. In the P1OUT register, bit 2 is set to be "0" in software in the initial state, then the collector and the emitter of the NPN transistor BC847C is isolated, there is negligibly small current on the coil of the relay, so the mechanical switch device will be opened under the electromagnetic force from the coil and the electrical appliance is switched off to the power supply in the beginning.

P1.3 is connected to a small empty pad outside the MCU on the PCB board. This pad is used to detect the working state of the communication between the MCU and the RF module. In the P1DIR register, bit 2 is set to be "1" since detecting the running state of the software by using an oscilloscope is in the output direction for the MCU. In the P1REN register, bit 2 is set to be "0" then the pullup/pulldown resistor for this pin will be disabled. In the P1OUT register, bit 2 is set to be "0" to give the initial state "0" for the output of the P1.3 port pin.

P1.4 is connected to the GO pin of the RF module. On the other side, GO pin is also connected to the GDO2 pin of the CC1101 chip on the RF module. GO pin is the general output pin of the RF module, which will send data to the port P1.4 of the MCU, so bit 4 in the P1DIR register is set to be "0" to make the port pin P1.4 is in the input direction. In the P1REN register, bit 4 is set to be "1" to enable the pullup/pulldown register. In the P1OUT register, bit 4 is set to be "1" to ensure the port P1.4 is pulled up.

P1.5 is also the SIMOO pin for the MCU. It is connected to the SI pin of the RF module. Since MCU is the master machine and RF module is the slave machine, the port pin P1.5 is used to send data from the MCU to the RF module, then bit 5 in the P1DIR register is set to be "0" to ensure the port pin P1.5 is in the output direction. In the P1REN register, if bit 5 is set to be "0" then the pullup/pulldown resistor for this pin is disabled. In the P1OUT register, bit 5 is set to be "1" to give the initial state of the output of P1.5 as high.

P1.6 is also the SOMIO pin for the MCU. It is connected to the SO pin of the RF module. Since MCU is the master machine and RF module is the slave machine, port pin P1.6 is used to receive data from the RF module, then bit 6 in the P1DIR register is set to be "1" to ensure the port pin P1.6 is in the input direction. In the P1REN register, bit 6 is set to be "1" to enable the pullup/pulldown register. In the P1OUT register, bit 6 is set to be "1" to ensure the port pin P1.6 is pulled up.

P1.7 is connected to the SCLK pin of the RF module. It is connected to the internal clock source inside the MCU. This pin is used to output the clock signal to control the clock of the RF module to receive data from the MCU, thus bit 7 in the P1DIR register is set to be "0" to ensure the port pin P1.7 is in the output direction. In the P1REN register, bit 7 is set to be "0" then the pullup/pulldown resistor for this pin is disabled. In the P1OUT register, bit 7 is set to be "1" to give the initial state of the output of P1.7 as high.

P2.0 is connected to the GIO pin of the RF module. On the other side, GIO pin is connected to the GDO0 pin of the CC1101 chip on the RF module. The GIO pin is the general input/output pin of the RF module, which will send data to the port P2.0 of the MCU from the RF module, so the bit 0 in the P2DIR register is set to be "0" to ensure the port pin P2.0 is in the input direction. In the P2REN register, the bit 0 is set to be "1" to enable the pullup/pulldown register. In the P2OUT register, the bit 0 is set to be "1" to ensure the port P2.0 is pulled up. In this Smart-plug device system, the I/O interrupt of the port pin P2.0 is used to control the function of repeating the RF message. Fetching and processing the received data packet from other ELIQ devices via the wireless communication will be implemented in the interrupt service routine of P2 port, thus the bit 0 of P2IE register is set to be "1" to enable the I/O interrupt of P2.0 and bit 0 of P2IES register is set to be "1" to enable the I/O interrupt of P2.0 and bit 0 of P2IES register is set to be "1" to enable the I/O interrupt of P2.0 and bit 0 of P2IES register is set to be "1" to enable the I/O interrupt of P2.0 and bit 0 of P2IES register is set to be "1" to enable the I/O interrupt of P2.0 and bit 0 of P2IES register is set to be "1" to ensure the high-to-low transition occurs in the signal from the GIO pin of the RF module to the P2.0 pin of the MCU, while the initial state of the bit 0 of the P2IFG register is set to be "0".

P2.6 and P2.7 are connected to the external crystal oscillator. P2.6 is the input terminal of the external crystal and P2.7 is the output terminal of the external crystal. As described in Section 3.1.6, the MULTICOMP-HC49U-3.2768-20-30-60-12-ATF-CRYSTAL is used as the external crystal for the MCU MSP430AFE233. The port pin P2.6 and the port pin P2.7 will receive the clock signal from the external crystal, so both of bit 6 and bit 7 in the P2DIR register are set to be "0" to ensure the port pin P2.6 and port pin P2.7 are in the input direction. In the P2REN register, both of bit 6 and bit 7 are set to be "1" to enable the pullup/pulldown register. In the P2OUT register, both of bit 6 and bit 7 are set to be "1" to ensure P2.6 and P2.7 are pulled up.

In summary, the initialized value of every bit in P1DIR register, P1OUT register, P1REN register, P2DIR register, P2OUT register, P2REN register, P2IES register, P2IFG register and P2IE register are shown in Table 5.4 below:

register	initialized value
P1DIR	10101111
P1OUT	11110001
P1REN	01010000
P2DIR	0000000
P2OUT	11111111
P2REN	00111111
P2IES	0000001
P2IFG	0000000
P2IE	0000001

Table 5.4 The initialization of each bit of the I/O ports registers

In software, the code to configure the P1 I/O ports is:

P1DIR = 0xAF; P1OUT = 0xF1; P1REN =0x50; P2DIR = 0x00; P2OUT = 0xFF; P2REN = 0x3F; P2IES = 0x01; P2IFG = 0x00; P2IE = 0x01;

5.1.1.3 SD24_A A/D converter initiation

5.1.1.3.1 Configuring sampling frequency

The SD24_A A/D converter possesses a feature that the SD24_A interrupt is triggered every time the converted data from the digital filter output is stored into the SD24MEMx register, that means SD24_A A/D converter can generate the interrupt every sampling instant, which will be quite convenient for the data sampling process.

The frequency of the mains voltage signal from outside is 50Hz if the mains voltage is stable. According to the Nyquist Theorem, a signal waveform must be sampled at least twice as fast as the frequency of the signal to reconstruct the original signal waveform accurately. However, the more sampling points in one sine-wave period, the better original waveform can be retrieved, similarly, if more data samples are captured in one sine-wave period of the signal, the RMS (Root Mean Square) values of the voltage and current from the sampled instantaneous voltage values and the sampled instantaneous current values can be calculated more accurately. The RMS values of both of the voltage and current from the sampled instantaneous voltage value and the effective current value similarly in this project. It is designed to capture 3200 data samples in one second to calculate the effective voltage value and the effective current value similarly in one sine-wave period of the signal, 64 samples will be captured, which is much larger than the number of sampling points to satisfy the Nyquist Theorem.

The frequency of the clock from the external crystal is 3.2768MHz. In the SD24CTL register, the SD24SSELx bits will select which one is the clock source from MCLK, SMCLK, ACLK or external TACLK. Here SMCLK is chosen as the clock source for the SD24_A, so the SD24SSELx bits are equal to "0 1". Both of the SD24XDIVx bits and the SD24DIVx bits can divide the clock together to generate the modulating frequency f_M for the sigma-delta modulator. Here the SD24DIVx bits are set to be equal to "1 0" and the SD24XDIVx bits are set to be equal to "0 0" to let the SMCLK be divided by 4. So the modulator frequency f_M to the 2nd order sigma-delta modulator in the SD24_A is:

$$f_{\rm M} = \frac{3.2768 \rm MHz}{4} = 0.8192 \rm MHz$$
 (5.1)

OSR is the oversampling ratio value in the SD24_A. The sampling frequency f_s is defined as $f_s = \frac{f_M}{OSR}$. In SD24CCTLx register, the SD24XOSR bit and the SD24OSRx bits will select OSR to be either 32, 64, 128, 256, 512 or 1024. In this project, OSR is designed to be 256, so the SD24XOSR bit is set to be "0" and the SD24OSRx bits equal to "0 0". Since the modulation frequency $f_M = 0.8192$ MHz, the sampling frequency f_s in the SD24_A is:

$$f_s = \frac{f_M}{OSR} = \frac{0.8192MHz}{256} = 3200Hz$$
 (5.2)

So the sampling frequency f_s in the SD24_A is set to be 3200Hz, that means 3200 data samples can be input to the SD24MEMx from the output of the digital filter in one second, also, it can be read 3200 instantaneous voltage value and also 3200 instantaneous current value in one second in software.

5.1.1.3.2 Configuring analog-to-digital conversion parameters

As described in section 5.1.1.3.1, in the SD24CTL register, the SD24SSELx bits are set to be "0 1", the SD24DIVx bits are set to be "1 0" and the SD24XDIVx bits are set to be "0 0". The SD24REFON

bit is used to select whether the on-chip reference voltage is turned on or turned off. In this project, the on-chip reference voltage 1.2V is designed to be used in the analog-to-digital conversion, so the SD24REFON bit is set to be "1".

15	14	13	12	11	10	9	8
reserved					SD24XDIVx		SD24LP

7	6	5	4	3	2	1	0
SD24	DIVx	SD24	SSELx	SD24VMIDON	SD24REFON	SD24OVIE	reserved

Table 5.5 The function of each bit in the SD24CTL register [8]

In software, the code to initialize the SD24CTL register is:

#define SD24SSEL_1 (0x0010u)
#define SD24DIV_2 (0x0080u)
#define SD24REFON (0x0004u)
SD24CTL = SD24SSEL_1 | SD24DIV_2 | SD24REFON;

As described in the basic design principle, two analog-to-digital channels need be used to measure the effective voltage value and the effective current value on the connected electrical appliance respectively. Thus, SD24_A channel 0 is designed to capture the voltage value and thSD24_A channel 1 is designed to capture the current value.

In the SD24INTCTLx register, the SD24INCHx bits will select which differential input pair to be used in the corresponding SD24 A channel. Since the differential input pair A0.0 is designed to connect the input AC signal in channel 0 and the differential input pair A1.0 is designed to connect the input AC signal in channel 1, both of the SD24INCH0 bits in the SD24INTCTL0 register and the SD24INCH1 bits in the SD24INTCTL1 register are set to be "0 0 0". The SD24GAINx bits are used to choose the preamplifier gain value for the differential input AC signal from 1, 2, 4, 8, 16 or 32 before the differential input AC signal coming into the 2nd sigma-delta modulator. Here the differential input AC signal need not be amplified in both of the channel 0 and channel 1 so both of the SD24GAIN0 bits in the SD24INTCTL0 register and the SD24GAIN1 bits in the SD24INTCTL1 register are equal to "0 0 0" to keep the preamplifier gain as 1. The SD24INTDLYx bits are used to choose how many samples delay for the first interrupt after the analog-to digital conversion starts. This interrupt delay can avoid the data conversion confusion and make the software work more stable. Here both of the SD24INTDLYO bits in the SD24INTCTLO register and the SD24INTDLY1 bits in the SD24INTCTL1 register are chosen to be "0 0" to make the fourth sample cause the first interrupt after the analog-to-digital conversion starts to avoid the data conversion confusion as far as possible. Thus, all of the bits in the SD24INCTL0 register and the SD24INCTL1 register will be set to be "0" as the initial state.

7	6	5	4	3	2	1	0
SD24II	NTDLYx		SD24GAINx			SD24INCHx	

Table 5.6 The function of each bit in the SD24INTCTLx register [8]

In software, the code to initialize the SD24INTCTLx register is:

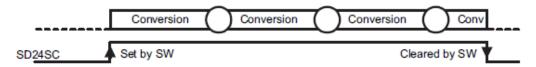
#define SD24INCH_0 (0x0000u)
SD24INCTL0 = SD24INCH_0;
SD24INCTL1 = SD24INCH_0;

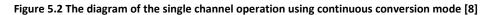
In the SD24CCTLx register, the SD24UNI bit is to select whether the bipolar mode or unipolar mode is used to accept the input AC signal. If choosing the unipolar mode, the analog input pair in the SD24_A can only be entered into the positive signal, while the bipolar mode can deal with both the positive signal and negative signal. Since the voltage shift level circuit is not used between the live wire, neutral wire and the MCU for both of the voltage sampling circuit and the current sampling circuit, the bipolar mode is selected by setting the SD24UNI bit = "0" in both of the SD24CCTL0 register and the SD24CCTL1 register. The SD24DF bit is used to choose whether the data format of the converted digital signal is offset binary or two's complement. Since the converted digital signal is singed binary number from the positive or negative analog signal, two's complement data format is selected by setting the SD24DF bit = "1" in both of the SD24CCTL0 register and the SD24CCTL1 register. Since the SD24_A interrupt needs to be used when sampling the data, the SD24IE bit is set to be "1" to enable the SD24_A interrupt in both of the SD24CCTL0 register and the SD24CCTL1 register. The SD24SC bit will start the analog-to-digital conversion on the corresponding channel by setting this bit equal to "1". The SD24LSBACC bit is set to be "0" then the 16 most significant bits of the conversion data from the decimation digital filter output will come into the SD24MEMx register. The SD24LSBTOG bit in both of the SD24CCTL0 register and the SD24CCTL1 register are set to be "0" then the SD24LSBACC bit in the SD24CCTL0 register or in the SD24CCTL1 register will not be toggled each time the SD24MEM0 register or the SD24MEM1 register is read by software to keep the SD24MEM0 register or SD24MEM1 register store the 16 most significant bits of the conversion data from the digital filter output. The SD24GRP bit is set to be "0" to make both of channel 0 and channel 1 work independently in single channel mode since both of the channel 0 and channel 1 don't need be grouped with higher channel to work together in this project. The SD24SNGL bit is set to be "0" in both of the SD24CCTL0 register and the SD24CCTL1 register to make both of channel 0 and channel 1 work in the continuous data conversion mode then the data conversion will continue until the SD24SC bit is cleared by software. Figure 5.2 below shows the single channel operation by selecting the continuous conversion mode. There is no need to use the high impedance input buffer to deal with the input signal, so the high impedance input buffer mode is disabled in both of the channel 0 and channel 1 by setting both of the SD24BUF0 bits in the SD24CCTL0 register and SD24BUF1 bits in the SD24CCTL1 register equal to "0 0".

15	14	13	12	11	10	9	8
reserved	SD24BUFx		SD24UNI	SD24XOSR	SD24SNGL	SD24	OSRx

7	6	5	4	3	2	1	0
SD24LSBTOG	SD24LSBACC	SD240VIFG	SD24DF	SD24IE	SD24IFG	SD24SC	SD24GRP

Table 5.7 The function	of each bit in the	e SD24CCTLx register [8]
	•••••••••••••••	





In software, the code to initialize the SD24CCTLx register is:

#define SD24OSR_256 (0x0000u)
#define SD24DF (0x0010u)
#define SD24SC (0x0002u)
#define SD24IE (0x0008u)
SD24CCTL0 = SD24OSR_256 | SD24DF | SD24SC | SD24IE;
SD24CCTL1 = SD24OSR_256 | SD24DF | SD24SC | SD24IE;

5.1.1.4 Timer_A initiation

IDx

In the TACTL register, the TASSELx bits are set to be "1 0" to choose SMCLK as the Timer_A clock source. The IDx bits are set to be "0 0" to determine the ratio of the divider is 1. The MCx bits are set to be "1 0" to make the Timer_A work in the continuous mode. The TACLR bit is set to be "1" to clear the count value in the TAR register and the ratio value of the timer clock divider. The TAIE bit is set to be "1" to enable the Timer_A interrupt and the TAIFG interrupt request.

15	14	13	12	11	10	9	8
		TAS	SELx				
· · · · · · · · · · · · · · · · · · ·							
7 6 5 4 3 2							0

Table 5.8 The function of each bit in the TACTL register [8]

unused

TACLR

TAIE

TAIFG

The count value of Timer_A will be stored into the TAR register.

MCx

7	6	5	4	3	2	1	0
			TA	Rx			

Table 5.9 The function of each bit in the TAR register [8]

In the TACCTLO register, the CAP bit is set to be "0" to choose the compare mode for the TACCRx register. The CCIE bit is set to be "1" to enable the capture/compare interrupt and the CCIFG interrupt request.

Design and implementation of the ELIQ Smart-plug device system

15	14	13	12	11	10	9	8
CN	Лх		ISx	SCS	SCCI	unused	CAP

7	6	5	4	3	2	1	0
	OUTMODx		CCIE	CCI	OUT	COV	CCIFG

Table 5.10 The function of each bit in the TACCTLO register [8]

Since the CAP bit in the TACCTLO register is set to be "0", the TACCRO register will work in the compare mode. In software, the decimal data 32768 will be stored into the TACCRO register initially. This value will compare with the count value in the Timer A register.

	•						
15	14	13	12	11	10	9	8
TACCRx							

7	6	5	4	3	2	1	0
			TAC	CRx			

Table 5.11 The function of each bit in the TACCR0 register [8]

In the continuous mode, the timer counts up from 0 to 0FFFFh in the TAR register repeatedly. The decimal value 32768 stored into the TACCR0 register is the independent time interval. Each time the timer counts up to the value stored in the TACCR0 register, the TACCTL0 register interrupt is generated. In the interrupt service routine, the next time interval value which also equals to decimal value 32768 will be added to the value stored in the TACCR0 register. Then if the count value in the TAR register achieves at the value stored in the TACCR0 register again, the TACCTL0 register interrupt is generated again. Since the SMLK is selected as the Timer_A clock source, that means the clock frequency for the timer is 3.2768MHz, the time interval between the two adjacent TACCTL0 register interrupts is:

Time interval =
$$\frac{1}{3.2768 \times 10^6} \times 32768 = \frac{1}{100}$$
 s = 10 ms (5.3)

In software, the code to initialize the Timer_A is:

#define TASSEL1	(0x0200u)	
#define TACLR	(0x0004u)	
#define CCIE	(0x0010u)	
#define UEP_CYCLES_PER_RTC	_INTERRUPT	32768
#define MC1	(0x0020u)	
#define TAIE	(0x0002u)	
TACTL = TASSEL1 + TACLR;	// Set	clock source and clear TAR (SMCLK, divide by 1)
TACCTL0 = CCIE;	// CCR0 ir	nterrupt enabled
TACCTL1 = CCIE;	// CCR1 int	errupt enabled
TACCR0 = UEP_CYCLES_PER_RT	C_INTERRUPT;	// Set compare register 0
TACTL = MC1 + TAIE;	// Start Tim	er_A in continues mode and enable interrupt

5.1.2 Sampling voltage and current value in one second

The SD24_A analog-to-digital converter has a fully differential input, the maximum full scale input voltage range is:

$$\pm V_{FSR} = \pm \frac{V_{REF/2}}{GAIN_{PGA}}$$
(5.4)

The on-chip reference voltage 1.2V is turned on in the SD24_A module, the bipolar mode is selected and the gain of the preamplifier is selected to be 1, so the maximum input voltage range now is:

$$\pm V_{FSR} = \pm \frac{1.2/2}{1} = \pm 0.6V \tag{5.5}$$

The resolution is :

resolution
$$\Delta = \frac{V_{FSR}}{2^{15}+1} = \frac{0.6v}{32768} \approx 0.0183 \text{mv}$$
 (5.6)

The converted digital value is:

converted digital value =
$$\frac{\text{differential value of analog input pair}}{\text{resolution }\Delta} = (\text{calculated analog value})_2$$
 (5.7)

The output from the digital filter to the SD24MEMx register in the SD24_A is a signed binary value. The simultaneous instantaneous voltage and current samples are captured by the two independent SD24_A A/D converters at a sampling rate of 3200Hz. Track of the number of samples that are present in one second is kept and used to obtain the RMS values for both of the voltage and current respectively. Here the RMS values of both of the voltage and current are regarded to be equal to the effective voltage value and the effective current value similarly. As described in section 4.3, the effective current value on the electrical appliance will be inferred from the measured effective voltage value on the sampling resistor. Channel 0 of the SD24_A converters system is used to capture the instantaneous voltage samples which are divided by the dividing resistor circuit and channel 1 of the SD24_A converters system is used to capture the sampling resistor to infer the instantaneous current value on the electrical appliance. The input voltage samples in both of the channel 0 and channel 1 of the SD24_A converters system are collected by using the SD24 interrupts. The function deals with the

timing critical events in software. The SD24 interrupt is generated once every $\frac{1}{3200}$ second. In

the SD24 interrupt service routine, a variable called adc_buffer used as the global data buffer will read the data value stored in the SD24MEMx register firstly. Then the data will be squared by using the multiplier to get the squared value. After that step, the squared value will be stored in a dedicated 48-bit register since the squared value may exceed the range of the 16-bit signed binary data. When the SD24 interrupt is generated next time and the function goes into the SD24 interrupt service routine again, the new squared value will be accumulated on the original squared value in the dedicated 48-bit register. As the sampling frequency is 3200Hz, that means 3200 data samples of the input voltage signal in both of the channel 0 and channel 1 can be

captured in one second. After 3200 squared value of samples have been accumulated in the dedicated 48-bit register, the calculation of the RMS values of voltage and current in one second will start. A variable in software will be used as the sample counter to keep track of how many samples have been accumulated over the frame period. When the value of the sample counter variable reaches 3200, the main function will be notified to process the accumulation value of both of the squared instantaneous voltage value and the squared instantaneous current value from the SD24_A interrupt service routine. Then the software process will be returned from the SD24_A interrupt service routine.

The formulas to calculate the accumulated squared values of the input voltage signal on both of the channel 0 and channel 1 are shown below:

$$ACC_{squared voltage value(channel 0)} = \sum_{n=1}^{sample \ count} V_{n(channel 0)}^{2}$$
(5.8)

$$ACC_{squared voltage value(channel 1)} = \sum_{n=1}^{sample \ count} V_{n(channel 1)}^{2}$$
(5.9)

5.1.3 RMS value calculation for voltage and current

After reset and the peripherals initiation, the main function will wait for the acknowledgment that 3200 squared instantaneous voltage values and 3200 squared instantaneous current values have been accumulated in the dedicated registers in one second from the interrupt service routine, then the RMS values of voltage and current in one second can be calculated from these 3200 data samples.

The formulas to calculate the RMS values of both of the voltage and current from the value read from the SD24MEM0 register of channel 0 and the value read from the SD24MEM1 register of channel 1 in software are shown below:

$$V_{RMS} = K_{\nu} \times \sqrt{\frac{\sum_{n=1}^{sample \ count} VALUE_{SD24MEM0 \ (channel \ 0)}^{2}}{sample \ count}}$$
(5.10)

$$I_{RMS} = K_i \times \sqrt{\frac{\sum_{n=1}^{sample \ count \ VALUE_{SD24MEM1} \ (channel 1)^2}{sample \ count}}$$
(5.11)

Where K_v is the scaling factor for the voltage and K_i is the scaling factor for the current. Sample count is the number of samples in one second, which should equal to 3200 under these configurations as long as the frequency of the mains is stable. The value of K_v and K_i can be inferred backward according to the conversion from the input voltage signal to the analog inputs of the SD24_A to the value written into the SD24MEMx register in both of the channel 0 and channel 1 of the SD24_A A/D converters system. The relationship of the mains voltage value and the value written into the SD24MEM0 register in channel 0 and the relationship of the current value on the electrical appliance and the value written into the SD24MEM1 register in channel 1 are:

$$VALUE_{SD24MEM0\ (channel\ 0)} = \frac{\frac{V_{mains}}{\frac{6.6}{2^{15}}}}{\frac{6.6}{2^{15}}}$$
(5.12)

$$VALUE_{SD24MEM1 (channel 1)} = \frac{I_{appliance} * 0.01}{\frac{0.6}{2^{15}}}$$
(5.13)

According to the formulas of the relationship between the mains voltage value and the value written into the SD24MEM0 register in channel 0 and the relationship between the current value on the electrical appliance and the value written into the SD24MEM1 register in the channel 1 above, the value of the scaling factors K_v and K_i can be inferred backward as the formulas shown below:

$$K_v = \frac{0.6}{2^{15}} \times 661 \tag{5.14}$$

$$K_i = \frac{0.6}{2^{15}} \times \frac{1}{0.01} \tag{5.15}$$

In software, dividing 2^x can be implemented by shifting the value x bits to the right. The calculation of the RMS value for both of the voltage and current on the electrical appliance is slow since the calculation steps such as multiplying, square, extraction of a root and shifting bits are time consuming functions. The time consumed in the complex calculations may exceed the sampling time interval, which may lead to the data conflict and calculation confusion in the software process. However, if the calculation of the RMS value is divided into two parts implemented in the SD24_A interrupt service routine and the main function respectively, the data conflict can be conflicted in software as far as possible. The calculation of the square and the accumulation of 3200 data samples are implemented in the SD24_A interrupt service routine, then the extraction of the accumulation value and multiplying the scaling factors will be implemented in the main function. The different variables are used to be the dedicated 48-bit registers to store the accumulation of both of 3200 squared instantaneous current values. In this way, the software process can be prevented from being congested and confused.

The reason using 3200 data samples in one second to calculate the RMS values of both of the voltage and current but not using 64 data samples in one sine-wave period to calculate the RMS values is that the deviation influence from the noises or spikes in the signal for the calculation can be avoided as far as possible if using many more sampled points to implement the calculation. Although the RC low pass filter circuit is added before the signal going into the analog input pairs of the SD24_A A/D converter of the MCU, there is still residual noise in the signal. If the data sample points deviated from the estimated value so far away in the signal are happened to be captured by the SD24_A A/D converter, it will influence the accuracy of the calculated RMS values results. The less sampled points to implement the calculation of the accuracy of the RMS values results from the influence of these deviated points. If only using 64 samples in one sine-wave period to calculate the RMS values, these points will

influence the results significantly. Thus, 3200 data samples are decided to be used in one second to implement the calculation of the RMS values of both of the voltage and current. In addition, this solution can also reduce the deviation of the calculated RMS values when the frequency of the mains voltage is not stable at 50Hz. For example, if the frequency of the main voltage is a little higher than the expected frequency, just sampling 64 points in one sine-wave period may lead to some points in the positive region of the next sine-wave period being captured by the SD24 A A/D converter. Then the RMS values result may be deviating from the influence of these points in the positive region of the next sine-wave period. However, if capturing 3200 sampled points in one second, that means capturing 3200 sampled points in 50 sine-wave periods, even if the frequency of the mains voltage signal is not stable at 50Hz, for example, the frequency of the main voltage is a little higher than the excepted frequency and some points in the positive region of the 51st sine-wave period, the calculated RMS values result will almost not be changed anything since there are 3200 data samples used to calculate the RMS values and the number of the points in the positive region of the 51st sine-wave period just occupies a very small percentage of the total number of the sampled points used to calculate the RMS values result. One second is still a quite short time interval compared to the time interval 15 seconds between each RF message sent from the ELIQ Smart-plug device to the ELIQ Energy Display Unit, which can satisfy the fast calculation to get the measured power consumption result for the RF communication.

5.1.4 Power consumption value calculation

When the RMS values of both of the voltage and current on the electrical appliance in one second are obtained, since the RMS values of both of the voltage and current are regarded to be equal to the effective voltage value and the effective current, then the power consumption value of the electrical appliance can be calculated by multiplying the RMS value of voltage and RMS value of current. The formulas are shown below:

power comsumption value = effective voltage value \times effective current value (5.16)

$$P_{appliance} = V_{RMS} \times I_{RMS} \tag{5.17}$$

5.2 Control switch on or off status of connected appliance

In the beginning, the output of the I/O port pin P1.2 is set to be "0" in software, the collector pin and the emitter pin of the NPN transistor BC847C are isolated, there is negligibly small current on the coil of the relay, so the mechanical switch device will be opened under the electromagnetic force from the coil and the electrical appliance is switched off from the power supply. When measurement of the power consumption starts, the output of P1.2 is toggled from "0" to "1" to make the NPN transistor BC847C conduct, then the mechanical switch device will be closed under the electromagnetic force from the coil and the electrical appliance is switched on to the power supply. If the measured power consumption of the electrical appliance is less than 2500w, the output of P1.2 is still "1" to keep the electrical appliance in switch on status. If the measured power consumption of the electrical appliance is more than 2500w, then the P1.2 is toggled from "1" to "0", turning off the NPN transistor BC847C, then the mechanical switch device will be opened under the electromagnetic force from the coil and the electrical appliance is switched off from the power supply.

5.3 SPI communication to RF module

The internal SPI port of the MCU is not used but the SPI communication is handled instead in software. A 32-bit unsigned variable is used to store the calculated power consumption value. A 16-bit unsigned variable is used to store the step value. An 8-bit unsigned variable is used to store the serial number and another 8-bit unsigned variable is used to store the battery status. All of these four variables consist of a struct variable. The report message data will be stored into this struct variable.

According to the data packet format of the chip CC1101 defined in the datasheet of CC1101, which can be seen clearly in Figure 5.3 below, there are two bytes for which one byte is used to store the length of the data packet and another byte is used to store the address of the message data consisting of the message header for the report message data. The message data will be added to a message buffer, toghther with the message header. Thus, in this message buffer, the first byte indicates the length, the number of bytes of the message data to be sent, the second byte indicates the destination address of the message data, then the payload data starts at the third byte.

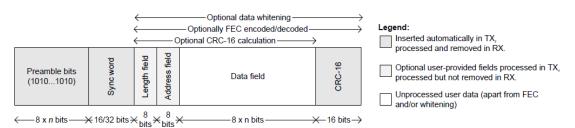


Figure 5.3 The format of the data packet for the chip CC1101 [9]

As can be seen from Figure 4.5, the schematic of the communication circuit between MCU and RF module presented in section 4.5, there are 4-wire SPI compatible interfaces (SI, SO, SCLK and CSn) on the chip CC1101 used to read and write the buffered data to implement the SPI communication between the MCU and the chip CC1101 where the MCU is the master and the chip CC1101 is the slave. All transfers on the SPI interface are done from most significant bit to least significant bit of the data.

Since the CSn port pin is active with the low state, the CSn pin must be kept low during the transfers on the SPI bus. If CSn goes high during transferring the data, the transfer will be cancelled immediately. The message data will be transferred serially to the SI pin of the RF module from the MOSI pin of the MCU.

Figure 5.4 below shows the flowchart of sending the value from the MCU to the RF module by using SPI communication. The data message contains the measured power consumption value will be encoded into the data packet firstly, then the data packet will be transferred to the RF module via the SPI interface once every 15 seconds, the time interval of transferring the data packet will be controlled by the Timer_A interrupt which is initiated in the beginning of the software process.

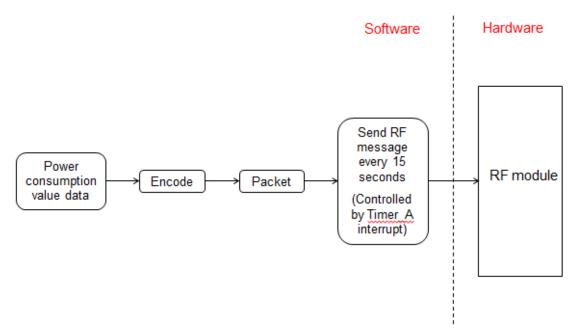


Figure 5.4 The flowchart of sending the value from MCU to RF module using SPI communication

As can be seen from Figure 5.4 above, Timer_A interrupt is used to control the SPI communication to the RF module. Since it is expected to send the message one time every 15 seconds in the project plan and the P2 interrupt service routine is called every 10ms, a variable with the value 1500 is added in the interrupt service routine to control an "if" statement, the function to send the packet data from the MCU to the RF module is written under this "if" statement, then the function to send the packet data will be called once when the Timer_A interrupt service routine is called 1500 times, thus, the time interval for the event to report is:

 $10 \text{ ms} \times 1500 = 15 \text{ s}$ (5.18)

That means the function to send the packet data from the MCU to the RF module is called once every 15 seconds, so the measured power consumption value is sent to the ELIQ Display Unit from the Smart-plug system through the RF communication once every 15 seconds.

5.4 Wireless communication

When the RF module is used to transmit the data to another device using the wireless communication, the data input from the SI pin of the RF module will go into the TX FIFO firstly, then the packet handler, the interleaver, the modulator, the frequency synthesizer and the power amplifier, the signal will go to the positive RF output port pin and negative RF output port pin and

then the antenna for the wireless communication.

When the RF module is used to receive the RF signals from another device using the wireless communication, the received positive RF signal and negative RF signal from the wireless communication will go to the LNA (low noise amplifier) firstly, then the down-conversion mixers, the analog-to-digital converters, the demodulator, the packet handler, and finally, the data packet will go to the digital interface to be transferred to the MCU through the SPI communication.

The 868 MHz ISM band is used for the wireless communication. GFSK(Gaussian shaped frequency-shift keying) is chosen to be the modulation mode used in this project. GFSK is a type of frequency shift keying modulation that uses a Gaussian filter to smooth the positive or negative frequency deviations, which represents a binary "1" or "0". A GFSK modulator is similar to a FSK modulator, except that before the baseband waveform (levels –1 and +1) goes into the FSK modulator, the signal is passed through a Gaussian filter to make the transitions smoother in order to limit the spectral width of the signal. Gaussian filtering is a standard way for reducing the spectral width of the signal and is called "pulse shaping" in this application. In this project, the carrier frequency is 868MHz with a deviation of 20KHz, the data rate is 38.4KBaud, the digital channel filter bandwidth is 100KHz and the output power is +10dBm.

5.5 Working as a repeater

This Smart-plug device can also repeat the received ELIQ protocol RF message for other ELIQ devices to work as a wireless repeater. The P2 I/O interrupt is used to control the received RF message from some transmitter devices such as an ELIQ sensor. After processing the received RF message in software, the same RF message will be transmitted outside to the receiver devices such as ELIQ Display unit or ELIQ wireless hub. With this function of repeating the message, the power of the RF message signal can be amplified and the wireless communication distance can be extended largely by using the Smart-plug device system.

As can be seen from Figure 4.5, the schematic of the communication circuit between the MCU and the RF module presented in section 4.5, the port pin P2.0 of the MCU is connected to the GIO pin of the RF module. The GDO0 pin of the chip CC1101 is attached to the GIO pin of the RF module and the GDO0 signal from the chip CC1101 is used to indicate data packet received. When CC1101 receives the RF message from other ELIQ devices via the wireless communication, the high-to-low transition occurs in the GDO0 signal from the chip CC1101 to the GIO pin of the RF module then to the port pin P2.0 of the MCU, the interrupt flag for P2.0 is set and the P2 interrupt is triggered, then fetching and processing the received RF message is implemented in the P2 interrupt service routine. The received message data will be transferred serially to the MISO pin of the MCU from the SO pin of the RF module. When the MCU receives the data packet from the RF module, the data packet will be unfolded to remove the preamble bits and synchronization words to get the useful data. Then the same data will be encoded and packeted again to transfer to the RF module from the MCU immediately via the SPI interface, the message data will still be transferred serially to the SI pin of the RF module from the MOSI pin of the MCU as same as the analysis in section 5.3.

Figure 5.5 below shows the flowchart of repeating the RF message when the Smart-plug system working as a repeater.

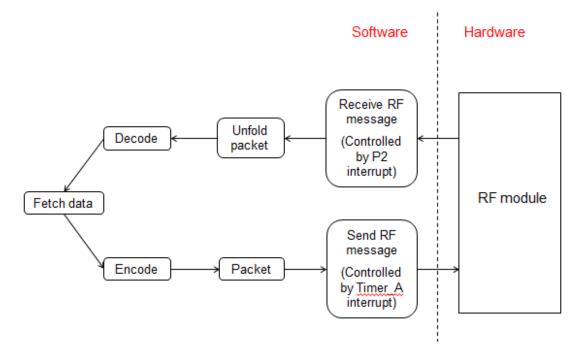


Figure 5.5 The flowchart of repeating the RF message when the Smart-plug system working as a repeater

6. Visual support

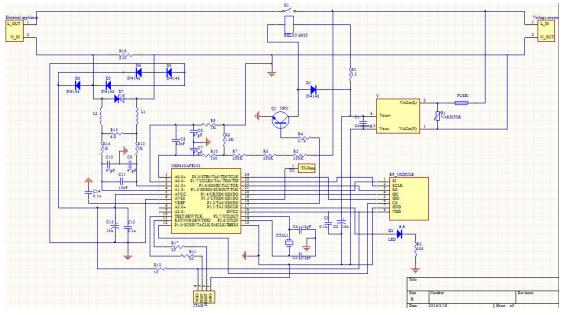


Figure 6.1 below shows the schematic of the whole circuits on the Smart-plug electrical board.

Figure 6.1 The schematic of the whole circuits of the Smart-plug system

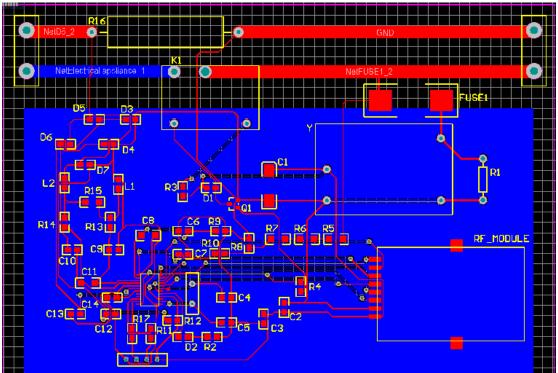


Figure 6.2 below shows the PCB layout of the whole circuits on the Smart-plug electrical board.

Figure 6.2 The PCB layout of the whole circuits of the Smart-plug system

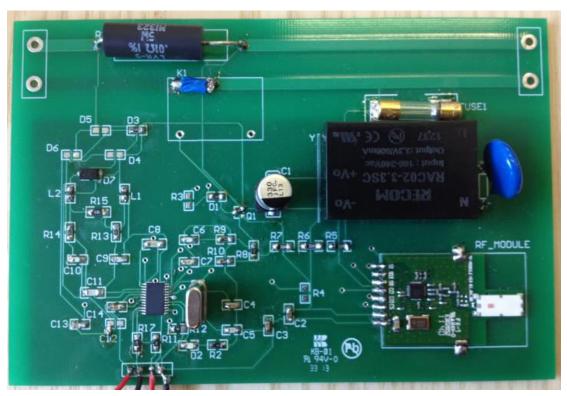


Figure 6.3 below shows a real photo of the Smart-plug electrical board.

Figure 6.3 The real photo of the electrical board of the Smart-plug system

7. Results

This ELIQ Smart-plug device system has achieved its basic expected functions that measuring the power consumption value of the connected electrical appliance and sending the data message which contains the measured power consumption value of the electrical appliance to the ELIQ Energy Display Unit via the RF wireless communication once every 15 seconds to display to the households successfully. Table 7.1 below shows the testing results displayed on the ELIQ Display Unit when measuring one 25W light and the different number of the same lights in parallel with the power consumption value of one light is 185W.

	Rated power value of the light	Measurement results
One 25W light	25W	37W
One 185W light	185W	180W
Two 185W lights in parallel	370W	362W
Three 185W lights in parallel	555W	540W
Four 185W lights in parallel	740W	716W
Five 185W lights in parallel	925W	895W
Six 185W lights in parallel	1110W	1050W

Table 7.1 The testing results of measuring the electrical appliances

with different power consumption value

When measuring two 185W lights in parallel, whose rated power value is 370W, the ELIQ Display Unit can display the power consumption value 362W, in this case, the accuracy of the power consumption measurement is:

$$\frac{^{362w}}{^{370w}} \approx 97.84\% \tag{7.1}$$

This is the best measurement accuracy among a series of tests above.

This ELIQ Smart-plug device system can also switch on or switch off the power supply to the connected electrical appliance according to whether the measured power consumption value of the connected appliance is less than or more than 2500W. In addition, this ELIQ Smart-plug device system can work as a repeater to repeat the same RF message for other ELIQ devices in order to amplify the power of the RF message signal and extend the RF wireless communication distance largely.

8. Discussion

8.1 Appliance with small power consumption cannot be measured accurately

As the tested results shown in the chapter 7 above, when measuring the 25W light, the ELIQ Display Unit will display the power consumption value of the light 35W. It is observed that the electrical appliance with small power consumption value which is less than 100W cannot be measured accurately to achieve the expected range of the accuracy degree of the measured result by trying several times of testing with different electrical appliances.

When measuring the electrical appliance with the power consumption value is about 25W, the effective current value on the appliance is:

$$\frac{25W}{230V} \approx 0.1087A$$
 (8.1)

The effective voltage value on the sampling resistor is:

 $0.1087A \times 0.01 \Omega = 0.001087V$ (8.2)

So the peak voltage value on the sampling resistor is:

$$0.001087V \times \sqrt{2} = 0.001537V \tag{8.3}$$

Since the resolution is :

resolution
$$\Delta = \frac{V_{FSR}}{2^{15}+1} = \frac{0.6V}{32768} \approx 0.0183 \text{mV}$$
 (8.4)

The digital output value transferred from the peak voltage value on the sampling resistor to the analog input pairs of the SD24_A A/D converter is:

$$\frac{0.001537V}{0.0183mV} \approx 84 = (000000001010100)_2$$
 (8.5)

That means the number of intervals from the lowest peak point to the highest peak point for the sine wave signal of the voltage on the sampling resistor is $84 \times 2 = 168$, there are only 168 steps from the lowest peak point to the highest peak point. Compared to $2^{15} \times 2 = 32768 \times 2 = 65536$ steps from the lowest peak point to the highest peak point for the full scale voltage value of the SD24_A A/D converter, 168 is quite small. Since 64 points need be sampled in one sine-wave period of the voltage to the analog input pairs of the SD24_A, it cannot be distinguished clearly for different sampling points to different steps if there are only 168 steps from the lowest peak point to the highest peak point of the signal. In addition, if noise is present in the signal, this will influence the calculation of the RMS value of the current value significantly since the digital output value can change dramatically due to the total number of intervals from the lowest peak point to the highest peak point being only 168. These factors will lead to the

circumstance that the electrical appliance with small power consumption value which is less than 100W cannot be measured accurately.

8.2 Sampling resistor with resistance tolerance1% still influences the accuracy of

measurement

The sampling resistor chosen to be used on the Smart-plug device electrical board is LOB5 R010 FLF, the 0.01Ω metal film current sense resistor with a rated power of 5W and the resistor tolerance is ±1%. As discussed in section 2.3.6.2, the SD24_A A/D converter has 16-bit resolution, the number of the intervals for the full scale voltage to the analog inputs of the SD24_A A/D converter is 65536 from the lowest peak point to the highest peak point of the sine wave signal. That means the signal will be divided into 65536 steps from the lowest peak point to the highest peak point, so if measuring a 100W electrical appliance, the number of intervals from the lowest peak point to the highest peak point in the signal can be inferred from the following calculations:

The effective current value on the sampling resistor is:

$$\frac{100W}{230V} \approx 0.4348A$$
 (8.6)

The effective value of the voltage to the analog input pairs of the SD24_A A/D converter is: $0.4348A \times 0.01 \Omega = 0.004348V$ (8.7)

The peak value of the voltage to the analog input pairs of the SD24_A A/D converter is: $0.004348V \times \sqrt{2} = 0.006149V$ (8.8)

The digital output value transferred from the peak voltage value on the sampling resistor to the analog input pairs of the SD24_A A/D converter is:

$$\frac{0.006149V}{0.0183mV} \approx 336 = (0000000101010000)_2$$
(8.9)

The number of intervals from the lowest peak point to the highest peak point for the sine wave signal of the voltage input to the analog input pairs of the SD24_A A/D converter is:

$$336 \times 2 = 672$$
 (8.10)

That means if measuring the 100W electrical appliance with such small power consumption, the signal from the lowest peak point to the highest peak point will be divided into 672 steps.

As the resistance tolerance of the sampling resistor chosen to be used in this project is 1%, the deviation of the voltage on the sampling resistor can reach 1%. That means if measuring the electrical appliance with 100W power consumption and the resistance deviation of the sampling resistor is 1%, there are about 6 steps or 7 steps deviated of the digital output compared to the

accurate converted result after the analog-to-digital conversion. If measuring the electrical appliance with larger power consumption value, there will be more steps deviated of the digital output compared to the accurate result.

Thus, if choosing the sampling resistor with a resistance tolerance 1%, the result of the calculation still cannot be accurate using the MCU with the 16 bits A/D converter, since when transferring the analog decimal data to the digital binary data, there will be not any difference among the 16 bits, 12 bits or 10 bits A/D converters in this case.

The bottomline is that in order for the Smart-plug device system to measure the power consumption value of the connected appliance more accurately, a sampling resistor with much lower resistance tolerance, such as 0.1% or 0.01%, must be used. However, the price of the metal film current sense resistor with only 0.1% or 0.01% resistance tolerance is much more expensive than the price of the metal film current sense resistor with 1% resistance tolerance, so the tradeoff between the price and the measurement performance of the Smart-plug device should be considered seriously when designing this product.

8.3 Component selection for the control unit

There are multiply choices of choosing the component to switch on or off the power supply to the connected appliance. For instance, both of a relay and a triac can implement the function of switching on or off the circuit. Table 8.1 below shows the comparison between the relay and the triac. The size of the triac is much smaller than the relay which can be searched on the market commonly, and only a very small current (which is about 10mA) can trigger the gate of the triac to switch on or switch off the circuit, however, the relay need large current which is about 60mA for the coil to make the voltage on the coil is more than the pick-up voltage value to switch on or switch off the circuit. Since the maximum output current from one I/O port pin of the MCU MSP430AFE233 is only about 10mA~15mA, that means the NPN transistor and some other electronic components need be added in the circuit on the board to amplify the output current from one I/O port pin of the MCU to achieve at enough current value for the relay to control the switch on or off status of the circuit, while the NPN transistor circuits need not be used to simplify the circuit and save the components and area of the board if choosing the triac as the control unit component [18][19]. Although the triac has these advantageous compared to the relay, the power dissipation of the triac is much higher than that of the relay when the current through it achieves at large value. The power dissipation of the triac increases along with the current through it increases, for example, at 18W, if the current through the triac is more than 10A [18]. In addition, the price of the triac is much more expensive a relay. In overall considerations above, as the power dissipation of the whole Smart-plug device system and the price of the components on the board are important factors, the relay is eventually chosen to be control unit component to switch on or off the power supply to the appliance in the live wire. The comparison of the relay and the triac is shown in Table 8.1 below.

Relay	Triac
Large size	Small size
Cheap price	Expensive price
Low power dissipation (500mW)	High power dissipation (0 – 18W according to current) [18]
Need large current through the coil to control switch on/off (at least 60mA)	Small current can trigger gate (10mA) [18]
Need driver circuit with NPN transistor to amplify current	Do not need driver circuit with NPN transistor

Table 8.1 The comparison between the relay and the triac

8.4 A/D converter output need load

The function of the A/D converter RAC02-3.3SC is to transfer the 230V AC signal from input to 3.3V DC signal to the output. In this Smart-plug electrical board, the A/D converter RAC02-3.3SC is used to provide the supply working voltage to both of the MCU and the RF module. When soldering the components on the Smart-plug electrical board, soldering the A/D converter RAC02-3.3SC which is the power supply device on the board should be the first step because it is necessary to detect whether the output voltage is really 3.3V DC to ensure that the output voltage is safe for both of the MCU and the RF module. However, if just soldering the A/D converter RAC02-3.3SC on the board without any load at the output and connecting the input of the A/D converter to the 230V AC mains, the detected voltage value of the output displayed on the multimeter is about 4.2V DC which is higher than the rated output voltage 3.3V DC. That is because the minimum load for proper working of the A/D converter is 10% then the specification of the A/D converter is valid. At no load condition, the converter will not be damaged but its output will be higher than the rated output voltage. So it is necessary to connect some load such as resistors on the output when detecting the output voltage of the A/D converter. After soldering all of the components including the MCU and the RF module on the Smart-plug electrical board, the output voltage is stable 3.3V DC when using the multimeter to detect as there are enough load connected to the output of the A/D converter, so it will be safe supply working voltage for both of the MCU and the RF module.

8.5 Acquiring relay components

The 3v relay is hard to find on the market while the 5V relay is easy to find on the market. In the relay RECOM RAC02-05SC, the coil rated voltage is 5V and the coil resistance is 45 Ω so the rated coil power is 200mW. When the voltage value on the coil reaches the coil pick-up voltage value of 2.25V, the mechanical switch device will be closed under the electromagnetic force from the coil then the electrical appliance will be connected to the household mains, so a LDO (low-dropout regulator) needs to be used in the circuit if choosing the 5V relay.

The LDO can transfer the DC voltage signal in a range from the input to the stable DC voltage to the output. If choosing the relay HKE V6-S-DC5V to control switching on or off power supply to the connected appliance, the LDO which can transfer the 5V DC signal from input to the stable 3.3V DC signal to the output needs to be added to the circuit and the A/D converter should be changed to the type with 5V DC output. The LDO HT7133 is a three terminal voltage regulator implemented in CMOS technology with features like low power consumption, low voltage drop and low temperature coefficient. It allows an input voltage up to 24V DC and it is available with the fixed output voltage 3.3V DC. In this case, the type HT7133 is suitable to be chosen as the LDO and the RECOM RAC02-05SC is chosen to be the A/D converter. Figure 8.1 below shows the block diagram of the internal hardware circuit inside the LDO HT7133. Figure 8.2 below shows the schematic of peripheral circuits for the LDO HT7133. There are one 10uF capacitor between the Vin port and common GND, as well as one 10uF capacitor between the Vout port and common GND to remove the possible residual AC voltage signal combined with the DC voltage signal together.

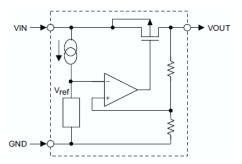


Figure 8.1 The block diagram of the internal hardware circuit inside the LDO HT7133 [20]

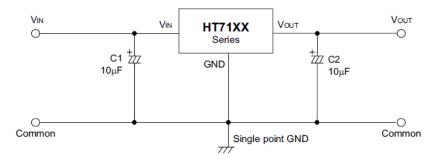


Figure 8.2 The schematic of peripheral circuits for the LDO HT7133 [20]

The output pin Vout+ of the A/D converter RECOM RAC02-05SC will be connected to the relay HKE V6-S-DC5V through a resistor since the voltage on the coil needs to exceed the pick-up voltage 3.75V to control the switch device inside the relay. It will be also connected to the input pin Vin of the LDO HT7133 to give the 5V DC signal for the LDO HT7133. Then the output pin Vout of the LDO HT7133 will be connected to the VDD pin of both of the MCU and the RF module to provide the 3.3V DC voltage signal as the supply working voltage for both of the MCU and the RF module.

8.6 Width and thickness of the copper wire on the PCB board

The ELIQ Smart-plug device can measure the power in an electrical appliance with the power consumption value ranges from 2W to 3000W. That means the maximum value of the current through the live wire and neutral wire can reach 13A, so the copper wire of the live line and the neutral line should be wide enough and thick enough in order to make the current with such large value flow through safely.

In this PCB layout design, the width of the copper wire of the live line and neutral line is set to be 3mm (118.11mil), the width of the copper wire of 3.3V DC signal is set to be 0.5mm (19.685mil), and the width of the copper wire of other small signal is set to be 0.254mm (10mil). The thickness of the copper wire is chosen to be 70um when manufacturing the PCB board.

9. Conclusion

9.1 Summary

The work progress of the project has achieved the initial goals, that is, the electrical appliance with the power consumption in a range from 100W to 1000W can be measured accurately by using this Smart-plug device system and the RF message which contains the measured power consumption value of the electrical appliance can be sent to the ELIQ Energy Display Unit via the RF wireless communication once every 15 seconds to display to the households. In addition, this Smart-plug device system can work as a repeater to repeat the RF message for other ELIQ devices, which can amplify the power of the RF message signal and extend the RF wireless communication distance effectively.

MSP430AFE233 is a type of suitable microcontroller unit to be the core chip on the Smart-plug device electrical board to implement the power consumption measurement of the connected appliance, switching on or off the power supply to the connected appliance and handle communication with the RF module. Besides the features of small size, ultra-low power consumption and cheap price, the MCU MSP430AFE233 integrates the SD24_A A/D converter which has a pair of analog inputs and can transfer the differential value of the analog voltage signal from the analog input pairs to the digital signal directly. Thus, the circuits on the Smart-plug electrical board can be significantly simplified without designing the level shifter circuit to transfer the bipolar voltage value to the unipolar voltage value, the number of components on the Smart-plug electrical board can be reduced and the area of the board can be smaller. The SD24 A interrupt is used to control sampling 3200 points from the signal in one second to calculate the RMS values of both of the voltage and current, the Timer A interrupt is used to control so that the RF message which contains the measured power consumption value of the connected appliance is sent to the ELIQ Energy Display Unit every 15 seconds, the I/O interrupt of P2 port is used to detect and receive the RF message from other ELIQ devices when the Smart-plug device working as a repeater.

The RF module with the core chip CC1101 is used to implement the wireless communication between different ELIQ devices. The Chip CC1101 is a low-cost sub-1 GHz transceiver designed for very low-power wireless applications in the ISM band at 868MHz. The RF transceiver is integrated with a highly configurable baseband modem. The chip CC1101 can be controlled by the MCU via the SPI interface.

9.2 Future work

Now the RECOM RAC02-3.3SC AC/DC converter is used as the power supply for both of the MCU and the RF module and controls the current on the coil of the relay by transferring the 230V AC signal from mains to the 3.3V DC signal. However, the size of the RECOM RAC02-3.3SC AC/DC converter is too large and the price of the RECOM RAC02-3.3SC AC/DC converter is too expensive, about \$16 per piece. If the design of the Smart-plug device is put in mass production, the whole

cost of the components on the Smart-plug device system must be considered and the area of the Smart-plug device electrical board should be minimized. Thus, designing the power supply circuit using resistors, capacitors, diodes and some other electronic components for the MCU, the RF module and the relay is necessary to save both of the cost and the area of the Smart-plug device electrical board. It is important to notice that the output current from the designed power supply circuit should be sufficient enough to drive the MCU, the RF module and the coil of the relay. In addition, the empty space between the different components on the ELIQ Smart-plug device electrical board should be as small as possible to make the board layout of the product more compact than the PCB layout designed in this project, which is also helpful to reduce the cost of the materials and the size of the product.

The designed Smart-plug device system can measure the power consumption value of the connected electrical appliance and send the RF message data which contains this measured power consumption value to the ELIQ Energy Display Unit to let the households know the current power consumption value of the electrical appliances in a house until now. Besides, this Smart-plug device system is also expected to send the measured power consumption value to the ELIQ Hub, which is also implemented with the RF module which is similar to the work already done. As far as the future work, it is expected to achieve the function that using the intelligent cellphone to implement the remote monitor to control the switching on or off status of the connected electrical appliance according to the power consumption value read from ELIQ online. Furthermore, the Smart-plug device system is also planned to control the switching on or off status of the connected electrical appliance automatically based on high demand time or low demand time of the electricity utilization in a city by importing the specialized algorithm in software. All of these features will bring lower cost and reduced more energy consumption.

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