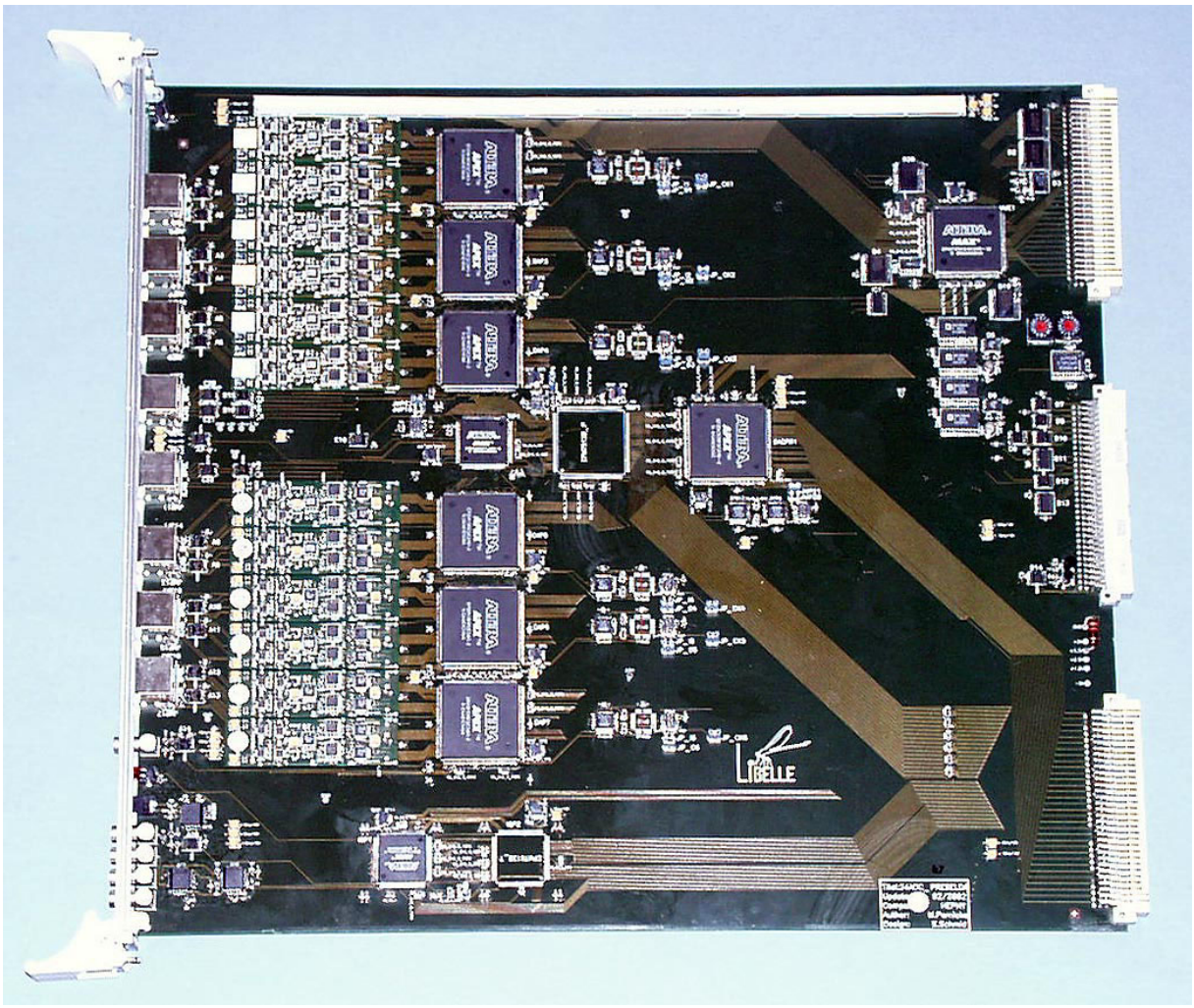

FADCTF system

Belle SVD 2.0 readout

BELLE

HEPHYVIENNA

User's Manual

V1.05 • 31 July 2002

DISCLAIMER

The FADCTF is a complex electronic system which can be damaged if handled improperly. In particular, the following guidelines must be respected by the operator. We decline any responsibility for errors, damage or injury resulting from such misuse.

- **Crate and modules belong together.**

Do not use the VME modules (FADCTF, Sequencer, PCI-Link) in a VME crate other than the one provided with the system.

The user defined ±V1 and ±V2 rails are used to supply special voltages to the FADCTF modules; while the Sequencer board provides ±12V which is required by the Sparc interface. Moreover, the FADCTF modules are mechanically coded with the corresponding counterparts in the crate.

- **Always power off to change modules.**

Never remove or insert a VME module of the system when the crate power is on. Ensure that each module is fully inserted (needs some force).

The VME interface Altera (EPM7256S; 5V core) is not specified for hot-swapping. It can take damage by contention between logic levels and power supply during plugging of the module or in case of bad contact.

- **Double-check the VME base addresses.**

It is extremely important that each FADCTF module has the correct VME base address set.

Altera programming and I/O interfacing to neighboring modules as used by the L0 trigger processor rely on the correct VME base address setting which corresponds to the mechanical coding. If the address is wrong and outputs of two modules are connected, both modules will be damaged by overheating.

- **Do not use the JTAG feature.**

Programming Altera devices on the FADCTF modules is for experts only.

All Altera devices (except for the VME protocol interface) can be programmed by the JTAG bus that is accessible by VME. Obviously, much harm can be done by improper use of this feature. The worst case is to blow up all Altera devices on the board.

Table of Contents

Abstract

This is a general description of the modules of the FACD system. A separate manual is dedicated to the VME connectivity of the system. Additional information for the expert such as electric schematics, the logic circuits inside the Altera units along with bus systems, timing, trigger simulation etc. are provided in a separate folder but are not contained herein.

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Overview

Introduction

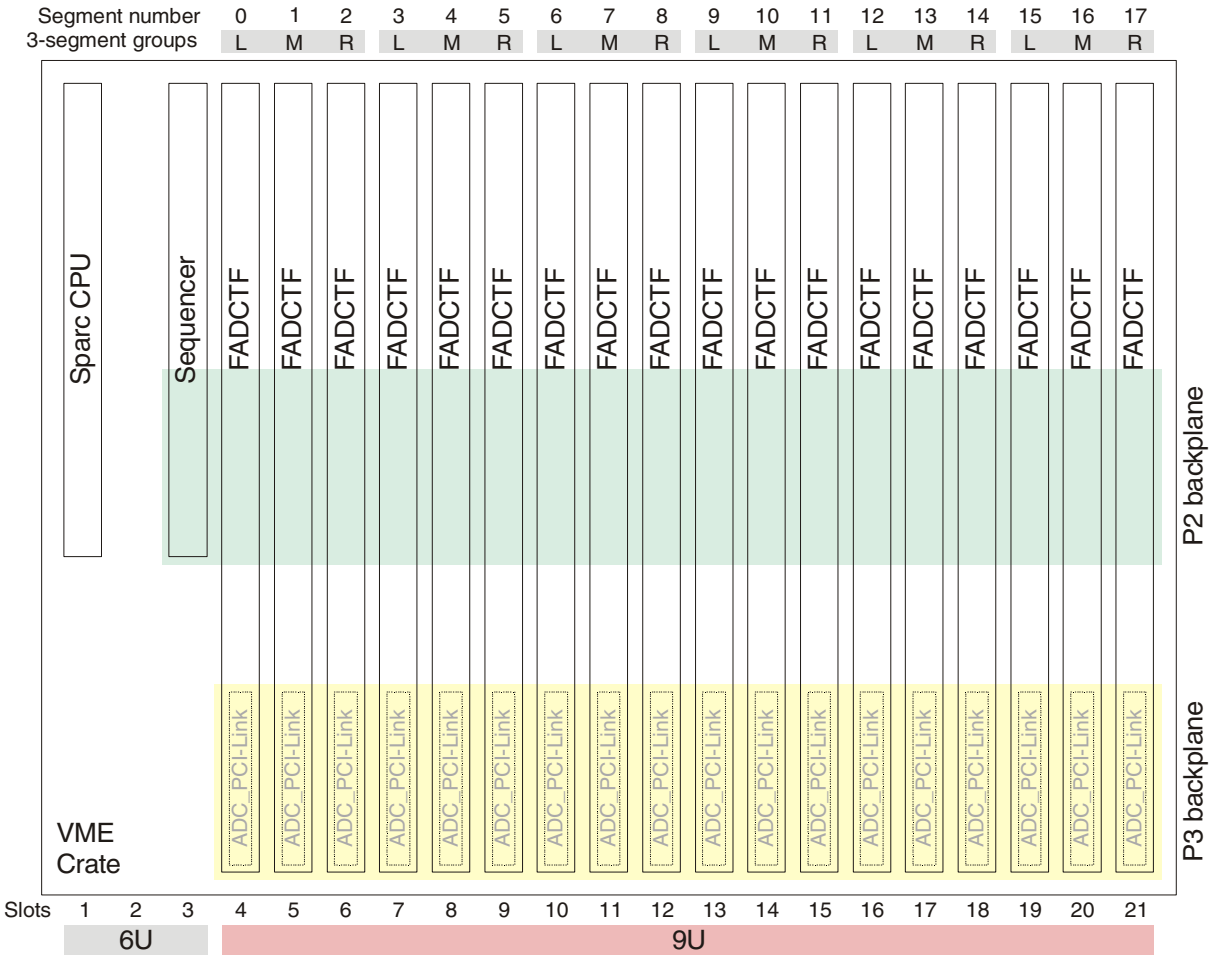
The FADC system receives the analog output data of the VA1TA readout chip via the REBO chain and digitizes them, finds tracks on a segment basis (trigger L0) by analyzing the Fast-Or signals, performs a simple hit finding algorithm and presents those data to the trigger L1.5 logic, buffers up to 5 accepted events and finally passes data on to the DAQ farm PCs.

Modules of the system

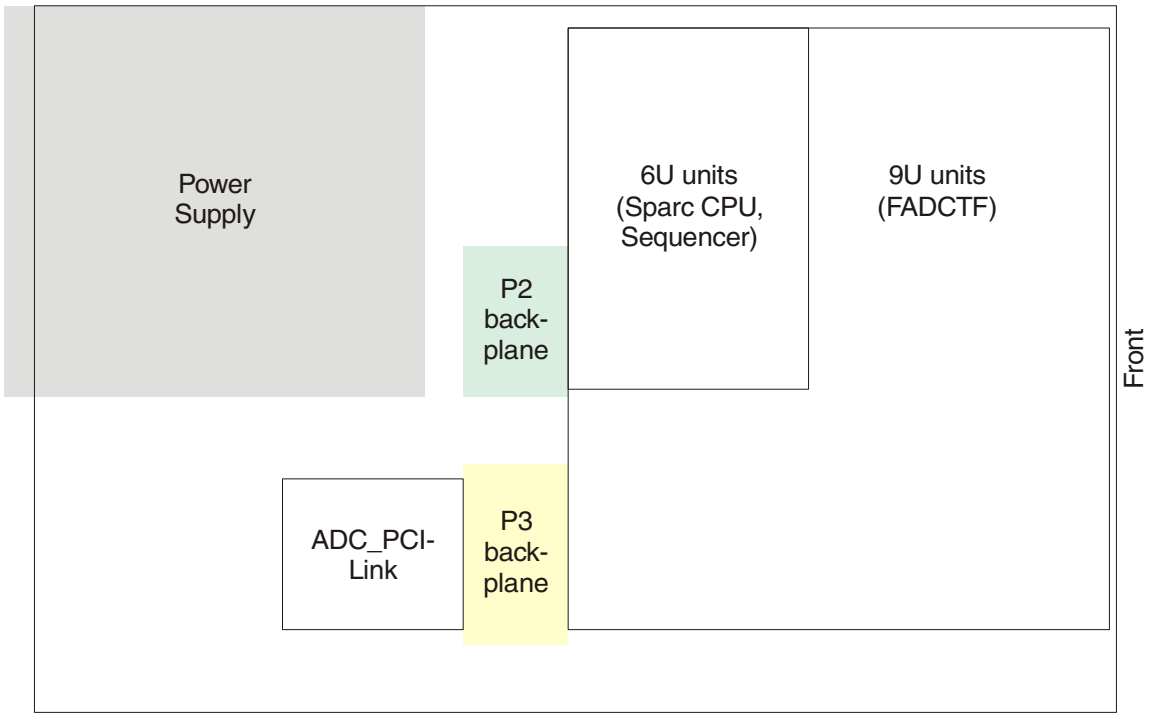
The FADC system consists of two 9U VME crates, one for the readout of rφ and the other for rz directions (please note that the detector strips run along the z axis in the rφ readout subsystem and vice versa). Each crate has 3 slots for 6U modules and 18 9U slots, which are filled with

- 1 Sparc CPU-50 crate controller (6U VME)
- 18 FADCTF mother boards (9U VME; equipped with 12 DB_2xADC daughter boards each)
- 1 sequencer board (6U VME; slot number must be 3 or above!)
- 1 custom P2 backplane (distributing timing and control signals)
- 1 custom P3 backplane (for FADCTF interconnection of Fast-Or signals with neighbor modules for the L0 processor and event signals for the possibility of a simple L1.5 trigger; and PCI-Link connection)
- 18 ADC_PCI-Link boards (sitting on the P3 backplane)

The diagram below visualizes these components.



FRONT VIEW



SIDE VIEW

Each FADCTF board will be mechanically coded such that it can only be inserted in either "L", "M" or "R" positions (e.g. "L" modules are allowed in slots 4,7,10,13,16,19). This is done for reasons of the L0 trigger. The ADC_PCI-Link boards are located on the back side of the crate. In order to provide the control signals to the P2 backplane, the Sequencer board must be installed in slot 3 (or higher).

IMPORTANT: The VME crate **MUST** be switched off whenever any module is inserted or removed since the Altera VME protocol FPGA may be damaged if hot-plugged. We decline any responsibility for the consequences of such action.

Power Consumption

The 9U VME crates can be operated with both European and US/Japanese power, as shown below.

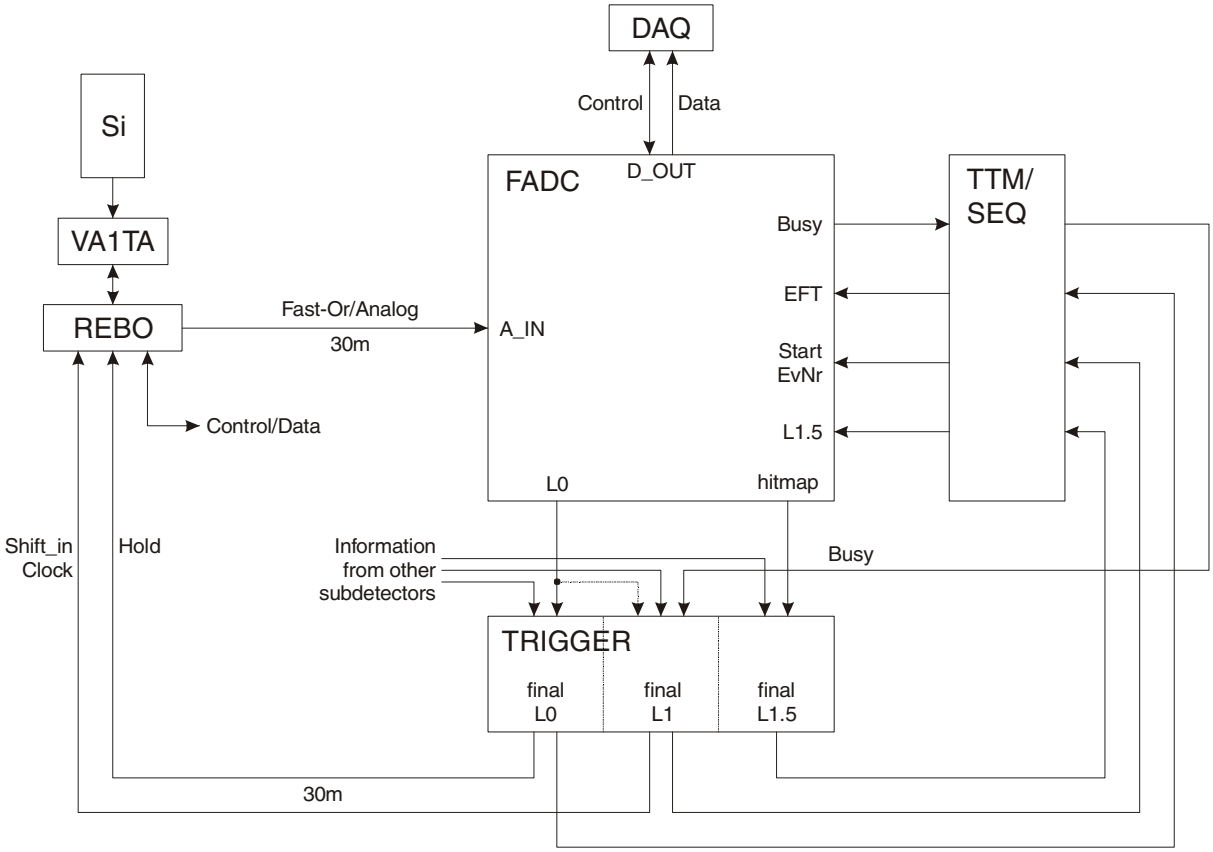
AC Input	Range
Voltage	92…265V
Current	16A max.
Frequency	47…63Hz

The current consumption of one fully equipped crate at the low voltage side is shown in the table below.

Rail [V]	Current [A]
+1.8	+12
+2.5	+16
+3.3	+60
+5.0	+33
– 5.0	– 19
Power	520W

Neighborhood

The FADC system is embedded within the SVD readout system and communicates with several parts. The regular data flow should be illustrated by the block diagram below. This figure is simplified and shows only parts which are relevant for the data flow with the FADC system. The description of the data flow is very coarse and lacks a lot of details as well, since it is only meant as a general introduction to the FADC functionality.



Let us assume that there are no triggers or data transfers are pending. In this idle condition, particles corssing the silicon detectors generate Fast-Or signals in the VA1TA front-end chips which are sent to the FADC via the REBO/MAMBO system. Only a subset of all possible Fast-Or combinations represent valid particle tracks. The FADC constantly watches out for such combinations and asserts an L0 trigger if detecting a track.

This information, when in coincidence with trigger information from other subdetectors, is used to generate a Hold signal for the VA1TA chips. At the same time, EFT toggles to turn off the Fast-Or detection during the potential subsequent readout phase. The delay between particle crossing a silicon detector and Hold signal arriving at the VA1TA chips must match its shaping time. As soon as the Hold is asserted, a snapshot of the detector signals is stored in the sample/hold circuits inside the VA1TA chips. Thus, some time is available for a more sophisticated trigger decision by the L1 system, which is fed by other subdetectors and possibly the L0 information of the SVD as well. In case of rejection, EFT is reset and the system is back in idle state.

An L1 trigger enables the shift_in and clock signals required for the VA1TA readout and at the same time communicates this condition to the FADC. After reception of start signal and event number, which are distributed via the TTM system and the Sequencer board, the FADC digitizes and stores the strip data arriving on the analog inputs (A_IN) in an internal FIFO which can buffer up to 4 events including an event and channel (0...11) number and start/stop bits (16 bits in total).

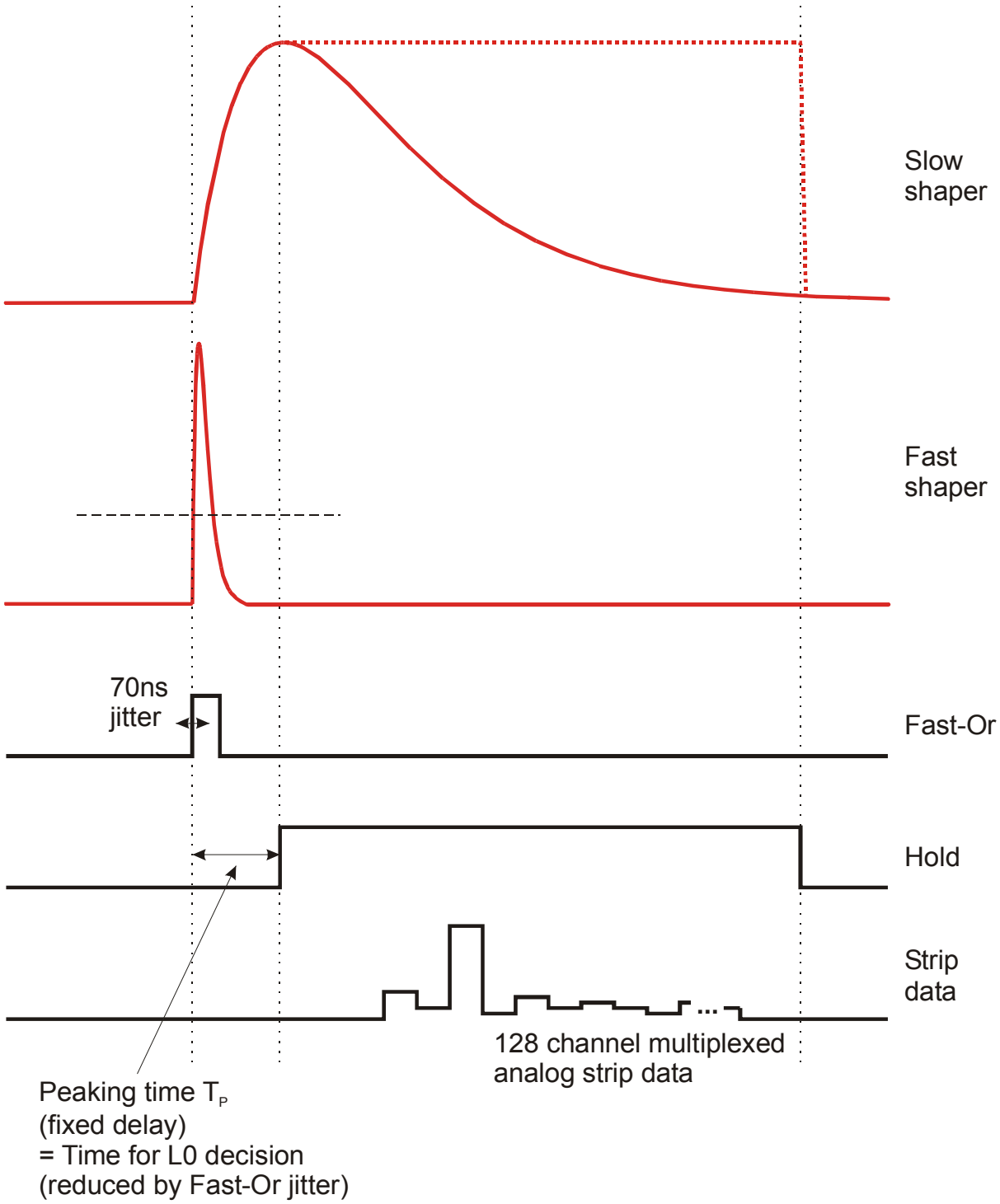
Moreover, the strip data are processed and passed on to the L1.5 trigger already during reception. This operation requires a threshold value for each strip, which must have been stored in an internal memory before. This threshold basically consists of the pedestal value plus a few times the channel noise and is compared to the current data, yielding a digital hit map. This coarse hit map is immediately sent to the L1.5 trigger, which searches for tracks on the strip level. If there is no positive L1.5 decision before the next start signal, the following event overwrites the current memory, thus discarding the previous data.

Upon reception of a L1.5 accept, the stored event data will be transferred to another internal FIFO ("final memory") with a maximum capacity of 2 events. From there, the data is pushed out through the DAQ PCI links to the Linux farm.

Due to the FIFOs inside the FADC, new signal inputs may arrive while earlier events are still in the queue. However, if a total of 5 FIFOs are filled, a busy signal is sent out which vetoes any further triggers until the current data are processed and the space for one event in the DAP FIFOs is freed. As a general rule, there is still room for one more event after the busy notification is sent out.

VA1TA/Rebo

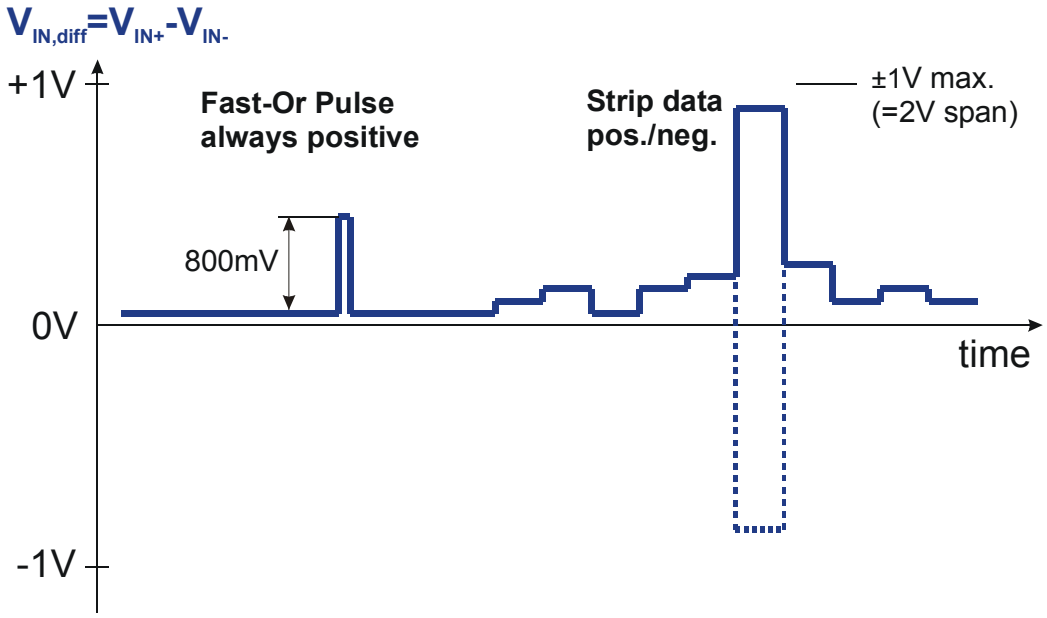
The VA1TA output signals are amplified by the REBO repeater boards. The typical waveforms are shown in the graph below.



The chip internal outputs of slow and fast shaper of a single channel are shown when a particle hit occurs in that particular channel. If the (tunable) threshold for the fast shaper is exceeded, a short digital pulse is generated and combined from all 128 channels with an OR logic, hence known as "Fast-Or", which is sent to the FADCTF. After the peaking time T_P, which is in the order of 600ns, a Hold signal has to be applied to the chip, such that the peak value of the slow shaping curve is stored in the chip internal sample/hold circuit. This condition is indicated by the dashed curve in the top waveform. When shift_in and clock signals are presented to the chip, it writes out the serialized strip data in analog form.

Depending on which side of the detector is read out, signal amplitudes may be positive or negative w.r.t. the pedestal, but the Fast-Or is always positive. Note that the Fast-Or is asynchronous and thus can occur at any time, unlike the synchronous strip data, which are later sent on the same line provided that shift_in and clock signals are received by the VA1TA.

The REBO sends differential signals to the FADC system, which are terminated with 2x50Ω against GND there. The expected levels at the input of the FADCTF are shown below.



The width of the Fast-Or pulse is approximately 100…130ns (with a jitter span of up to 70ns across the inputs), while the strip data is read out at 5MHz (corresponding to a period of 200ns). For test purposes, single channels can be displayed in transparent mode, where the fully shaped waveform is presented on the analog lines.

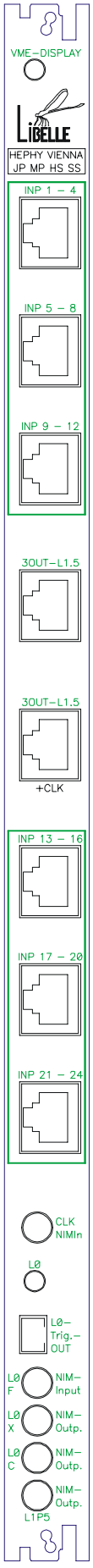
Modules

1 FADCTF

These boards are the core of the FADC system, containing a lot of logic functionality within several Altera FPGAs. Moreover, 12 DB_2xADC daughter boards digitize the analog signals and search for Fast-Or pulses.

1.1 Mother board (24ADC_PRESELDA)

The front panel layout and the side view of the module are shown below.



VME → Indicates VME bus activity

A_IN2 (INP 1-4) →

1...input 1 +	2...input 1 -
3...input 2 +	4...input 2 -
5...input 3 +	6...input 3 -
7...input 4 +	8...input 4 -

A_IN3 (INP 5-8) →

1...input 5 +	2...input 5 -
3...input 6 +	4...input 6 -
5...input 7 +	6...input 7 -
7...input 8 +	8...input 8 -

A_IN4 (INP 9-12) →

1...input 9 +	2...input 9 -
3...input 10 +	4...input 10 -
5...input 11 +	6...input 11 -
7...input 12 +	8...input 12 -

Analog inputs (upper half)

hitmap1 (3OUT-L1.5) ←

1...hitmap 0 +	2...hitmap 0 -	(corresponds to A_IN2)
3...hitmap 1 +	4...hitmap 1 -	(corresponds to A_IN3)
5...hitmap 2 +	6...hitmap 2 -	(corresponds to A_IN4)
7...hitmap 3 +	8...hitmap 3 -	(corresponds to A_IN5)

hitmap2 (3OUT-L1.5) ←

1...hitmap 4 +	2...hitmap 4 -	(corresponds to A_IN6)
3...hitmap 5 +	4...hitmap 5 -	(corresponds to A_IN7)
5...n/c	6...n/c	
7...strobe +	8...strobe -	

A_IN5 (INP 13-16) →

1...input 13 +	2...input 13 -
3...input 14 +	4...input 14 -
5...input 15 +	6...input 15 -
7...input 16 +	8...input 16 -

A_IN6 (INP 17-20) →

1...input 17 +	2...input 18 -
3...input 18 +	4...input 18 -
5...input 19 +	6...input 19 -
7...input 20 +	8...input 20 -

A_IN7 (INP 21-24) →

1...input 21 +	2...input 21 -
3...input 22 +	4...input 22 -
5...input 23 +	6...input 23 -
7...input 24 +	8...input 24 -

Analog inputs (lower half)

CLK_TN → [NIM] Optional clock input (20MHz, alternative to TTM/Sequencer)

L0 → Indicates that a L0 trigger track was found

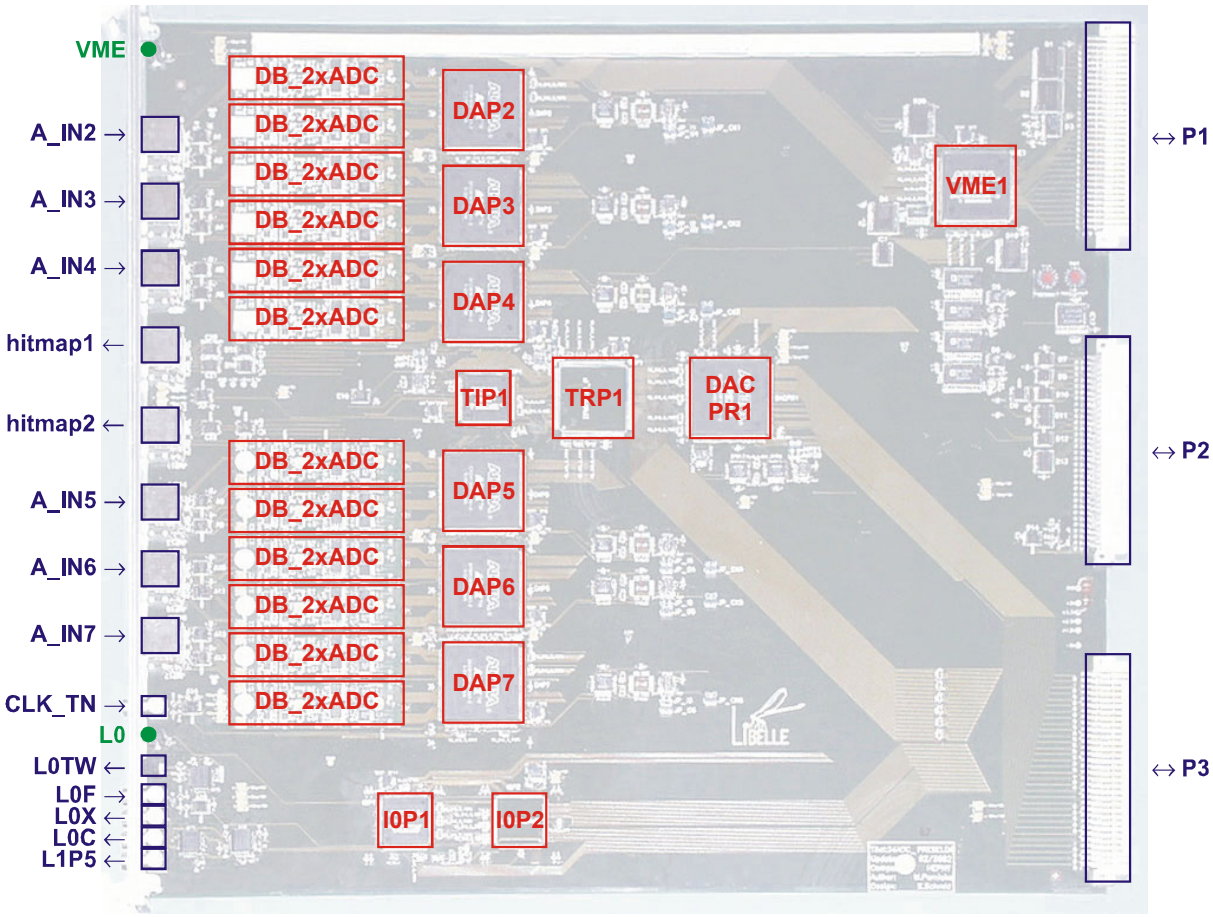
L0TW ← [Differential ECL] Output to the L0 trigger (width=120ns)

L0F → [NIM] unused (optional: L0 input from TOF segment)

L0X ← [NIM] Output to the L0 trigger (width=50ns)

L0C ← [NIM] unused (connected to the L0 trigger processor unit)

L1P5 ← [NIM] unused (optional: simple L1.5 trigger output)



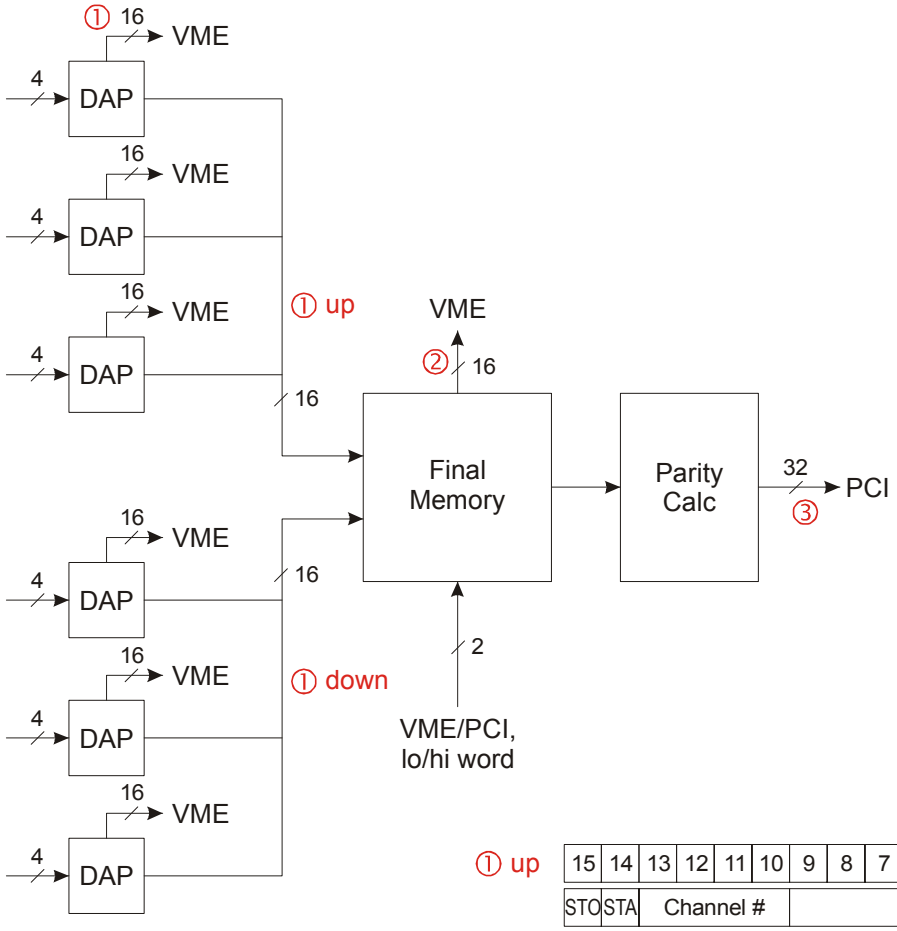
Each analog input connector (RJ45 type) on the front panel contains 4 twisted pair differential signals (from top to bottom as shown on the picture above: pin1=IN1+, pin2=IN1-, pin3=IN2+, ...), which are digitized on 2 DB_2xADC daughter boards (with 2 channels each). These 4 channels (10 bit each) are then sent to a DAP unit, which has a 4 event FIFO. Moreover, it processes the strip data for the L1.5 trigger, provided that a suitable pedestal threshold pattern has been stored in the DAP internal memory before. The analog data is digitized at 20MHz, but only every 4th value (synchronized to the start signal) is taken, since the VA1TA output is 5MHz. Thus, the zero-suppressed strip data of 4 input channels is multiplexed and sent to the L1.5 trigger on the "hitmap" RJ45 front panel connectors. The hitmap1 plug contains 4 twisted pairs each carrying the zero suppressed data of 4x4=16 channels (processed from A_IN2...A_IN5; hitmap1 pin1=h1+, pin2=h1-, pin3=h2+, ...); while hitmap2 carries 2x4=8 channels (A_IN6, A_IN7 on pins 1...4) plus a 20 MHz strobe signal pair (on pins 7 and 8).

The Fast-Or signals from the comparators on the DB_2xADC daughter boards are sent to the L0P1/2 units, which searches for valid trigger patterns and signals such an L0 condition on both the L0X (NIM) and the L0TW (differential ECL) outputs. This signal is shaped with a width of 50ns (NIM) or 120ns (ECL). Moreover, the L0 LED flashes.

For proper functionality, the L0 processor also needs Fast-Or signals from neighboring FADCTF modules (which correspond to neighboring detector modules). This is achieved by 16 input and 16 output lines on the P3

connector (8+8 lines to each neighbor module), where a custom designed backplane provides the interconnections.

Clock, timing and control signals are provided by the TTM system and sent to a custom P2 backplane via the Sequencer board. The TIP1 unit distributes these signals to the other logic blocks on the FADCTF board. Two control busses supply the upper and lower DAPs. The DACPR1 unit contains the final memory, to which the event data is transferred. This device contains a FIFO for 2 events (plus a small headroom), which are pushed out to the PCI-Link boards through the P3 connector.



① up

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STO	STA	Channel #				10 bit ADC data									

① down

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STO	STA	Event #				10 bit ADC data									

② lo word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STO	STA	Event #				10 bit ADC data up									

② hi word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STO	STA	Channel #				10 bit ADC data down									

③

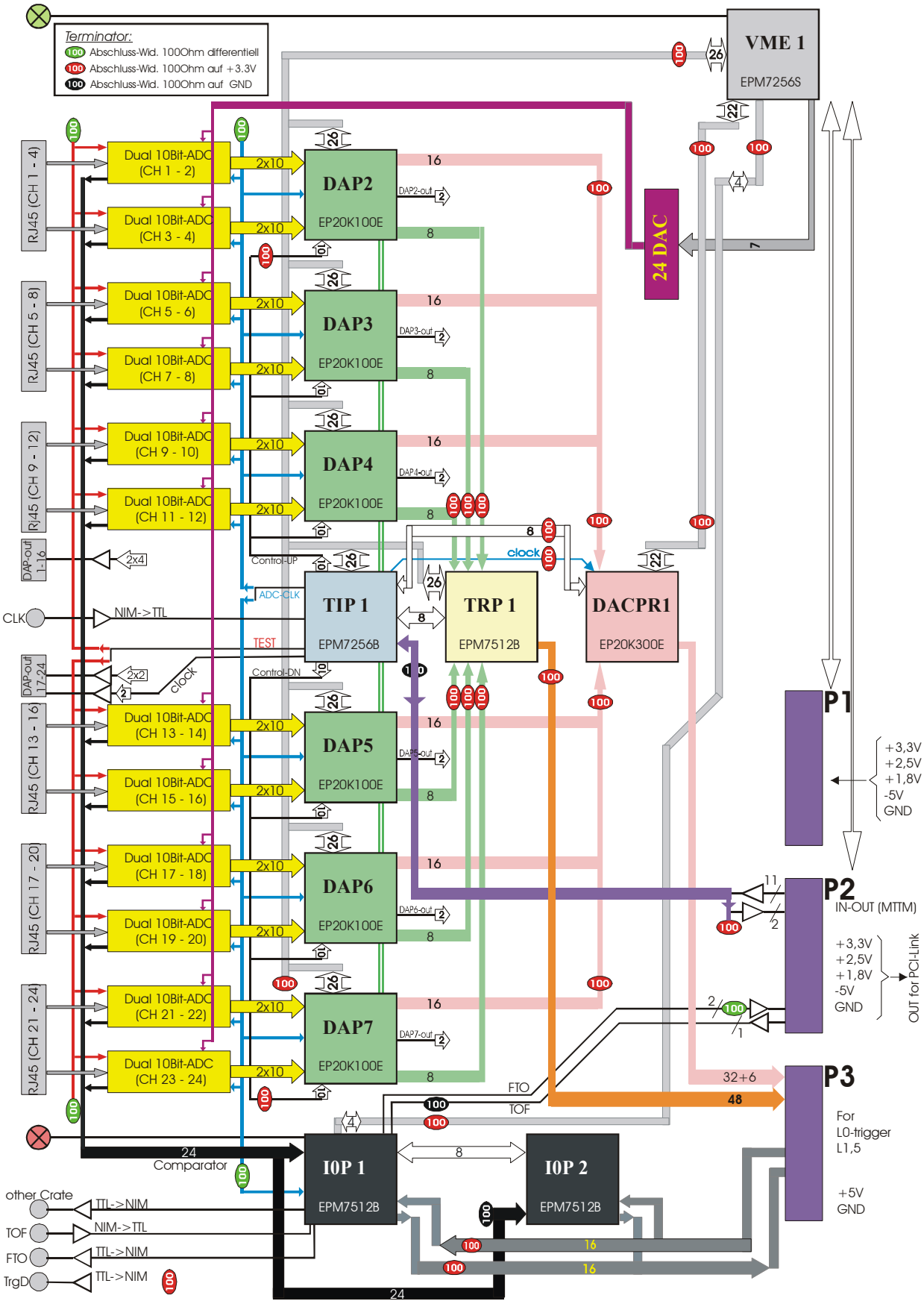
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	0	Event #														STO	STA	Channel #										10 bit ADC data up			
						10 bit ADC data down																									

The communication with the VME bus is handled by the VME1 bridge, which communicates to all logic units on the FADCTF board. Moreover, the logic units can be reprogrammed over VME. The 20K Altera FPGAs are loaded from external EEPROMs at startup or upon request, which can be written to via the VME1 unit. The same is true for the other FPGAs with internal flash memories. This is particularly interesting for fast changes in the L0 trigger patterns, which are contained within the LOP1/2 devices.

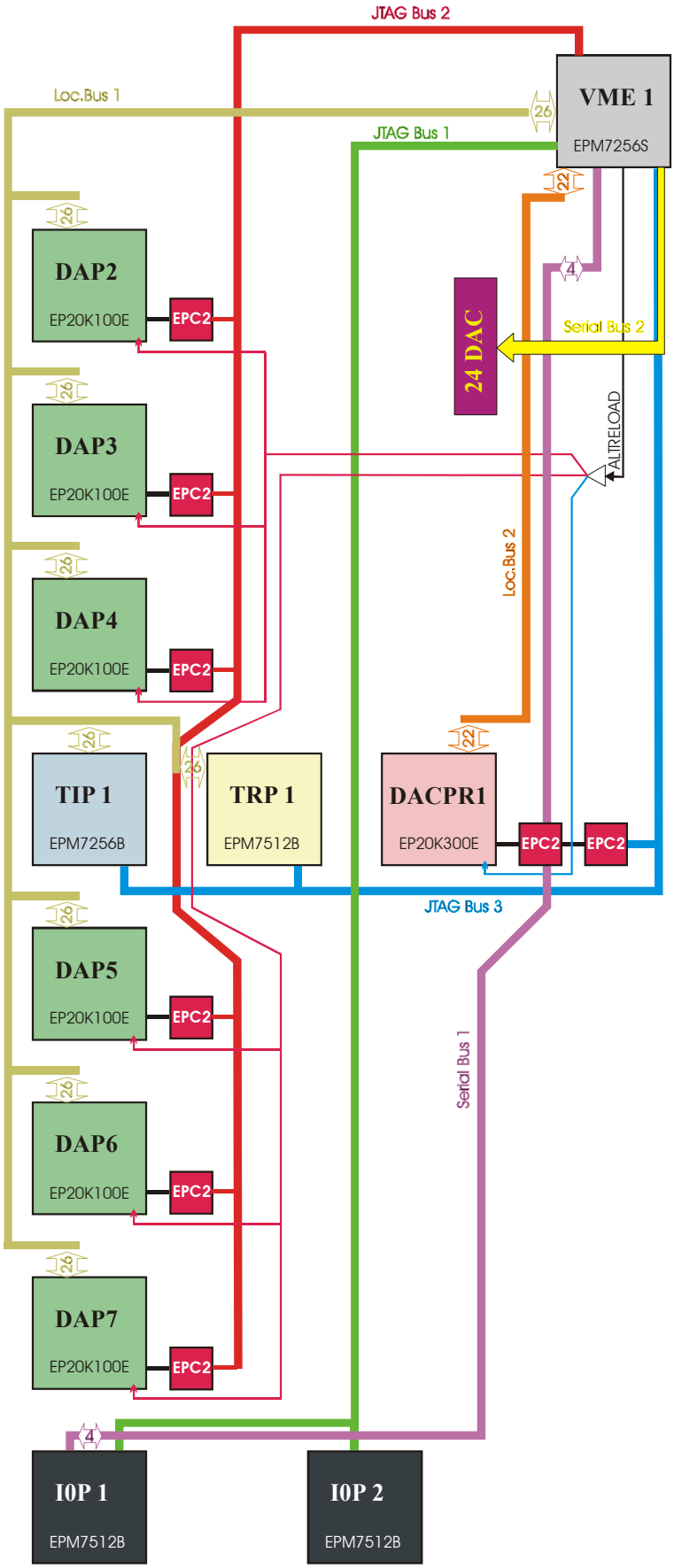
All logic devices are Altera FPGAs. The following table gives a summary of the functionality of each unit.

Name	Altera P/N	Function
DAPx	EP20K100E	ADC readout, 4-event FIFO, zero-suppression for the L1.5 hitmap data, Fast-Or counter
TIP1	EPM7256B	Clock, timing, control distribution
TRP1	EPM7512B	(optional) simple L1.5 trigger processor
DACPR1	EP20K300E	Final memory
LOPx	EPM7512B	L0 processor (LOP2 is optional and depends on utilization of gates within LOP1)

A block diagram with all interconnections between the logic units is shown on the next page.except for the JTAG buses.


Terminator:
100 Abschluss-Wid. 100Ohm differentiell
100 Abschluss-Wid. 100Ohm auf +3.3V
100 Abschluss-Wid. 100Ohm auf GND
VME 1
EPM7256S
24 DAC
RJ45 (CH 1 - 4)
RJ45 (CH 5 - 8)
RJ45 (CH 9 - 12)
RJ45 (CH 13 - 16)
RJ45 (CH 17 - 20)
RJ45 (CH 21 - 24)
Dual 10Bit-ADC (CH 1 - 2)
Dual 10Bit-ADC (CH 3 - 4)
Dual 10Bit-ADC (CH 5 - 6)
Dual 10Bit-ADC (CH 7 - 8)
Dual 10Bit-ADC (CH 9 - 10)
Dual 10Bit-ADC (CH 11 - 12)
Dual 10Bit-ADC (CH 13 - 14)
Dual 10Bit-ADC (CH 15 - 16)
Dual 10Bit-ADC (CH 17 - 18)
Dual 10Bit-ADC (CH 19 - 20)
Dual 10Bit-ADC (CH 21 - 22)
Dual 10Bit-ADC (CH 23 - 24)
2x10
DAP2
DAP3
DAP4
DAP5
DAP6
DAP7
EP20K100E
DAP2-out
DAP3-out
DAP4-out
DAP5-out
DAP6-out
DAP7-out
DAP-out 1-16
DAP-out 17-24
2x4
2x2
Control-UP
Control-DN
ADC-CLK
clock
TEST
CLK
NIM->TTL
TIP 1
EPM7256B
TRP 1
EPM7512B
DACPR1
EP20K300E
P1
+3,3V
+2,5V
+1,8V
-5V
GND
P2
IN-OUT (MTTM)
OUT for PCI-Link
P3
For
L0-trigger
L1,5
+5V
GND
FTO
TOF
32+6
48
24
Comparator
I0P 1
I0P 2
EPM7512B
other Crate
TTL->NIM
NIM->TTL
TOF
FTO
TrgD

The 3 JTAG buses (DAPx, TIP1/TRP1/DACPR1, IOP1/IOP2) used for programming and testing the Altera devices are shown below.

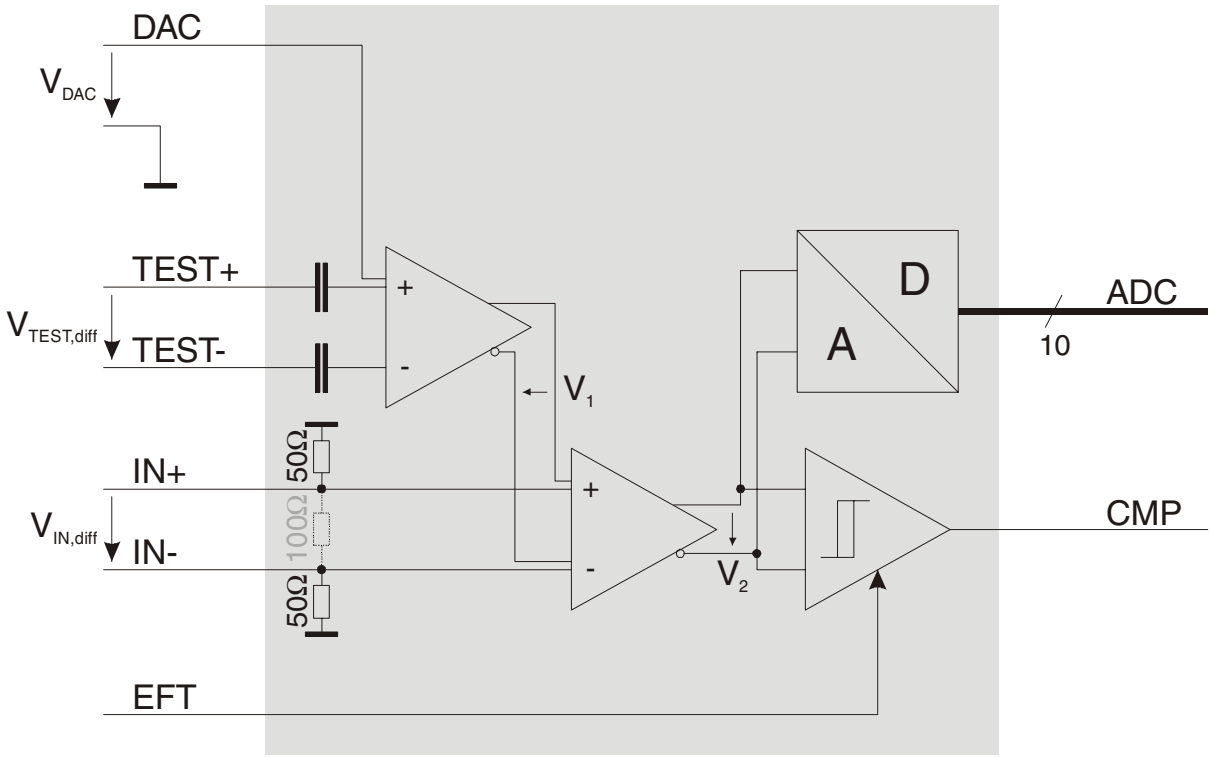


1.2 Daughter Board (DB_2xADC)

The ADC daughter board receives the analog output data of the VA1TA readout chip via the REBO chain and digitizes them with 10 bits at 20 MHz (although the strip data is only clocked at 5 MHz). Moreover, the Fast-Or trigger output is detected with a comparator in the time window where it is expected. During analog data readout, the comparator is disabled.

Each ADC daughter board has two channels with individual ADCs, level shifting and test inputs. Twelve such boards will be sitting on a single mother board. Alternatively, single ADC boards can be tested and debugged on a specific VME test board.

Only one of these two channels is shown in the simplified block diagram below.



This picture also defines the way in which differential and single input voltages are measured. EFT and CMP levels are TTL (0.3/3.5V). The ADC output range is 0..1023, represented on a 10 bit bus.

The nominal amplification factors are:

$$V_1 = 0.084 \cdot V_{TEST,diff} + 0.39 \cdot V_{DAC}$$

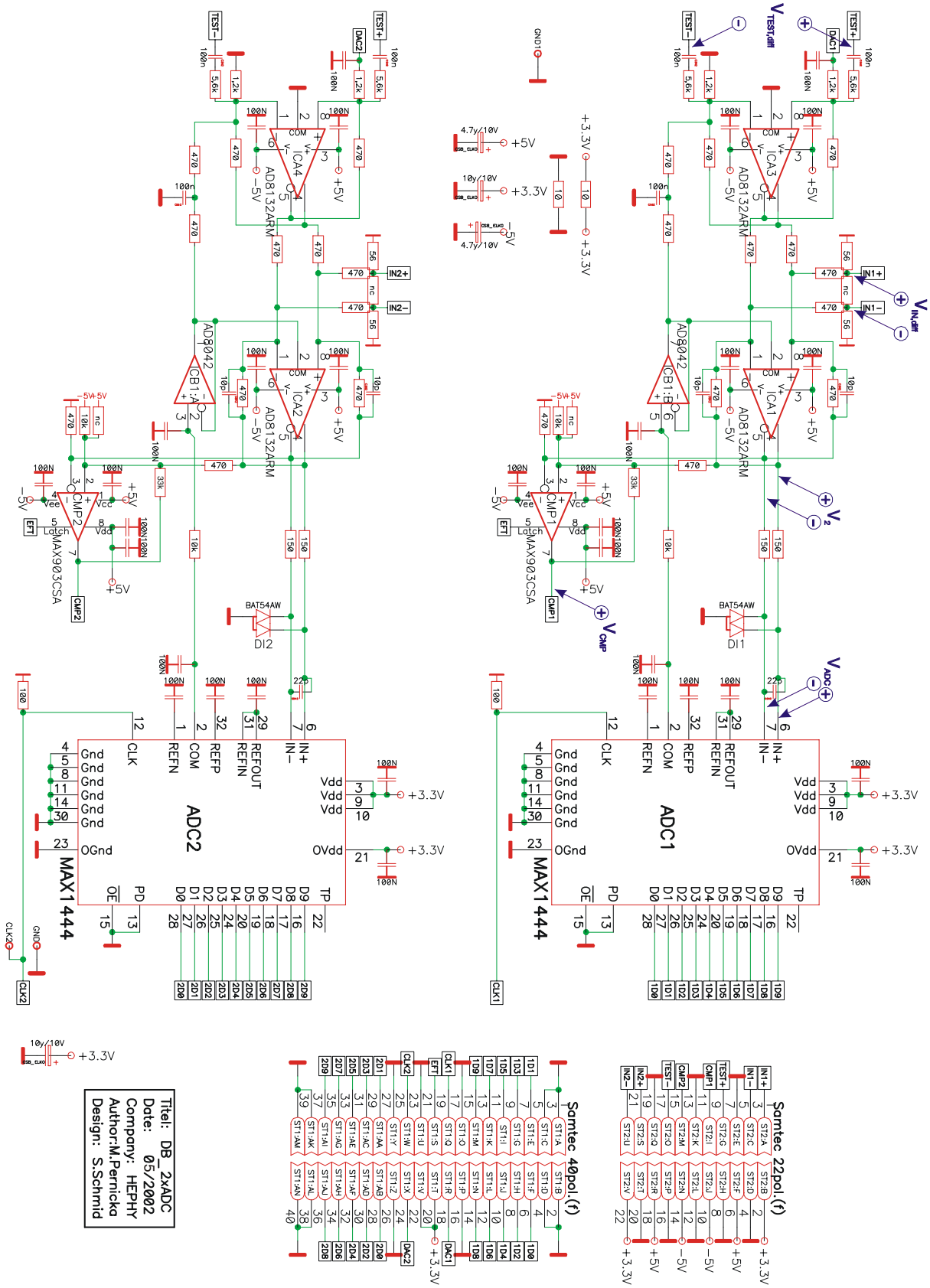
$$V_2 = V_{IN,diff} + V_1$$

$$ADC = 0.51 \cdot V_2 \text{ [mV]}$$

More details on the conversion factors are given in the last section of this document.

1.2.1 Schematics

The full schematics of the ADC daughter board are shown below, including probe test points.



Both identical ADC channels are shown here, while the Samtec connector pinout can be found at the bottom.

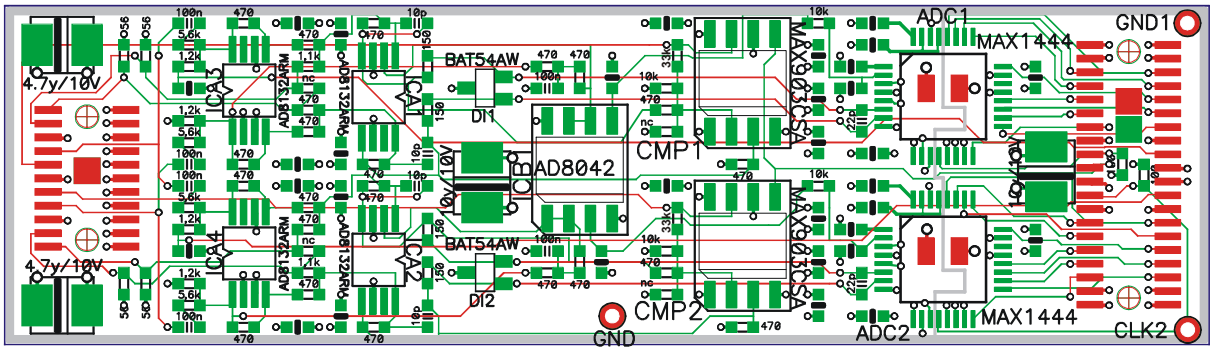
The differential analog inputs from the REBO are IN1± and IN2±. These inputs are symmetrical to GND and terminated to GND with 50Ω each. Alternatively, this could be changed to a purely differential 100Ω termination. A common mode has to be introduced to match the ADC inputs, which is done with the amplifiers ICA1 and ICA2, respectively. Moreover, AC coupled test inputs (TEST±; common to both channels) and DAC offsets (DAC1 and DAC2) are added through the amplifiers ICA3 and ICA4, respectively. Please note that these DACs are located on the mother board.

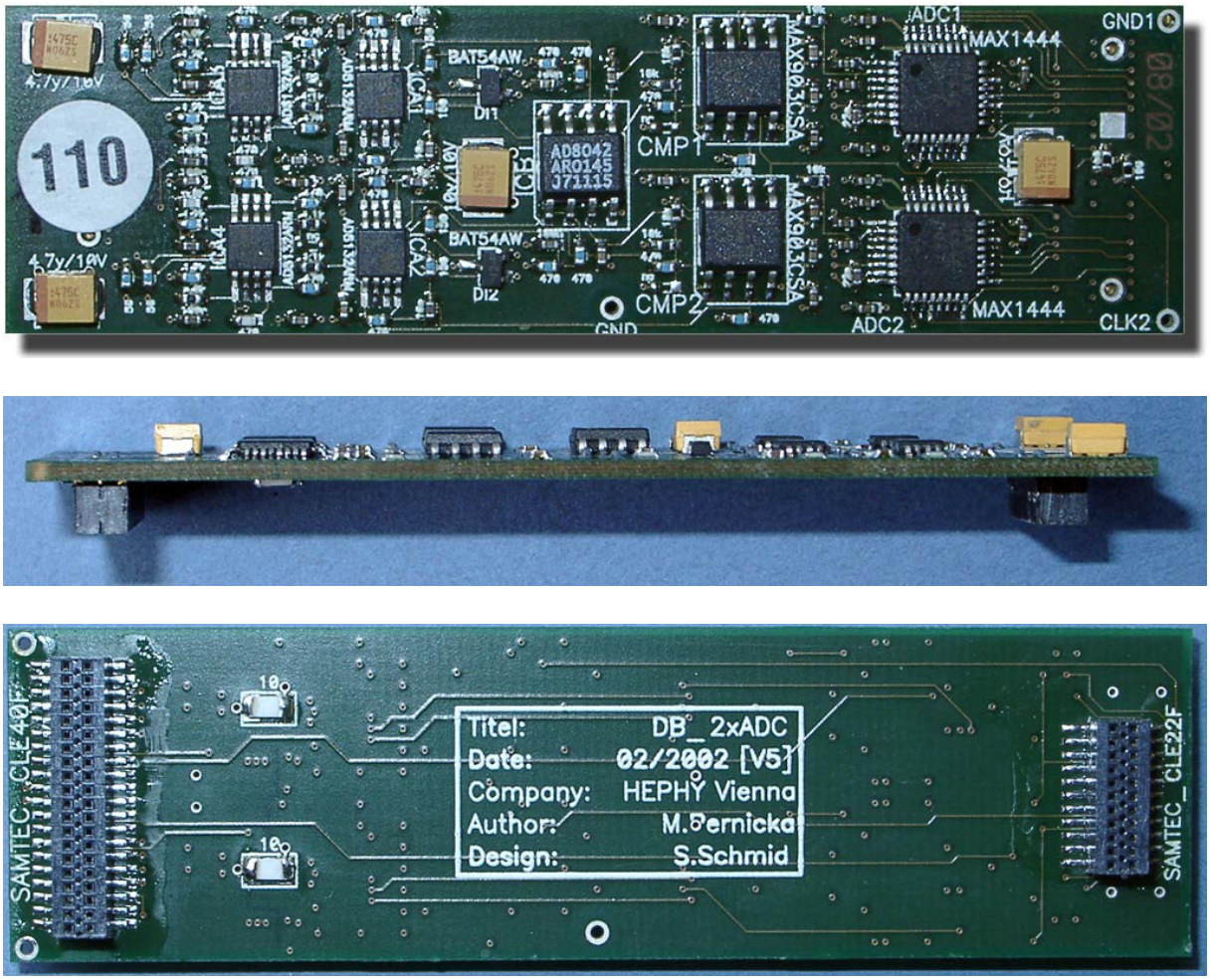
The ADCs internally generate their reference and common mode voltages. The latter is buffered by ICB1 and fed into the designated inputs on ICA1 and ICA2, respectively. Their outputs are presented to the ADCs through protection diodes towards GND and a low-pass filter. The nominal ADC clocks CLK1 and CLK2 will be 20 MHz, although the devices can be operated up to 40 MHz.

As long as the EFT signal to the comparators CMP1 and CMP2 is high, these devices watch for the Fast-Or trigger, which is signalled on the CMP1 and CMP2 lines, respectively. For trigger test purposes, a Fast-Or should be emulated only on specific channels. This can be achieved by individual DAC voltage settings and a common TEST signal applied to all channels. Those channels which should not produce a Fast-Or signal should have a low DAC setting such that the TEST signal will not exceed the comparator threshold. Other channels with a "normal" DAC setting will generate a comparator signal when a TEST pulse is applied. By that method, which is supported by the mother board, a completely arbitrary Fast-Or pattern can be produced, although using a TEST pulse that is common to all channels on all mother boards.

1.2.2 Layout

The electrical layout of the PCB is shown below, followed by photographs of an assembled device. Green components are mounted on top, while red parts are located on the bottom side.





1.2.3 Mechanics

The outer dimensions of the ADC daughter board (including components) are approximately 70 x 20 x 6 mm^3. The only mechanical connection are two Samtec sockets with 22 and 40 pins, respectively. All components except the connectors and a few capacitors are located on the top side, such that the device can be easily probed and debugged while in operation.

1.2.4 Pinout

1.2.4.1 22-pin Samtec socket

The following table describes the pinout of the 22-pin Samtec connector, which carries mainly analog signals.

Name	Pin #	Description
IN1+	1	Two differential analog input channels from the front-end. Termination is 50Ω to GND for each input by default, but can be changed to 100Ω differentially. Input range: 2.075V differential input span corresponds to full ADC range (1024). The offset can be set by DAC.
IN1-	3	
IN2+	19	
IN2-	21	
TEST+	7	Test input which is added to both regular inputs.

TEST-	15	Input range: 6.6V differential input span corresponds to 277 ADC counts.
CMP1	9	Fast-Or detect. Requires EFT=High for operation. Output levels are TTL (0.3/3.5V).
CMP2	13	
+5V	6,18	Supply for amplifiers and comparators.
+3.3V	2,22	Analog supply for ADCs.
-5V	10,14	Supply for amplifiers and comparators.
GND	4,5,8,11,12, 16,17,20	System ground (analog).

1.2.4.2 40-pin Samtec socket

The table below shows the pinout of the 40-pin Samtec connector, which mainly delivers digital signals.

Name	Pin #	Description
1D0…1D9	5…13	Two parallel digitized 10-bit busses. Output levels are LV-TTL (0.3/3.1V). Note that even and odd pins are swapped wrt to the bit order (e.g. 1D0=6, 1D1=5, 1D2=8, …).
2D0…2D9	27..36	
CLK1	17	Independent clocks for both channels. Input levels are LV-TTL (0.3/3.1V).
CLK2	23	
DAC1	18	Analog offsets for both channels to optimize the ADC range. Input range: 538mV input span corresponds to full ADC range (1024). Offset: +442mV input corresponds to central ADC (512) @ IN=0V and TEST=0V.
DAC2	24	
EFT	19	Enables Fast-Or detection if EFT=High. Input levels are TTL.
+3.3V	20,22	Digital supply for ADCs.
GND	1…4,15, 16,21,25, 26,37…40	System ground (digital).

1.2.5 Conversion

Three different types of input affect the ADC reading:

- IN (differential)
- TEST (differential)
- DAC (single)

The ADC offset voltage at zero differential input voltages can be set by the DAC value. Since the offset depends on the DAC setting, only a slope will be given for IN and TEST signals. Moreover, the comparator threshold values will be stated.

See the block diagram in section 0 for the definition of differential and single-ended voltage inputs.

The following relations are measured on one typical daughter board, but obviously do not exactly match the nominal values.

1.2.5.1 IN ↔ ADC

The input voltage $V_{IN,diff}$ is measured in terminated state between the differential inputs.

$$V_{IN,diff} = V_{IN,+} - V_{IN,-}$$

$$\Delta V_{IN,diff}\ [mV] = 2.026 \cdot \Delta ADC$$
$$\Delta ADC = 0.493 \cdot \Delta V_{IN,diff}\ [mV]$$

1.2.5.2 TEST ↔ ADC

The test voltage $V_{TEST,diff}$ is measured between the differential inputs. Please note that these inputs are AC coupled.

$$V_{TEST,diff} = V_{TEST,+} - V_{TEST,-}$$

$$\Delta V_{TEST,diff}\ [mV] = 23.34 \cdot \Delta ADC$$
$$\Delta ADC = 0.043 \cdot \Delta V_{TEST,diff}\ [mV]$$

1.2.5.3 DAC ↔ ADC

The DAC voltage V_{DAC} is measured towards GND. Please note that these equations below are obtained with $V_{IN,diff} = V_{TEST,diff} = 0V$.

$$V_{DAC}\ [mV] = 173 + 0.53 \cdot ADC$$
$$ADC = -328 + 1.90 \cdot V_{DAC}\ [mV]$$

1.2.5.4 Comparator

The comparator threshold values are given in terms of ADC output values.

$$Comp_{ON} = 618\ ADC$$
$$Comp_{OFF} = 595\ ADC$$

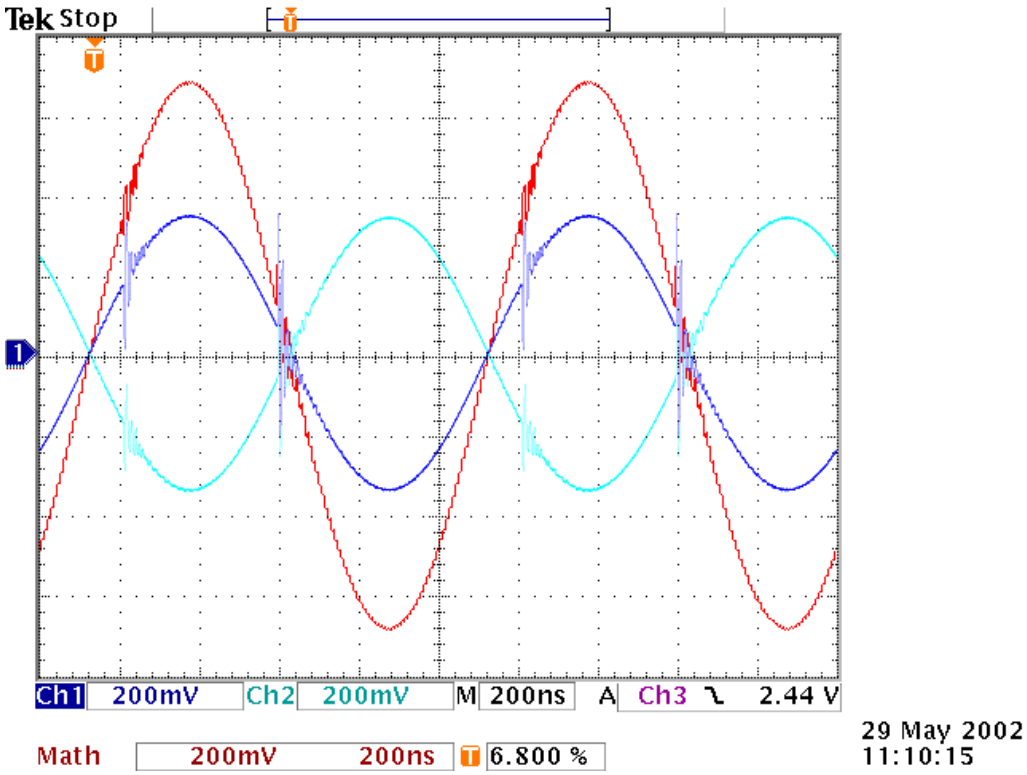
Thus the hysteresis corresponds to a differential input voltage difference of

$$\Delta V_{IN,diff} = 47\ mV\ .$$

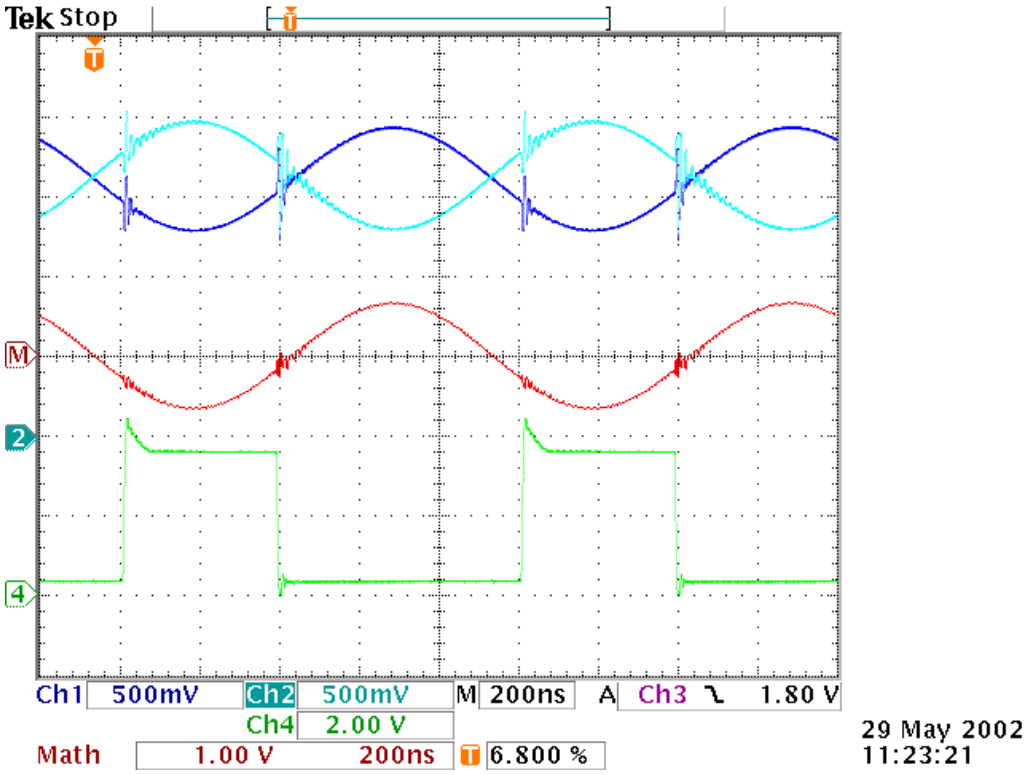
1.2.6 Signals

The scope screenshots shown here refer to the probe test points shown in the schematics in section 1.2.1.

1.2.6.1 IN → ADC

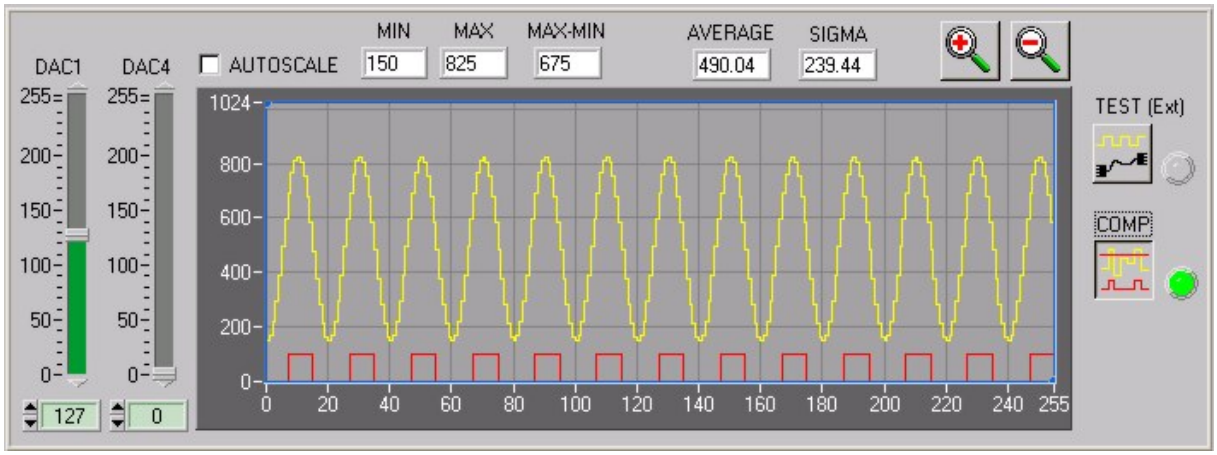


This is an arbitrary electrical input (blue: V_{IN+}, cyan: V_{IN-}, red: $V_{IN,diff}$) measured on the connector. The peak-to-peak amplitude of $V_{IN,diff}$ is approximately 1368mV. It translates to a V_2 voltage (ADC input before low-pass filter) as shown below. The comparator switching has some effect on the analog lines, but these spikes are not seen on the digitized.

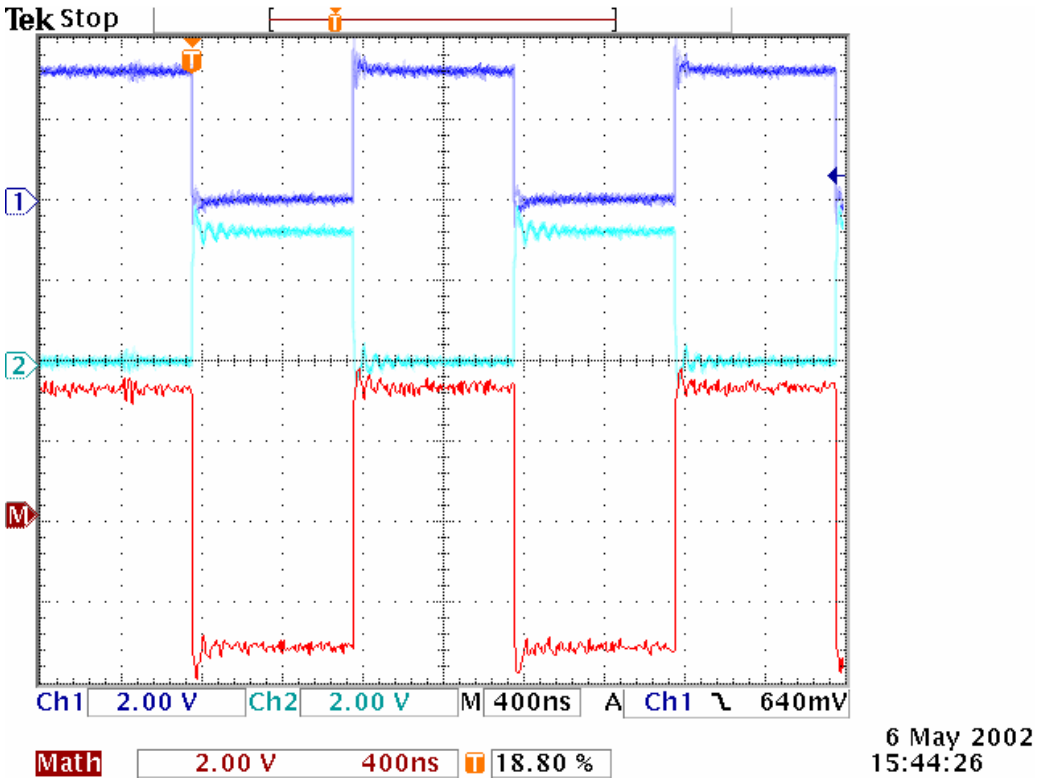


As indicated before, the amplifier stage is just buffering the input signal, yielding an amplitude of about 1334mVpp. The conversion corresponds very well with the nominal factor of 1. The green curve corresponds to the comparator output V_{CMP}, which is described below.

The next picture shows the ADC representation of the same signal (yellow) and the comparator output (red). Again, the measured amplitude of 675ADC corresponds very well to the nominal ADC gain of 0.51ADC/mV, referred to V_2.

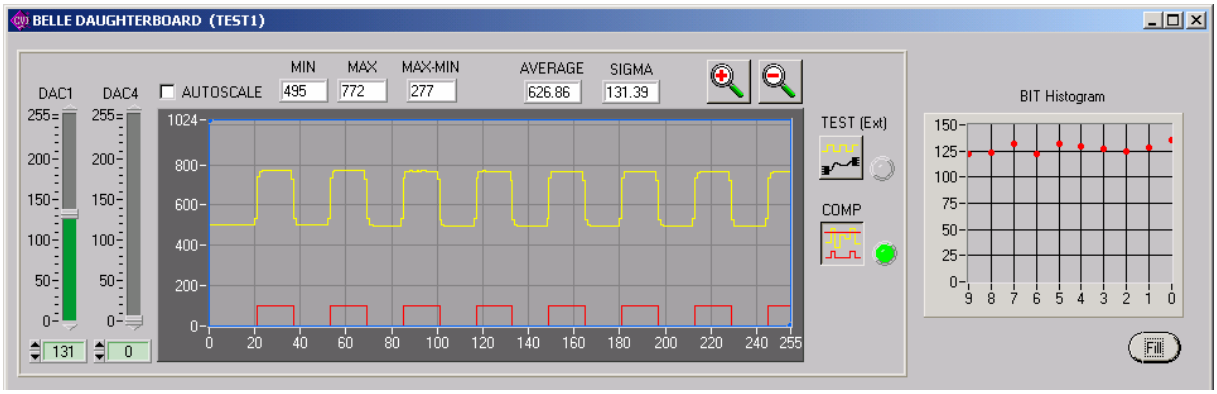


1.2.6.2 TEST → ADC



This is a differential test pulse input provided by a differential LV-TTL driver which is used on both the daughter board tester and the mother board to generate test pulses with a differential peak-to-peak amplitude of approximately 6600mVpp.

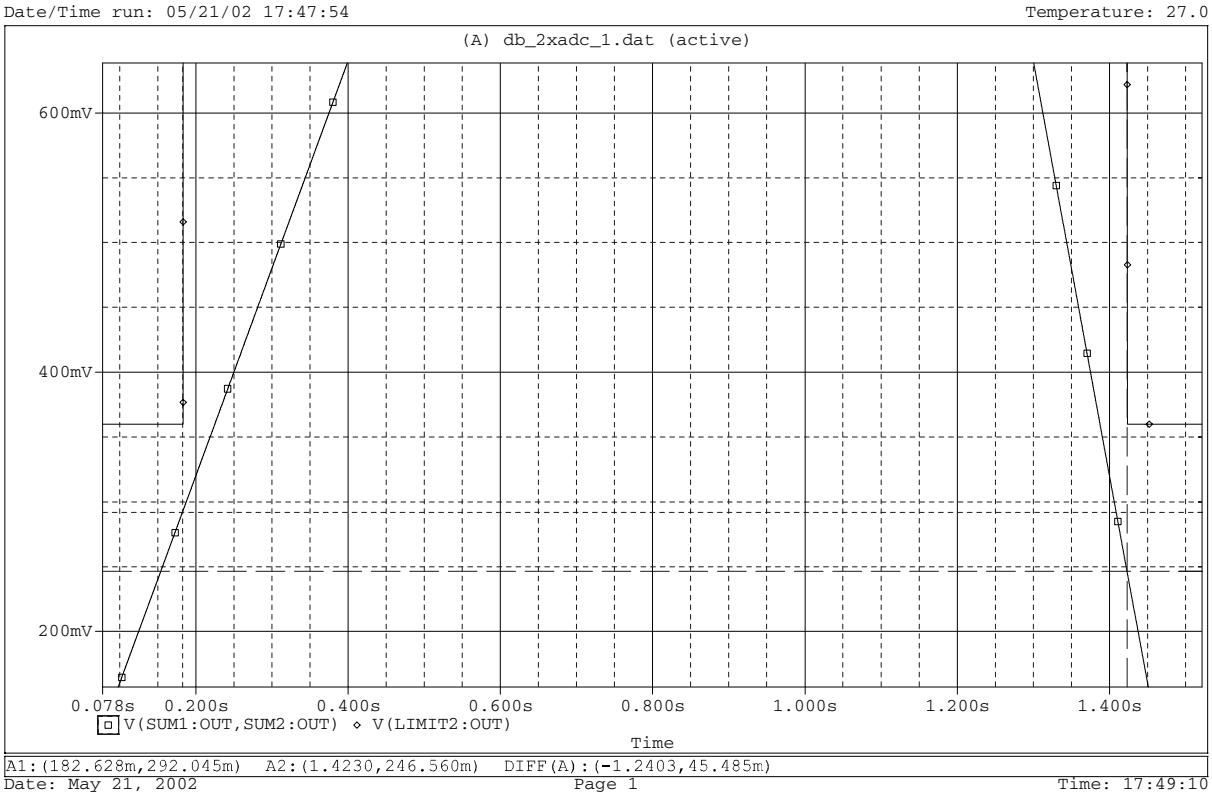
The corresponding ADC output is shown below, yielding an amplitude of 277ADC, which is in good agreement with the nominal gain of 0.043ADC/mV



1.2.6.3 Comparator

The comparator behavior was simulated with SPICE. Please note that the V_2 lines have a common mode voltage of 1.15V; i.e. they are not symmetric around zero, but both reside at that voltage when there is zero input. Moreover, the comparator limits are quite sensitive to its output, which is TTL with measured levels of 0.36V (low) and 3.64V (high).

The plot below shows a triangular differential input signal V_2 (with both positive and negative parts) and the corresponding comparator output signal V_{CMP}.



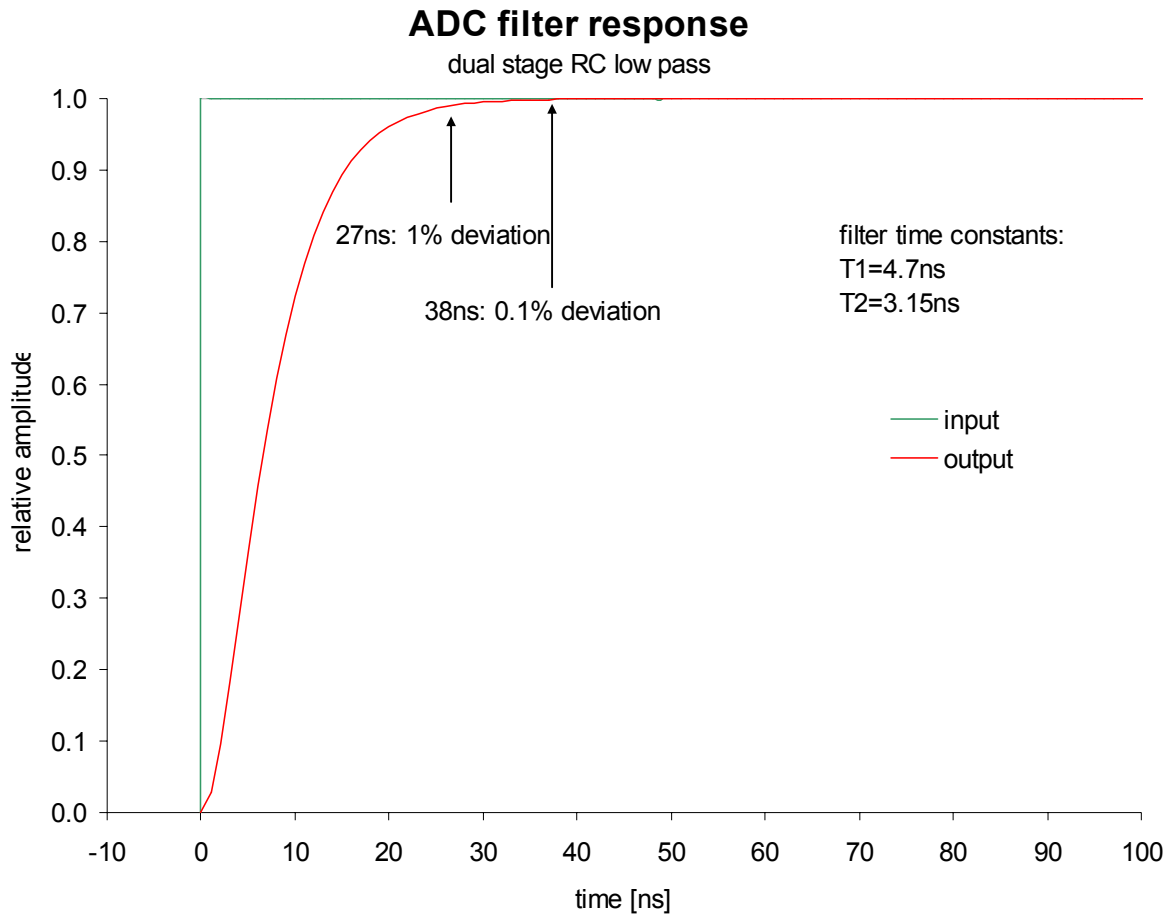
The simulated On/Off limits, referred to V_2, are approximately 292 and 247mV. The hysteresis of 45mV corresponds to 22 ADC counts or an input span ($V_{IN,diff}$) of 45mV. The measured values are in good agreement with the

simulation results (23 ADC counts). The scope screenshot in section 1.2.6.1 shows V_{CMP} in green.

1.2.6.4 ADC Step Response

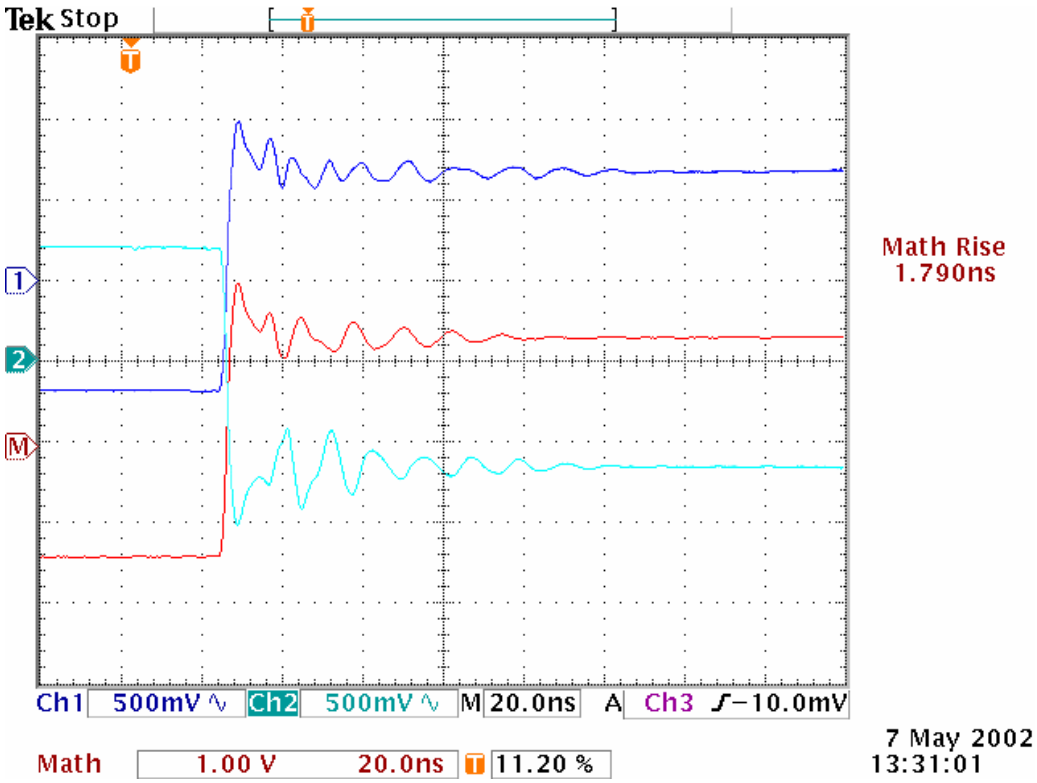
On their way towards the ADC, the input signals are subjected to two RC low-pass filters: The first RC stage is located in the feedback of ICA1 (R=470Ω, C=10pF, τ=4.7ns on each polarity). The second is directly in front of the ADC input and consists of a series resistor plus the discrete capacitor between the ADC inputs in parallel to the parasitic capacitance of the protection diodes, which is specified to be less than 10pF at 1V reverse voltage. Thus we have R=150Ω, C=21pF, τ=3.15ns in a single-ended equivalent circuit diagram.

The calculated step response, assuming an ideal input step function is shown below.

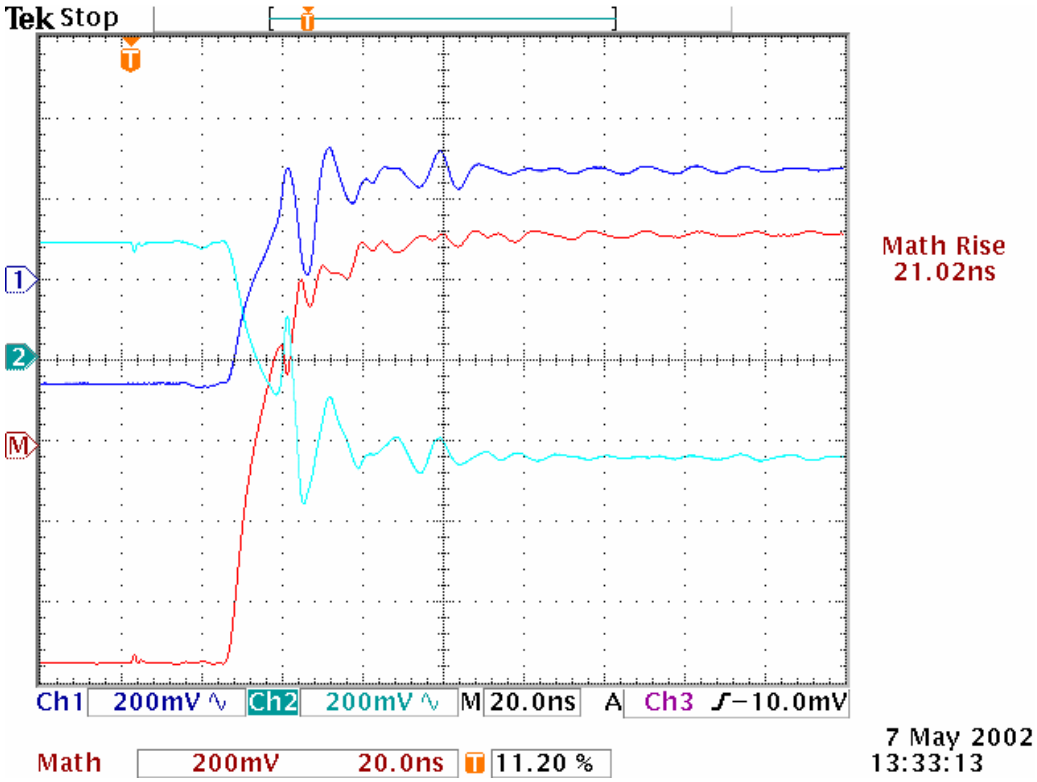


The VA1TA strip data is delivered with a period of 200 ns. Thus, 4 samples are taken by the ADC for each strip data, but only the last one (at a distance of approximately 170..180 ns from the edge) is of interest and will be processed.

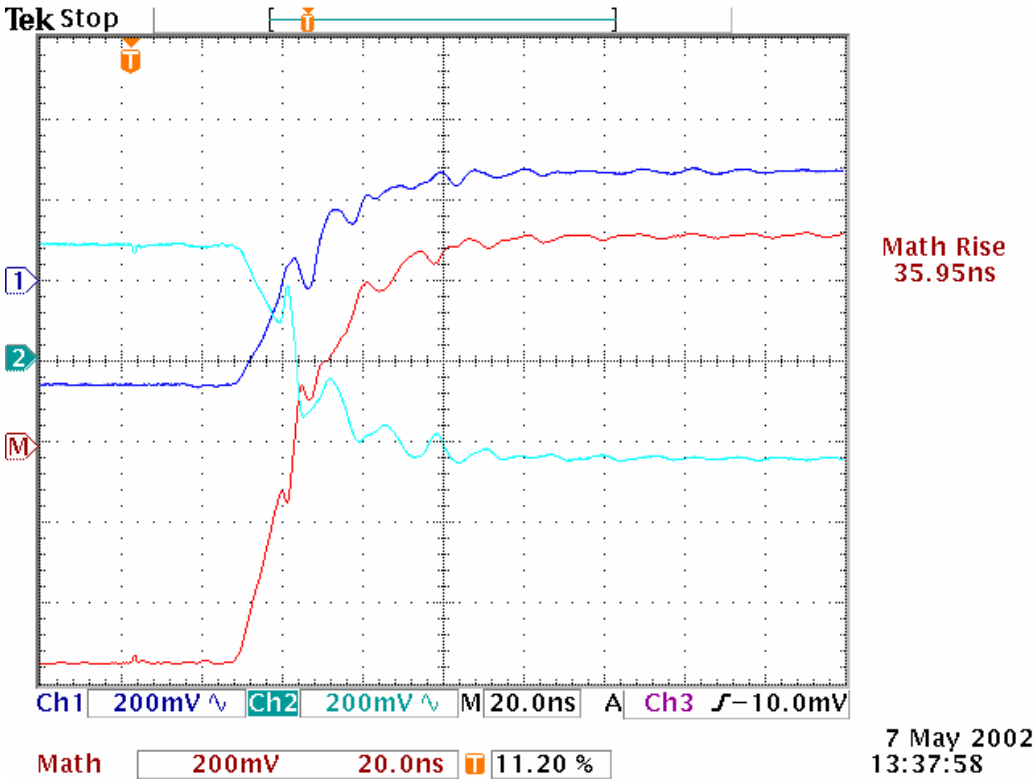
The scope screenshots below show a step function at the input, after the first filter stage and at the ADC input. Positive and negative inputs are shown in blue and cyan, respectively, and the difference is drawn in red.



Input pulse measured at $V_{IN,diff}$ (red).



Step function measured after the first filter (V_2).

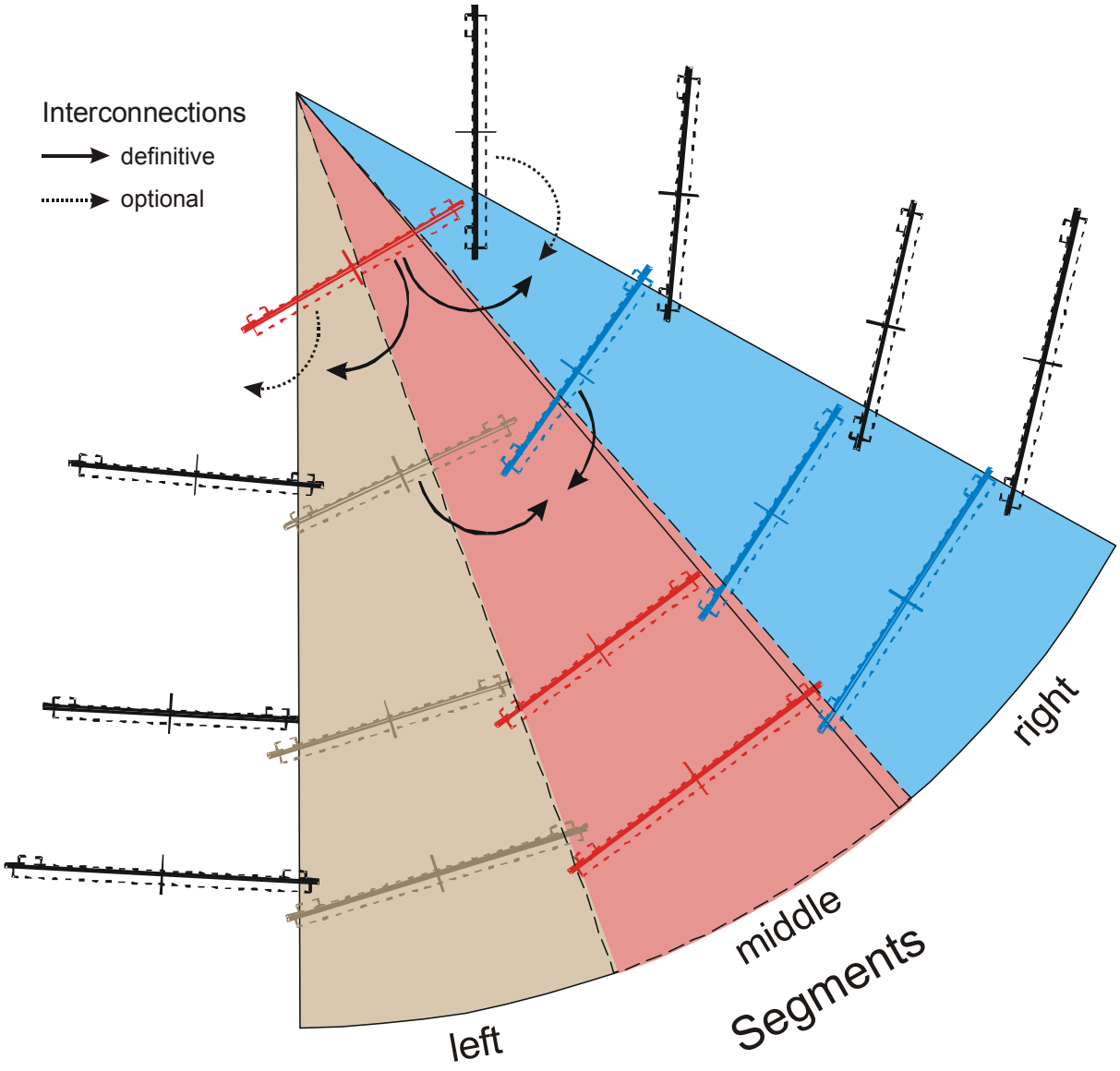


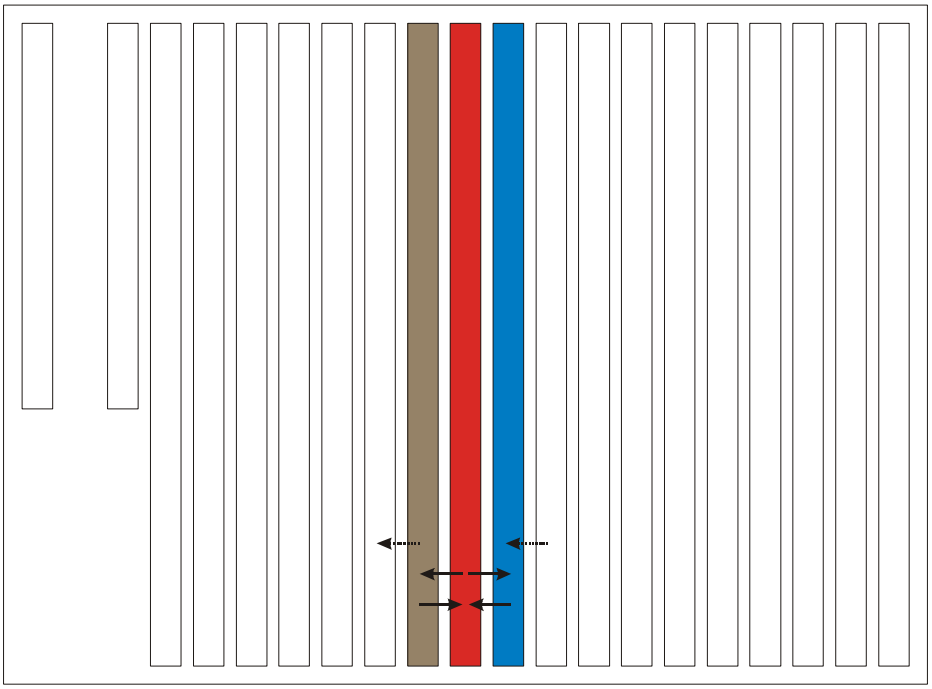
Step function at the ADC input (V_{ADC}). Compared to the calculation, both filters are stronger than expected, but without any impact on the sampling point.

1.3 Trigger processor for LO

The trigger processor looks for particle tracks in the four Silicon layers that origin from the beam interaction region.

Each FADCTF basically reads out one segment (1/18 of 360° = 20°) of the SVD detector modules. The graph below shows 1/6 (60°) of the silicon detector. This allows to build a fast LO trigger with the smallest segment of one single VA1TA (128 strips). The FADCTF modules are shown in the same colors as the detector modules which they read out. One FADCTF reads out either a segment of planes (1,3,4) or (2,3,4). The arrows indicate which information needs to be provided to neighboring modules to properly build LO triggers from the Fast-Or signals. This principle applies to both rφ and rz readout directions. Full modules (with all 4 VA1TA chips) have to be considered in the rz case. In the rφ case (where strips run along the z axis), not all 4 VA1TA chips need to be transferred in all cases, since those which are not contained within the segment may be omitted. For instance, only the leftmost quarter of the innermost red module in the following graph actually belongs to the blue segment, thus there is no need to consider the rest of that module.


Interconnections
definitive
optional
left
middle
right
Segments



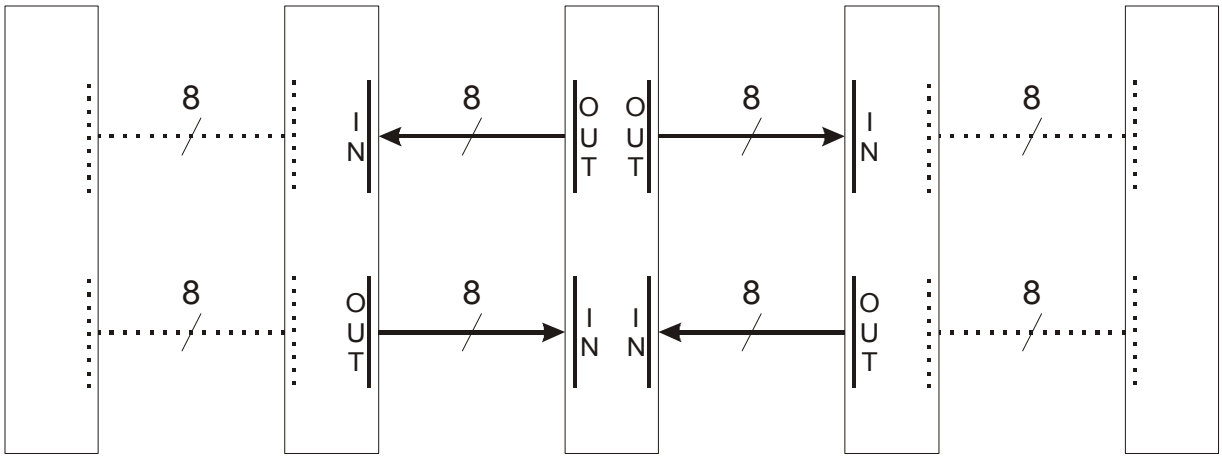
There are definitively interconnections within such a group of 3 segments/modules. Basically, the 6 triplets are independent on each other and symmetric in both rφ and rz cases, but the possibility of interconnection between neighboring triplets is foreseen in the hardware as indicated by the dashed arrows above. Including this feature could result in an increased L0 noise trigger rate that would be disadvantageous. The final implementation will be a tradeoff between efficiency and noise contribution.

The Fast-Or trigger patterns will be implemented within the LOP1 (and LOP2 if required) FPGAs for both rφ and rz directions. Simulations have been done in both cases to get the probabilities for all possible combinations that will be implemented inside the IOP1/2 units. Therefore, six different programs are needed: one each for left, middle and right modules in both rφ and rz variants.

The trigger simulation including a detailed description and online software is available at http://www.nanuk.at/cern/index.php?project=BELLE_trigger .

1.3.1 Interconnections

Maybe the most critical part of the system is the interconnection between left, middle and right modules on the custom P3 backplane. Every trigger processor has 8 inputs and 8 outputs that are used by the adjacent neighbor modules within a segment as shown in the picture below.



Due to the straight layout of the P3 backplane, the hardware makes no difference between inputs and outputs. The direction of the data flow is only defined by the type of the corresponding Altera pins. Thus, it is possible to accidentally connect two outputs by incorrect Altera programming or wrong module positioning which results in overheating and successive destruction of both FPGAs involved without any indication of that condition to the outside world. Therefore, some protection mechanisms are foreseen to prevent such an accident.

The VME crates will have mechanical coding of slots such that each module can only be inserted in the proper place. One mechanical code will be assigned to each of the 6 different FADCTF module types (left, middle and right for both rφ and rz variants). The crate slots will be correspondingly

coded in groups of 3. For example, the “left rz” modules can only be inserted in slots 4,7,10,13,16,19 of the proper crate.

However, the correct setting of the VME base address remains the crucial item. In order to make this easier, we propose to use the slot number for the A24...A31 bits of the module. We will provide a list showing the correct associations between slot number, mechanical coding and VME addresses and attach this list as a label onto every FADCTF module.

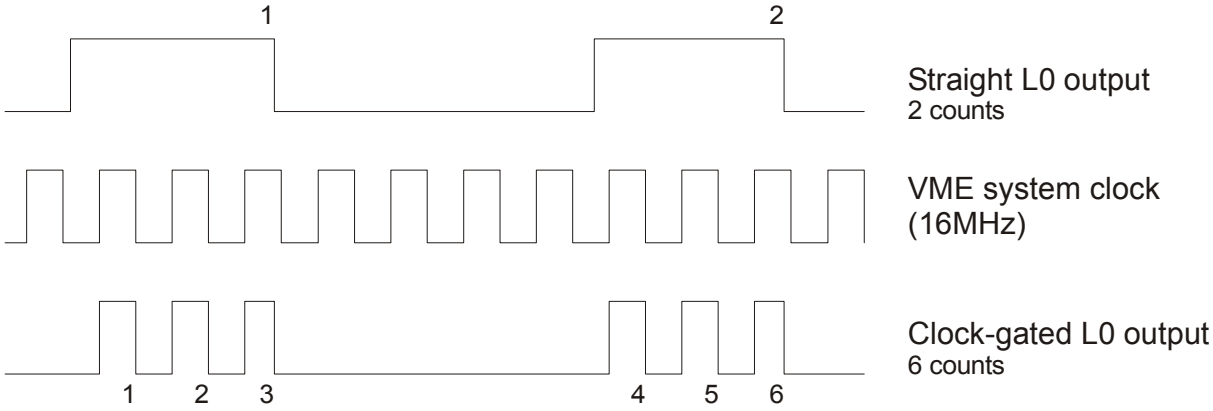
The loading of the Trigger Processor firmware will be restricted to the proper VME address, i.e. it is not possible to accidentally program a module in a “left rz” position with middle or right firmware provided that the VME address is correct.

There are 2 groups if I/O pins with 8 lines each. Depending on the module type, one of those will be declared as input, the other as an output by VME commands. This is done with two dedicated signal lines (“enable up” and “enable down”) from the VME protocol unit to the Trigger Processor.

With all of these protections, no accidents should happen provided that the VME address is set correctly (corresponding to the slot number and the mechanical coding).

1.3.2 L0 counter

The L0 Trigger Processor is asynchronous, it just connects all Fast-Or inputs in the proper way using “AND” and “OR” gates. The L0 trigger decisions are sent on two lines from the Trigger Processor to the VME protocol Altera, where they are counted. On one line, simply the number of triggers is counted, whereas on the other line, the L0 decision is “AND”-gated with the VME system clock (running at 16MHz), such that several counts appear there depending on the width of the L0 trigger as shown in the drawing below.



The average L0 width can be deducted from the ratio of the two counters. Together with the individual Fast-Or counters in the DAPs and some statistics, the “randomness” of the Fast-Or triggers can be calculated.

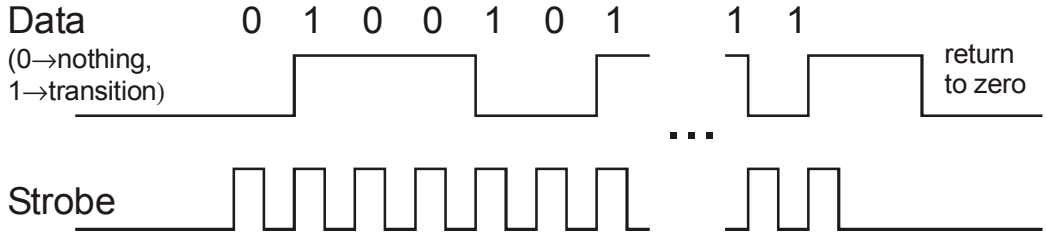
1.4 Hitmap output

The serial hitmap output is presented at a frequency of 20MHz, since the zero suppressed and digitized strip data of a full module (4 VA1TA chips) is

multiplexed there. The data is presented in the non-return-to-zero change-on-ones (NRZ1) code, which is characterized by the following translation.

- 0 → same output state as before
- 1 → change in output state (e.g. 0 to 1 if previous state was 0)

In other words, a data "1" is characterized by a transition, while data "0" does not change the current state. The data are sent out in differential LV-TTL (0.3/3.1V) including a strobe pair.



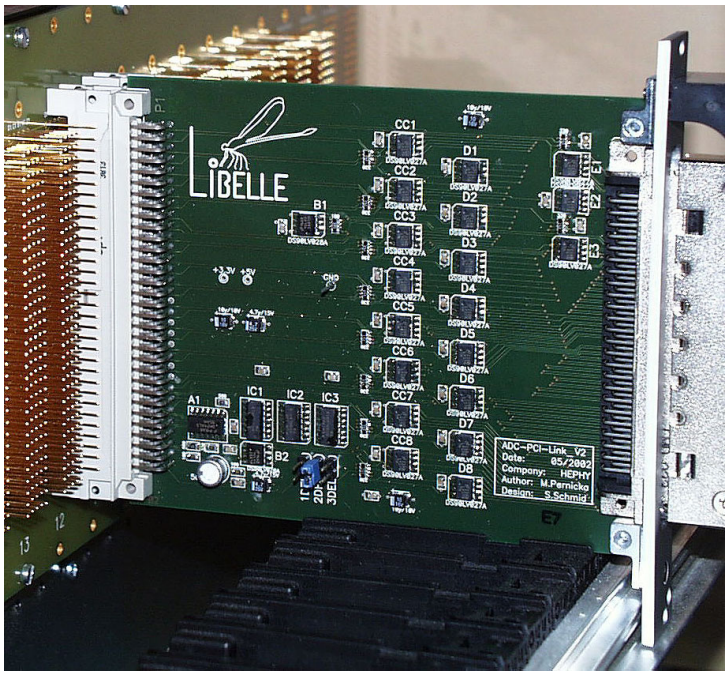
1.5 (Optional) Trigger processor for L1.5

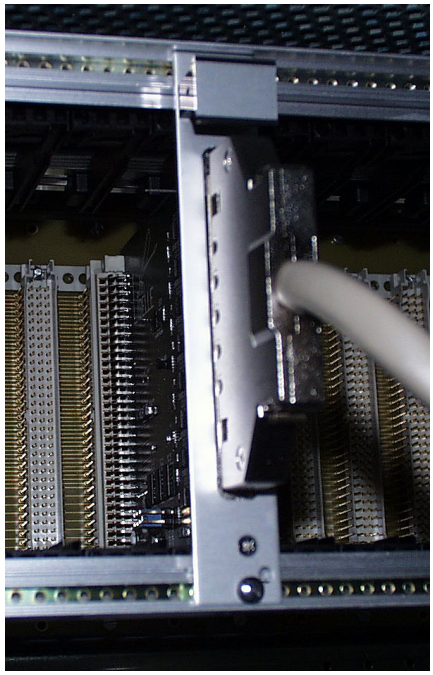
Optionally, the FADCTF can also use the detected hitmap output to create a L1.5 trigger. Each DAP (with 4 analog input channels) is connected to the L1.5 trigger processor over 8 lines. Moreover, an interconnection bus of 24 lines is provided to each left and right neighboring modules.

A simple implementation of the L1.5 processor would be to combine groups of 64 silicon detector strips by "OR" to one line. The decision time in that case is less than 50ns, but other combinations are possible as well. The number of gates in the TRP1 Altera chip is a hard limit for the implementation. The limit of bus lines, however, could be could be overcome by time-multiplexing of the signals if necessary.

2 PCI-Link

The PCI-Link provides the connection between the FADCTF and the DAQ PCs. One PCI-Link card is connected to each 24ADC_PRESELDA module through the P3 backplane as shown in the photographs below. On the other end, 3 PCI cards are hosted by one Linux PC and the connection is made with a 96pin Sony connector and differential LVDS signals.





The outer dimensions of the ADC daughter board (including the front panel) are approximately 100 x 120 x 20 mm^3.

The signals coming from the FADCTF module have open collector outputs and are terminated with 330Ω on the PCI-Link module, and the signals from this module to the FADCTF are also open collector outputs and are terminated there. The signals between the PCI-Link and the PCI card are differential LVDS. Incoming signals are terminated differentially with 100Ω.

The table below explains the signals between PCI-Link module and the PCI card in the Linux PC.

Name	Direction	Function
XREQUEST	FADCTF ↓ PC	Goes low when the FADCTF wants to transfer 32 bit data to the PC (i.e. data is to be read out from the Final Memory)
XVALID	FADCTF ↓ PC	Goes low when data are transferred (during the falling transition of the corresponding clock pulse is omitted for timing reasons). The final data transfer is determined with XVALID low followed by a data word and then a clock.
XCLOCK	FADCTF ↓ PC	Same clock as used on the FADCTF modules (20MHz). It would be possible to change to 10MHz (untested).
XOCLK XDIR XPRV	FADCTF ↓ PC	Transmitted, but unused
XENABLE XREADY	PC ↓ FADCTF	Must both be low when a data transfer to the PC is possible

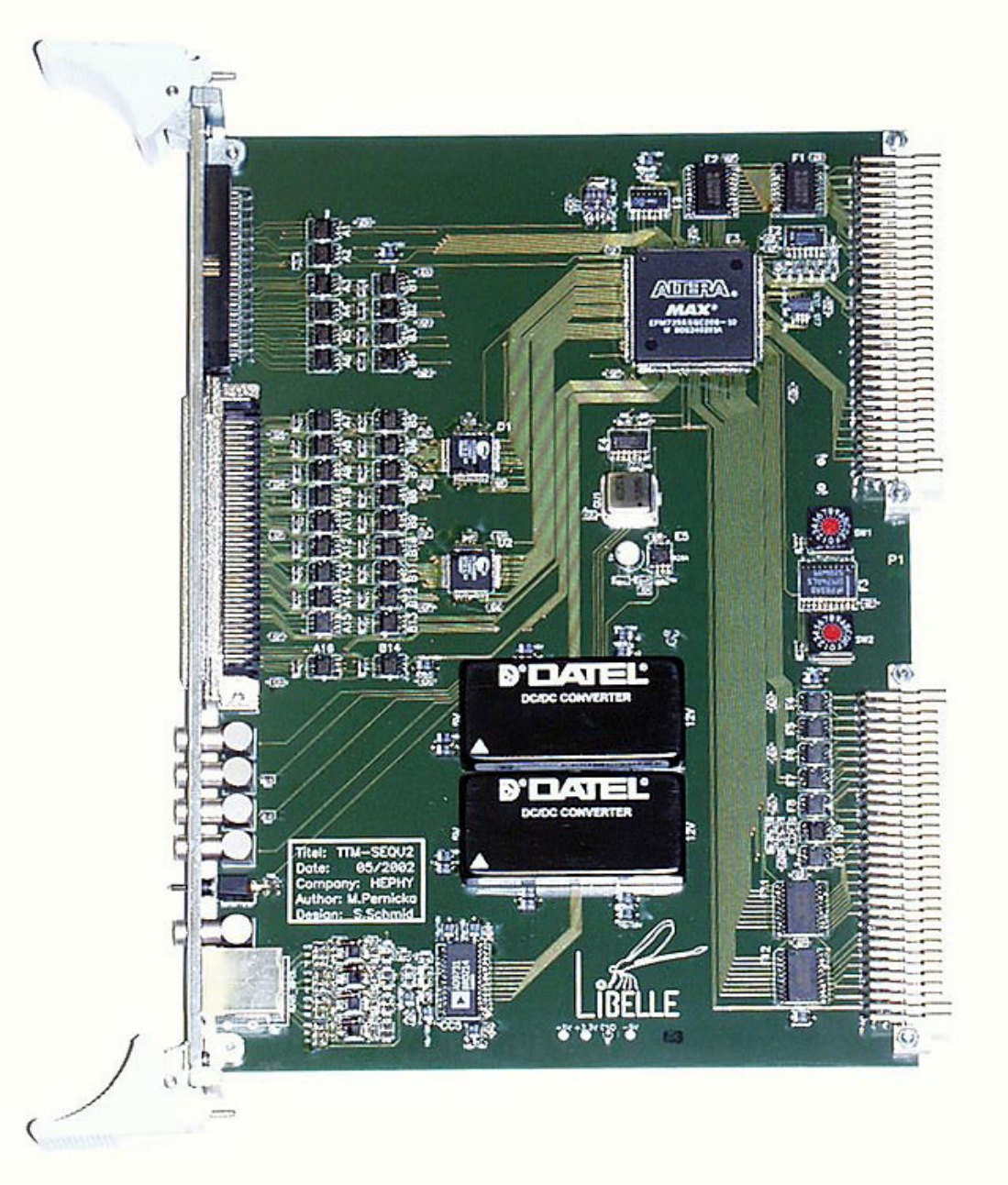
As soon as data is available in the final memory (FIFO not empty), the XREQUEST signal is sent out. When the PC is ready to receive data, both XENABLE and XREADY go low, and the PCI-Link can begin to send data. The 20MHz system clock is sent out on XCLOCK all the time (except for one cycle which is interleaved due to timing specifications), while XVALID=Low indicates valid data to be received on the XDATA lines. After the transfer is finished, XVALID goes high to indicate idle state. XOCLK, XDIR and XPRV are unused.

The delay between clock and data can be adjusted with a jumper in three steps, resulting in 32, 37 or 42ns delay to the clock line wrt the data. The clock must be symmetrical (50% duty cycle), otherwise the delay between data and clock will be different because the inverted clock is used there.

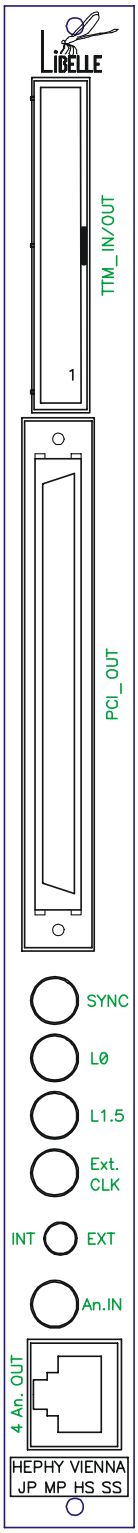
3 TTM-Sequencer (V2, 6U VME)

Basically, the task of the Sequencer is to distribute the clock, timing and control signals from the TTM to the FADCTF modules via the P2 backplane. However, the Sequencer board (version 2) has some additional features. For test purposes in a standalone configuration without a TTM system, it can generate the relevant TTM signals (clock, start, EFT, Event Number, ADC clock) and a test pulse on its own. Moreover, it can be used to generate common signals on 4 channels to be plugged into one particular input of the FADCTF modules. Finally, one PCI-Link output can be plugged into the Sequencer to be read back via VME. There are TTL monitoring outputs which indicate the wired-or L0 and (optional) L1.5 signals over all FADCTF modules in the crate, These two signals and the state of the wired-or BUSY signal can be read by VME.

The mechanical dimensions of the TTM-Sequencer are that of a standard 6U VME board. The photograph below shows the module.



The front panel of the Sequencer is shown below.



TTM_IN/OUT ↔	[Differential TTL] Connection to the TTM system
PCI_OUT ↔	[LVDS] Test input for PCI-Link
SYNC ←	[TTL] Start signal output (scope trigger)
L0 ←	[TTL] Wired-or L0 monitor
L1.5 ←	[TTL] Wired-or L1.5 monitor
Ext. CLK →	[NIM] Optional clock input (20MHz)
INT/EXT	Switch: EXT=repeat TTM signals, INT=use sequencer
An. IN →	Analog input (terminated with 50Ω) to be added to An. OUT
4 An. OUT ←	4 (identical) analog test outputs (RJ45 connector)

The various modes of operation will be explained below.

3.1 External TTM signals

Whenever the front panel switch is in the “external” (right) position, the Sequencer acts as a repeater for the TTM signals described in the following table. With the switch in “internal” (left) position, TTM or internal signals can be selected by a VME register. The signal flow is from the TTM to the

Sequencer for all signals except BUSY and REV, which are propagated in the opposite direction.

Name	Function
CLK20	20 MHz system clock
ADCCLK5	gate for the data taking in transparent mode
Start	begin of a 128-channel strip data block (=begin of valid data)
Stop	end of 128-channel strip data block (=end of valid data) (not used in the FADCTF system)
EFT	Enables (high) or disables (low) Fast-Or comparator
EVTAG[0…3]	4-bit event number
BUSY	indicates that FADCTF FIFOs are almost full (only space for 1 event left) and must be read before further events can be stored
REJ	L1.5 trigger accept signal (=data should be transferred to final memory and read out)
REV	unused

The Sequencer is transparent to these signals between TTM and P2 backplane with one exceptions: The stop signal is not used. The window of the ADC clock on the P2 backplane is opened by a start signal and closed again after 128 cycles. In transparent mode, the ADCCLK5 gate is forwarded to the P2 bus and synchronized to 200ns or 50ns multiples in the TIP1 of the FADCTF.

3.2 Internal signals

This operation requires the front panel switch in “internal” (left) position and the internal mode enabled by VME (see the programmer’s manual for VME details). Either the 20MHz internal oscillator or the front panel input can be selected as a clock source, while the latter can be varied to check out the limits.

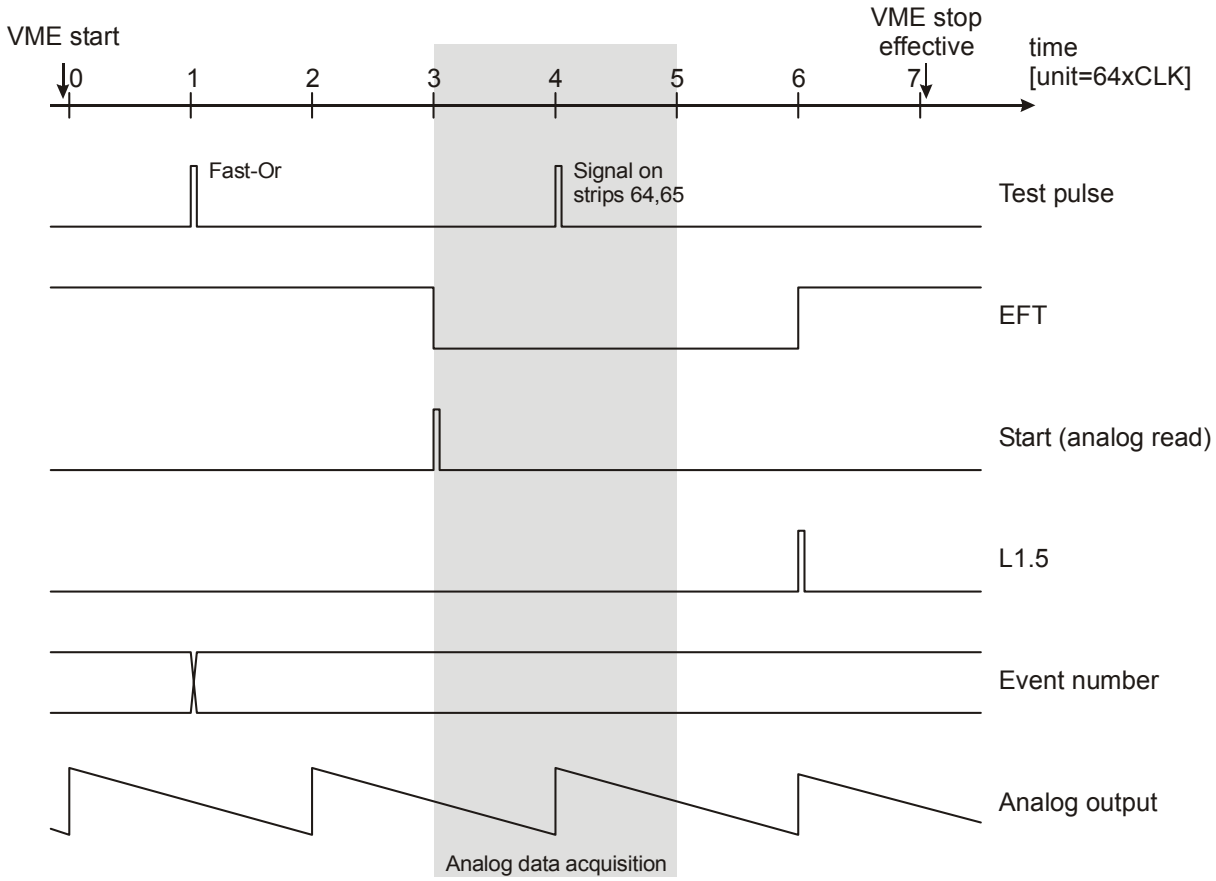
3.2.1 Sequencer operation

With this facility, a complete module and crate test is possible without any external components. Different signals and event types can be produced in this mode.

EFT is enabled in idle mode. Once the STA bit is set by VME, a TTM signal cycle is initiated with a time unit TU=64·200ns=12.8μs (assuming a 20MHz system clock). After TU+2 clock cycles, a test pulse is issued onto the P2 backplane (and thus to all FADCTF modules) which emulates the Fast-Or signal (the Test Procedures section below informs on how to enable/disable the Fast-Or detection for individual channels). After 3 TU, EFT is disabled and a start signal is created. After one more TU, another test pulse is sent out, thus representing a hit in strips 64 and 65 (counting from zero). Finally,

after two more TU, EFT is set high again and a L1.5 accept signal is created only if the 1.5 bit is set by VME. If the STO bit is set, the cycle is finished; otherwise it starts over in a loop.

The timing and signals are illustrated below.



3.2.2 Transparent mode simulation

In order to test the ADCCLK5 synchronization in the TIP1 of the FADCTF, the Sequencer can generate ADCCLK5 gate signals of variable length. Such a gate is issued by a VME write command to N_START. The first 4 N_START commands generate a gate of only 200ns width, thus representing one (5 MHz) or four (20 MHz) samples depending on the sampling speed set on the FADCTF. The next 4 N_STARTs result in and ADC clock window of 400ns width, followed by 600ns, 800ns and so on. Eventually, the DAP FIFO buffer is filled and – provided that the FADCTF is set to test mode – automatically transferred to the final memory, where it can be read out. The gate length count of the Sequencer can be reset to the initial state by writing to N_RESET.

3.3 Input/Output signals

3.3.1 Analog output

A 10 bit DAC (of which only the 7 least significant bits are used) can be directly set by VME. Its output is connected to four identical amplifiers whose outputs are routed to an RJ45 connector which is pin-compatible to

the FADCTF inputs. Thus, any group of 4 channels can be tested by connecting this analog output to any FADCTF input.

There is no (synchronized) memory buffer between VME and DAC, so it should only be used for DC measurements, since the timing is not defined otherwise. Alternatively, an inverse ramp (with DAC values from 127…0) can be automatically issued during the sequence which has a fixed timing wrt the start signal as shown in the graph above. The ADCs will measure the sum of the test pulse and the analog output.

Moreover, there is an analog input on the front panel (LEMO connector; terminated with 50Ω) which is added to the DAC output and commonly distributed to the 4 outputs.

3.3.2 PCI-Link input

The 32 bit data on the PCI-link is synchronously filled into two parallel 16k word FIFOs. The handshake procedure is controlled by VME commands, which can read the state of XREQUEST and set XEANBLE and XREADY.

In idle condition, both XENABLE and XREADY are high. Upon reception of an XREQUEST, one has to set XENABLE and XREADY low and the Sequencer waits for XVALID to indicate valid data, which are strobed into the FIFOs using the XCLOCK.

The parallel FIFOs can then be read out over the VME bus.

3.3.3 Scope trigger output

The start signal is available on a front panel connector (LEMO style) to be used as a scope trigger. The level is TTL with a 500Ω serial resistor (such that it can be terminated with 50Ω at the cost of level reduction).

3.3.4 L0 and L1.5 Trigger outputs

Each FADCTF module can produce L0 and L1.5 (optional) trigger signals, which are sent to the P2 backplane with open collector drivers, such that the bus signals are the wired-or result of all module signals. The status of these wired-or L0 and L1.5 signals can be queried by VME or monitored on two front panel outputs (LEMO style) which again provide TTL levels (protected by serial resistors).

3.4 ±12V converters

The Sequencer board also provides two DC/DC converters to generate ±12V, which is needed by the Sparc interface. These voltages are put onto the dedicated bus lines. Obviously, the Sequencer board must not be plugged to a VME crate that already supplies the ±12V by itself.

4 VME bus systems

The system uses the VME connectors P1, P2 and P3 with 5*32 contacts each. All standard pin assignments are respected, but several user defined signals are added. Moreover, there are some extra power support pins. Therefore, the crate should be only used for modules of the FADCTF system.

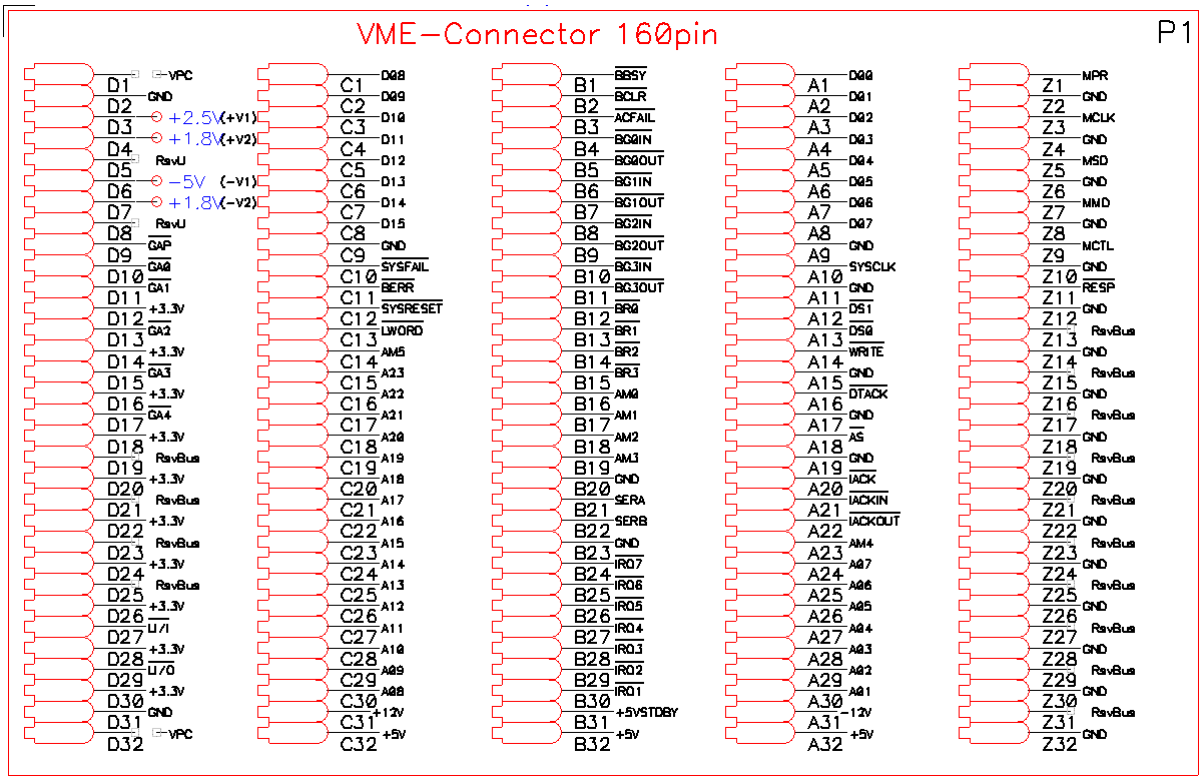
P2 and P3 use custom backplanes which are plugged onto the rear of the crate. All three buses will be described in the following sections.

4.1 P1 connector

Four user defined voltage pins are used for special supply voltages. The ±12V voltages are provided by the Sequencer board and needed by the Sparc interface.

Pin	Name	Voltage
D3	+V1	+2.5V
D4	+V2	+1.8V
D6	– V1	– 5.0V
D7	– V2	+1.8V
A31	– 12V	– 12V
C31	+12V	+12V

The picture below shows all signals on the P1 connector.



4.2 P2 connector

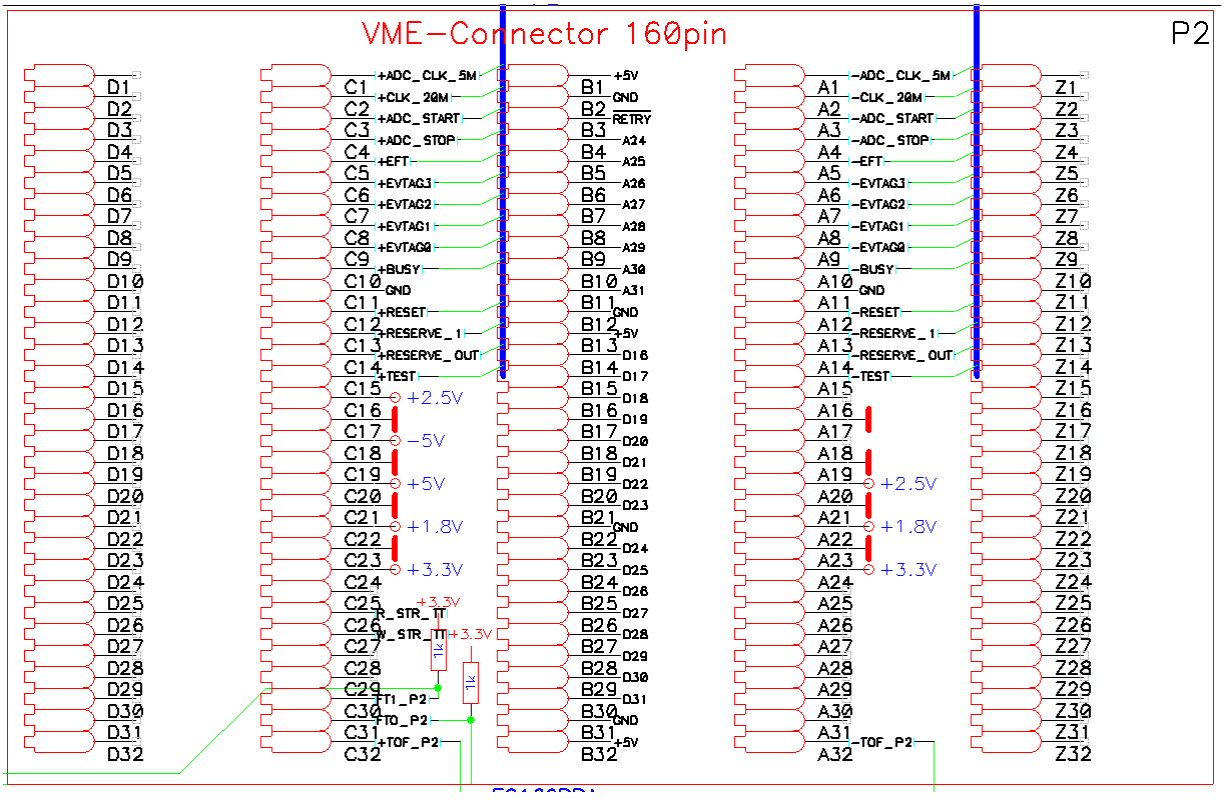
On the P2 connector a special bus is plugged onto the rear side which connects some user defined pins from slots 3 until 21. This bus uses only rows A and C, while row B carries standard VME signals.

The TTM signals (row A), some reserve signals and the test signals are transmitted differentially with LVDS levels. This bus is properly terminated at slot 21, which is the far end from the Sequencer (slot 3).

The user defined bus signals are described in the table below.

Pins	Name	Source	Description
A/C1	ADC_CKL_5M	TTM/Seq.	Gate for data taking in external test-mode
A/C2	CLK-20M	TTM/Seq.	20MHz system clock
A/C3	ADC_START	TTM/Seq.	Start signal for data taking
A/C5	EFT	TTM/Seq.	High=Enable Fast-Or comparators; Low=Disable
A/C6…9	EVTAG1…4	TTM/Seq.	Event number
A/C12	REJ	TTM/Seq.	Accept signal from L1.5 trigger
A/C15	TEST	Sequencer	Test pulse
A/C30	FT1_P2	FADCTF	Wired-or of all L1.5 trigger outputs (optional)
A/C31	FT0_P2	FADCTF	Wired-or of all L0 trigger outputs
A/C32	TOF_P2	FADCTF	Wired-or of all TOF trigger outputs (currently unused)

The voltage support pins for +2.5,-5,+5,+1.8 and +3.3V were only used for the first version of the Sequencer board and thus are obsolete now.

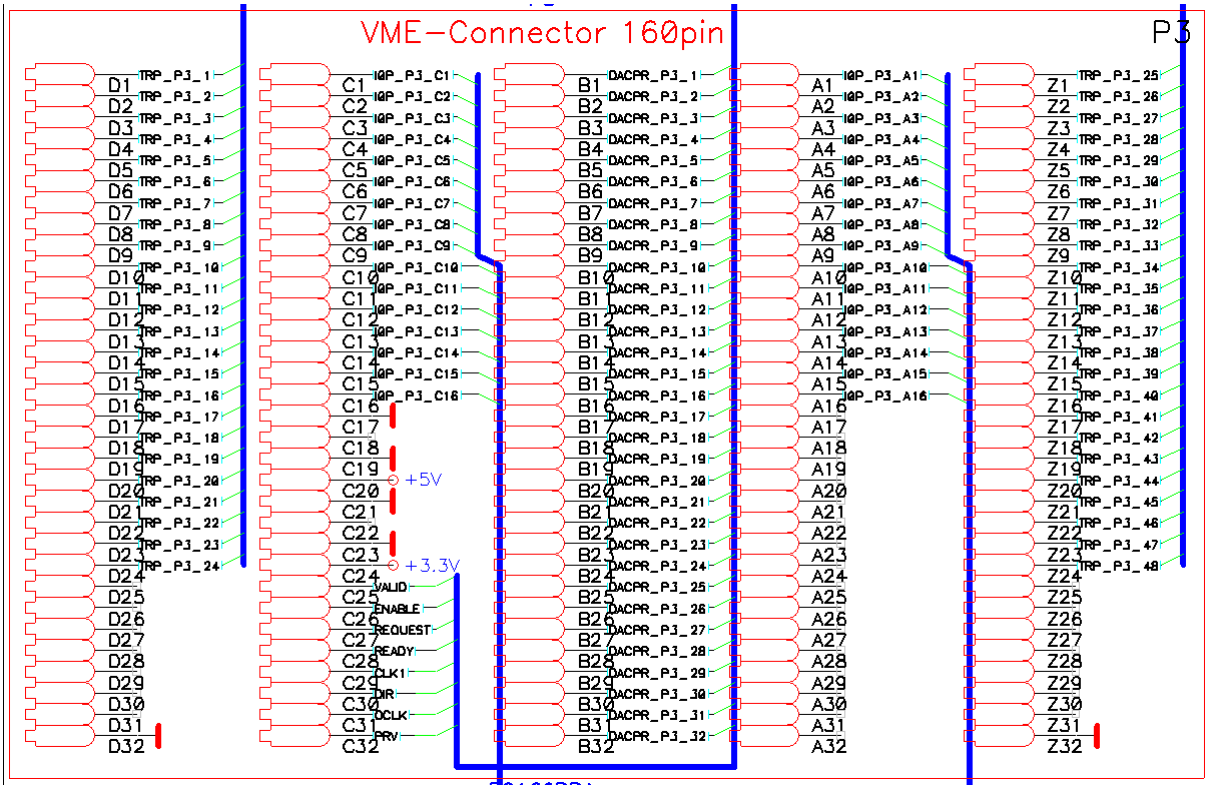


4.3 P3 connector

The P3 connector is almost fully user defined and again has a custom backplane plugged onto the rear side which connects the PCI-Link modules and provides the interconnection between neighboring FADCTF modules.

Row B is used to transfer the 32-bit data word to the PCI-Link module with the control lines con C25…32. The power supply for the PCI-Link is provided on C20 (+5V) and C24 (+3.5V). C17,19,21 and 23 are GND.

Rows C and A are used to transmit or receive the Fast-Or (LO) information from the neighboring FADCTF modules (2x8 lines to each neighbor). Rows D and Z also provide interconnections for the L1.5 processor (optional).



VME communication

The VME communication is explained in the Programmer's Manual.

Test procedures

Two different types of tests can be performed on the FADCTF: internal tests involving only the FADCTF crate (or parts of it) and external tests where the whole DAQ chain is checked.

1 Internal tests

In normal operation, the Sequencer board is used to transceive and distribute the TTM signals. However, in a standalone mode it can also generate all these signals which are required for autonomous testing

purposes. It has its own clock generator and is able to create EFT, start, L1.5 and the event number.

When the test sequence is initialized in standalone mode, EFT is high and a test pulse is sent after a certain time (acting as a Fast-Or, see below for details). Then, EFT is turned off and a start signal is transmitted. Again, a short test pulse is created simulating a hit in two subsequent strip channels. See below for details on how to generate arbitrary hit patterns. This test procedure has a well defined timing and can be executed repeatedly.

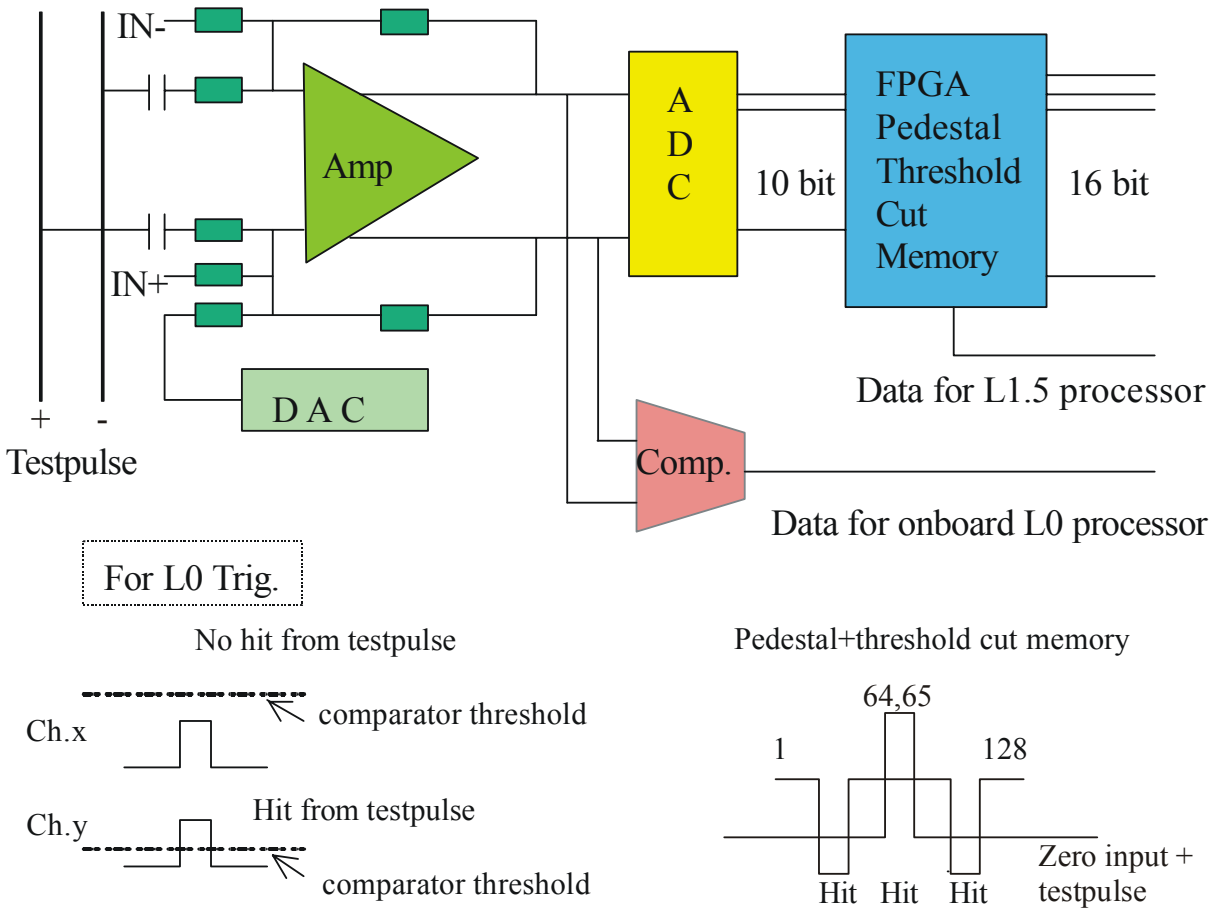
1.1 Fast-Or

A fast digital test pulse (originating from the Sequencer) is received by the mother board which is commonly forwarded to all daughter board inputs. All 24 DAC settings can be accessed in order to individually shift the baseline of each channel such that a Fast-Or is only detected by the comparator if the signal is above a certain threshold. Thus, by switching the DAC settings to a very low value, the test pulse above baseline will not reach the comparator threshold and no Fast-Or is detected on that particular channel. By this method, any arbitrary Fast-Or pattern can be generated by setting a normal DAC level (and thus baseline) to channels which shall fire and a low DAC level to the ones which shall be quiet. Please note that a continuous Fast-Or resulting from a baseline setting above the comparator threshold is not accepted by the subsequent logic.

1.2 Strip data

The Fast-Or on the analog input is followed by zero input (=no signal; will be represented by a central ADC value around 512 counts with a normal DAC setting around 127) for the strip data. Any arbitrary zero-suppressed hitmap output can be produced by loading proper values into the pedestal threshold cut memory such that specific channels are above or below the threshold. In addition, strips 64 and 65 (counting from zero) are also pulsed by a test signal similar to the Fast-Or test pulse. It is recommended that the DAC offsets of each input channel is set individually, such that the output data can be easily verified (e.g. forming a staircase by increasing the DAC offsets with the input channel number).

The graph below indicates the test procedures for Fast-Or and Strip data.



1.3 Sequencer board

The Sequencer does not only provide the clock, control and timing signals, but is can also be used to output an arbitrary waveform on the 4 channels of an RJ45 connector which can be connected to any of the FADCTF inputs for test purposes.

Moreover, the PCI-Link output can be plugged into the Sequencer board to read back the output data via VME.

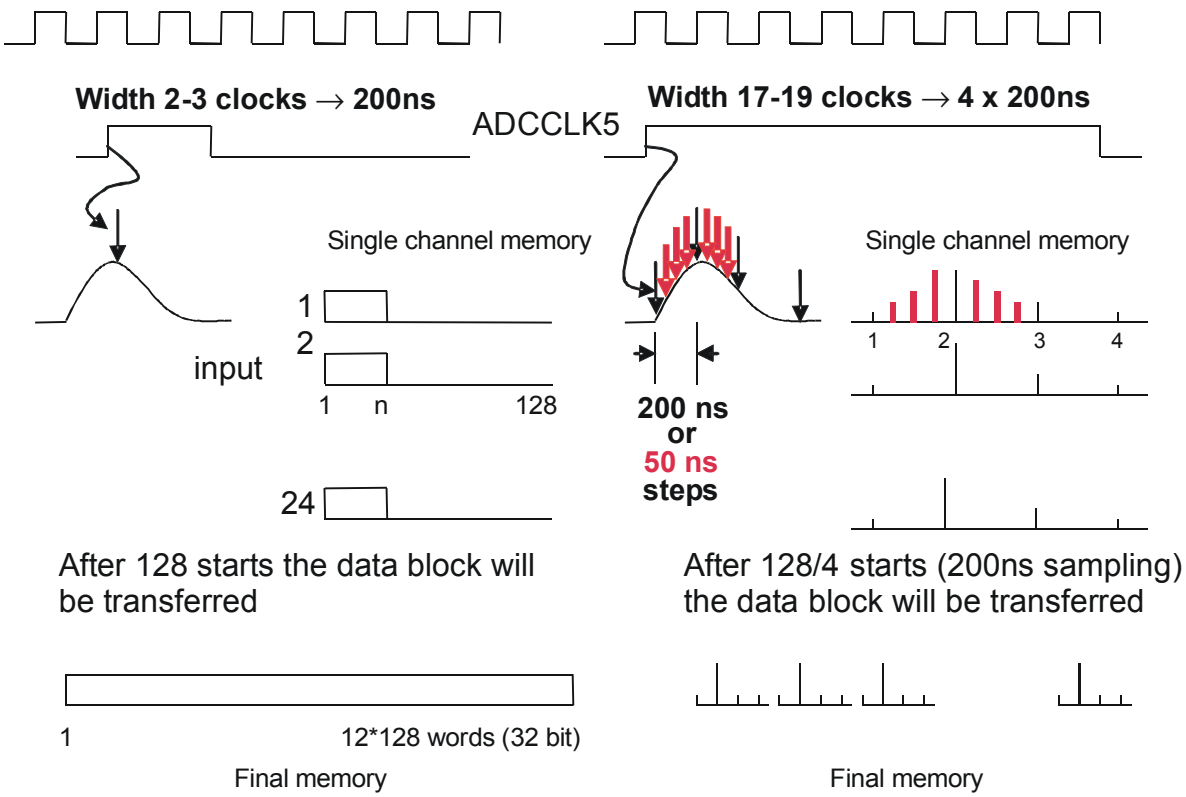
2 External tests

These tests invoke external components such as the VA1TA chips or the TTM system.

2.1 VA1TA transparent mode

The VA1TA chips can be switched to transparent mode, where the output is not multiplexed, but directly shows the shaper output of one single strip channel. While the ADC always runs at 20MHz, only every fourth digitized value is stored (thus 5MHz = VA1TA output rate) in normal operation. Optionally, the readout speed can be set to the full 20MHz sampling which can be useful in transparent mode as illustrated below.

Test of the 24 single transparent channels of a 24 VA1TAs



3 How to test the hybrid with VA1TA, REBO and FADCTF module

3.1 General

It is possible to test every input channel of the VA1TA chip by switching the chip into transparent mode and selecting one of the 128 inputs. In this mode, the shaper output of the selected channel is directly presented at the output without the subsequent sample/hold and multiplexing stages that are operative in normal mode.

Moreover, a test signal (AC coupled step pulse) is sent to the VA1TA input simulating a particle signal. The VA1TA preamp/shaper convert this current spike into a CR-RC shaping curve with an adjustable peaking time of approximately 500ns.

The VA1TA transparent mode output is sampled in the FADCTF modules with either 5 or 20 MHz. One can either collect several samples of the shaping curve to reconstruct the maximum by software or collect only a single sample and tune the timing until it is obtained at the peak of the shaping curve.

In any case, all 24 inputs of an FADCTF work in parallel.

3.2 Method

The user has to decide how many components he/she will include in the test. As an example, the START signal (to initiate a data taking sequence) can

originate from the TTM, the Sequencer or the FADCTF itself. The CLOCK can be taken from TTM or from the Sequencer.

Due to limitations in the number of available pins there is no global switch between 5 and 20 MHz (corresponding to 200 and 50 ns), but each DAP (Data Processor) has to be switched individually.

The FADCTF module(s) must be switched to the test mode (TESTEX) by a VME command writing D02=1 to the TIP1_B register (VME address offset 0x018800). If the internal START signal should be used, it must be set with D03=1 in the same write command. For such tests, only the DAP FIFO memory with address 0 is used. The Final Memory, to which the data are then transferred, can store 2 events at maximum.

The ADCCLK5 signal from the TTM system defines the time slots where one or more samples are taken from the input. This gate will be synchronized to the 200ns ADC sampling period. The width of ADCCLK5 defines the number of samples to be stored; e.g. if it is 200ns or less, only one sample will be taken. The maximum length is 128*200ns or 128*50ns, depending on the sampling rate (5 or 20MHz). If the ADCCLK5 gate is always on, 128 samples will be taken after the start (STARTEX) signal and after that, the data block is transferred to the Final Memory where it can be read out. The event number can be taken either from the TTM, from the Sequencer or from the Timing control (the latter two can be set by VME). In any case, 128 stored samples are required before the data block can be read out.

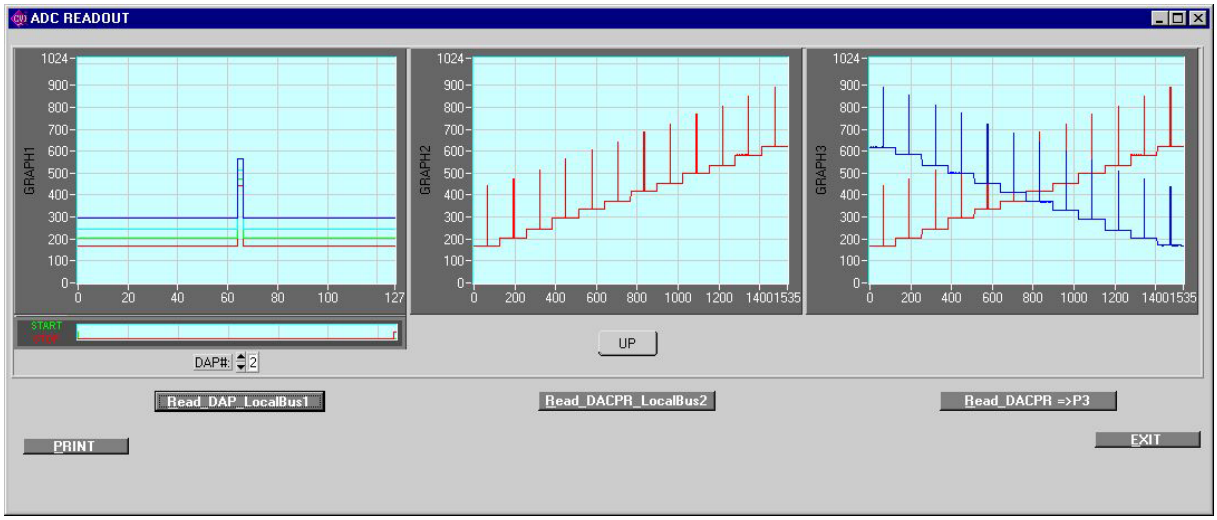
In order to read another 128 samples, another Start signal is required.

4 Screenshots

4.1 Standard internal test

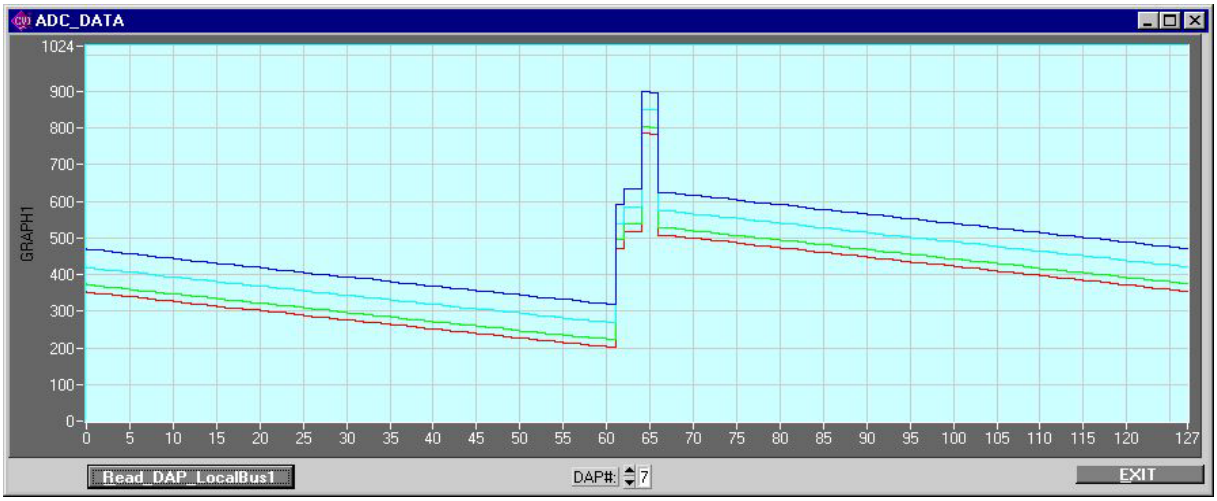
Every input is set to a different pedestal (DAC setting) in order to easily distinguish the different inputs.

The left plot shows an overlay of 4 inputs with the test pulse over 128 samples; the center plot shows 12 channels as they are serialized in the Final Memory (half-word) and the right plot monitors both low and high half-words of the final memory.



4.2 Sequencer DAC ramp

The Sequencer can generate a DAC ramp synchronous to the start signal which is available on the RJ45 analog output connector. When this signal is connected to an FADCTF input, the (falling) ramp with 128 different signal values is measured by the ADC with the test pulse superimposed as shown below. Again, four different pedestal DAC settings are used to distinguish the inputs.



4.3 Transparent mode simulation

A triangular input is presented to the Sequencer analog input and fed from its RJ45 output into the FADCTF. The picture below shows the result of the transparent (nibble) mode test of the FADCTF with the Sequencer. In the beginning, there are 4 single samples (200ns window each), followed by 4x2 samples (400ns), 4x3 (600ns) and 4x4 (800ns). After that (beginning at sample 40), the ADC sampling is switched to 50ns period (20MHz). This produces 4x20 samples (1000ns), followed by a fraction of 4x24 samples (1200ns).