TIP551

Optically Isolated
4 Channel 16 Bit D/A
Version 1.0 Revision A

User Manual

Issue 1.0

08. September 1997

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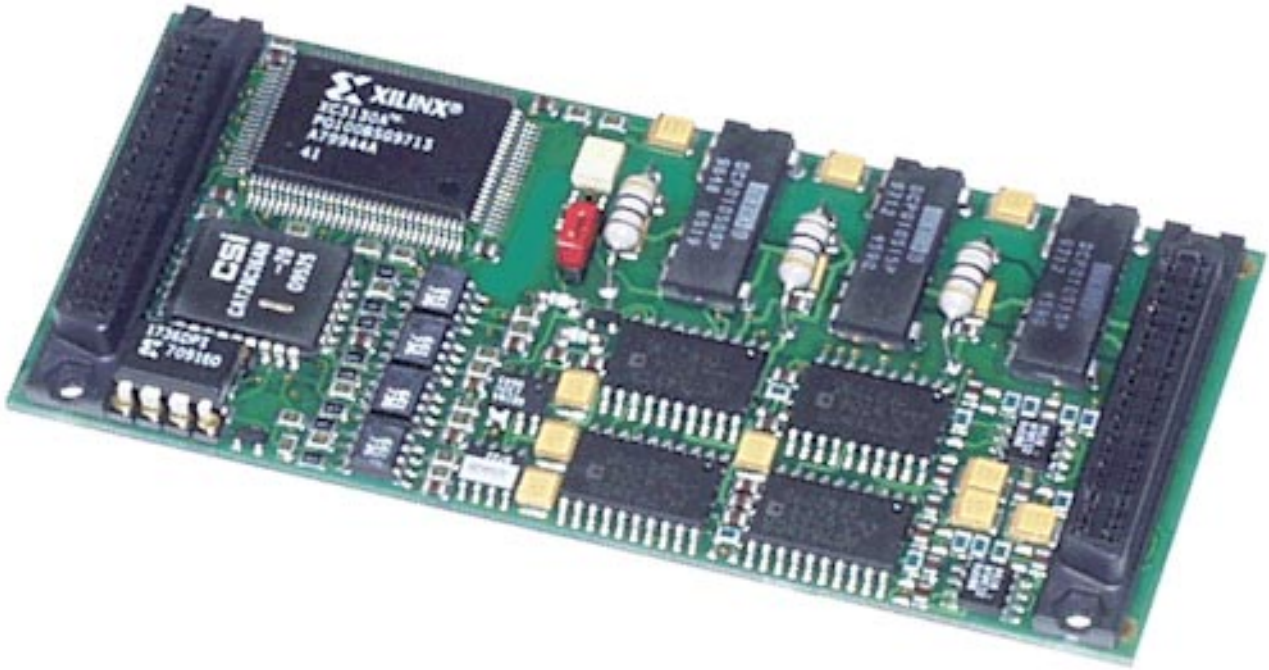

TIP551-10

Optically isolated
4 channel 16 bit D/A
0V to 10V or +/-10V

Issue	Desscription	Date
Preliminary issue		20. Aug. 1997
Issue 1.0		08. Sep. 1997

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1. Product Description

The TIP551 is an IndustryPack® compatible module with four 16 bit D/A channels which are galvanically isolated from the IndustryPack logic interface.

Output voltage ranges of ±10 V or 0 V to 10 V are selectable by jumper for the four D/A channels. After RESET all D/A channels default to 0V.

Each TIP551 is calibrated at the factory. Calibration information of the D/A channels is stored in the Identification PROM unique to each IP.

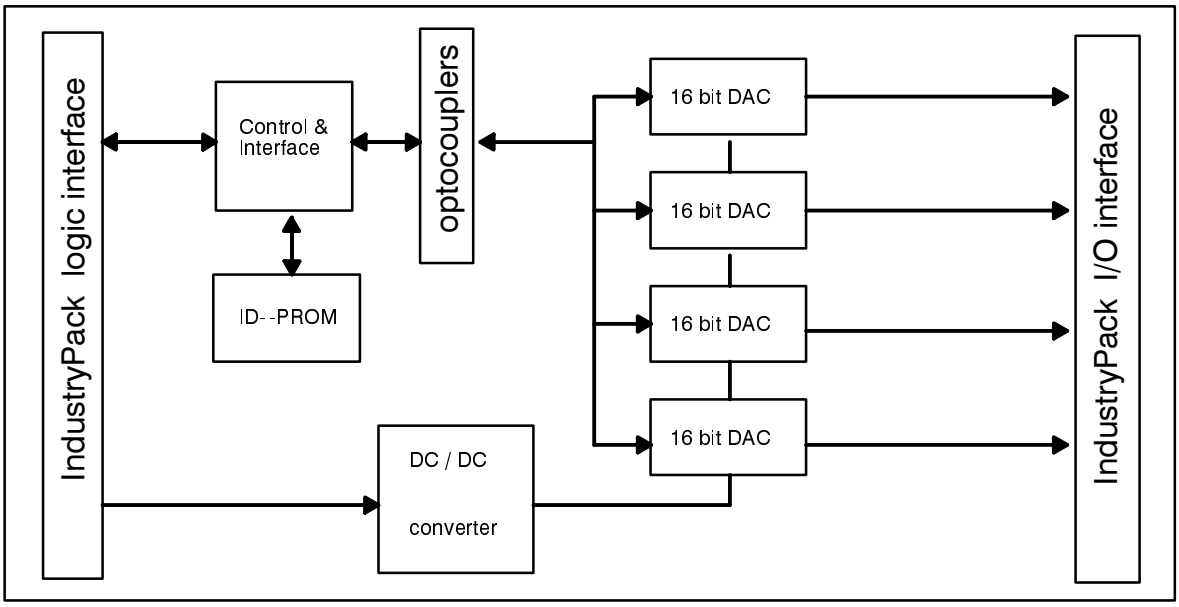

Figure 1: TIP551 Block Diagram

2. Technical Specification

Logic Interface	IndustryPack® Logic Interface
Size	single wide IP
I/O Interface	50-conductor flat cable
Analog Outputs	4 channels
Isolation	All D/A channels are galvanically isolated from the IP Interface
Output Voltage Range	±10V or 0V to 10V, jumper selectable, common for all 4 channels
Settling Time of DAC's	to 0.01% typ. 10 µs
Calibration Data	Calibration data for gain and offset correction of each channel stored in ID PROM
Output Current	±4mA for each channel
Load Capacitance	typical 1 nF
Accuracy	INL ± 4LSB typ. after calibration DNL ±0.5 LSB
Monotonicity	16 bits over the specified temperature range
Wait States	$\overline{\text{IDSEL}}$ 1 wait state $\overline{\text{IOSEL}}$ 0 wait state
Power Requirements	400mA @ 5V no load 430mA @ 5V with 4mA output current for each channel
Temperature Range	Operating -40°C to 85°C Storage -45°C to 125°C
Humidity	5 - 95% non-condensing

3. Functional Description

3.1. Analog Output

The TIP551 includes 4 channels of analog outputs with a rtesolution of 16 bits and a voltage range of ±10V or 0V to 10V. The maximum output current for each channel is ±4mA. Each channel has a typical settling time to 0.01% of 10µs .

Two voltage ranges are jumper selectable: ±10V or 0V to 10V. Voltage range selection covers all 4 channels.

The 4 analog outputs of the TIP551 are galvanically isolated from the IndustryPack logic interface by optocoupler. On board DC/DC converters supply the power to the isolated part of the TIP551.

3.2. Data Correction

There are two errors which affect the DC accuracy of the DAC. The first is the zero error (offset). For the DAC this is the data value required to produce a zero voltage output signal. This error is corrected by subtracting the known error from all readings.

The second error is the gain error. Gain error is the difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the data value by a correction factor.

The data correction values are obtained during factory calibration and are stored in the modules individual version of the ID PROM. The DAC has a pair of offset and gain correction values for each single output channel. The correction values are stored in the ID PROM as two's complement byte wide values in the range -32768 to 32767. For higher accuracy they are scaled to ¼ LSB.

Because offset and gain correction values are dependent on the selected output voltage range the TIP551 has 2 different sets of ID PROM data. Depending on the jumper settings for the voltage range the corresponding set of correction values is automatically selected.

3.2.1. DAC Correction Formula for 0V - 10V Output Range

The basic formula for correcting unipolar DAC output value is:

$$\mathbf{Data = Value * (1 - - Gain_{corr} / 262144) - - Offset_{corr} / 4}$$

Data is the digital value that will be sent to the DAC, Value is the desired output value, $Gain_{corr}$ and $Offset_{corr}$ are the correction factors from the ID PROM.

3.2.2. DAC Correction Formula for ±10V Output Range

The basic formula for correcting bipolar DAC output value is:

$$\mathbf{Data = Value * (1 - - Gain_{corr} / 131072) - - Offset_{corr} / 4}$$

Data is the digital value that will be sent to the DAC, Value is the desired output value, $Gain_{corr}$ and $Offset_{corr}$ are the correction factors from the ID PROM.

$Gain_{corr}$ and $Offset_{corr}$ correction factors are stored separately for each for the four DAC outputs.

Note

Floating point arithmetics or scaled integer arithmetics is necessary to avoid rounding error while computing above formula.

4. ID Prom Contents

The Voltage Range bit of the DAC Status Register is used to select the correct set of ID PROM correction values and the output code.

4.1. ID PROM Contents TIP551-10 V1.0

ADDRESS	FUNCTION		
$ 01	ASCII 'I'		$ 49
$ 03	ASCII 'P'		$ 50
$ 05	ASCII 'A'		$ 41
$ 07	ASCII 'C'		$ 43
$ 09	Manufacturer ID		$ B3
$ 0B	Model Number		$ 23
$ 0D	Revision		$ 10
$ 0F	RESERVED		$ 00
$ 11	Driver-ID low-byte	$ 00	
$ 13	Driver-ID high-byte	$ 00	
$ 15	number of bytes used	$ 1D	
$ 17	C R C		
$ variable			
$ 19	Version -10	$ 0A	
$ 1B	DAC1 Offset	Ch.1 Low Byte	$ board dependent
$ 1D	DAC1 Offset	Ch.1 High Byte	$ board dependent
$ 1F	DAC2 Offset	Ch.2 Low Byte	$ board dependent
$ 21	DAC2 Offset	Ch.2 High Byte	$ board dependent
$ 23	DAC3 Offset	Ch.3 Low Byte	$ board dependent
$ 25	DAC3 Offset	Ch.3 High Byte	$ board dependent
$ 27	DAC4 Offset	Ch.4 Low Byte	$ board dependent
$ 29	DAC4 Offset	Ch.4 High Byte	$ board dependent
$ 2B	DAC1 Gain	Ch.1 Low Byte	$ board dependent
$ 2D	DAC1 Gain	Ch.1 High Byte	$ board dependent
$ 2F	DAC2 Gain	Ch.2 Low Byte	$ board dependent
$ 31	DAC2 Gain	Ch.2 High Byte	$ board dependent
$ 33	DAC3 Gain	Ch.3 Low Byte	$ board dependent
$ 35	DAC3 Gain	Ch.3 High Byte	$ board dependent
$ 37	DAC4 Gain	Ch.4 Low Byte	$ board dependent
$ 39	DAC4 Gain	Ch.4 High Byte	$ board dependent

.....	Not used	.....
$ 3F		$ 00

Figure 2: ID PROM Contents TIP551-10 V1.0

5. IP Addressing

The TIP551 is controlled by a set of registers, which are directly accessible in the I/O address space of the IP. All registers are automatically cleared by assertion of IP_RESET.

ADDRESS	NAME	FUNCTION	SIZE	ACCESS
$ 01	CHANSEL	DAC Channel Select Register		byte R/W
$ 03	STATUS	DAC Status Register	byte	R/W
$ 04	DATAREG	DAC Data Register	word	R/W
$ 07	LOADDAC	DAC Load Register	byte	W
$ 09	IDWRENA	ID Write Enable Register		byte R/W

Note

IDWRENA is for factory use only, do **not** write to this register.

5.1. Channel Select Register Address $01

The DAC Channel Select Register CHANSEL is used to select an output channel. This is done by writing the corresponding bit pattern into bit 0 to bit 1. A write access to the CHANSEL register starts the serial datatransfer to the DAC of the value stored in the DAC Data Register DATAREG. Be sure that the desired value is stored in the DATAREG before starting the conversion by writing to the DAC Channel Select Register CHANSEL. If Bit 7 is set to '1' a load signal is automatically generated after serial data transferto the desired DAC has completed. The load signal updates all 4 DAC's with the value of the shift register of each DAC. Write accesses to the DAC Channel Select Register during DACBUSY active are ignored and set the ERROR flag in the DAC Status Register STATREG.

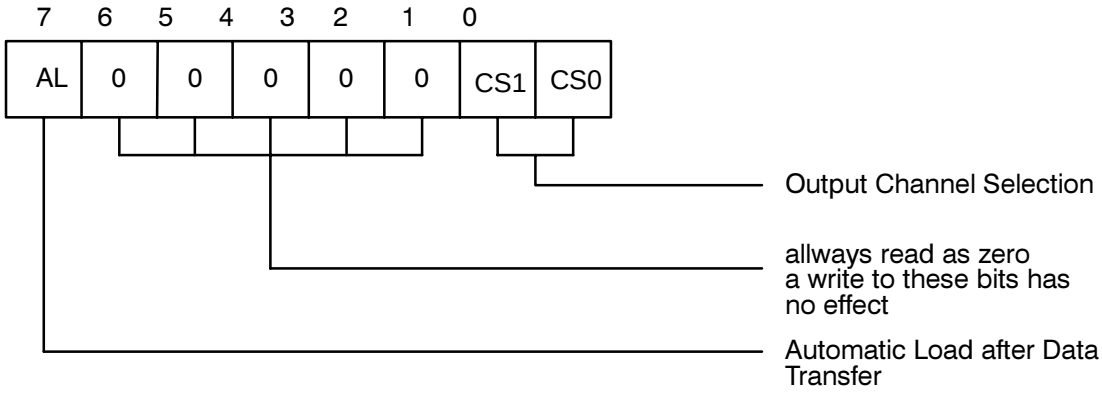

Figure 3: CHANSEL Channel Select Register

5.1.1. Output Channel Selection

Bit 0 to bit 2 of the Channel Select Register are used to select the output channel of the TIP551.

CS1	CS0	CHANNEL
0	0	1
0	1	2
1	0	3
1	1	4

Figure 4: Output Channel Select Table

5.1.2. Automatic Load Bit

If bit 7 is set to '1' all 4 DAC's are updated automatically after data transmition to the selected DAC channel. If bit 7 is set to '0' the user can update all DAC's with a write access to the DAC Load Register immediatly or with the next channel selection with bit 7 is set to '1' after data transmition.

5.2. Status Register Address $03

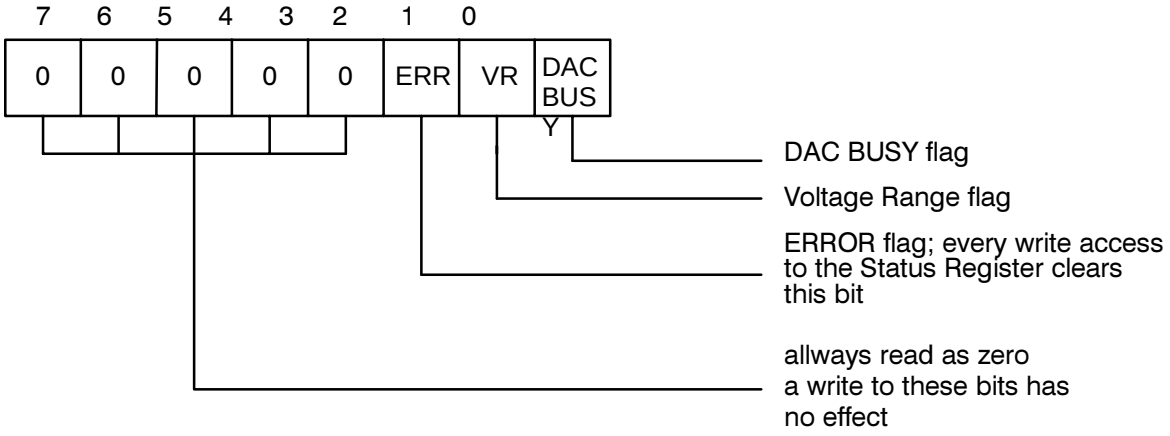

Figure 5: STATREG Status Register

5.2.1. DACBUSY

Reading Bit 0 of the DAC Status Register STATREG as ‘1‘ indicates that a serial data transfer to the DAC is in progress. Write accesses to the DAC Channel Select Register CHANSEL during DACBUSY active are ignored and set the ERROR flag in the DAC Status Register STATREG.

5.2.2. VR Voltage Range

Bit 1 of the DAC Status Register indicates the selected Voltage Range according to the jumper setting for the output voltage ranges of the TIP551. Reading bit 1 as ’0’ means +/- 10V output range and binary two‘s complement as output code , reading bit 1 as’1’ means 0V to 10V output range and straight binary as output code.

5.2.3. ERROR

Write accesses to the DAC Channel Select Register CHANSEL or a write access to the DAC Load Register LOADREG during DACBUSY active are ignored and set the ERROR flag (bit 2) in the DAC Status Register STATREG to ‘1‘. Any write access to the DAC Status Register STATREG clears the ERROR flag.

5.3. Data Register Address $04

The DAC Data Register DATAREG is a 16 bit wide read/write register. The DAC Data Register contains the desired DAC value. A write access to the DAC Channel Select Register CHANSEL starts the serial data transfer to the DAC and if selected the conversion into an analog value. Now a new value can be written to the DAC Data Register DATAREG, or after transfer and conversion are completed (DACBUSY = '0') the same value of the DAC Data Register can be written to another channel. The data of the DAC Data Register DATAREG are valid as long as they are not changed by a new write access to this register. To use the same value for another output channel just write the new channel to the DAC Channel Select Register.

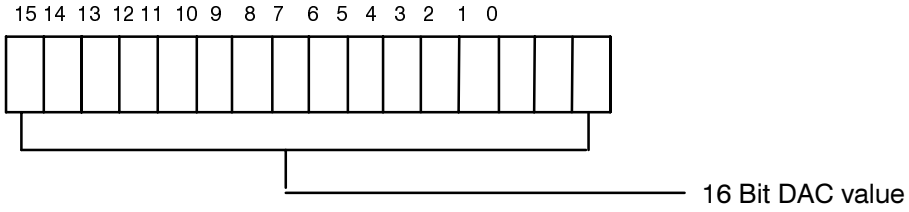

Figure 6: DATAREG Data Register

Note

For output mode look Figure 10 Analog Output Code

5.4. Load Register Address $07

The DAC Load Register LOADREG is a 8 bit wide write only register. Avery write access to the DAC Load Register updates all 4 DAC output's with the last value writen into the DAC's internal shiftregisters. Write accesses to the DAC Load Register LOADREG during DACBUSY active are ignored and set the ERROR flag in the DAC Status Register STATREG.

6. Analog Output Code

6.1. Bipolar Output Code

If the DAC channels are configured for +/- 10V output range by the corresponding jumpers the following analog output code is valid:

DATAREG	OUTPUT
$7FFF	+ Full-Scale
$8000	- Full-Scale
$0000	Midscale

6.2. Unipolar Output Code

If the DAC channels are configured for 0V to10V output range by the corresponding jumpers the following analog output code is valid:

DATAREG	OUTPUT
$FFFF	Full-Scale
$8000	Midscale
$0000	Zero-Scale

7. Jumper Configuration

The TIP551 must be configured by a 3 pin jumperfield for the desired output voltage range ±10V or 0V to 10V. See the following table for the corresponding jumper settings. The jumper seting is valid for all 4 DAC channels.

Voltage range ±10V:	J1	1-2 installed
Voltage range 0V to 10V:	J1	2-3 installed

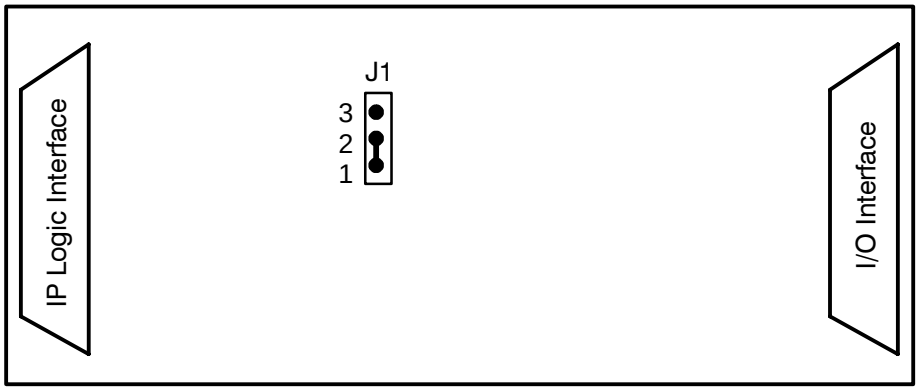

Figure 7: TIP551 Jumper Configuration for Voltage Ranges

Note

Factory configuration is 0 to 10V for all channels.

8. IP I/O connector

8.1. Analog Output Connections

Pin-Number	Signal
01	DAC output 1
02	AGND
03	DAC output 2
04	AGND
05	DAC output 3
06	AGND
07	DAC output 4
08	AGND

Figure 8: TIP551 Analog Output Connections

8.2. Power Input Connections

Pin-Number	Function
44	AGND
45	-15V
46	AGND
47	+15V
48	AGND
49	+5V
50	AGND

Figure 9: TIP551 Power Input Connections

Note

The power input connections are reserved for special versions of the TIP551 without on board DC/DC converter. Do not supply any voltage to these pins for the TIP551- -10 version.