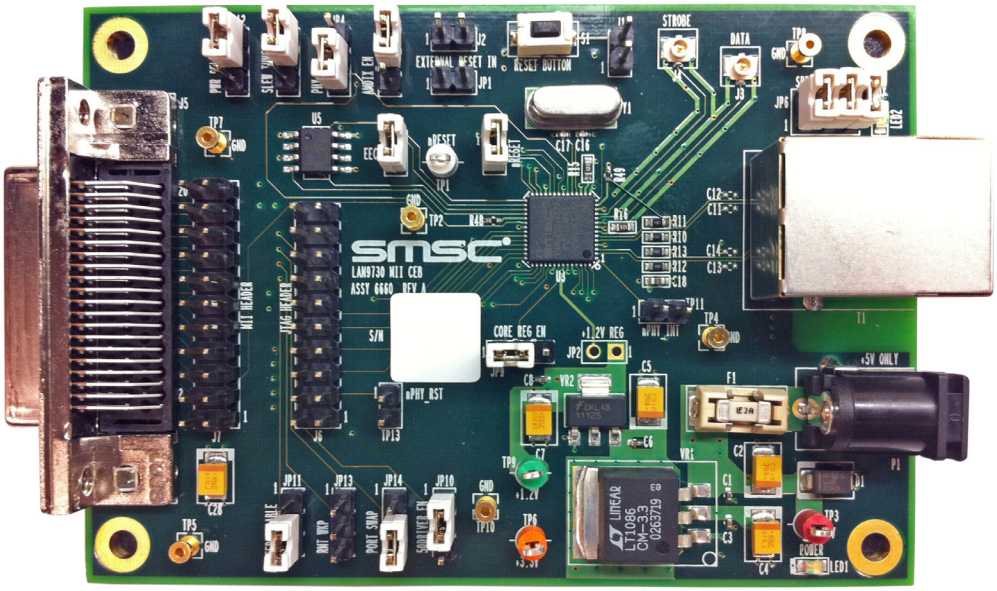
EVB-LAN9730-MII Evaluation Board User Manual



1 Introduction

The LAN9730 is a high-performance, small form factor solution for USB to 10/100 Ethernet port bridging. With applications ranging from embedded systems, set-top boxes, and PVR's, to USB port replicators and test instrumentation, the LAN9730 is targeted as a high-performance, low-cost USB/Ethernet connectivity solution.

The LAN9730 contains an integrated 10/100 Ethernet PHY, HSIC interface, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 kB of internal packet buffering. The LAN9730 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol and USB 2.0 specification, enabling compatibility with industry standard Fast Ethernet and USB 2.0 applications. The HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification 1.0. High-Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s.

The EVB-LAN9730-MII is an Evaluation Board (EVB) that utilizes the LAN9730 to provide a fully functional, self-powered HSIC to Ethernet interface. The EVB-LAN9730-MII provides fully integrated Ethernet and HSIC interfaces via the onboard RJ45 and HSIC Data/Strobe coaxial connectors. The EVB-LAN9730-MII supports internal and external PHY modes. An external PHY may be connected via the onboard 40-pin female MII connector. The onboard 256x8 EEPROM is used to load the EVB-LAN9730-MII's USB configuration parameters and MAC address.

EVB-LAN9730-MII software drivers are available for Windows® XP, Windows Vista, Mac® OS X, Linux®, and Windows CE. Additional manufacturing and diagnostic tools are available for debugging and external EEPROM configuration.

A simplified block diagram of the EVB-LAN9730-MII can be seen in Figure 1.1.

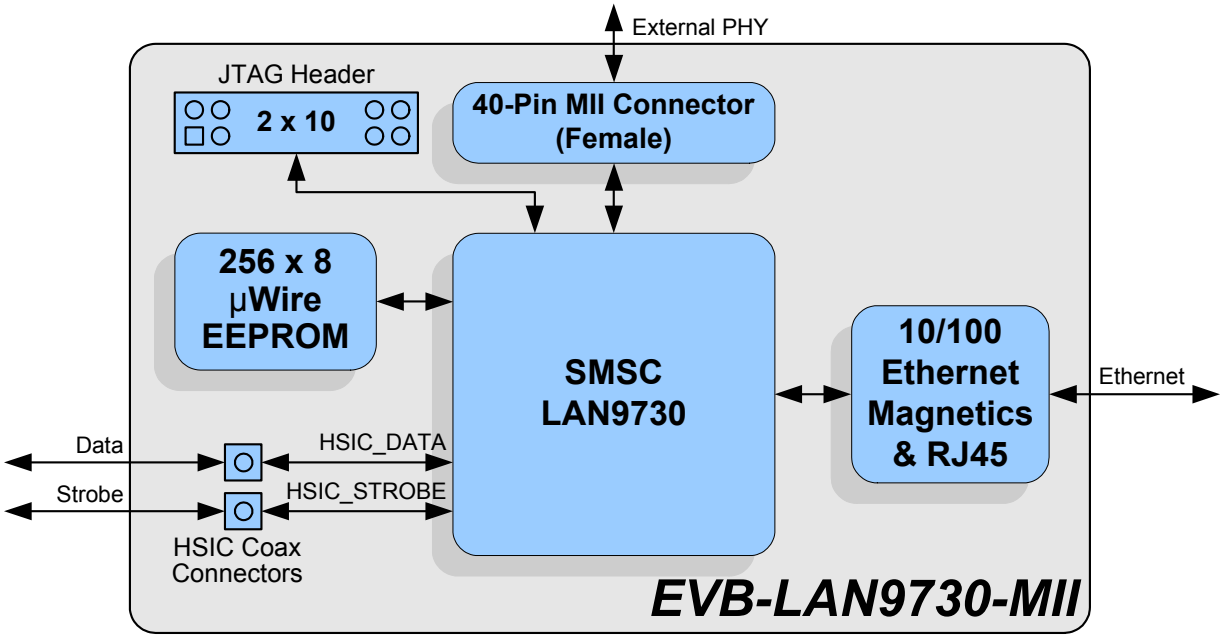


Figure 1.1 EVB-LAN9730-MII Block Diagram

The EVB-LAN9730-MII kit includes two U.FL coaxial cables (Hirose part number U.FL-2LP-068N2-A-(100)) used for connection of the HSIC Data and Strobe signals to a USB HSIC Host. A U.FL RF coaxial cable extraction tool (Hirose part number U.FL-LP-N-2) is provided for properly removing the coaxial cables from the HSIC interconnects. The HSIC coaxial cables and extraction tool can be seen in Figure 1.2.

Note: To avoid inadvertent damage, do not use the extraction tool while the EVB-LAN9730-MII is powered.

Figure 1.2 EVB-LAN9730-MII Coaxial Cables and Extraction Tool

1.1 References

Concepts and material available in the following documents may be helpful when using the EVB-LAN9730-MII.

Table 1.1 References

DOCUMENT	LOCATION
SMSC LAN9730 Datasheet	http://www.smsc.com/lan9730
AN8-13 Suggested Magnetics	http://www.smsc.com/lan9730
SMSC EVB-LAN9730-MII Evaluation Board Schematic	http://www.smsc.com/lan9730

2 Board Details

This section includes the following EVB-LAN9730-MII board details:

- Configuration
- Mechanicals

2.1 Configuration

The following sub-sections describe the various board features including jumpers, LEDs, test points, and system connections. A top view of the EVB-LAN9730-MII is shown in Figure 2.1.

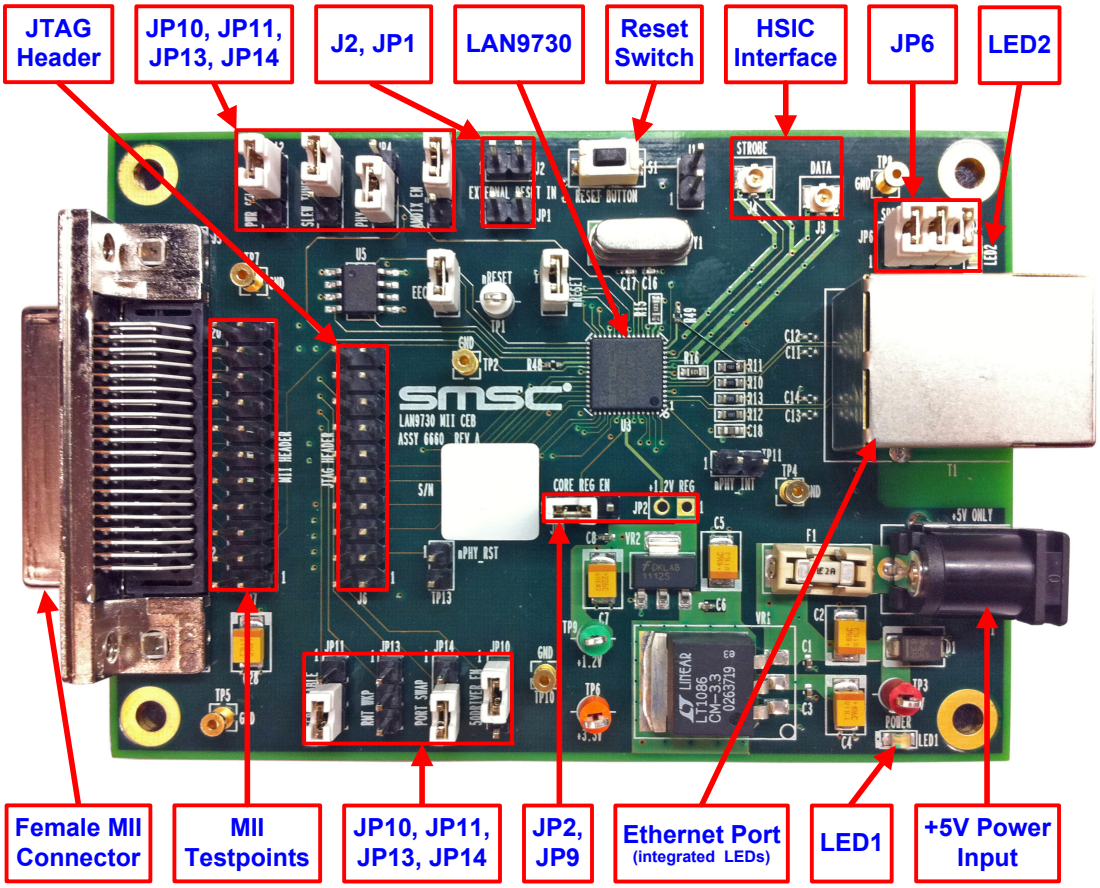


Figure 2.1 EVB-LAN9730-MII Top View

Note: The EVB-LAN9730-MII includes a 2 A fuse (F1) to protect from overcurrent conditions. If this fuse becomes damaged, it can be replaced with a 2 A Littlefuse 154002.DR.

2.1.1 Jumpers

The following table details the jumper definitions and default settings for the EVB-LAN9730-MII.

Jumper settings may be changed as needed. However, any deviation from the default settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

Note: A dashed line in the *Settings* column indicates an installed jumper. All jumper settings are shown in their default state (self-powered, internal Ethernet PHY operation).

Table 2.1 Jumpers

JUMPER	DESCRIPTION	SETTINGS	
JP1	External Host Reset Connect	1 2	**IN:** Connects J2 (external host reset input) to JP5 for input to nRESET **OUT:** Disconnects J2 (external host reset input) to JP5 for input to nRESET **Note:** JP5 must also be installed to utilize an external host reset input on J2.
JP2	+1.2 V Power Supply Select (Note 2.1)	1 2 (DNP)	**IN:** +1.2 V power supplied by an external +1.2 V power source **OUT:** +1.2 V power supplied by the LAN9730's internal regulator
JP4	Ethernet PHY Select	1 2	Selects external Ethernet PHY
		2---3	Selects internal LAN9730 Ethernet PHY
JP5	External Reset Connect	1 2	**IN:** Connects external reset events (S1, J1, J2) to nRESET **OUT:** Disconnects external reset events (S1, J1, J2) to nRESET
JP6	LED Connects (Note 2.2)	1---2	**IN:** Connects Ethernet Speed LED indicator (T1 - Yellow) **OUT:** Disconnects Ethernet Speed LED indicator (T1 - Yellow)
		3---4	**IN:** Connects Ethernet Link/Activity LED indicator (T1 - Green) **OUT:** Disconnects Ethernet Link/Activity LED indicator (T1 - Green)
		5---6	**IN:** Connects Ethernet Full Duplex LED indicator (LED2) **OUT:** Disconnects Ethernet Full Duplex LED indicator (LED2)
JP7	EEPROM Chip Select Connect	1---2	**IN:** Connects the LAN9730's EECS pin to the CS pin of the on-board EEPROM **OUT:** Disconnects the LAN9730's EECS pin from the CS pin of the on-board EEPROM
JP8	HSIC Slew Tune Boost Select	1 2	Selects 30% HSIC_DATA and HSIC_STROBE slew rate boost
		2---3	Selects no HSIC_DATA and HSIC_STROBE slew rate boost

Table 2.1 Jumpers (continued)

JUMPER	DESCRIPTION	SETTINGS	
JP9	+1.2 V Internal Regulator Select (Note 2.1)	1---2	+1.2 V power supplied by the LAN9730's internal regulator
		2 3	+1.2 V power supplied by an external +1.2 V power source
JP10	HSIC Driver Output Impedance Select	1---2	Selects 50 Ohm output impedance on HSIC_DATA and HSIC_STROBE
		2 3	Selects 40 Ohm output impedance on HSIC_DATA and HSIC_STROBE
JP11	EEPROM Select	1 2	Disables EEPROM usage
		2---3	Enables EEPROM usage
JP12	Self/Bus Power Select	1---2	Self-powered device
		2 3	Bus-powered device
JP13	Remote Wakeup Select	1 2	Remote wakeup is supported
		2---3	Remote wakeup is not supported
JP14	Port Swap Select	1 2	HSIC_DATA and HSIC_STROBE pin functionality is swapped
		2---3	HSIC_DATA and HSIC_STROBE pin functionality is not swapped
JP15	Auto-MDIX Select	1---2	Auto-MDIX is enabled
		2 3	Auto-MDIX is disabled

Note 2.1 The EVB-LAN9730-MII is configured to utilize the LAN9730's +1.2 V internal regulator by default (JP2 depopulated and JP9 populated in the 1-2 position). To utilize an external +1.2 V power source, JP2 must be populated and JP9 must be populated in the 2-3 position. Incorrect JP2 and JP9 jumper settings may disable the board.

Note 2.2 Refer to Table 2.2, "LEDs" for descriptions of the various LED functions.

2.1.2 LEDs

Table 2.2 LEDs

REFERENCE	COLOR	INDICATION
LED1	Green	+3.3 V Power Active
LED2	Green	Ethernet Full Duplex **ON:** Full duplex **OFF:** Half duplex **Note:** This LED can be disabled by removing the jumper from the 5-6 position of JP6.
T1	Green	Ethernet Link/Activity **Solid:** Link established **Blinking:** Link activity **OFF:** No link **Note:** This LED can be disabled by removing the jumper from the 3-4 position of JP6.
	Yellow	Ethernet Speed **ON:** 100BASE-TX **OFF:** 10BASE-T **Note:** This LED can be disabled by removing the jumper from the 1-2 position of JP6.

2.1.3 Test Points

Table 2.3 Test Points

TEST POINT	DESCRIPTION	CONNECTION
TP1	nRESET White Test Point	nRESET (LAN9730)
TP2	Ground Gold Post Test Point	GND
TP3	+5.0 V Red Test Point	+5.0 V
TP4	Ground Test Point (DNP)	GND
TP5	Ground Gold Post Test Point	GND
TP6	+3.3 V Orange Test Point	+3.3 V
TP7	Ground Gold Post Test Point	GND
TP8	Ground Gold Post Test Point	GND
TP9	+1.2 V Green Test Point	+1.2 V
TP10	Ground Gold Post Test Point	GND

2.1.4 System Connections

Table 2.4 System Connections

PLUG/HEADER	DESCRIPTION	PART
P1	+5 V Power Supply Barrel Connector	CUI PJ-102AH
T1	RJ45 Ethernet Port with Integrated Magnetics & LEDs	Pulse J0011D01BNL
J1	1x2 External Reset Button Header **PIN 1:** GND **PIN 2:** Reset Generator Input **Note:** JP5 must be installed to utilize J1.	Adam Tech PH1-2-U-A
J2	1x2 External Host Reset Header **PIN 1:** nRESET **PIN 2:** GND **Note:** JP1 and JP5 must be installed to utilize J2. (Note 2.3)	Adam Tech PH1-2-U-A
J3	HSIC DATA Coaxial Connector	Hirose U.FL-R-SMT-1(01)
J4	HSIC STROBE Coaxial Connector	Hirose U.FL-R-SMT-1(01)
J5	40-pin Female MII Connector **Note:** This connector follows the standardized MII pinout. Refer to the EVB-LAN9730-MII schematic for additional information.	AMP 5787170-4
J6	2x10 JTAG Header for IEEE 1149.1 Compliant TAP Controller **Note:** Refer Table 2.5 to for a full pin list.	Adam Tech PH2-20-U-A
J7	2x11 MII Test Point Header **Note:** Refer Table 2.6 to for a full pin list.	Adam Tech PH2-22-U-A
TP11	1x2 nPHY_INT Header **PIN 1:** nPHY_INT **PIN 2:** Ground **Note:** In internal PHY mode, nPHY_INT is a configurable output. In external PHY mode, nPHY_INT is an input.	Adam Tech PH1-2-U-A
TP13	1x2 TDO/nPHY_RST Header **PIN 1:** TDO/nPHY_RST **PIN 2:** Ground **Note:** In internal PHY mode, TDO output is enabled. In external PHY mode, nPHY_RST output is enabled for use as an external PHY reset.	Adam Tech PH1-2-U-A

Note 2.3 External host resets must be of the push-pull type. If the external host reset is open drain, R7 must be removed from the PCB, or the external host reset must be wired directly to JP1.2.

Table 2.5 2x10 JTAG Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	nTRST	11	No Connect
2	Ground	12	Ground
3	TDO	13	No Connect
4	Ground	14	Ground
5	TDI	15	No Connect
6	Ground	16	Ground
7	TMS	17	No Connect
8	Ground	18	Ground
9	TCK	19	No Connect
10	Ground	20	+3.3 V

Table 2.6 2x11 MII Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	Ground	12	TXER
2	Ground	13	TXCLK
3	MDIO/GPIO1	14	TXEN
4	MDC/GPIO2	15	TXD0/GPIO4/EEP_DISABLE
5	TDI/RXD3	16	TXD1/GPIO5/RMT_WKP
6	TMS/RXD2	17	TXD2/GPIO6/PORT_SWAP
7	TCK/RXD1	18	TXD3/GPIO7/50DRIVER_EN
8	nTRST/RXD0	19	COL/GPIO0
9	RXDV	20	CRS/GPIO3
10	RXCLK	21	Ground
11	RXER	22	Ground

2.1.5 Switches

Table 2.7 Switches

SWITCH	DESCRIPTION	FUNCTION
S1	Reset switch	When pressed, triggers a board reset. **Note:** JP5 must be installed to utilize the on-board reset switch. Refer to Table 2.1, "Jumpers" for additional JP5 information.

2.2 Mechanicals

Figure 2.2 details the EVB-LAN9730-MII mechanical dimensions.

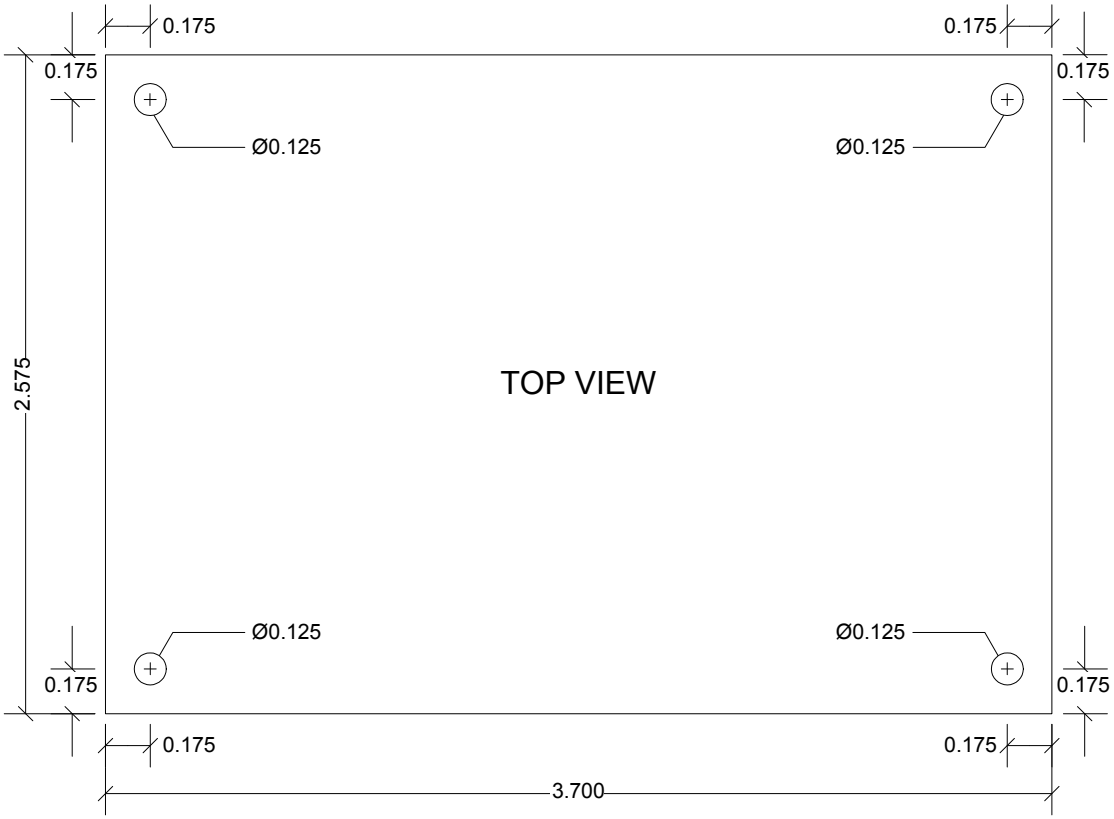


Figure 2.2 EVB-LAN9730-MII Mechanicals

3 User Manual Revision History

Table 3.1 Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (10-14-11)	Initial Release	

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EVB-LAN9730-MII