CDK
Cheetah Development Kit

Hardware User Guide

Revision 0.0
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Revision History

Rev.	Date	Description	Author
0.0	2007/1/16	First Version	Hank Tsai

TABLE OF CONTENT

Preface

Read This First

About the Document

This user's manual describes how to set up, operate and use Cheetah Development Kit (CDK). It has been written for experienced users to getting start in short time.

Documentation Organization

This document contains the following chapters:

Chapter 1 CDK EVB Overview

This chapter contains general overview of CDK EVB, including block diagram, main features

Chapter 2 Setting up CDK

This chapter describes how to start using CDK EVB, including System requirement, how to set up every jumper.

Chapter 3 Hardware Description

This chapter describes the hardware architecture of CDK EVB in more detail, including power, clock, reset, control, peripherals and bus interface.

Appendix A FPGA Pin Assignment

Provide detailed FPGA pin assignment.

Appendix B Mechanical Dimension

Provide mechanical dimension information of IO Daughter Board

Recommended information for further reading

The list shown below is the recommended information for user's further understanding to CDK EVB.

- AMBA Specification (ARM IHI 0011)
- Socle Cheetah chip datasheet
- programmer's guide
- Xilinx Spartan-3 datasheet

Chapter 1

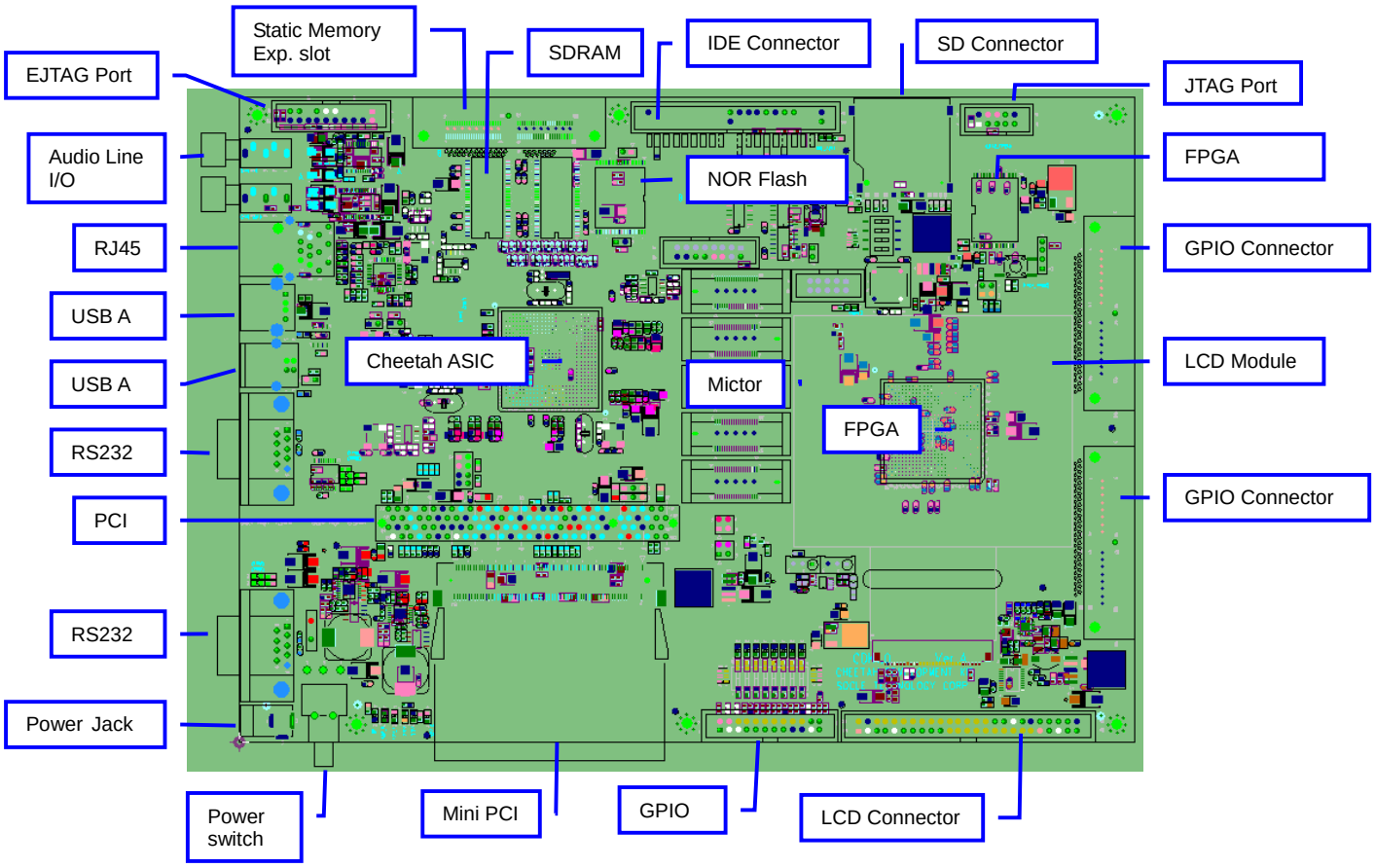
CDK EVB Overview

This chapter gives a brief description of the architecture, features of CDK EVB. It contains the following sections:

- Introduce
- Features
- System Architecture

1.1 Introduce

Socle Cheetah Connectivity ASIC includes two major portions -- one is a highly integrated, pre-verified and silicon-proven System-on-Chip (SoC) design platform core, the other is metal programmable logic cells and I/Os. By changing only 4-6 metal layers, fine-grained fabrics implement logic, the metal programmable logic cells allow timing-optimized ASIC-like cell to be built and ensure performance is optimal. The CDK EVB is designed with Socle Cheetah Connectivity ASIC and one on-chip FPGA to emulate on-chip metal programmable logic cells for user to develop, verify application and hardware/software easily.
The board also provides clock handling, URAT, MAC, RTC, SDRAM,…etc. circuit and integrated software as a reference design.
Fig 1-1 is the overview for CDK EVB. It shows the locations of every component,



F1-1 CDK EVB Overview

1.2 Features

The following is the main features list of CDK EVB:

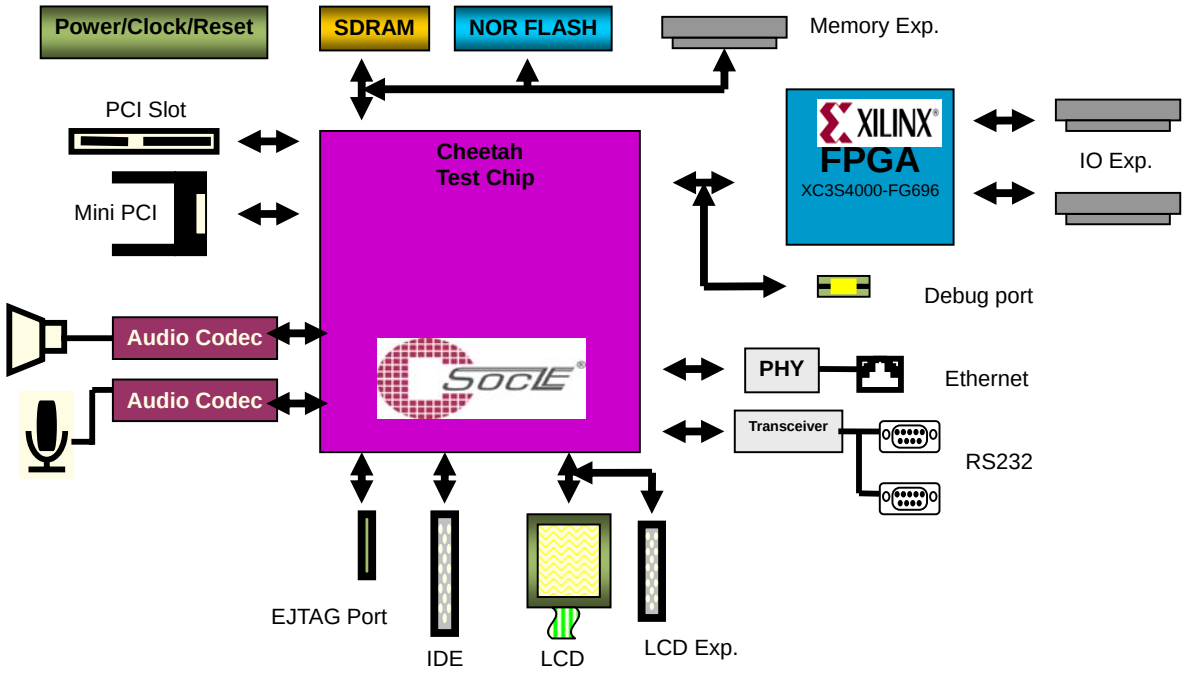
- A power jack connector for 12V AC/DC switching adapter power supply input.
- Socle Cheetah Chip on baord
- Support one Xilinx Spatan XC3S4000-FG676 FPGA for user's design
- Memory
  - Support up to 16MB Intel StrataFlash for Boot code
  - Support up to 64MB SDRAM
  - Support a memory expansion slot
- Peripheral
  - Ethernet
    - One RJ-45 port

Use IC-Plus IP101A PHY on board
- UART
  Two RS232 ports (DB9 type)
  One 8 pins connector for UART
- IDE
  One 2x20 header
- SD connector
- Audio
  Two UDA1342 audio codecs
  One Line In connector
  One Line out connector
- PCI
  One 32bit PCI slot
  One 124 pins tpyeIIIA Mini PCI connector
- LCD
  3.5” TFT LCD module on board
- One 2x25 header for other LCD option
- USB
  One A type connector
  One B type connector

- Other
  - One IO/Memory Expansion slot
    Support up to 200 IO pins for system IO and memory expansion
  - One standard 2.54mm 2x17 pin header with I2C, SPI, PWM, GPIO port A, and ADC signals
  - Support LA mictor type debug ports with all set of MFIO signals
  - One JTAG port for ICE debug
  - Seven LEDs to display GPIO port A status
  - One switch with PA0~PA3 for system setting
  - Jumpers for measure Cheetah power consumption

1.3 System Block Diagram

The Fig1-2 shows the CDK EVB Block Diagram.



F1-2 CDK Block Diagram

Chapter 2
Setting Up and Hardware Reference

This chapter describes how to use the CDK EVB and shows the positions of jumper, headers and connectors. It contains the following sections:

- Install CDK EVB
- Jumper Setting
- Switch Setting
- Connector
- LED Display

2.1 Install CDK EVB
This section describes how to connect hardware components

2.1.1 Requirement
The development system should contain the following items at least:
- CDK EVB
- 12V output power adapter
- Multi-ICE or other debug tool
- IBM compatible PC

Install Steps

1. Plug IO board into CDK AHB Expansion Connector (optional)
2. Switch on power supply
3. Power on ICE

To prevent damaging to all boards, make sure to power down before inserting or removing any device.

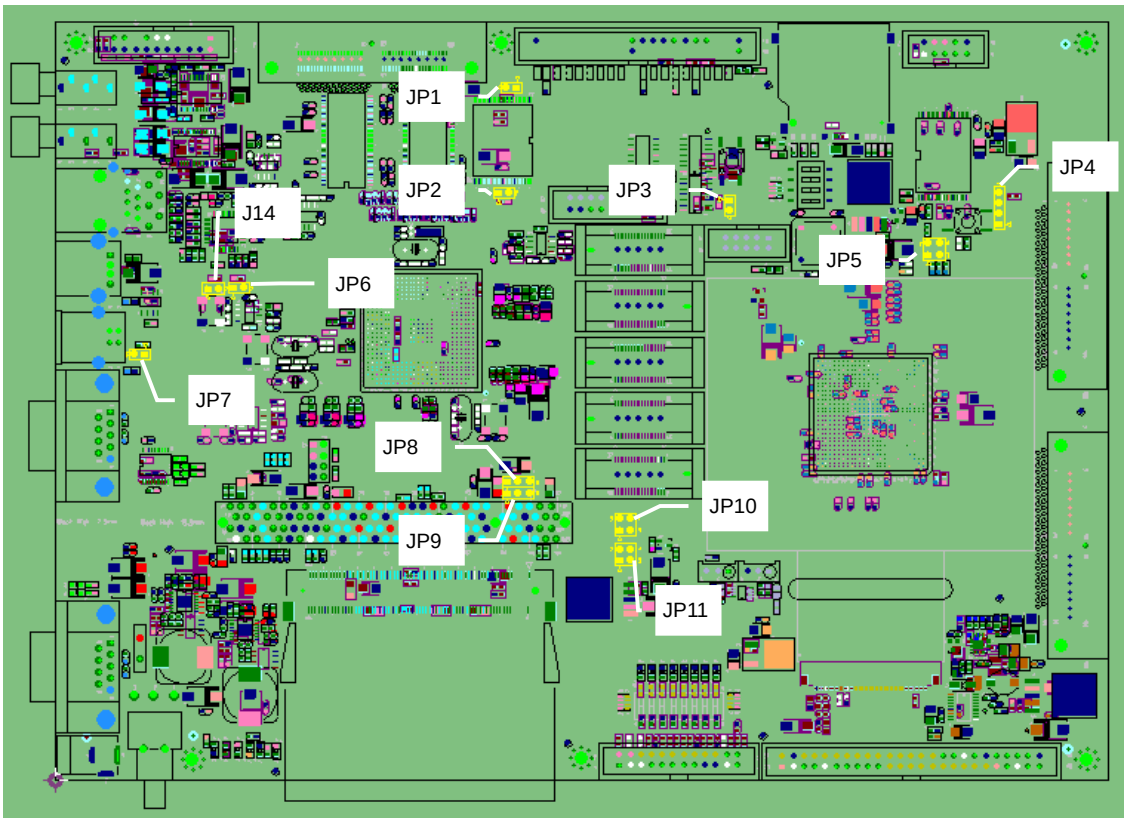
2.2 Jumper Setting
In general, jumpers are used to select options for certain features. On CDK EVB,

some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (short) or remove it from the jumper pins. Fig 2-2 is the jumper/connector location diagram for CDK EVB. The default settings shipped from Socle company are marked with a ★.
Make sure to have all of configuration jumpers on CDK EVB in the proper location

Table 2-1 Jumper List

Location	Function
JP1	NOR Flash Write Protected Setting
JP2	Flash Data Bus Size Selection
JP3	FPGA Status Selection
JP4	Xilinx FPGA image download chain selection
JP5	FPGA configuration mode selection
JP6	USB Mode Selection
J14	AMBA Extension Mode Selection
JP7	VBUS Source Setting
JP8	PCI Slot I/O Voltage Selection
JP9	PCI Slot I/O Voltage Selection
JP10	Cheetah 3.3V Power Connector
JP11	Cheetah 1.2V Power Connector

F2-1 Jumper Location



2.2.1 NOR Flash Write Protected Setting

Select Flash Programming or Write Protected. This is a 1X2 pin header.

JP1	Description	Default Setting
ON	Flash Programming Mode	
OFF	Flash Write Protected Mode	

2.2.2 NOR Flash Data Bus Size Selection

Select Boot Flash data bus size

JP2	Description	Default Setting
ON	8 Bit Mode	
OFF	16 Bit Mode	

2.2.3 FPGA Status Selection

Set FPGA status for generating system reset

JP3	Description
ON	FPGA active/No FPGA on board
OFF	FPGA no image

2.2.4 Xilinx FPGA Image Download Chain Setting

Set FPGA image download chain. This is a 1X4 pin header.

JP4	Description	Default Setting
1-2, 3-4	Program PROM & FPGA	★
2-3	Program FPGA only	

2.2.5 FPGA configuration Mode selection

Select different FPGA configuration mode
The configuration mode is selected by setting the appropriate level on the dedicate mode input pins.

JP5	Description	Default Setting
OFF	Master serial mode	★
1-2, 3-4 ON	Parallel Mode	

2.2.6 USB Mode Selection

Select USB function mode

JP6	Description
OFF	UDC
ON	UHC

2.2.7 AMBA Extension Mode Selection

Select Multi-function I/O function.

J14	Description
OFF	AMBA Bus
ON	CTM MP design interface

2.2.8 VBUS Source Selection

Select digital power supply for ARM test chip-A core.

JP7	Description
ON	VBUS from System Board
OFF	VBUS from Host

2.2.9 PCI Slot I/O Voltage Selection

Select PCI Slot I/O in 3.3V or 5V mode. This is a 1X3 pin header.

JP8	Description	Default Setting
1-2	3.3V Mode	
2-3	5V Mode	★

2.2.10 PCI Slot I/O Voltage Selection

Select PCI Slot I/O in 3.3V or 5V mode. This is a 1X3 pin header.

JP9	Description	Default Setting
1-2	3.3V Mode	
2-3	5V Mode	★

2.2.11 Cheetah 3.3V Power Connector

JP10	Description
1-2, 3-4 ON	Link 3.3V to Cheetah
1-2, 3-4 OFF	No 3.3V to Cheetah

2.2.12 Cheetah 1.2V Power Connector

JP11	Description
1-2, 3-4 ON	Link 1.2V to Cheetah
1-2, 3-4 OFF	No 1.2V to Cheetah

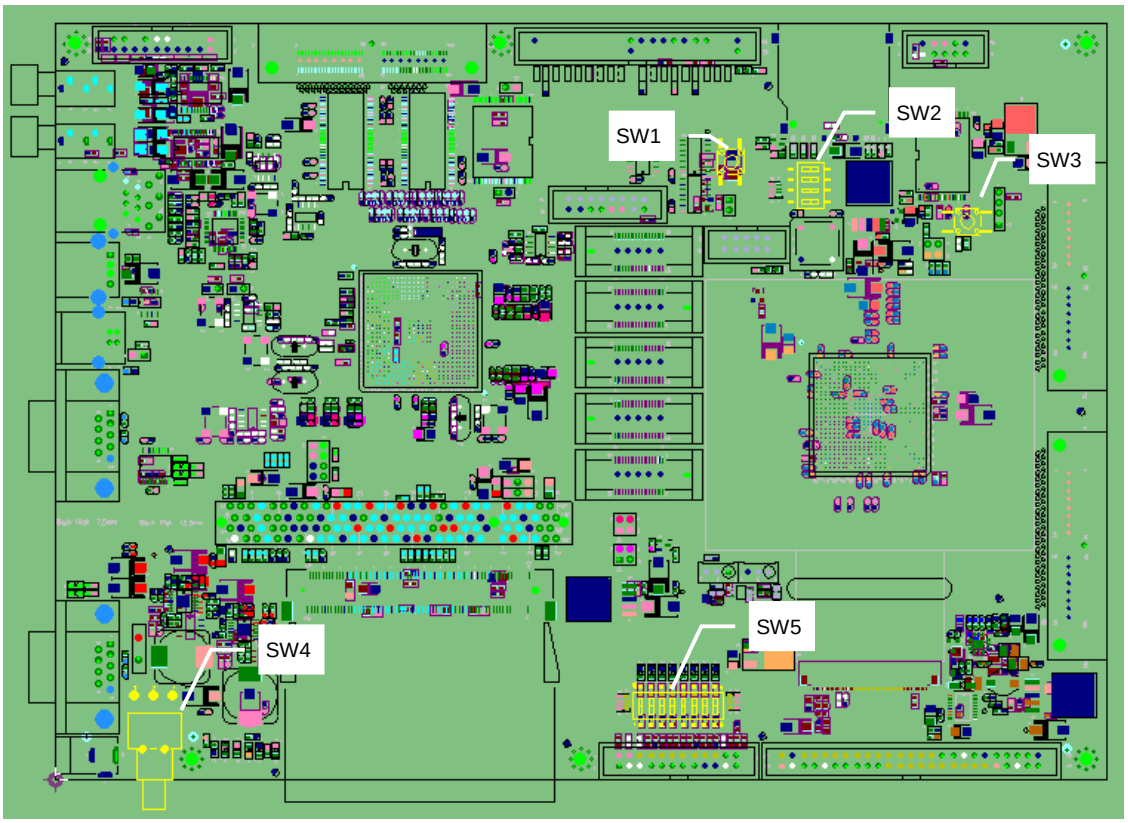
2.3 Switch Setting

The section shows the location of all the switches on the board, and describes the function of each switch.

Table 2-2 Connector List

Location	Function
SW1	System Reset Push Button
SW2	Design Setting Switch to FPGA(Reserved)
SW3,	Xilinx FPGA Re-program Start
SW4	System Power Switch
SW5	GPIO Setting Switch

F 2-2 Switch Location



2.3.1 System Reset Button

This push button SW2 is provided to reset all system.

2.3.2 Design Setting Switch to FPGA

SW2 provides setting pins to FPGA for user's definition.

2.3.3 FPGA Re-program Switch

SW3 restarts or resets download image process from EEPROM to Xilinx FPGA

2.3.4 System Power Switch
SW4 switches on/off system power.

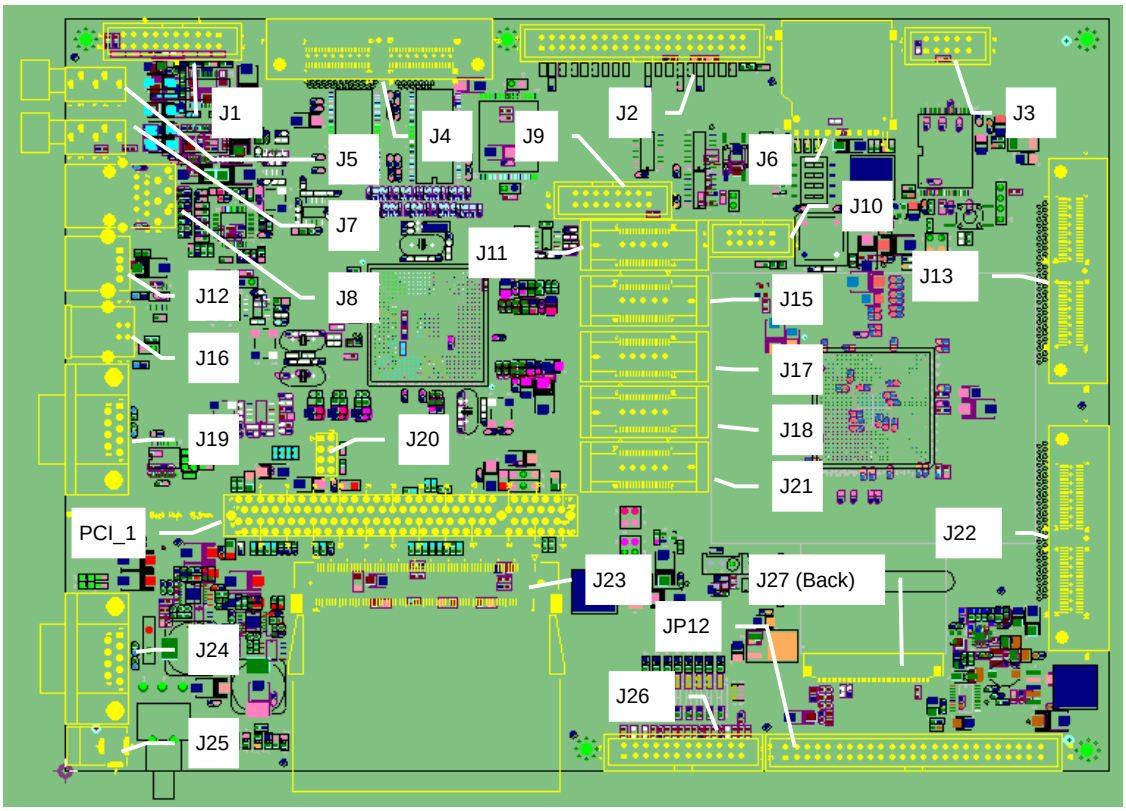
2.3.5 GPIO Setting Switch
SW5 provides High/Low signal to GPIO Port,

2.4 Connectors
The section shows the location of all the connectors on the board, and describes the function of each connector.

Table 2-3 Connector List

Location	Function
J1	ICE JTAG Port
J2	IDE Connector
J3	Download Connector for Xilinx FPGA
J4	Static Memory Expansion Slot
J5	Audio Line in Port
J6	SD Connector
J7	Audio Line Out Port
J8	Ethernet Port
J9	ADC Connector
J10	Debug Port to FPGA
J11,J15, J17, J18, J21	LA Debug Port (Mictor Type Cnnector)
J12	LCD Module Connector
J13, J22	IO Expansion Connector
J16	USB B-type Port
J19	RS232 Port0
J20	RS232 Port2
J23	Mini PCI Connector
J24	RS232 Port1
J25	Power Jack
J26	I2C/SPI/PWM/GPIO Connector
JP12	External LCD Connector
PCI_!	PCI Slot

F 2-3 Connector Location



2.5 LED Display

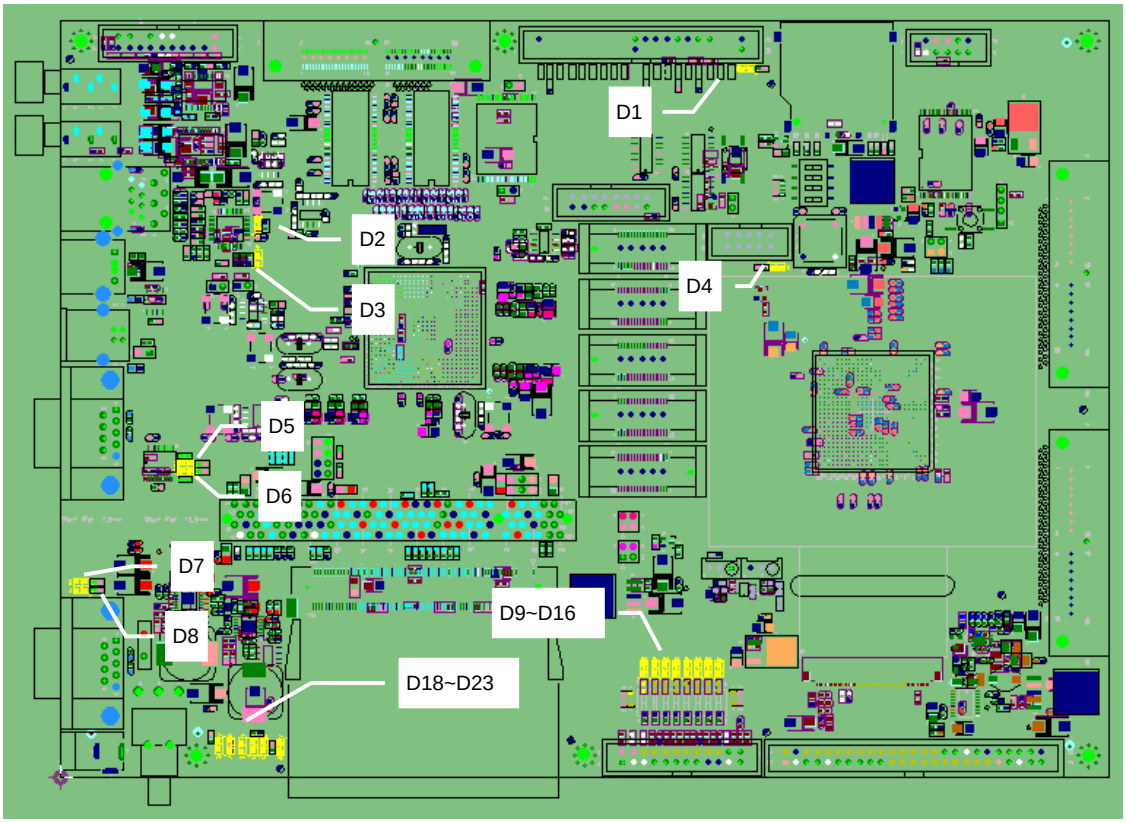
LED displays are to show board's condition.

Table 2-4 LED Display List

Location	Description
D1	IDE Active
D2	MAC COL
D3	MAC LINK
D4	FPGA Image load Done
D5	TXD0 Active
D6	RXD0 Active
D7	TXD1 Active
D8	RXD1 Active
D9~D16	GPIO PA Status, 1->light
D18	5V Power OK
D19	3.3V Power OK

D20	2.5V Power OK
D21	1.2V Power OK for FPGA
D22	1.2V Power OK for ASIC
D23	1.8V Power OK for Configuration Flash

F 2-4 LED Location



Chapter 3

Hardware Description

This chapter describes hardware of CDK EVB. It contains the following sections:

- Power
- Reset
- Clock
- Memory
- Expansion Slot
- Peripheral

3.1 Power

The power for entire CDK EVB Development Board is provided by an external 12V power adapter. Use different regulators to provide power to different components Below is the power scheme of CDK EVB.

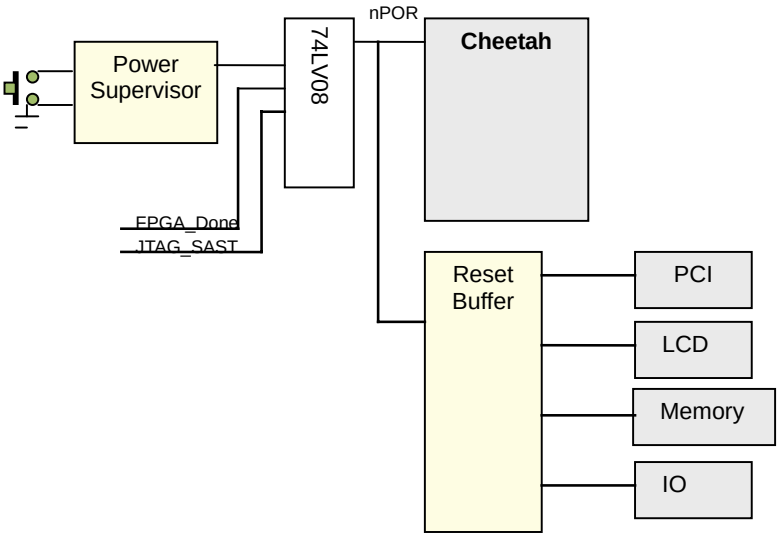
Power		
Device/Connector	**Voltage Requirement**	**Description**
Switching power adapter	Provide +12V	
Cheetah Chip	Core:1.2V IO: 3.3V	
FPGA	Core:1.2V AuxPower: 2.5V IO: 3.3V	
Image EEPROM	Core:1.8V IO: 3.3V	
NOR Flash/SDRAM	3.3V	
MAC PHY	3.3V	
PCI/Mini PCI	3.3V/5V	
UART Transciver	3.3V	
LCD display	5V/3.3V	
Audio	3.3V	
IO/Memory Expansion Slot	5V	

3.2 Reset

There are three sources for reset signal

1. TPS3836-E18 output.
2. EJTAG_RSTn from ICE.
3. FPGA configuration Done Signal

The reset signal will provide Cheetah ASIC reset and different components through 74LV126 buffer.
Press **SW1** to generate a Manual reset signal to whole system when power is on. Below is the reset scheme of CDK.



3.3 Clock

All clock sources for devices are listed in the following table.

Clock		
Device	**Clock Speed**	**Description**
Cheetah	16MHz (Crystal X4)	Main Clock
	27MHz (OSC5)	LCD controller
	33MHz (OSC6)	PCI
	48MHz (OSC4)	USB2.0 and UART
	50MHz (OSC3)	RMII
	32KHz (Crystal X1)	RTC
	48MHz (Crystal X3)	USCB2.0 PHY
	12MHz (Crystal X5)	High speed UART
	33.8699MHz (OSC1)	Audio
	48MHz(Crystal X2)	CTM MP Design
FPGA	(OSC2)	

3.4 Memory

The CDK EVB supports one 16MB Intel StrataFlash NOR type Flash, two 32MB SDRAM on board, It also can extend memory through memory expansion slot J4.

If the Flash on board is not used, just remove R208. For detailed memory map, please refer to “Cheetah Connectivity Specification”.

3.5 System Expand

CDK provides one FPGA (optional) for users to extend system design. There are 133 connections between Cheetah ASIC and FPGA. Set J14 opened, these signals can be AMBA interface, otherwise they will be CTM MP design interface. Besides, 200 pins IO/ expansion slot (J22, J23) provide user to integrate many peripherals circuit on daughter board to meet different application functions. For the pin assignment table and the layout dimension information that provides design reference of daughter board, please refer to Appendix A.

3.6 Peripherals

3.6.1 UART

The CDK EVB supports two RS232 ports (J19, J24) and one UART interface connector (J20). Two couples of LED displays (D5, D6 and D7, D8) show the TX and RX signals status.

3.6.2 Ethernet

Cheetah provides RMII interface to Ethernet PHY. and RJ45 port for Ethernet application.

3.6.3 USB

The EVB provide one USB type A connector and one USB type B connector. User can only use one of them by setting JP6. See Jumper Setting in Chapter 2.

3.6.4 Audio

Cheetah can control UDA1342 via I2C interface to have sound features in playback mode. UDA1342 supports I2S-bus data format. Sound data can communicate between Cheetah and Codec via I2S bus.

3.6.5 LCD

Cheetah builds-in a TFT/STN LCD controller that supports resolution programmable up to 1024X768. The EVB provides one Amprie’s 3.5” LCD module with 320X240 display resolution and touch screen function. If use other LCD module, JP12 provides all LCD controller interface.

3.6.6 GPIO and Serial Interface

The CDK EVB provides one GPIO port, PA[7:0]. 8 LEDs to shows status of these signals for debug. Besides, one connector J26 with serial interface, including I2C, SPI, PWM, and PA[7:0] is provided for IO extension or debug.

Appendix A

FPGA Pin Assignment

This Appendix provides FPGA pin assignment for all devices and connectors.

A.1 MFIO Pin Assignment on FPGA

TableA.1

Name	Pin Location on FPGA	Name	Pin Location on FPGA
MFIO0	A14	MFIO67	D26
MFIO1	A22	MFIO68	E25
MFIO2	A23	MFIO69	E26
MFIO3	D16	MFIO70	G20
MFIO4	E18	MFIO71	G21
MFIO5	F14	MFIO72	F23
MFIO6	F20	MFIO73	F24
MFIO7	G19	MFIO74	G22
MFIO8	C15	MFIO75	G23
MFIO9	C17	MFIO76	F25
MFIO10	D18	MFIO77	F26
MFIO11	D22	MFIO78	G25
MFIO12	E22	MFIO79	G26
MFIO13	B23	MFIO80	H20
MFIO14	C23	MFIO81	H21
MFIO15	E21	MFIO82	H22
MFIO16	F21	MFIO83	J21
MFIO17	B22	MFIO84	H23
MFIO18	C22	MFIO85	H24
MFIO19	C21	MFIO86	H25
MFIO20	D21	MFIO87	H26
MFIO21	A21	MFIO88	J20
MFIO22	B21	MFIO89	K20
MFIO23	D20	MFIO90	J22
MFIO24	E20	MFIO91	J23
MFIO25	A20	MFIO92	J24
MFIO26	B20	MFIO93	J25
MFIO27	E19	MFIO94	K21
MFIO28	F19	MFIO95	K22

MFIO29	C19	MFIO96	K23
MFIO30	D19	MFIO97	K24
MFIO31	A19	MFIO98	K25
MFIO32	B19	MFIO99	K26
MFIO33	F18	MFIO100	L19
MFIO34	G18	MFIO101	L20
MFIO35	B18	MFIO102	L21
MFIO36	C18	MFIO103	L22
MFIO37	F17	MFIO104	L25
MFIO38	G17	MFIO105	L26
MFIO39	D17	MFIO106	M19
MFIO40	E17	MFIO107	M20
MFIO41	A17	MFIO108	M21
MFIO42	B17	MFIO109	M22
MFIO43	G16	MFIO110	L23
MFIO44	H16	MFIO111	M24
MFIO45	E16	MFIO112	M25
MFIO46	F16	MFIO113	M26
MFIO47	A16	MFIO114	N19
MFIO48	B16	MFIO115	N20
MFIO49	G15	MFIO116	N21
MFIO50	H15	MFIO117	N22
MFIO51	E15	MFIO118	N23
MFIO52	F15	MFIO119	N24
MFIO53	A15	MFIO120	N25
MFIO54	B15	MFIO121	N26
MFIO55	G14	MFIO122	AA22
MFIO56	H14	MFIO123	AA21
MFIO57	D14	MFIO124	B14
MFIO58	E14	MFIO125	AB23
MFIO59	D13	MFIO126	AC26
MFIO60	C13	MFIO127	AC25
MFIO61	F22	MFIO128	Y21
MFIO62	C25	MFIO129	Y20
MFIO63	C26	MFIO130	AB26
MFIO64	E23	MFIO131	AB25
MFIO65	E24	MFIO132	C14
MFIO66	D25	MFIO133	AA23

A.2 High Density IO Connector Pin assignment

TableA.2.1 High Density IO Connector – J9

Pin	Name	Pin Location on FPGA	Pin	Name	Pin Location on FPGA
1	P1_1	B13	2	P1_51	M1
3	P1_2	F6	4	P1_52	M2
5	P1_3	E3	6	P1_53	N7
7	P1_4	E4	8	P1_54	N8
9	P1_5	D1	10	P1_55	N5
11	P1_6	D2	12	P1_56	N6
13	P1_7	G6	14	P1_57	N3
15	P1_8	G7	16	P1_58	N4
17	P1_9	E1	18	P1_59	N1
19	P1_10	E2	20	P1_60	N2
21	P1_11	F3	22	P1_61	A3
23	P1_12	F4	24	P1_62	A5
25	P1_13	G4	26	P1_63	A6
27	P1_14	G5	28	P1_64	C4
29	P1_15	F1	30	P1_65	C8
31	P1_16	F2	32	P1_66	C12
33	P1_17	H6	34	P1_67	E13
35	P1_18	H7	36	P1_68	H11
37	P1_19	G1	38	P1_69	H12
39	P1_20	G2	40	P1_70	B3
41	P1_21	J6	42	P1_71	F7
43	P1_22	H5	44	P1_72	G10
45	P1_23	H3	46	P1_73	E5
47	P1_24	H4	48	P1_74	D5
49	P1_25	H1	50	P1_75	B4
51	P1_26	H2	52	P1_76	A4
53	P1_27	K7	54	P1_77	C5
55	P1_28	J7	56	P1_78	B5
57	P1_29	J4	58	P1_79	E6
59	P1_30	J5	60	P1_80	D6
61	P1_31	J2	62	P1_81	C6
63	P1_32	J3	64	P1_82	B6
65	P1_33	K5	66	P1_83	E7
67	P1_34	K6	68	P1_84	D7
69	P1_35	K3	70	P1_85	B7
71	P1_36	K4	72	P1_86	A7
73	P1_37	K1	74	P1_87	G8
75	P1_38	K2	76	P1_88	F8
77	P1_39	L7	78	P1_89	E8
79	P1_40	L8	80	P1_90	D8

81	P1_41	L5	82	P1_91	B8
83	P1_42	L6	84	P1_92	A8
85	P1_43	L1	86	P1_93	G9
87	P1_44	L2	88	P1_94	F9
89	P1_45	M7	90	P1_95	E9
91	P1_46	M8	92	P1_96	D9
93	P1_47	M6	94	P1_97	C9
95	P1_48	M5	96	P1_98	B9
97	P1_49	M3	98	P1_99	A13
99	P1_50	L4	100	P1_100	E10
101	5V		109	GND	
102	5V		110	GND	
103	5V		111	GND	
104	5V		112	GND	
105	5V		113	GND	
106	5V		114	GND	
107	5V		115	GND	
108	5V		116	GND	

TableA.2.2 High Density IO Connector – J11

Pin	Name	Pin Location on FPGA	Pin	Name	Pin Location on FPGA
1	P1_101	AE13	2	P1_151	AF12
3	P1_102	AA7	4	P1_152	AE12
5	P1_103	AA13	6	P1_153	Y13
7	P1_104	AB8	8	P1_154	W13
9	P1_105	AC9	10	P1_155	AA5
11	P1_106	AC11	12	P1_156	AD2
13	P1_107	AD10	14	P1_157	AD1
15	P1_108	AD12	16	P1_158	AB4
17	P1_109	AF4	18	P1_159	AB3
19	P1_110	Y8	20	P1_160	AC2
21	P1_111	AF5	22	P1_161	AC1
23	P1_112	AF13	24	P1_162	AB2
25	P1_113	AE4	26	P1_163	AB1
27	P1_114	AD4	28	P1_164	Y7
29	P1_115	AB6	30	P1_165	Y6
31	P1_116	AA6	32	P1_166	AA4
33	P1_117	AE5	34	P1_167	AA3
35	P1_118	AD5	36	P1_168	Y5
37	P1_119	AD6	38	P1_169	Y4
39	P1_120	AC6	40	P1_170	AA2

41	P1_121	AF6	42	P1_171	AA1
43	P1_122	AE6	44	P1_172	Y2
45	P1_123	AC7	46	P1_173	Y1
47	P1_124	AB7	48	P1_174	W7
49	P1_125	AF7	50	P1_175	W6
51	P1_126	AE7	52	P1_176	V6
53	P1_127	AB8	54	P1_177	W5
55	P1_128	AA8	56	P1_178	W4
57	P1_129	AD8	58	P1_179	W3
59	P1_130	AC8	60	P1_180	W2
61	P1_131	AF8	62	P1_181	W1
63	P1_132	AE8	64	P1_182	V7
65	P1_133	AA9	66	P1_183	U7
67	P1_134	Y9	68	P1_184	V5
69	P1_135	AE9	70	P1_185	V4
71	P1_136	AD9	72	P1_186	V3
73	P1_137	AA10	74	P1_187	V2
75	P1_138	Y10	76	P1_188	U6
77	P1_139	AC10	78	P1_189	U5
79	P1_140	AB10	80	P1_190	U4
81	P1_141	AF10	82	P1_191	U3
83	P1_142	AE10	84	P1_192	U2
85	P1_143	Y11	86	P1_193	U1
87	P1_144	W11	88	P1_194	T8
89	P1_145	AB11	90	P1_195	T7
91	P1_146	AA11	92	P1_196	T6
93	P1_147	AF11	94	P1_197	T5
95	P1_148	AE11	96	P1_198	T2
97	P1_149	Y12	98	P1_199	AD13
99	P1_150	W12	100	P1_200	R8
101	5V		109	GND	
102	5V		110	GND	
103	5V		111	GND	
104	5V		112	GND	
105	5V		113	GND	
106	5V		114	GND	
107	5V		115	GND	
108	5V		116	GND	

A.3 Low Density IO Connector Pin assignment

TableA.3.1 Low Density IO Connector – J9

Pin	Name	Pin Location on FPGA	Pin	Name	Pin Location on FPGA
1	P2_1	W16	2	P2_6	AC22
3	P2_2	AB14	4	P2_7	AE24
5	P2_3	AD25	6	P2_8	AF24
7	P2_4	Y17	8	P2_9	AE23
9	P2_5	AB22	10	P2_10	AF23

TableA.3.2 FPGA Setting Switch –SW2

Pin	Name	Pin Location on FPGA	Pin	Name	Pin Location on FPGA
1	GND		5	SYS_IN0	AA20
2	GND		6	SYS_IN1	AD15
3	GND		7	SYS_IN2	AD19
4	GND		8	SYS_IN3	AD23

Appendix B

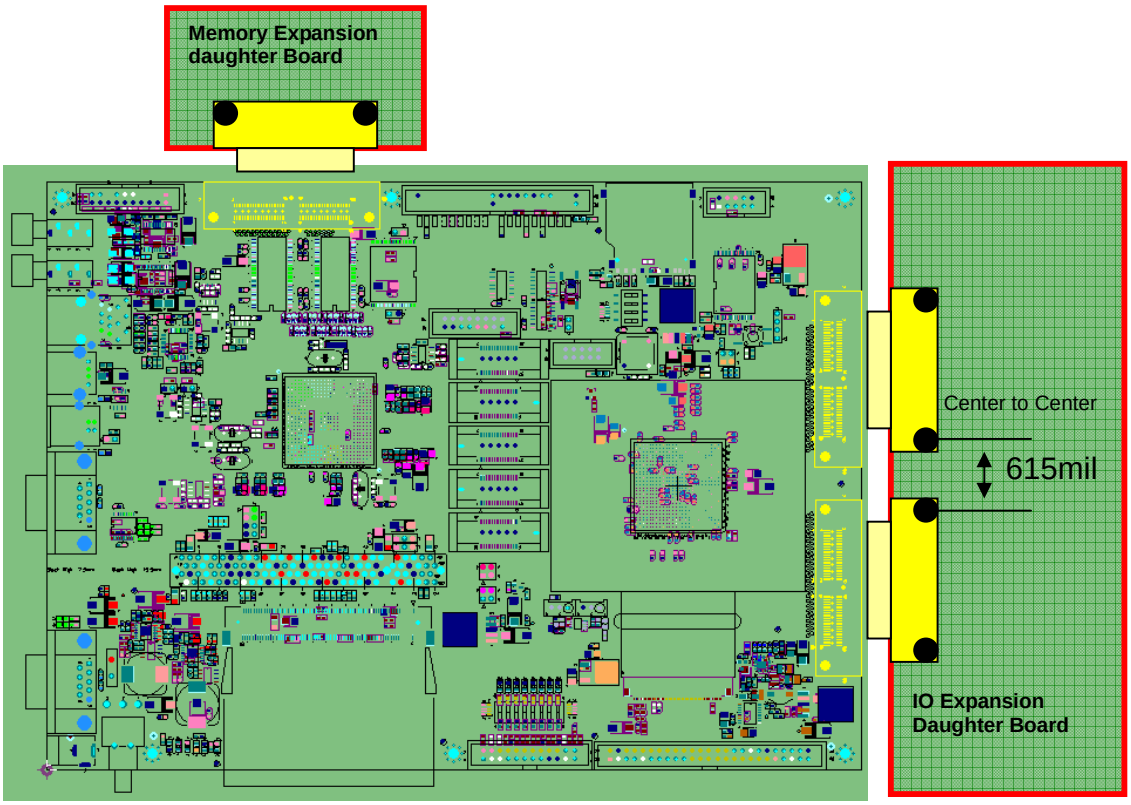
Mechanical Details

This Appendix gives the mechanical dimension for IO Expansion Slot for user to develop application board.

B.1 Layout Dimension

The mechanical dimension of the expansion slots of the board is shown below. It contains the recommended dimension for making daughter board.

Recommend IO Expansion Daughter Board Layout Domension



Connector Information

Connector Vendor	Part Number	Agency Supplier
SAMTEC	QTS-050-01-L-D-RA-WT-LS1	三顧股份有限公司