User's Manual

EVB-5554 Evaluation & Development Kit for Freescale PowerPC MPC5554 Microcontroller

	Ordering code
EVB-5554	ITMPC5554



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Features

The ITMPC5554 Target Board is an evaluation and a development system for the Freescale MPC5554 microcontroller. The ITMPC5554 package consists of a USB cable, a power supply and a target board populated with the Freescale MPC5554 CPU, 2 MB SRAM (4 devices 128Kx32-bit), JTAG debug and Nexus debug connectors and an on-board integrated iSYSTEM JTAG debugger. The application under the development or test can run from the internal CPU flash or from the external SRAM.

Specifications

Clock Speed – up to 132 MHz

Power requirement: 6 - 12V DC , + in the center @ 500 mA

Power output: 5V, 3.3V, and 2.5V regulated supplies

Board Size: 131 mm x 110 mm

EVB-5554 Features

MPC5554

- Ext. 2Mbit (4 devices 128K x 32-bit) SRAM (CY7C1338F)
- 8MHz clock (ext. crystal)
- Power Indicators Supply voltage indications for 5V, 3.3V, and 2.5V supplies
- User Indicator two user indicators to provide user conceived visual response during testing
- Configuration jumper Jumpers J1 to J5 configures processor startup mode; Jumper J6 enables/disables the iSYSTEM on-board integrated USB-JTAG debugger
- Two debug options available JTAG, Nexus
- Low cost and user friendly support manual and software

Software Development

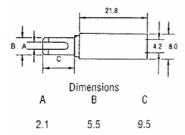
The board has been tested and does run at speeds up to 132 MHz, which you can set by engaging the PLL module in your software. Software development on the EVB-5554 can be performed using the iSYSTEM on-board integrated USB-JTAG debugger. Alternatively, external development tools can be connected to the ONCE (JTAG) or P2 (Nexus) connector. This provides real-time access to all hardware, peripherals and memory on the board. Software is usually uploaded to the external SRAM where it's executed during the development. Then it can be programmed into the CPU Flash in order to execute in standalone when the power is applied.

Getting Started - Setting up the EVB-5554 Board

Power Supply

Permissible input voltage: 6-12 V DC, + in the center. The required current load capacity of the power supply depends on the specific configuration of the ITMPC5554. A power supply with a minimum of 500mA is recommended and delivered in the package. Low voltage DC plug must conform to the DIN 45323 standards:

- The hole diameter is 1.95 2.5 mm (standard: 2.1 mm)
- The external diameter is 6.2 5.5 mm (standard: 5.5 mm)



Switch-on the EVB-5554 after the AC adapter is plugged into the wall and connected to the EVB-5554. Check that power indicators (LD11, LD12, LD13) lit, indicating that 5V, 3.3V and 2.5V voltage is present.

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Note: When connecting an external debugger, make sure that the emulator is powered on first, then the target board and vice versa when switching off the system. First, switch off the target and then the emulator.

Use of On-Board Integrated Debugger

Follow below instructions, in order to get a sample application running with "out of the box" experience.

If winIDEA 2007 CD is not part of the package, please obtain winIDEA 2007 setup from your local iSYSTEM office or from www.isystem.com.

- Install winIDEA 2007 (IDE) full setup on a PC.
- Set jumpers J1-J5 in their default position.
- Set jumper J6, which enables on-board integrated debugger.
- Make sure that power switch on the ITMPC5554 is in off position.
- Connect the power supply to the ITMPC5554.
- Switch on the ITMPC5554.
- Run winIDEA by selecting Start>Programs>... and open ITMPC5554 sample workspace (.jrf) running from the internal flash c:\winIDEA\2007\Examples\Targets\ITMPC5554\IntFLASH).
- Connect USB cable between the PC and the ITMPC5554.
- Windows should auto-detect a new USB device and install belonging USB driver. In case of any problems, the driver is located under winIDEA install directory (e.g. c:\winIDEA\2007\USBDrv).
- Execute Debug/Download. This should program and run the application until main function.
- The application is now ready for debugging. If you run the application, a successful operation is indicated with blinking LED LD11 and LD12.

The on-board integrated USB-JTAG debugger runs without restrictions for 90 days after using it for the first time. After the 90 day period expires, the debugger falls back to a restriction of a 32k byte download limit.

The debugger can be upgraded to a regular debugger (no limits) by purchasing the debug enable license. Additionally, you need to purchase a regular winIDEA license. Please contact your local iSYSTEM distributor for more details on upgrading your development tool.

What To Do Now?

winIDEA allows you to run code step by step, set execution and access breakpoints, examine and modify the source code, rebuild the project using GNU compiler, which is optionally installed during winIDEA installation, and much more. For more information refer to the winIDEA documentation. Software in the combination with the development board can be used as a basis for developing future applications also on your hardware. This project illustrates various programming issues, which are essential to all winIDEA projects:

- Initialization of bus interface unit
- Initialization of configuration registers
- Implementation of dispatch table
- Format of linker definition file
- Correct project settings (Project>Settings), which ensure that the compiler is invoked successfully

More interesting examples are also included on the support CD.

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Troubleshooting

EVB-5554 doesn't show signs of life by first start

- a) Check the power supplied to the EVB board Diodes LD11, LD12 and LD13.
- b) When using the on-board integrated JTAG debugger, make sure that Jumper J6 is enabled. When Jumper J6 is not enabled, a connection to the JTAG or Nexus port must be made.
- c) Try "slow" JTAG Scan Speed if the debugger cannot connect to the CPU.
- d) Execute debug Reset instead of debug Download.

Unable to download the code to the board

- a) Check the power supplied to the EVB board.
- b) Ensure that the correct workspace was loaded into winIDEA.
- c) Check the hardware configuration:
 - Tools>Hardware Plug-In
 - Hardware>Hardware ...
 - Hardware>Emulation Options
- d) Reset the board and try to connect again.

Checksum failed error

a) When performing any kind of checksum, remove all software breakpoints

Default Memory Map

The MPC5554 of the MPC5500 family has two levels of memory hierarchy. The fastest accesses are to the unified 32 Kbytes cache. The next level in the hierarchy contains the 96-Kbyte internal SRAM and internal 2MB Flash memory. Both the internal SRAM and the Flash memory can hold instructions and data. The external bus interface has been designed to support most of the standard memories used with the MPC55xx family. The provided software uses the default memory map. If you modify the memory map make sure that all memory banks and chip select configuration settings are adjusted accordingly.

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EVB-5554 Memory Map

Internal Memory

Address Range	Memory Type	Description
0x 0000 0000- 0x 001F FFFF	2MB - Internal Flash Memory	Internal Flash memory (512KB – 2MB)
0x 2000 0000- 0x 3FFF FFFF	512MB - External Memory	External Memory (see note below)
0x C3F0 0000- 0x C3F0 3FFF	Bridge A Peripherals	Acts as an interface between the system bus and the lower bandwidth peripherals
0x FFF0 0000- 0x FFFF FFFF	Bridge B Peripherals	Acts as an interface between the system bus and the lower bandwidth peripherals
0x 4000 0000- 0x 4000 7FFF	Internal SRAM, Powered Standby	32 Kbytes
0x 4000 8000- 0x 4000 FFFF	Internal SRAM	32 Kbytes

External Memory

There are 4 SRAM devices connected to CS1 and CS2 and cover a 2MB memory area. Offset depends on the CPU configuration. In our case, CS1 is configured to point at 0x2000 0000 through the winIDEA initialization sequence.

Address Range	
0x 2000 0000 – 0x 2007 FFFF	
0x 2008 0000 – 0x 200F FFFF	
0x 2010 0000 – 0x 2017 FFFF	
0x 2018 0000 – 0x 201F FFFF	

SRAM Memory

The MPC5554 internal SRAM module provides a general-purpose 96-Kbyte memory block that supports mapped read/write accesses from any master. Included within the 96-Kbyte SRAM block is a 32-Kbyte block powered by a separate supply for a standby operation.

Flash Memory

The MPC5554 provides 2 Mbytes of programmable, non-volatile, Flash memory storage. The non-volatile memory (NVM) can be used for instruction and/or data storage.

Downloading the code into the memory

winIDEA allows you to load the code directly into the internal Flash memory through the standard debug download. winIDEA identifies, which code from the download file fits in the internal FLASH, and loads it to the Flash through the flash programming procedure hidden to the user. All other code propagates to the target through standard memory writes.

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Demo software has the example configured for the internal Flash. Load the project into winIDEA and execute debug download (Debug->Download), which will download the code directly to the Flash memory. For more information see the winIDEA users manual.

Demo software has also the example configured for the external SRAM. Load the project into winIDEA and execute debug download (Debug->Download), which will download the code to the external SRAM. Access to the external SRAM is configured in the initialization sequence ('Hardware/Emulation Options/Initialization' tab), which winIDEA executes prior to debug download.

Settings and Options

Jumpers

Jumpers J1 to J5 configures processor startup mode. See MPC5554 Reference Manual for more details on the CPU signals BOOTCFG[0:1], PLLCFG[0:1] and WKPCFG. Some boards may not have J1-J5 populated since the CPU has internal pull-ups/downs on belonging signals, which match with the default jumper settings. Jumper J6 selects whether iSYSTEM on-board integrated USB-JTAG debugger is used or an external debug tool.

Jumper pin 1 is marked with a white square on the ITMPC5554 PCB. If pin 1 cannot be located directly from the ITMPC5554, please use Figure 2 for assistance.

Note: Don't change jumper settings while the ITMPC5554 Target Board is supplied with power!

J1	BOOTCFG0
1-2*	BOOTCFG0 = 0
2-3	BOOTCFG0 = 1
J2	BOOTCFG1
1-2*	BOOTCFG1 = 0
2-3	BOOTCFG1 = 1
J3	PLLCFG0
1-2	PLLCFG0 = 0
2-3*	PLLCFG0 = 1
J4	PLLCFG1
J4 1-2	PLLCFG1 = 0
<u> </u>	
1-2	PLLCFG1 = 0
1-2 2-3*	PLLCFG1 = 0 PLLCFG1 = 1
1-2 2-3* J5	PLLCFG1 = 0 PLLCFG1 = 1 WKPCFG
1-2 2-3* J5 1-2	PLLCFG1 = 0 PLLCFG1 = 1 WKPCFG WKPCFG = 0
1-2 2-3* J5 1-2 2-3*	PLLCFG1 = 0 PLLCFG1 = 1 WKPCFG WKPCFG = 0 WKPCFG = 1

Figure 1: Jumper configuration (* - default position)

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Status Indicators

Three LED diodes show the presence of supply voltages. LD11 (+5V), LD12 (+3.3V) and LD13 (+2.5V) must light when the power is applied to the evaluation board. LD14 and LD15 are available for the user as a status indicator.

Component List

Name	Description
U22	Motorola MPC5554 CPU
U1,U8,U9,U10	SRAM Cypress CY7C1338F
P1(bottom)	Connector for manufacturing purpose
P2	Nexus debug connector
P4	Power supply connector
ONCE	JTAG debug connector
J1	BOOTCFG0
J2	BOOTCFG1
J3	PLLCFG0
J4	PLLCFG1
J5	WKPCFG
J6	Debug mode
J28	USB connector (integrated debugger)
LD11	Power LED 5V
LD12	Power LED 3,3V
LD13	Power LED 2,5V
LD14	User LED
LD15	User LED
SW1	Power switch

Connectors

14-pin JTAG debug connector (ONCE)

CPU_TDI	1	2	GND
CPU_TDO	3	4	GND
CPU_TCK	5	6	GND
N.C.	7	8	N.C.
CPU_RESET	9	10	CPU_TMS
3V3	11	12	N.C.
N.C.	13	14	CPU_TRST

External JTAG debug tool connects to a 14-pin JTAG debug connector. **Jumper J6 must be open when using external debugger.**

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Nexus 38-pin Mictor debug connector

Signal	Pin	Pin	Signal
Not used	1	2	Not used
Not used	3	4	Not used
MDO9	5	6	CLKOUT
BOOTCFG	7	8	MDO8
RSTIN	9	10	EVTIN
TDO	11	12	VTREF
MDO10	13	14	RDY
TCK	15	16	MDO7
TMS	17	18	MDO6
TDI	19	20	MDO5
NTRST	21	22	MDO4
MDO11	23	24	MDO3
Not used	25	26	MDO2
Not used	27	28	MDO1
Not used	29	30	MDO0
Not used	31	32	EVTO
Not used	33	34	MCKO
Not used	35	36	MSEO1
Not used	37	38	MSEO0

External Nexus debug tool connects to a Nexus 38-pin Mictor debug connector. **Jumper J6 must be open when using external debugger**.

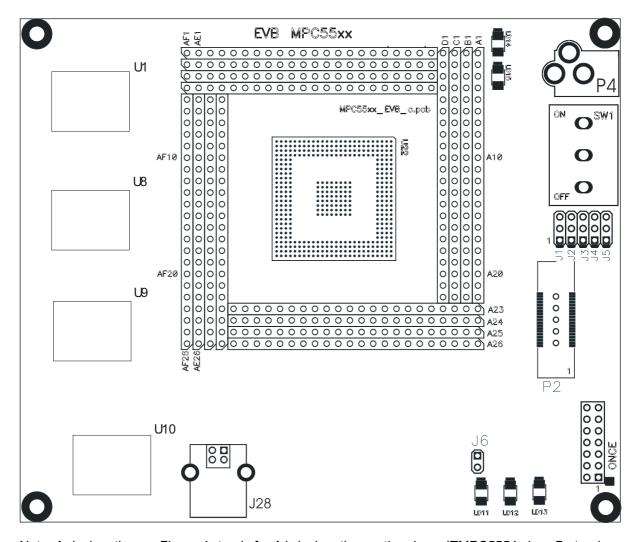
CPU expansion connector

The CPU expansion connector makes all the CPU signals accessible and can be used in order to expand the development system by connecting the ITMPC5554 to another module. The CPU expansion connector uses the same numbering scheme as the original CPU in the PBGA416 package. The CPU expansion connector builds the matrix that matches with the CPU PBGA416 pinout.

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Appendix A

View of the ITMPC5554



Note: A designation on Figure 4 stands for A1 designation on the above ITMPC5554 view, B stands for B1, AF stands for AF1 etc.

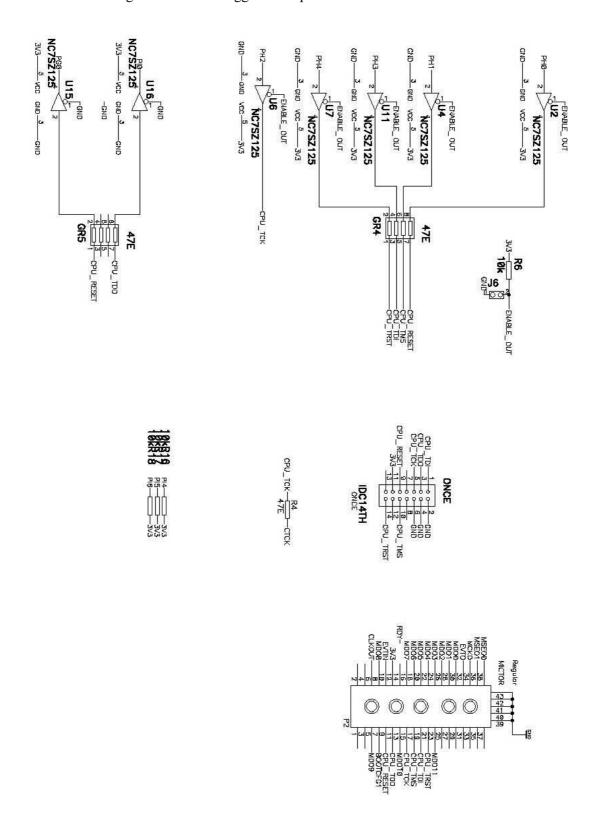
	Ą	В	o	Д	ш	14	G	н	-	м	ы	M	z	Д	×	H	Þ	>	W	X	ΑA	AB	AC	AD	AE	ΑF	
26	V _{SS}	V _{DDE7}	VDD	IDI	TEST	EVTO	ETPUB15	ETPUB13	ETPUB9	ETPUBS	ETPUB2	SINB	PCSB1	PCSB2	SCKA	Vpp	VFLASH	RSTCFG	RESET	VSSSYN	EXTAL	XTAL	VDDSYN	V_{DD33}	VDD	V _{SS}	56
25	VDD33	V _{SS}	V _{DDE7}	TCK	OCLI	EVII	GPIO204	ETPUB14	ETPUB11	ETPUB7	ETPUB3	ETPUB0	PCSB0	SCKB	SINA	PCSA2	PCSA5	RSTOUT	TXDB	VRCVSS	BOOTCFG0	PLLCFG0	VRC33	V _{DD}	Vss	ENGCLK	25
24	$v_{\rm DD}$	MDO0	V _{SS}	V _{DDE7}	TIMS	JCOMP	MCKO	GPIO203	ETPUB12	ETPUBS	ETPUB4	ETPUB1	PCSB3	PCSB4	SOUTA	PCSA0	TXDA	RXDA	CNRXC	BOOTCFG1	PLLCFG1	VRCCIL	VDD	V _{SS}	CLKOUT	VDDE5	24
23	MD08	MD04	MD01	Vss	VDDE7	MSE00	MSEOI	RDY	V _{DDЕН6}	ETPUB10	ETPUB6	TCRCLK	SOUTB	PCSA3	PCSB5	PCSA1	PCSA4	CNTXC	RXDB	WKCFG	V _{DDЕН6}	VDD	V _{SS}	NC	VDDE5	CNRXB	23
22	MD011	MD07	MD03	VDDEH8			-						-										NC	VDDES	CNRXA	CNTXB	22
21	GPIO 205	MDO10	MD06	MD02	-																		VDDE5	CNTXA	EMIOS23	EMIOS20	21
20	ETPUB27	ETPUB31	MD09	MD05																			V _{DDEH4}	EMIOS22	EMIOS19	EMIOS18	20
19	ETPUB24	ETPUB28	ETPUB30	ETPUB29																			EMIOS21	EMIOS17	EMIOS16	EMIOS14	19
18	ETPUB20	ETPUB25	ETPUB26	ETPUB23																			EMIOS12	EMIOS15	EMIOS13	EMIOS11	18
17	ETPUB18	ETPUB21	ETPUB22	ETPUB17																			EMIOS8	EMIOS10	EMIOS9	EMIOS7	17
16	ETRG1	ETRIG0	ETPUB19	ETPUB16																			EMIOS2	EMIOS6	EMIOSS	EMIOS4	16
15	AN15	AN14	AN13	AN12																			DATA14	EMIOS3	EMIOS1	EMIOS0	15
4	VSS	Vss	V _{DDEH9}	VDDEH9																			DATA12	DATA15	BG	BB	41
13	AN35	AN32	AN33	AN34																			VDDE2	DATA13	BR	DATA7	13
12	AN28	AN31	AN30	AN29																			DATA10	DATA11	OE	DATAS	12
=	AN27	AN26	AN25	AN24																			DATA8	DATA9	DATA6	VDDE2	=
10	AN23	AN22	VRL	AN6																			DATA31	GPIO 207	DATA4	DATA3	10
6	VRH	BLASR	AN7	AN2			6																DATA30	V _{DD33}	DATA2	DATA1	6
œ	ANS	AN4	AN3	AN18		-	(As viewed nom me top of me package)																VDDE2	DATA29	DATA0	GPIO 206	60
7	ANI	0NV	AN21	AN10			om me top o																DATA28	DATA27	DATA23	DATA22	7
9	AN16	AN20	VSSA	AN9			4s viewed in																DATA26	DATA25	DATA21	DATA20	9
5	V_{DDA}	9INA	AN17	AN38			<i>-</i>																VDD	DATA24	DATA19	VDDE2	5
4	AN11	4N39	AN8	V _{SS}	ααΛ	VDDEHI	ETPUA21	ETPUA17	ETPUA13	ETPUA9	ETPUAS	ETPUA1	TCRCLK	CSO	WE0	VDDE2	V _{DD33}	ADDR8	ADDR10	VDDE2	ADDR12	ADDR14	V _{SS}	V _{DD}	DATA17	DATA18	4
8	AN37	AN36	V _{SS}	VDD	VDDEH	ETPUA26	ETPUA25	ETPUA18	ETPUA14	ETPUA10	ETPUA6	ETPUA2	ETPUA0	<u>cs1</u>	WE1	RD_WR	TA	TIS	ADDR9	ADDR11	ADDR13	ADDR15	ADDR31	V _{SS}	VDD	DATA16	8
23	VSTBY	V _{SS}	V _{DD}	ETPUA31	ETPUA29	ETPUA27	ETPUA22	ETPUA19	ETPUA15	ETPUA11	ETPUA7	ETPUA3	TEA	CSS	WE2	TSIZ0	TSIZ1	ADDR17	ADDR19	ADDR21	ADDR23	ADDR25	ADDR27	ADDR30	Vss	VDD	7
1	V _{SS}	α_{Λ}	VDD33	ETPUA30	ETPUA28	ETPUA24	ETPUA23	ETPUA20	ETPUA16	ETPUA12	ETPUA8	ETPUA4	BDIP	<u>cs3</u>	WE3	VDDE2	ADDR16	ADDR18	ADDR20	ADDR22	ADDR24	VDDE2	ADDR26	ADDR28	ADDR29	V _{SS}	
	A	М	υ	Д	щ	į.	ტ	н	-	⊭ 7•	ı	×	z	e.	~	H	Þ	>	W	¥	ΑA	AB	AC	ΑD	AE	ΑĒ	

Figure 4: Expansion connector

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Schematic

Note: On-board integrated JTAG debugger is not part of the schematic.



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