Date: Aug 19, 2014

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-MC*-A026A/E	Rev.	1.00
Title	Point for Caution on Usage of Synchronous Serial Communication Unit (SSU)		Information Category	Technical Notification		
Applicable Product	H8S/2113 Group H8S/2426, H8S/2426R, H8S/2424 Group H8S/2427, H8S/2427R, H8S/2425 Group H8S/2456, H8S/2456R, H8S/2454 Group H8S/2472, H8S/2463, H8S/2462 Group H8S/2604 Group H8S/2628 Group H8SX/1544 Group H8SX/1520R Group H8SX/1520 Group H8SX/1582	Lot No. All lots	Reference Document	H8S/2113 Group User's Manual: Hardware (R01UH0179EJ0200) H8S/2426, H8S/2426R, H8S/2424 Group User's Manual: Hardware (R01UH0310EJ0500) H8S/2427, H8S/2427R, H8S/2425 Group User's Manual: Hardware (R01UH0311EJ0300) H8S/2456, H8S/2456R, H8S/2454 Group User's Manual: Hardware (R01UH0309EJ0500) H8S/2472 H8S/2463 H8S/2462 Group Hardware Manual (REJ09B0403-0200) H8S/2604 Group Hardware Manual (REJ09B0426-0100) H8S/2628 Group Hardware Manual (REJ09B0155-0400) H8SX/1544 Group Hardware Manual (REJ09B0381-0300) H8SX/1520R Group Hardware Manual (REJ09B0282-0100) H8SX/1520 Group Hardware Manual (REJ09B0104-0300) H8SX/1582 Hardware Manual (REJ09B0199-200)		

When using the synchronous serial communication unit (SSU) in the above applicable products, caution is required on the following point.

1. Point for Caution

(1) Access to SSTDR and SSRDR Registers

Do not access SSTDR and SSRDR registers not validated by the setting of the DATS bits of the SSCRL register. If accessed, transmission or reception thereafter may not be performed normally.

(2) Continuous Transmission/Reception in SSU Slave Mode

During continuous transmission/reception in SSU slave mode, negate the $\overline{\text{SCS}}$ pin (high level) for every frame. If the $\overline{\text{SCS}}$ pin is kept asserted (low level) for more than one frame, transmission or reception cannot be performed correctly.

(3) Note for Reception Operations in SSU Slave Mode

In continuous reception when slave reception in SSU mode has been selected, read the SS receive data register (SSRDR) before each next round of reception starts (i.e. before an externally connected master device starts a next round of transmission).

If the next round of reception starts after the receive data register full (RDRF) bit in the SS status register (SSSR) has been set to 1 but before SSRDR has been read, and SSRDR is read before the reception of one frame is complete, the conflict/incomplete error (CE) bit in SSSR will be set to 1 on completion of reception.

Furthermore, when the next round of reception starts after the RDRF bit has been set to 1 but before SSRDR has been read,

and SSRDR has not been read by the end of the reception of the frame, the CE and overrun error (ORER) bits will not have been set and the received data will be discarded.

Further note that this point for caution does not apply to simultaneous transmission and reception in SSU slave mode or to clock-synchronous mode.

(4) Note on Master Transmission and Master Transmission/Reception Operations in SSU Mode

To perform master transmission or transmission/reception in SSU mode, perform one of the following operations:

- After the TDRE flag in SSSR is set to 1, store the next byte of transmit data in SSTDR before transmission of the second to last bit starts.
- Store the next byte of transmit data in SSTDR after confirming that the TEND flag in SSSR has been set to 1.
- Use the SSU with the TENDSTS bit in SSCR2 cleared to 0, or with both the TENDSTS and SCSATS bits in SSCR2 set to 1.