PLC-655

C&T65555

Flat Panel Control Board

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Introduction

Welcome to the PLC-655 Series. The PLC-655 is a PCI bus flat panel graphic acceleration card. This card uses C&T 65555 LCD/CRT Controller Chips to support high resolution LCD/CRT display panel. It is made for the SBCs that are not equipped with LCD/CRT interface from the factory and is the best solution for internal flat panel connection.

PLC-655 is a 50-pin LCD connector (TTL Signal) with FP24-01 Connection Module for extra 44-pin and 41-pin connectors. This model is for internal flat panel connection application, for example: for connection with LCD-Kit01, WS-842CD, MPC-6020..etc.

PLC-655L1 is a One-Channel LVDS flat panel control board which supports 18/24-bit LCD panel display. It is equipped with on-board 50-pin LCD connector (TTL signal) and 44-pin D-sub connector on the iron plate for one channel LVDS signal.

PLC-655L2 is a Two-Channel LVDS flat panel control board with on-board 50-pin LCD connector (TTL signal) and 44-pin D-sub connector on the iron plate for two channel LVDS signal. It supports 36-bit LCD panel display.

1.1 Specifications :

Bus : PCI bus

LCD/CRT Interface : C&T 65555 Chipset with 2MB Video DRAM

CRT Resolution : 1280 x 1024, 256 colors
1024 x 768, 64K colors
800 x 600, 16M colors

36-bit LCD Interface Resolution:
1280 x 1024, 256 colors
1024 x 768, 64K colors
800 x 600, 16M colors

Output Connector :

LCD : 44-pin D-sub female LVDS Interface connector (CN1)
2x25 pin header LCD Interface connector (CN4)

CRT : 15-pin D-sub female connector (CN2)
2x5 box header/2.54mm connector

Output Voltage : 3.3 V or 5 V (selectable from JP5)

LCD Type : TFT or DSTN (selectable from JP2)
Support 24-bit and 36-bit data signals

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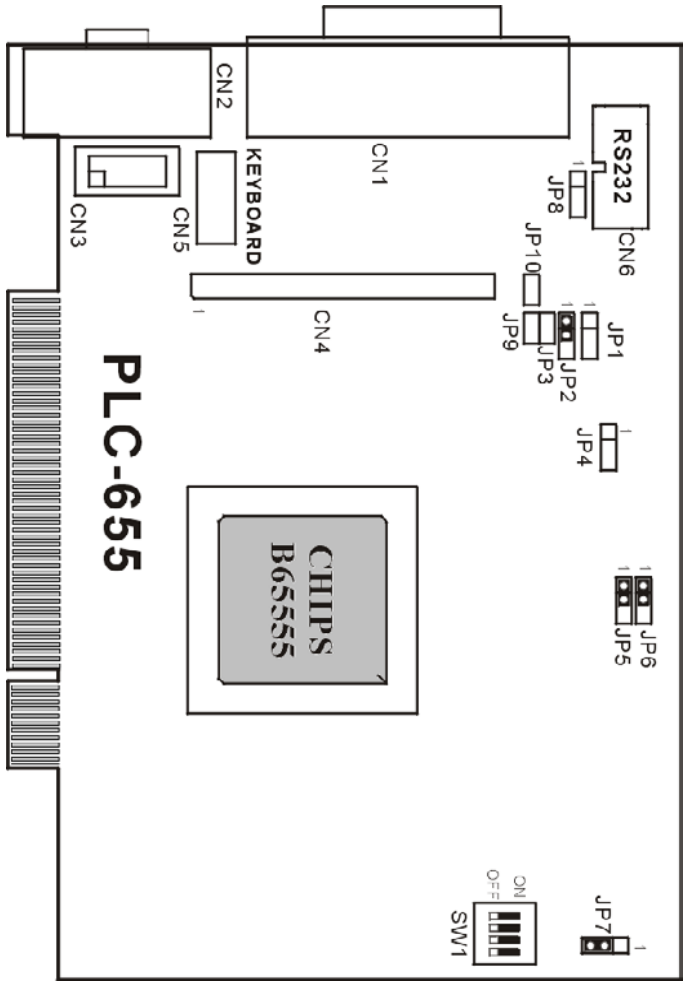
Installation

This chapter describes how to install the PLC-655. The layout of PLC-655 is shown on the next page and the Unpacking Precautions that you should be careful with are described on the following page. Also included is the jumpers and connectors description for this PLC-655.

2.1 PLC-655's Layout

(please, refer to the next page)

2.2 PLC-655's Layout



2.2 Unpacking Precautions

- ✓ Some components on PLC-655 are very sensitive to static electric charges and can be damaged by a sudden rush of power. Ground yourself to remove any static charge before touching your PLC-655 . You can do it by using a grounded wrist strap at all times or by frequently touching any conducting materials that is connected to the ground.
- ✓ Disconnect power supply before handling and doing connection on PLC-655. Do not plug any connector or jumper while the power is on. It will cause fatal damage to your LCD panel.
- ✓ Make sure that every connector is connected in correct direction. Any incorrect connection may cause smoke or burn of electrical parts or fatal damage of your LCD panel.

2.3 JUMPER SETTING

• JP1: FPVDD or FPVEE Selector

This jumper decides which signal is used to generate the panel bias voltage VEE. The default setting is **FPVEE**.

PIN NO.	DESCRIPTION
1-2	USE FPVDD
2-3	USE FPVEE

• JP2 and JP3: TFT or DSTN Selector

Panel Type	JP2	JP3
TFT	**1-2**	**OFF**
DSTN	2-3	ON

• **JP4: Output +12V and +5V Power Supply**

JP4 supplies +12V and +5V voltage for any additional device or application.

Warning: don't short any two pins of this jumper. It will cause short circuit.

PIN NO.	DESCRIPTION
1	VDD SAFE (+5V)
2	GND
3	+12V SAFE

• **JP5: LCD VOLTAGE SETTING**

PIN NO.	DESCRIPTION
1-2	**3.3 V**
2-3	5 V

• **JP7: SELECT BIOS**

The BIOS used on PLC-655 is 128K Flash ROM. It is divided into two segments, 64K each, BIOS 1 & BIOS 2. Each Segment is programmed with 8 types of LCD resolution.

PIN NO.	DESCRIPTION
1-2	BIOS 1
2-3	**BIOS 2**

• **SW1: LCD PANEL TYPE SETTING (BIOS 1)**

PIN NO.				RESOLUTION
1	2	3	4	
ON	ON	ON	ON	#1: 1024x768 DSTN Color Panel
ON	ON	ON	OFF	#2: 1280x1024 TFT Color Panel
ON	ON	OFF	ON	#3: 640x480 DSTN Mono Panel
ON	ON	OFF	OFF	#4: 800x600 DSTN Color Panel
ON	OFF	ON	ON	#5: 640x480 Sharp 16-bit TFT Color Panel
ON	OFF	ON	OFF	#6: 640 x 480 18-bit TFT Color Panel
ON	OFF	OFF	ON	#7: 1024 x 768 TFT Color Panel 36bits
ON	OFF	OFF	OFF	#8: 800 x 600 TFT Color Panel

• **SW1: LCD PANEL TYPE SETTING (BIOS 2)**

PIN NO.				RESOLUTION
1	2	3	4	
ON	ON	ON	ON	#1: 1024x768 DSTN Color Panel
ON	ON	ON	OFF	#2: 1280x1024 TFT Color Panel
ON	**ON**	**OFF**	**ON**	#3: 640x480 DSTN Color Panel
ON	ON	OFF	OFF	#4: 800x600 DSTN Color Panel
ON	OFF	ON	ON	#5: 640x480 Sharp 16-bit TFT Color Panel
ON	OFF	ON	OFF	#6: 640 x 480 18-bit TFT Color Panel
ON	OFF	OFF	ON	#7: 1024 x 768 TFT Color Panel 18bits
ON	OFF	OFF	OFF	#8: 800 x 600 TFT Color Panel

• **JP8: CN1 Pin40 Inverter ON/OFF Control**

PIN NO.	DESCRIPTION
1-2	**USE FPVEE**
2-3	USE ENABKL

2.4 PLC-655'S CONNECTOR

- **CN1: Dsub-44pin LVDS-LCD Connector**

PIN NO	FUNCTION	PIN NO	FUNCTION
1	+12V	23	TX1CLK+
2	+12V	24	TX20-
3	GND	25	TX20+
4	GND	26	TX2-
5	+5V	27	TX2+
6	+5V	28	TXC-
7	KBVCC	29	TXC+
8	GND	30	TX21-
9	SOUT	31	TX21+
10	SIN	32	DSR
11	RTS	33	CTS
12	TX0-	34	DTR
13	TX0+	35	TX22-
14	TX1-	36	TX22+
15	TX1+	37	TX2CLK-
16	TX10-	38	TX2CLK+
17	TX10+	39	GND
18	TX11-	40	JP8
19	TX11+	41	KBDAT
20	TX12-	42	KBCLK
21	TX12+	43	TX3+
22	TX1CLK-	44	TX3-

- **CN2: DSub-15pin CRT (VGA monitor) Connector**
  (connect to CRT Panel)

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	HS
5	VS	6	NC
7	NC	8	GND
9	GND	10	GND
11	NC	12	NC
13	NC	14	NC
15	NC		

- **CN3: 5X2 header CRT Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RED	6	NC
2	GREEN	7	NC
3	BLUE	8	GND
4	HS	9	GND
5	VS	10	GND

- **CN4: 25X2 header LCD Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VPCLK	2	P33
3	P34P	4	P31
5	P35	6	P32
7	P30	8	P28
9	P39	10	P27
11	P25	12	P26
13	P24	14	P21
15	P23	16	P22
17	P16	18	P20
19	P17	20	P18
21	P19	22	P14
23	P13	24	P12
25	P15	26	P11
27	P7	28	P10
29	PLCD	30	PLCD
31	P9	32	P8
33	P4	34	P6
35	P3	36	P5
37	P2	38	P1
39	M	40	P0
41	SHFCLK	42	ENABLK
43	FPVDD	44	FLM
45	FPVEE	46	LP
47	GND	48	GND
49	+12V	50	+12V

• **CN5: Keyboard Connector** (connect to CPU card)

PIN NO.	DESCRIPTION
1	KB-CLK
2	KB-DAT
3	NC
4	GND
5	+5V

• **CN6: 5X2 header RS-232 Connector** (connect to CPU card)

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	NC	6	DSR
2	SIN	7	RTS
3	SOUT	8	CTS
4	DTR	9	NC
5	GND	10	NC

Appendix A. FP24-01 Connection Module

The FP24-01 converts PLC-655's on board 50pin LCD interface signal to the 44-pin and 41pin (Hirose DF9-41P-1V) LCD connectors. The 44-pin or 41-pin connector will only support 24-bit flat panel.

• **J3 : 44-pin LCD Interface Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+12V	2	+12V
3	GND	4	GND
5	5V/3.3V	6	5V/3.3V
7	FPVEE	8	GND
9	P0	10	P1
11	P2	12	P3
13	P4	14	P5
15	P6	16	P7
17	P8	18	P9
19	P10	20	P11
21	P12	22	P13
23	P14	24	P15
25	P16	26	P17
27	P18	28	P19
29	P20	30	P21
31	P22	32	P23
33	GND	34	GND
35	SHFCLK	36	FLM
37	M	38	LP
39	GND	40	ENABKL
41	NC	42	NC
43	FPVDD	44	5V/3.3V

• **J1 : 41-pin LCD Interface Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	P20	2	GND
3	P16	4	5V or 3.3V
5	P21	6	P0
7	P17	8	P8
9	P22	10	P1
11	P18	12	P9
13	P23	14	P2
15	P19	16	P10
17	5V or 3.3V	18	P3
19	FLM	20	P11
21	M	22	P4
23	LP	24	P12
25	SHFCLK	26	P5
27	5V or 3.3V	28	P13
29	5V or 3.3V	30	P6
31	ENABKL	32	P14
33	FPVDD	34	P7
35	FPVEE	36	P15
37	GND	38	+12V
39	GND	40	+12V
41	N/C		

• **J2 : LCD Backlight Power Connector**

PIN NO.	DESCRIPTION
1	N/C
2	GND
3	+12V
4	GND
5	FPVEE Inverter Enable

Appendix B. LVDS-01 Connection Module

(One Channel LVDS Piggy Back Module)

The LVDS-01 supports the TFT LCD which equipped the 1pixel/clock for LVDS Interface.

1. CONNECTOR DESCRIPTION

• **JP2 : Hirose DF14A-20P-1.25H LVDS Connector**

PIN NO.	DESCRIPTION
1	PLCD
2	PLCD
3	GND
4	GND
5	TX0-
6	TX0+
7	GND
8	TX1-
9	TX1+
10	GND
11	TX2-
12	TX2+
13	GND
14	TXC-
15	TXC+
16	GND
17	TX3-
18	TX3+
19	GND

20	GND

Note : PLCD is a power supply from CPU board which can be set as +3V or +5V. See the CPU board's user manual for this setting.

- **J4 : LCD Backlight Inverter's Power Connector**

PIN NO.	DESCRIPTION
1	N/C
2	GND
3	12V (0.9A)
4	GND
5	FPVEE

FPVEE: power sequencing control for panel bias voltage VEE, it may be configured also as ENABKL

2. JUMPER SETTING

- **J1 :**

PIN NO.	DESCRIPTION
1	SHFCLK
2	DCLK
3	VPCLK

1-2 ON: for TFT application (default)
2-3 ON: for DSTN LCD application

- **J2 :**

PIN NO.	DESCRIPTION
1	PDATA
2	SHFCLK

OFF: for TFT application
ON: for DSTN LCD application

Appendix C. LVDS-02 Connection Module

(Two Channels LVDS Piggy Back Module)

The LVDS-02 supports the TFT LCD which equipped the 2 pixels/clock for LVDS interface.

1. CONNECTOR DESCRIPTION

- **CN1 : Hirose DF14A-20P-1.25H LVDS Connector**

PIN NO.	DESCRIPTION
1	PLCD
2	PLCD
3	GND
4	GND
5	TX10-
6	TX10+
7	TX11-
8	TX11+
9	TX12-
10	TX12+
11	TX1CLK-
12	TX1CLK+
13	TX20-
14	TX20+
15	TX21-
16	TX21+
17	TX22-
18	TX22+

19	TX2CLK-
20	TX2CLK+

Note : PLCD is a power supply from CPU board which can be set as +3V or +5V. See the CPU board's user manual for this setting.

- **J3 : LCD Backlight Inverter's Power Connector**

PIN NO.	DESCRIPTION
1	N/C
2	GND
3	12V (0.9A)
4	GND
5	FPVEE

FPVEE: power sequencing control for panel bias voltage VEE, it may be configured also as ENABKL