DATA TRANSLATION

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DT3162
User's Manual

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Radio and Television Interference

This equipment has been tested and found to comply with CISPR EN55022 Class A and EN50082-1 (CE) requirements and also with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Changes or modifications to this equipment not expressly approved by Data Translation could void your authority to operate the equipment under Part 15 of the FCC Rules.

Note: This product was FCC-Certified under test conditions that included use of shielded cables and connectors between system components. It is important that you use shielded cables and connectors to reduce the possibility of causing interference to radio, television, and other electronic devices.

Canadian Department of Communications Statement

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class A prescrites dans le Règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.

Table of Contents

About this Manual

This manual describes the features of the DT3162 frame grabber board and provides technical reference information.

Intended Audience

This document is intended for engineers, scientists, technicians, or others responsible for programming and/or using the DT3162 board to perform machine vision and/or image analysis operations. It is assumed that you have some familiarity with imaging principles and that you are familiar with the operating characteristics of your video source.

What You Should Learn from this Manual

This manual provides detailed information about the features of the DT3162 board. It is organized as follows:

- "Principles of Operation," describes all of the supported features of the board.
- Appendix A, "Specifications," lists the specifications of the board and the Camera Interface Module.
- Appendix B, "Connector Pin Assignments," describes the pin assignments for the connectors on the DT3162 board and on the Camera Interface Module and STP15 screw terminal panel.
- Appendix C, "RS-170 and CCIR Specifications and the DT3162," describes the differences between the RS-170 and CCIR specifications and the DT3162 board.

- Appendix D, "Values for Use with the DT-Active Monochrome Frame Grabber Control," lists the supported values for the DT3162 and the DT-Active Monochrome Frame Grabber Control.
- An index complete this manual.

Conventions Used in this Manual

The following conventions are used in this manual:

- Notes provide useful information that requires special emphasis, cautions provide information to help you avoid losing data or damaging your equipment, and warnings provide information to help you avoid catastrophic damage to yourself or your equipment.
- Items that you select or type are shown in **bold**.
- `Courier font` is used to represent source code.

Related Information

Refer to the following documents for more information on using the DT3162 board:

- *DT3162 Getting Started Manual* (UM-19133). This manual (GS3162.PDF), included on the Imaging OMNI CD™, describes how to set up, install, and wire signals to the DT3162 board, how to configure the DT3162 Device Driver, how to verify the operation of the board, and how to troubleshoot issues with the DT3162 board should they occur.
- *DT-Active Frame Grabber Controls Getting Started Manual* (UM-19336). This manual (DTFG.PDF), included on the Imaging OMNI CD, describes how to install the DT-Active Frame Grabber Controls in Visual Basic and Visual C++, and describes the properties, methods, and events included in the controls.

- *GLOBAL LAB Image/2 User's Manual* (UM-17790), available from Data Translation, describes how to use GLOBAL LAB® Image/2 and GLOBAL LAB Image/2 Streamline™ to create scientific applications using object-oriented image processing tools.
- *DT Vision Foundry User's Manual* (UM-17755), available from Data Translation, describes how to use DT Vision Foundry™ to create machine vision applications using object-oriented image processing tools.

Additionally, it may be helpful to read other material in order to gain a better understanding of image processing concepts, algorithms, and their applications. Data Translation's Technical Support Department recommends the following resources for understanding image processing concepts, processing, and coding:

Baxes, Gregory A. *Digital Image Processing, Principles & Applications.* New York: John Wiley & Sons, 1994. Introduction to image processing and hardware/software basics.

Benson, K. Blair, and Donald G. Fink. *HDTV Advanced TV for the 1990's.* New York: McGraw-Hill, 1990. Details high-definition television concepts.

Castleman, K. R. *Digital Image Processing*. Englewood Cliffs, NJ: Prentice-Hall, 1987. Explains major image processing concepts and mathematical concepts involved in digital image manipulation.

Gonzalez, Rafael C., and Paul Wintz. *Digital Image Processing.* Menlo Park, CA: Addison-Wesley, 1987. Explains major image processing concepts and mathematical concepts involved in digital image manipulation, including FFT processing, filtering operations, geometric functions, histograms, and linear equalization.

Lindley, Craig. *Practical Image Processing in C.* Somerset, NJ: John Wiley & Sons, Inc., 1991. Explains basic image processing techniques using C, provides many programming examples, covers TIFF and PICT file formats, and describes how to map images into VGA memory space.

Luther, Arch C. *Digital Video in the PC Environment.* New York: McGraw-Hill, 1991. Explains Digital Video Interactive (DVI) technology.

Pratt, William K. *Digital Image Processing.* Somerset, NJ: John Wiley & Sons, Inc., 1991. Detailed text on image processing, including morphological processing, feature extraction, image segmentation, and shape analysis.

Rosenfeld, Azriel, and Avinash C. Kak. *Digital Picture Processing.* New York: Academic Press, Inc., 1990. Describes image processing techniques and concepts.

Russ, John C. *Computer-Assisted Microscopy,* The Measurement and Analysis of Images. New York: Plenum Press.

Watkinson, John. *The Art of Digital Video.* Stoneham, MA: Focal Press, 1990. Provides an in-depth description of digital video fundamentals.

Where to Get Help

Should you run into problems installing or using the DT3162 board, the Data Translation Technical Support Department is available to provide technical assistance. Refer to the *DT3162 Getting Started Manual* for more information. If you are outside the U.S. or Canada, call your local distributor, whose number is listed in your Data Translation product handbook, or contact the Data Translation web site (www.datatranslation.com).

Principles of Operation

This chapter describes the features of the DT3162 board from a functional point of view. To aid the discussions in this chapter, refer to the block diagram of the DT3162, shown in Figure 1.

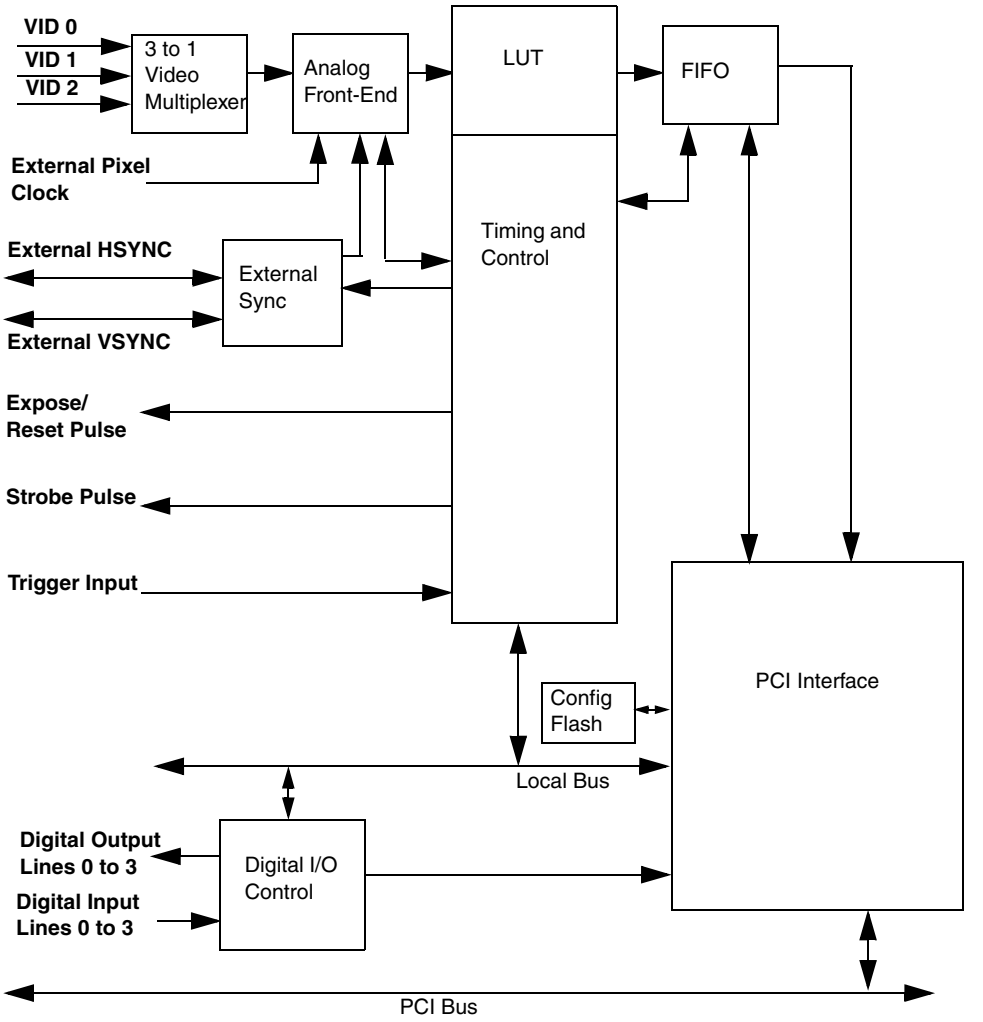

Figure 1: DT3162 Block Diagram

Video Input Signals

This section describes the following aspects of the supported input signals:

- Video signal types,
- Video input sources,
- Brightness and contrast settings,
- Pixel clock,
- Triggers, and
- Look-up tables (LUTs).

Video Signal Types

The DT3162 can acquire monochrome images from following types of standard, monochrome, composite video input signals:

- RS-170/RS-343 –Standard for 60 Hz monochrome video signals. A video frame consists of 525 lines, 480 lines of which are visible.
- CCIR –Standard for 50 Hz monochrome video signals. A video frame consists of 625 lines, 575 lines of which are visible.

Note: Refer to Appendix C for more information on the differences between the RS-170 and CCIR specifications and the values defined by the DT3162 board.

In addition, the DT3162 can acquire monochrome images from nonstandard sources, such as variable-scan, slow-scan, asynchronous/reset, and high-resolution cameras. These nonstandard video sources must provide their own control signals.

Video Input Sources

The DT3162 accepts one of three AC-coupled monochrome video input sources. You specify the video source (VideoSource0, VideoSource1, or VideoSource2) through software.

Pin C1 of connector J1 on the DT3162 is provided for video source 0. Pin C2 of connector J1 on the DT3162 is provided for video source 1. Pin C3 of connector J1 on the DT3162 is provided for video source 2. You can access these signals using either the EP332 cable or the Camera Interface Module.

Brightness and Contrast

The DT3162 provides programmable brightness and contrast settings. Brightness allows you to move the entire grayscale range of the image up or down to make the image lighter or darker. Contrast affects the amplitude of the input signal and allows you to emphasize or de-emphasize the difference between light and dark values.

Values for brightness range from 0 to 255, in increments of 1. Values for contrast range from 0 to 99, in increments of 1.

You can use software to automatically adjust the image settings for the board's current environment by selecting recalibration. Recalibration is useful if the board has experienced temperature changes or the degradation of components over time, or if you want to calibrate the image settings of all DT3162 boards used in the same environment.

If you wish, you can also use software to restore the image settings to their factory-default calibration values.

Pixel Clock

The DT3162 provides an internal pixel clock or can accept an external pixel clock. You select the pixel clock source using software.

The pixel clock locks and synchronizes to the horizontal sync input signal. Synchronization occurs on the falling edge of the horizontal sync signal. Once locked and synchronized, the pixel clock generates the acquisition timing for the board.

The following sections describe the pixel clock sources in more detail.

Internal Pixel Clock

If you select the board's internal pixel clock, the total pixels per line (which includes the active and blank pixels) multiplied by the horizontal frequency determines the frequency of the pixel clock. The frequency of the internal pixel clock determines the video input signal digitization rate.

External Pixel Clock

Connector J1 on the DT3162 board accepts two types of external pixel clock sources:

- **Single-ended (TTL) Pixel Clock Input Source** –This clock source is accessible on pin C4 of connector J1 on the DT3162. You can access this signal using the EP332 cable.

  Specify ExternalSource1 in software to select this pixel clock source.

- **Differential (LVDS) Pixel Clock Input Source** –This clock source is accessible on pin 9 (Pixel Clock –) and pin 10 (Pixel Clock +) of connector J1 on the DT3162. The Camera Interface Module allows you to attach a TTL-level pixel clock signal through the CAMERA connector, which is then converted to a differential LVDS pixel clock input that the DT3162 board uses.

However, if you need to provide a differential pixel clock directly to the board, you need to build you own cable.

Specify ExternalSource2 in software to select this pixel clock source.

The frequency of the external pixel clock can range between 100 kHz and 40 MHz, determined by the signal that you attach. This signal is rising-edge sensitive.

Triggers

The DT3162 board supports both a software trigger and an external trigger input. The external trigger input is provided through pin 6 of connector J1 on the DT3162. You can access this signal using either EP332 cable or the Camera Interface Module.

If you specify an internal trigger (Internal) using software, the acquisition occurs when you execute an acquisition command.

If you specify an external trigger using software, the acquisition is synchronized with an external event. Through software, you can specify whether you want to acquire an image when a low-to-high (OnLowToHigh) transition occurs or when a high-to-low (OnHighToLow) transition occurs. You can also specify whether to use a single external trigger (ExternalToStart) to start the acquisition of a series of frames or fields, or whether to use a separate trigger (ExternalForEach) to acquire each frame or field in a series of frames or fields. Refer to page 13 for more information on frames and fields.

Note: If you plan to use the expose/reset and/or strobe output signals, you must specify either an Internal trigger (for use when acquiring one frame only) or an ExternalForEach trigger (for use when acquiring one or more frames).

Look-Up Tables (LUTs)

The DT3162 board provides two LUTs that you can use to change the value of an incoming pixel or affect the displayed image (also called palette matching). When the LUT gets an input pixel value, the DT3162 board retrieves the output value for that particular pixel from the LUT and passes the output value to the region of interest (see page 22 for more information). Since the board has a 10-bit ADC, each LUT has 1024 locations. However, since the board processes the 10-bit data into 8-bit data, you can enter only pixel values of 0 to 255 in each location.

You specify the relationship between the pixel input value and the LUT output value by loading the LUT with different processing setups. For example, you can pass an image unaltered (the default setting for LUT 0, known as identity), or you can perform pixel point operations, such as image multiplication and division, intensity correction, and reverse-video (the default setting for LUT 1), before passing the image on.

As an example, assume that the LUT is loaded with the identity pattern. Pixel input values 0 to 3 have an output value of 0 (black). Pixel input values 4 to 7 have an output value of 1, and so on, up to pixel input values 1020 to 1023, which have an output value of 255 (white).

As another example, if you load the LUT with an inverse or negative pattern, pixel input values 0 to 3 have an output value of 255, pixel input values 4 to 7 have an output value of 254, and so on, up to pixel input values 1020 to 1023, which have an output value of 0.

As a final example, assume that you are only interested in looking at pixels whose input values to the LUT range from 600 to 855. You could load an output value of 0 for pixel input value 600, an output value of 1 for pixel input value 601, and so on, up to 255 for pixel input value 855. The rest of the LUT locations could then be loaded with either 0 (black) or 255 (white).

Using software, you can select the LUT to use, and load an ASCII file or array that specifies the relationship between the pixel input values and the output values for the selected LUT.

Sync Signals

This section describes the following aspects of the sync signals:

- Sync input sources, and
- Sync output mode.

Sync Input Sources

To digitize the incoming video signal, the DT3162 board requires both a horizontal and a vertical sync input signal.

The way in which the board determines the sync information depends on whether composite or variable-scan video signals are connected to the board. Refer to the following subsections for more information.

Composite Video Signal

If you use a composite video source, the sync signals are stripped from the selected video source and fed into the sync circuitry. Specify the sync input source as InternalSync using software.

Note: You set the horizontal sync input frequency by specifying the line frequency, described on page 17. The vertical sync input frequency is the line frequency divided by the number of lines per frame.

If you enable sync output mode, specify the sync input source as internal, since the syncs coming back to the board are stripped from the video source.

Variable-Scan Video Signals

If you want to use variable-scan video signals, the camera or imaging/device must provide the horizontal and vertical sync signals. Pin 1 of connector J1 on the DT3162 accepts a vertical sync signal; pin 2 of connector J1 on the DT3162 accepts a horizontal sync signal. Both the EP332 cable and the CAMERA connector on the Camera Interface Module accept horizontal and vertical sync input signals.

Note: Pins 1 and 2 of connector J1 on the DT3162 accept sync input signals only if sync output mode, described in the following section, is disabled.

If you are using a variable-scan video signal, specify the sync input source as ExternalSync using software. You can also specify the polarity of the horizontal and vertical sync signals (ActiveHigh or ActiveLow). Selecting an active-high polarity means that the sync input pulse is a low-to-high going signal; selecting an active-low polarity means that the sync input pulse is a high-to-low going signal.

Sync Output Mode

Typically, the camera generates the sync signals (composite or variable-scan) for the DT3162 board, and the board locks to them.

If this is not appropriate for your application or you are using a progressive scan camera, you can enable sync output mode. If sync output mode is enabled, the DT3162 board generates the sync output signals to drive the camera or video device. The video signal from the camera or video device is then digitized as usual, using the syncs generated by the board as the sync basis.

You can enable or disable sync output mode through software. When sync output mode is enabled, the vertical sync signal is output on pin 1 of connector J1 on the DT3162 board; the horizontal sync signal is output on pin 2 of connector J1 on the DT3162 board. The sync signals are normally output when sync output mode is enabled; however, if expose/reset is enabled, the vertical sync does not occur until the acquisition operation is started.

Note: Pins 1 and 2 of connector J1 on the DT3162 provide sync output signals only if sync output mode is enabled. If sync output mode is disabled, these pins are used for sync inputs.

When sync output mode is enabled, specify the sync input source as internal (composite) and the acquire type as progressive.

Using software, you can also specify the following settings if sync output mode is enabled:

- **The horizontal sync pulse width** –Values range from 1 to 4095 pixels, in increments of 1. Setting this value determines the time that the horizontal sync output pulse is in its active state (determined by the sync polarity).

- **The vertical sync pulse width** –Values range from 1 to 4095 lines, in increments of 1. Setting this value determines the the number of lines that the vertical sync output pulse is in its active state (determined by the sync polarity).
- **The sync output polarity** –Values are ActiveHigh or ActiveLow. Selecting an active-high polarity means that the sync output pulses are low-to-high going signals; selecting an active-low polarity means that the sync output pulses are high-to-low going signals.

Note: You set the horizontal sync output frequency by specifying the line frequency, described on page 17. The vertical sync output frequency is the line frequency divided by the number of lines per frame.

Image Acquisition

This section describes the following topics related to image acquisition:

- Fields and frames,
- Acquisition modes,
- Data transfer and storage, and
- Overlays.

Fields and Frames

You can use software to specify whether to acquire fields or frames of video information. A field is defined as the number of lines between two consecutive vertical sync signals. It can be an even field, consisting of lines 0, 2, 4, and so on, or an odd field, consisting of lines 1, 3, 5, and so on. A frame can be either interlaced or progressive (noninterlaced), defined as follows:

- **Interlaced frame** –Consists of two consecutive fields, each containing the number of lines per field in the active video area (see page 18 for more information). An even and an odd field are acquired to create the complete frame.
- **Progressive (noninterlaced) frame** –Consists of a single field, containing the number of lines in the progressive frame of the active video area.

Through software, you can specify which of the following fields/frames to acquire:

- Even fields only,
- Odd fields only,
- Interlaced frames, or
- Progressive frames.

Note: If you select Interlaced, the field that you start on is determined by the values for first active line (see page 22) and ROI top (see page 23).

Acquisition Modes

Using software, you can specify one of three ways to acquire the specified fields or frames:

- **Single-pass synchronous mode** –The DT3162 board acquires a specified number of frames or fields, saves the corresponding region on interest (ROI) in each frame/field to buffers in memory, then stops. Refer to page 22 for more information on ROIs.

  In single-pass synchronous mode, all system resources are devoted to the acquisition until the specified number of ROIs have been saved; you cannot perform another operation until the synchronous acquisition completes, including stopping the operation.

  For example, assume that you specified the acquire type as interlaced, the acquisition mode as single-pass synchronous mode, and the number of buffers as 3. When the acquisition operation is started, the software allocates three buffers, acquires the first frame and saves its ROI in buffer 1, acquires the second frame and saves its ROI in buffer 2, acquires the third frame and saves its ROI in buffer 3, then stops the operation. You can then manipulate the data in the buffers as needed.

  Specify SinglePassSync in software to use this mode.

- **Single-pass asynchronous mode** –Like single-pass synchronous mode, the DT3162 board acquires a specified number of frames or fields, saves the corresponding region on interest (ROI) in each frame/field to buffers in memory, then stops.

Unlike single-pass synchronous mode, however, this asynchronous operation starts and then returns control to you immediately, allowing you to perform other operations while data is acquired. Therefore, you can stop the operation before all the ROIs have been acquired, if you wish, using software.

Specify SinglePassAsync in software to use this mode.

- **Continuous asynchronous mode** –The DT3162 board continuously acquires an unlimited number of fields or frames and saves the corresponding ROIs to buffers in memory until you stop the acquisition. You are responsible for managing the data in the buffers so that it is retrieved before the buffer is overwritten.

  Continuous mode is an asynchronous acquisition, where the operation starts and then returns control to you immediately, allowing you to perform other operations while data is acquired.

  For example, assume that you specified the acquire type as interlaced, the acquisition mode as continuous, and the number of buffers as 3. When the acquisition operation is started, the software allocates three buffers, acquires the first frame and stores its ROI in buffer 1, acquires the second frame and stores its ROI in buffer 2, then acquires the third frame and stores its ROI in buffer 3. Then, the process repeats so that ROI 4 is stored in buffer 1 (overwriting any data previously stored there), ROI 5 is stored in buffer 2 (overwriting any data previously stored there), ROI 6 is stored in buffer 3 (overwriting any data previously stored there), and so on. The operation repeats until you stop it. You must manage the buffers so that the data in buffers 1 through 3 is read before the buffers are overwritten.

  Specify ContinuousAsync in software to use this mode.

Note: During asynchronous acquisitions, your application program is notified by Active-X events that various conditions (such as a frame completed or the acquisition completed) have occurred.

Data Transfer and Storage

The DT3162 board uses the scatter/gather memory management architecture so that memory locations do not have to be contiguous. The board operates as a PCI bus initiator/master using burst mode for data transfers to memory. Typical video transfer rates are 40 MB/s (maximum 132 MB/s). Data is stored in monochrome format, or 8-bits per pixel.

Overlays

For the DT3162 board, you can use software to add overlays, such as text or graphics, on top of another displayed image that was acquired. Overlays are useful for creating animation or to display helpful information for the user.

Video Area

The video image area is composed of pixels and lines of video. The total video area is the complete set of horizontal and vertical input lines from which you extract the active video area and the region of interest (ROI) within the active video area that you want to acquire. The total video area includes all parts of the signal, including nonvisual portions such as horizontal and vertical blanking information. (Blanking information is the data not included in the active video area; it contains sync and other information.)

Using software, you can set the line, or horizontal, frequency. For internal (composite syncs), this value determines how often the lines occur. If sync output mode is enabled, this value also determines how often the lines are output. Values range from 1 to 65535 Hz, in increments of 1.

The total video area is as wide as the total pixels per line (the entire area between two consecutive horizontal sync signals) and as tall as the total lines per frame.

You can use software to define the total video area for the DT3162 board. Table 1 lists the settings you can program.

Table 1: Total Video Area Settings

Setting	Description	Range[a]
Total Pixels per Line	The total number of pixels in a single horizontal line of video, where a horizontal line is defined as the area between two consecutive horizontal sync signals.	1 to 4095 pixels
Total Lines per Frame	The total number of lines in a single frame of video.	1 to 4095 lines

a. In increments of 1.

The following sections describe the active video area and the ROI within the active video area that you want to acquire and save.

Active Video Area

The active video area floats in the total video area. The active video area is defined as that part of the incoming signal that contains valid video data (not blanking or sync information). Therefore, the active video area consists of the visible portion of those lines containing visible pixel data.

Using software, you can define the active area for the DT3162 board. The following sections describe how to use the settings of the board to define the horizontal and vertical components of the active video area.

Horizontal Video Signal

Each line of video contains horizontal sync information, blanking information, and active video. Figure 2 shows the components of a single horizontal line of video. Pixel measurements are relative to the horizontal reference point, which is defined as the beginning of the horizontal sync.

Note that the ROI is an area that you establish within the active video area. For more information about ROIs, refer to page 22.

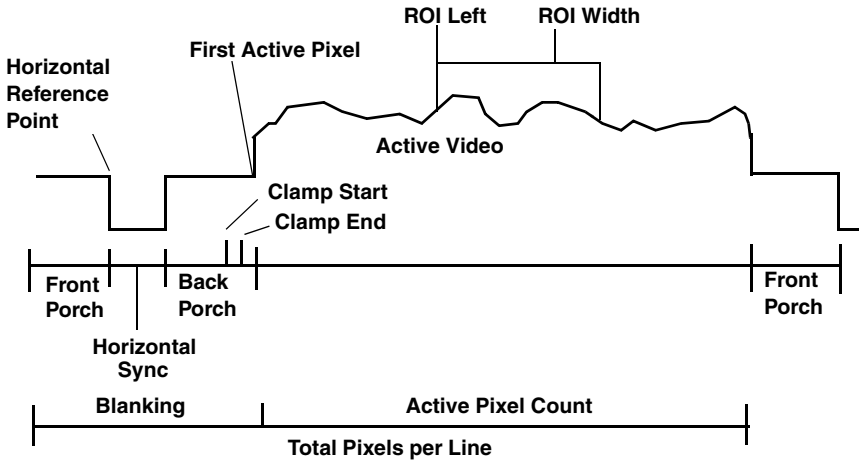

Figure 2: Horizontal Video Signal

In the horizontal video signal, blanking occurs during the horizontal sync and image border periods, which are defined by the front porch (before the horizontal sync) and back porch (after the horizontal sync).

Table 2 lists the horizontal input settings you can program on the DT3162 board.

Table 2: Horizontal Input Settings

Setting	Description	Range[a]
Clamp Start	The position at which the clamping circuit starts holding the blanking level portion of the video signal to a reference level.	16 to 4095 pixels
Clamp End	The position at which the clamping circuit stops holding the blanking level portion of the video signal to a reference level.	16 to 4095 pixels
First Active Pixel	The position of the first active video signal on the line, as a pixel value offset from the beginning of the horizontal sync.	0 to 4095 pixels
Active Pixel Count	The number of pixels per line in the active video area.	1 to 2047 pixels

a. In increments of 1.

Vertical Video Signal

Each field of video contains vertical sync information, blanking information, and lines of active video. Figure 3 shows the components of a single vertical field of video. Line measurements are relative to the vertical reference point, which is defined as the beginning of the vertical sync.

Note that the ROI is an area that you establish within the active video area. For more information about ROIs, refer to page 22.

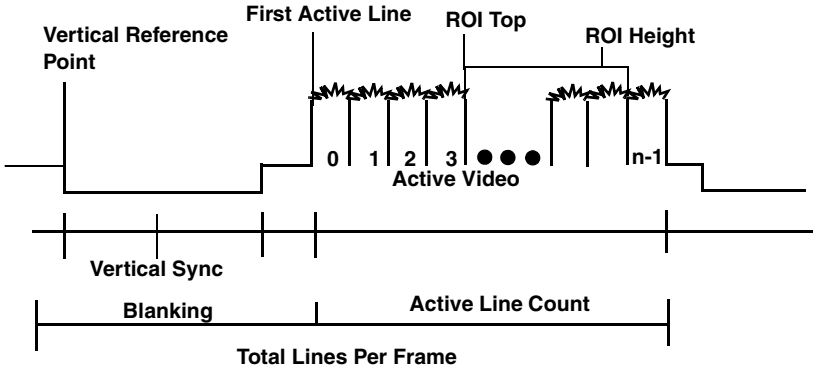

Figure 3: Vertical Video Signal

You can use software to define the vertical input settings for the DT3162. Table 3 lists the settings you can program.

Table 3: Vertical Input Settings

Setting	Description	Range[a]
First Active Line	The position of the first active video signal within the field, as a line offset from the beginning of the vertical sync.	0 to 2047 lines
Active Line Count	The number of lines per frame in the active video area.	1 to 2047 lines

a. In increments of 1.

Note: For more information on the relationship between the values listed in Table 3 and the specifications for RS-170 and CCIR, refer to Appendix C.

Region of Interest (ROI)

The ROI is the portion of the active video area that you want to acquire and save.

The top of the ROI is the first line of video relative to the active video area. The left side of the ROI is the first pixel of video relative to the active video area. The width of the ROI is the number of pixels per line of video. The height of the ROI is the number of lines per frame.

Table 4 shows the settings you can program on a DT3162 board to define the ROI.

Table 4: ROI Settings for the DT3162 Board

Setting	Description	Range
ROI Left	The first pixel in the region of interest, relative to the first active pixel, to acquire.	0 to 2039[a] pixels
ROI Width	The number of pixels per line of video to acquire.	8 to 2048[b] pixels
ROI Top	The first line of the region of interest, relative to the first active line, to acquire.	0 to 2047[a] lines
ROI Height	The number of lines per frame to acquire.	1 to 2048[a] lines

a. In increments of 1.
b. In increments of 8.

The spatial relationship between the ROI, the active video area, and the total video area is shown in Figure 4.

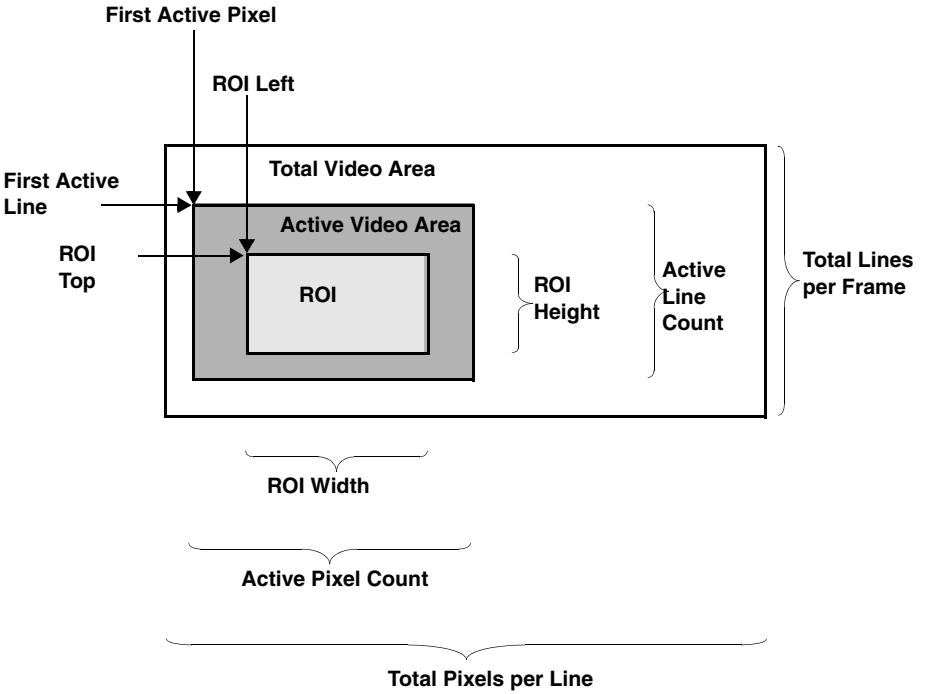

Figure 4: Spatial Relationship

Expose/Reset Signal

The DT3162 board can generate an expose/reset output signal for controlling asynchronous cameras. Asynchronous cameras are used primarily in applications that monitor moving parts. The expose/reset signal allows you to reset the asynchronous camera to the beginning of a frame, which allows you to acquire an image as the part is moving under the camera. You can access the expose/reset signal, which is provided on pin 7 of connector J1 on the DT3162 board, using the EP332 cable or the CAMERA connector on the Camera Interface Module.

Note: Sync output mode must be enabled to use the expose/reset signal.

Using software, you can enable the expose/reset pulse and specify the following settings for this signal:

- **The expose/reset start line** –Values range from 1 to 65535 lines, in increments of 1. Setting this value determines the number of lines between when the board receives the qualified acquisition trigger and when it starts outputting the expose/reset pulse.

  The qualified acquisition trigger can be an internal (software) trigger if you are acquiring one frame only, or an external trigger (ExternalForEach) if you are acquiring more than one frame. Refer to page 6 for more information on triggers.

- **The expose/reset stop line** –Values range from 2 to 65535 lines, in increments of 1. Setting this value determines the number of lines between when the board receives the qualified acquisition trigger and when it stops outputting the expose/reset pulse.

Note: The expose/reset stop line plus the vertical sync delay must be less than or equal to 65535.

The qualified acquisition trigger can be an internal (software) trigger if you are acquiring one frame only, or an external trigger (ExternalForEach) if you are acquiring more than one frame. Refer to page 6 for more information on triggers.

- **The vertical sync delay** –Values range from 1 to 65535 lines, in increments of 1. Setting this value determines the delay between the end of the expose/reset pulse and the beginning of the next vertical sync.

Note: The expose/reset stop line plus the vertical sync delay must be less than or equal to 65535.

- **The expose/reset polarity** –Values are ActiveHigh or ActiveLow. Selecting an active-high polarity means that the expose/reset output pulse is a low-to-high going signal; selecting an active-low polarity means that the expose/reset output pulse is a high-to-low going signal.

Strobe Output Signal

You can generate a strobe output pulse to control lighting for a progressive scan camera. The strobe output pulse is provided on pin 12 of connector J2 on the DT3162 board. To access this signal, use the STP15 screw terminal panel and EP337 cable.

Using software, you can enable the strobe output pulse and specify the following settings for this signal:

- **The strobe start line** –Values range from 1 to 65535 lines, in increments of 1. Setting this value determines the number of lines between when the board receives the qualified acquisition trigger and when it starts outputting the strobe pulse.

  The qualified acquisition trigger can be an internal trigger if you are acquiring one frame only, or an external trigger (ExternalForEach) if you are acquiring more than one frame. Refer to page 6 for more information on triggers.

- **The strobe stop line** –Values range from 1 to 65535 lines, in increments of 1. Setting this value determines the number of lines between when the board receives the qualified acquisition trigger and when it stops outputting the strobe pulse.

  The qualified acquisition trigger can be an internal (software) trigger if you are acquiring one frame only, or an external trigger (external for each) if you are acquiring more than one frame. Refer to page 6 for more information on triggers.

- **The strobe output polarity** –Values are ActiveHigh or ActiveLow. Selecting an active-high polarity means that the strobe output pulse is a low-to-high going signal; selecting an active-low polarity means that the strobe output pulse is a high-to-low going signal.

Digital I/O Signals

DT3162 boards provide four dedicated digital input lines and four dedicated digital output lines. Pins 1 to 4 of connector J2 on the DT3162 board are provided for the digital input signals. Pins 6, 7, 8, and 11 of connector J2 on the DT3162 board are provided for the digital outputs. To access the digital I/O signals, use the STP15 screw terminal panel and EP337 cable.

The digital I/O signals are simple register-driven, TTL-level signals that you can use for any purpose, such as controlling or actuating external devices. A bit value of 0 identifies a low TTL level; a bit value of 1 identifies a high TTL level.

The DT3162 can generate a PCI-bus interrupt when one or more of the digital input lines changes state. This feature is useful when you want to monitor critical signals or when you want to signal the host computer to transfer data to or from the board. You enable the interrupts on a line-by-line basis using software.

You can use software to read or write to the digital I/O lines and to determine which digital input lines changed state.

Specifications

The input impedance for the video input signal is 75 Ω with a 1 V signal peak-to-peak.

Table 5 lists the digital output electrical specifications for the DT3162 board.

Table 5: Digital Output Electrical Specifications

Feature	Minimum Specification	Maximum Specification
High-Level Output Current (IOH)	–	2.0 mA
Low-Level Output Current (IOL)	–	20 mA
High-Level Output Voltage (VOH)	2.4 V	–
Low-Level Output Voltage (VOL)	–	0.5 V

Table 6 lists the digital input electrical specifications for the DT3162 frame grabber board.

Table 6: Digital Input Electrical Specifications

Feature	Minimum Specification	Maximum Specification
Input High Level (V_{IH})	2.0 V	6.0 V
Input Low Level (V_{LL})	-0.3 V	0.8 V
Input Capacitance (C_{IN})	–	6 pF

Table 7 lists the power specifications for the DT3162 board.

Table 7: Power Specifications

Feature	Specification
+5 V	
Typical:	30 mA
Maximum:	45 mA
+3.3 V	
Typical:	250 mA
Maximum:	375 mA
+12 V	
Typical:	110 mA
Maximum:	165 mA
–12 V	
Typical:	40 mA
Maximum:	60 mA
Total Power	
Typical:	3 W
Maximum:	4.2 W

Table 8 lists the physical and environmental specifications for the DT3162 board.

Table 8: Physical and Environmental Specifications

Feature	Specification
Dimensions Overall including faceplate and connectors: PCB:	 10.6 cm x 19.5 cm (4.2 in x 7.7 in) 10.6 cm x 18.1 cm (4.2 in x 7.1 in)
Weight	130 g (4.6 ounces)
Operating temperature	0 to 50° C (32 to 122° F)
Storage temperature	-25 to 70° C (-13 to 158° F)
Humidity	0 to 90%, noncondensing

Table 9 lists the specifications of Camera Interface Module.

Table 9: Camera Interface Module Specifications

Feature	Specification
External Trigger Input Low level input voltage range: High level input voltage range: Minimum isolation voltage: Maximum sustained reverse bias voltage: Minimum pulse width: Maximum frequency:	 0 to 0.8 VDC 3.5 to 32 VDC 250 VAC/DC, sustained for 60 s 10 VDC 500 µs 300 Hz
Power Consumption	5 V (from the DT3162) @ 10.5 mA typical; External +12 V @ 4.7 mA typical without camera
Enclosure Dimensions	158 mm (6.22 inches) x 34.3 mm (1.35 inches) x 77.5 mm (3.05 inches)
Weight	278 g (0.613 g)
Operating Temperature	0° to 50° C (32° to 122° F)
Storage Temperature	-25° to 70° C (-13° to 158° F)
Humidity	0 to 90% noncondensing

Table 10 lists the specifications for the connectors on the DT3162 board and the Camera Interface Module.

Table 10: Connector Specifications

Connector	Specifications
DT3162 J1 Connector	Molex MicroCross™ connector (DVI-I Digital/Analog Visual Interface) part number 74320-1004
DT3162 J1 Mating Connector Plug: 2 Meter Cable:	 Molex plug part number 74323-2031 Molex DVI connector and cable part number 88741-9000
DT3162 J2 Connector	AMP 15-pin subminiature-D connector (HTEMP, R/A, REC) part number 748390-5
DT3162 J2 Mating Connector	AMP 15-pin male subminature-D connector part number 749798-1
Camera Interface Module J1 Connector	Molex MicroCross connector (DVI-I Digital/Analog Visual Interface) part number 74320-3004
Camera Interface Module J2 Connector	Hirose 12-pin connector part number HR10-10R-12SA
Camera Interface Module J3 and J4 Connectors	AMP 4-pin BNC jack connectors part number 1274291-2

Connector Pin Assignments

J1 Connector

The DT3162 has a Molex MicroCross connector, labelled J1, which accommodates the following signals: three video sources, one differential pixel clock, one TTL pixel clock, one horizontal sync, one vertical sync, one trigger input, one expose/reset signal, and a +5 V power signal. Figure 5 illustrates the pin locations of connector J1. Table 11 describes the pin assignments of this connector.

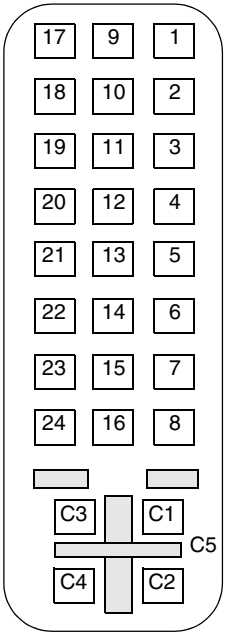

Figure 5: DT3162 - Connector J1

Table 11: DT3162 - J1 Connector Pin Assignments

Pin	Description	Pin	Description
1	Vertical Sync Input/Output	2	Horizontal Sync Input/Output
3	Digital Ground	4	Reserved
5	Reserved	6	Trigger Input
7	Expose/Reset Output	8	Reserved
9	Pixel Clock Input –[a]	10	Pixel Clock Input +[a]
11	Digital Ground	12	Reserved
13	Reserved	14	+5 V (250 mA) Output
15	Digital Ground	16	Reserved
17	Reserved	18	Reserved
19	Digital Ground	20	Reserved
21	Reserved	22	Digital Ground
23	Reserved	24	Reserved
C1	Video Input 0	C2	Video Input 1
C3	Video Input 2	C4	TTL Pixel Clock Input
C5	Analog Ground		

a. The Camera Interface Module accepts a TTL pixel clock and converts it to these differential signals for use by the DT3162. If you want to provide a differential pixel clock source, you must build your own cable to mate with this connector.

J2 Connector

The DT3162 has a 15-pin subminiature-D connector, labelled J2, which accommodates the digital I/O, strobe output, and +5 V signals. Figure 5 illustrates the pin locations of connector J2. Table 11 describes the pin assignments of this connector.

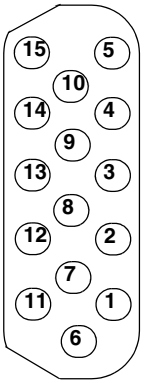

Figure 6: DT3162 - Connector J2

Table 12: DT3162 - J2 Connector Pin Assignments

Pin	Description	Pin	Description
1	Digital Input 0	2	Digital Input 1
3	Digital Input 2	4	Digital Input 3
5	Ground	6	Digital Output 0
7	Digital Output 1	8	Digital Output 2
9	Not Connected	10	Ground
11	Digital Output 3	12	Strobe Output
13	Ground	14	+5 V (250 mA) Output
15	Ground		

Camera Interface Module Connectors and Screw Terminals

The Camera Interface Modules contains one Hirose connector (CAMERA), two BNC connectors (VIDEO 1 and VIDEO 2), two screw terminal blocks (TB1 and TB2), and one Molex VCP connector (J1).

The 12-pin, female Hirose connector (CAMERA) provides access to the signals defined in Table 13. By configuring jumpers on the Camera Interface Module, you can affect which signals are accessed through pins 6 to 11 on this connector. Refer to the *DT3162 Getting Started Manual* for more information on configuring these jumpers.

WARNING!

Refer to you camera documentation before configuring pins 6 through 11 of this connector. Misconfiguration of pin 11 may cause damage to the DT3162, Camera Interface Module, and/or your camera.

Table 13: Hirose (CAMERA) Connector Pin Assignments

Pin	Description	Pin	Description
1	Digital Ground	2	+12 V[a]
3	Video 0 Return	4	Video 0
5	Digital Ground	6	HSync or Expose/ Reset[b]
7	VSync or Expose/Reset[c]	8	Digital Ground
9	HSync, Pixel Clock, or Expose/Reset[d]	10	Digital Ground[e]
11	Pixel Clock, Expose/Reset, or +12 V[a,f]	12	Digital Ground

a. This is the input from the 12 VDC terminal block.
b. To access the HSync signal on pin 6, install jumper W3 (by default, this jumper is installed); or to access the Expose/Reset signal on pin 6, install jumper W2.
c. To access the VSync signal on pin 7, install jumper W11 (by default, this jumper is installed); or to access the Expose/Reset signal on pin 7, install jumper W10.
d. To access the HSync signal on pin 9, install jumper W5; to access the Pixel Clock signal on pin 9, install jumper W6; or to access the Expose/Reset signal on pin 9, install jumper W4 (by default, this jumper is installed).
e. To access the Digital Ground signal on pin 10, install jumper W1 (by default, this jumper is installed). If jumper W1 is not installed, this pin is not connected to any signal.
f. To access the Pixel Clock signal on pin 11, install jumper W9; to access the Expose/Reset signal on pin 11, install jumper W7; or to access the+12 V signal on pin 11, install jumper W8 and connect the +12 V signal to Solder Pad 1 (SP1).

The VIDEO 1, female BNC connector provides access to the video input 1 signal. The VIDEO 2, female BNC connector provides access to the video input 2 signal.

Screw terminal block TB1 (+12 V) accepts an external +12 VDC signal and a ground signal. For most applications, a 12 VDC regulated 2.5 A camera power supply is suitable. The camera power input from the Camera Interface Module is rated for 0.75 A (maximum) at 13 VDC (maximum). The power input protection circuitry consists of a 0.75 A hold PTC resettable fuse, a 1500 W transient suppressor diode, and a 3 A Schottsky diode for reverse bias protection. The power filtering consists of a ferrite bead, 100 pf capacitor, and a 10 µf capacitor.

Screw terminal block TB2 (TRIGGER) accepts an external trigger input signal and a ground signal. The external trigger circuitry is optically coupled then inverted to maintain input polarity, and driven to the DT3162.

The VCP connector (J1) on the Camera Interface Module connects to connector J1 on the DT3162 board. The pin assignments of the VCP connector on the Camera Interface Module are listed in Table 14.

Table 14: Camera Interface Module - VCP Connector Pin Assignments

Pin	Description	Pin	Description
1	Vertical Sync Input/Output[a]	2	Horizontal Sync Input/Output[a]
3	Digital Ground	4	Not Connected
5	Not Connected	6	Trigger Output
7	Expose/Reset Input	8	Reserved
9	Pixel Clock Output −[b]	10	Pixel Clock Output+[b]
11	Digital Ground	12	Not Connected
13	Not Connected	14	+5 V (250 mA) Input
15	Digital Ground	16	Reserved
17	Reserved	18	Reserved
19	Digital Ground	20	Not Connected

Table 14: Camera Interface Module - VCP Connector Pin Assignments

Pin	Description	Pin	Description
21	Not Connected	22	Digital Ground
23	Reserved	24	Reserved
C1	Video Input 0	C2	Video Input 1
C3	Video Input 2	C4	Reserved
C5	Analog Ground		

a. Use software to specify whether these signals are inputs or outputs (sync output enabled or disabled).

b. The LDVS signals on pins 9 and 10 are generated from a single-ended TTL pixel clock from the camera that is attached to the CAMERA connector.

STP15 Connectors and Screw Terminals

The STP15 contains one 15-pin connector and two screw terminal blocks (TB1 and TB2).

The 15-pin connector provides access to the signals from connector J2 on the DT3162 board. Figure 7 shows the layout of the STP15 and the screw terminal descriptions.

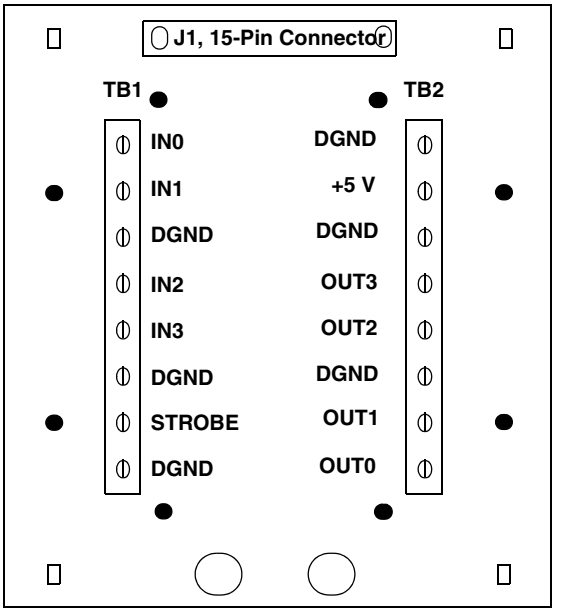

Figure 7: Layout of the STP15 Screw Terminal Panel

Notes: In Figure 7, IN refers to digital input signals, OUT refers to digital output signals, STROBE refers to strobe output signal, DGND refers to digital ground signals, and +5 V refers to a +5 V (100 mA) output signal from the DT3162 board.

The dark filled circles in Figure 7 represent holes that you can use to mount the STP15 on a DIN rail. To mount the STP15 on a DIN rail, you need two DIN rail mount adapters (Phoenix Contact part number 1201578 or Data Translation part number 18083), and four thread form screws (Bossard part number BN2724M3x8 or Data Translation part number 18193).

RS-170 and CCIR Specifications and the DT3162

RS-170 Specification

This section describes the differences between what is defined by the RS-170 specification and what the DT3162 defines for both vertical and horizontal signals.

RS-170 Vertical Signals and the DT3162

Each frame of RS-170 video contains 525 lines (262.5 lines per field), 483 total active lines, and 241.5 active lines per field. Field 2 (the even field) is dominant.

Figure 8 shows the relationship between the line numbers defined by the RS-170 specification and those defined by the DT3162 in a vertical signal, as well as the transition between fields.

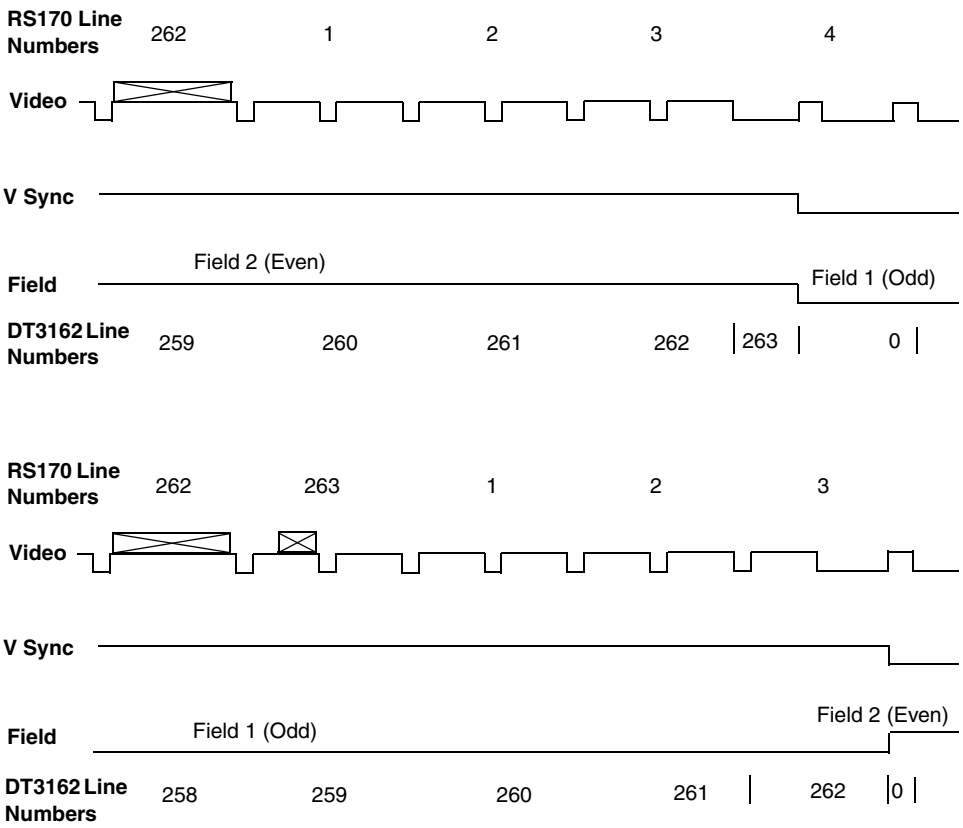

Figure 8: Line Numbers and Field Transitions for RS-170 Vertical Signals

Figure 9 shows the active lines and the numbering relationship between the RS-170 specification and the DT3162.

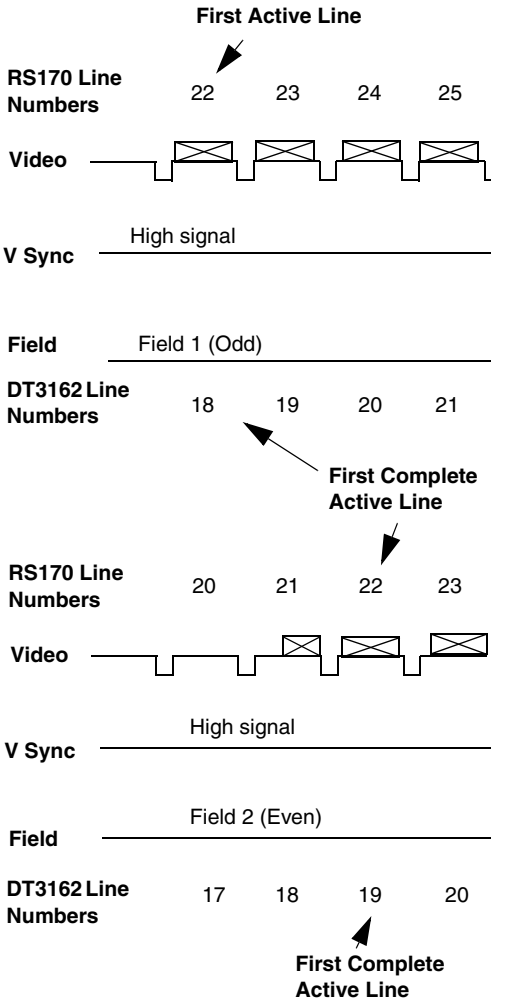

Figure 9: Active Lines for RS-170 Vertical SIgnals

RS-170 Horizontal Signals and the DT3162

As defined by the RS-170.CCF configuration file provided with the DT3162, each line of RS-170 video contains 794 total pixels and 640 active pixels. Figure 10 shows the default settings for RS-170 horizontal signals.

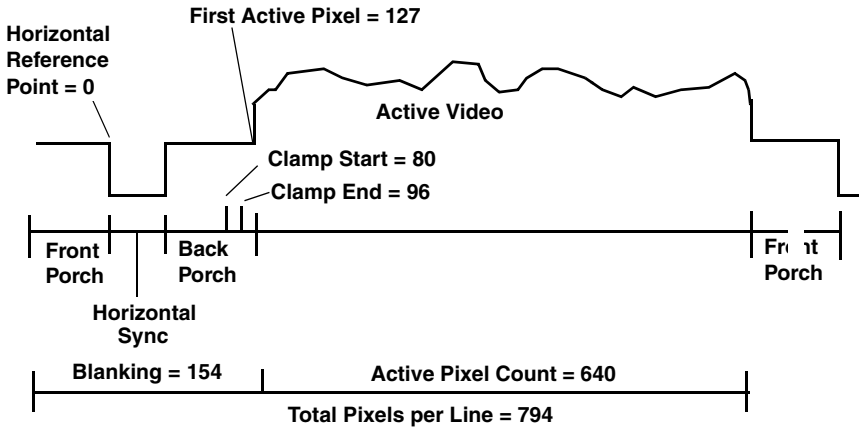

Figure 10: Default Values for RS-170 Horizontal Video Signals

CCIR Specification

This section describes the differences between what is defined by the CCIR specification and what the DT3162 defines for both vertical and horizontal signals.

CCIR Vertical Signals and the DT3162

Each frame of CCIR video contains 625 lines (312.5 lines per field), 575 total active lines, and 287.5 active lines per field. Field 1 (the odd field) is dominant.

Figure 11 shows the relationship between the line numbers defined by the CCIR specification and those defined by the DT3162 in a vertical signal, as well as the transition between fields.

Note: To maintain field 1 dominance and not acquire half lines at the top of field 1 and at the bottom of field 2, only 572 lines can be acquired. If field dominance is not an issue or you do not care about the half lines at the top and the bottom of the frame, you can configure the DT3162 to capture 576 lines. This is accomplished by changing the first active line from 47 to 45 and changing the frame height from 572 to 576.

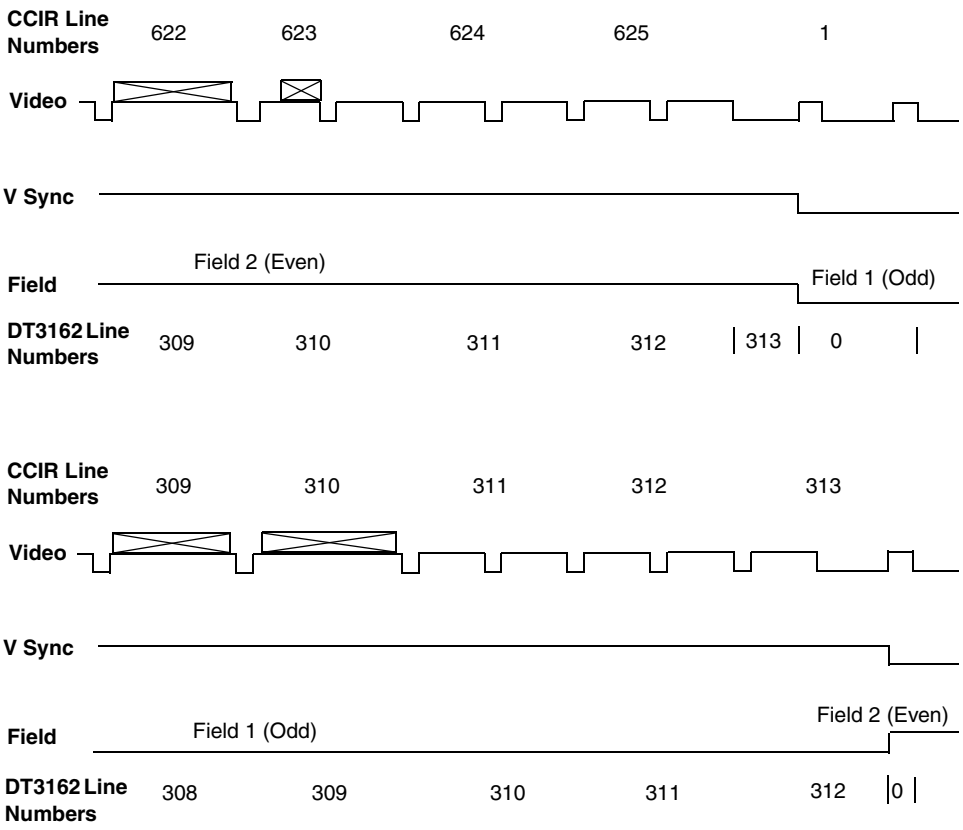

Figure 11: Line Numbers and Field Transitions for CCIR Vertical Signals

Figure 12 shows the active lines and the numbering relationship between the CCIR specification and the DT3162.

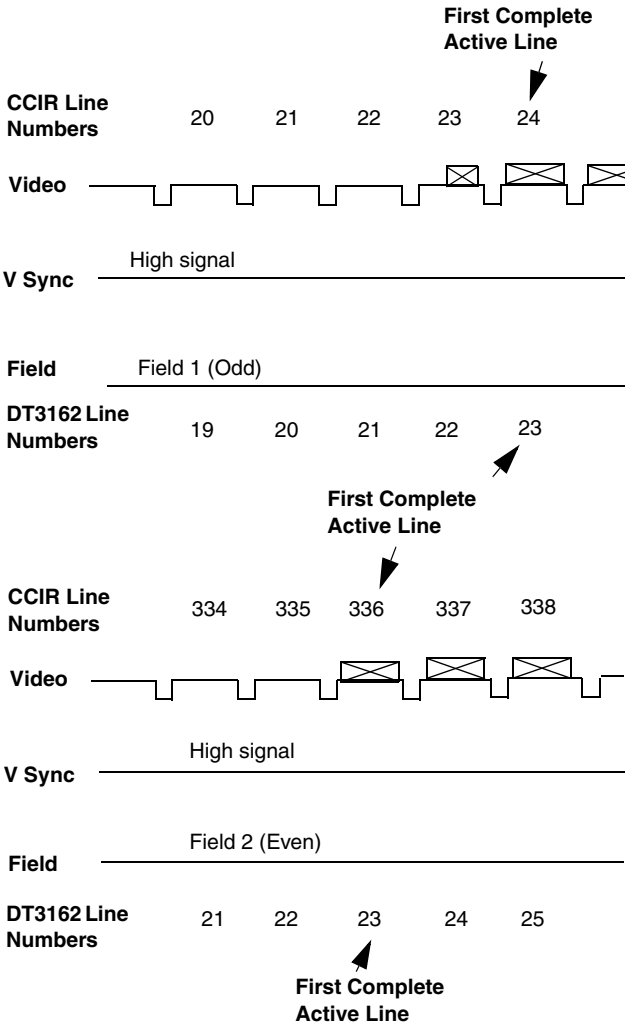

Figure 12: Active Lines for CCIR Vertical SIgnals

CCIR Horizontal Signals and the DT3162

As defined by the CCIR.CCF configuration file provided with the DT3162, each line of CCIR video contains 960 pixels and 768 active pixels. Figure 13 shows the default settings for CCIR horizontal signals.

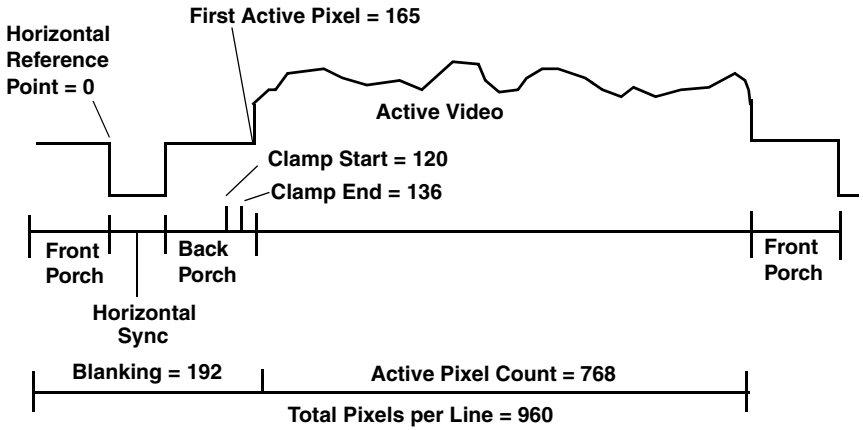

Figure 13: Default Values for CCIR Horizontal Video Signals

Values for Use with the DT-Active Monochrome Frame Grabber Control

Table 15 lists the DT3162 values for each property of the DT-Active Monochrome Frame Grabber control.

Table 15: DT3162 Values for the DT-Active Monochrome Frame Grabber Control

Category	Property	DT3162 Values
General Properties	ActiveLUT	0 or 1, in increments of 1
	Timeout	0 to 65535 ms, in increments of 1 ms
Strobe Properties	StrobeEnabled	TRUE or FALSE
	StrobeStartLine	1 to 65535 lines, in increments of 1 line
	StrobeStopLine	1 to 65535 lines, in increments of 1 line
	StrobePolarity	ActiveHigh or ActiveLow
Expose Properties	ExposeEnabled	TRUE or FALSE
	ExposeStartLine	1 to 65535 lines, in increments of 1 line
	ExposeStopLine	1 to 65535 lines, in increments of 1 line
	ExposePolarity	ActiveHigh or ActiveLow
	VSyncDelay	1 to 65535 lines, in increments of 1 line
Sync Input Properties	SyncInSource	InternalSync or ExternalSync
	HSyncInPolarity	ActiveHigh or ActiveLow
	VSyncInPolarity	ActiveHigh or ActiveLow
Sync Output Properties	SyncOutEnabled	TRUE or FALSE
	HSyncOutPulseWidth	1 to 4095 pixels, in increments of 1 pixel
	VSyncOutPulseWidth	1 to 4095 lines, in increments of 1 line
	SyncOutPolarity	ActiveHigh or ActiveLow

Table 15: DT3162 Values for the DT-Active Monochrome Frame Grabber Control

Category	Property	DT3162 Values
Trigger Properties	TriggerType	Internal, ExternalToStart, or ExternalForEach
	TriggerTransition	OnHighToLow or OnLowToHigh
Video Signal Properties	LineFrequency	1 to 65535 Hz, in increments of 1 Hz
	ClampStart	16 to 4095 pixels, in increments of 1
	ClampEnd	16 to 4095 pixels, in increments of 1
	TotalPixelsPerLine	1 to 4095 pixels, in increments of 1
	FirstActivePixel	0 to 4095 pixels, in increments of 1
	ActivePixelCount	1 to 2047 pixels, in increments of 1
	TotalLinesPerFrame	1 to 4095 lines, in increments of 1
	FirstActiveLine	0 to 2047 lines, in increments of 1
	ActiveLineCount	1 to 2047 lines, in increments of 1
	AcquireType	Progressive, InterlacedEvenFieldOnly, InterlacedOddFieldOnly, Interlaced
Image Adjustment Properties	Brightness	0 to 255, in increments of 1
	Contrast	0 to 99, in increments of 1
Digital I/O Properties	InputLineCount	4
	InputLineEventMask	0 to 15
	OutputLineCount	4

Table 15: DT3162 Values for the DT-Active Monochrome Frame Grabber Control

Category	Property	DT3162 Values
Region of Interest Properties	RoiLeft	0 to 2039 pixels, in increments of 1
	RoiTop	0 to 2047 lines, in increments of 1
	RoiWidth	8 to 2048 pixels, in increments of 8
	RoiHeight	1 to 2048 lines, in increments of 1
Video Input Properties	PixelClockSource	InternalSource, ExternalSource1, or ExternalSource2
	VideoInputSource	VideoSource0, VideoSource1, or VideoSource2
Overlay Properties	OverlayBitmapFile	The path to the overlay file.
	OverlayColorKey	To specify an absolute color, use the format 0x00BBGGRR. To specify a system color, use the format 0x800000xx, where *xx* is the system color index.
	OverlayEnabled	TRUE or FALSE

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