TQMP2020
User's Manual

TQMP2020 UM 102
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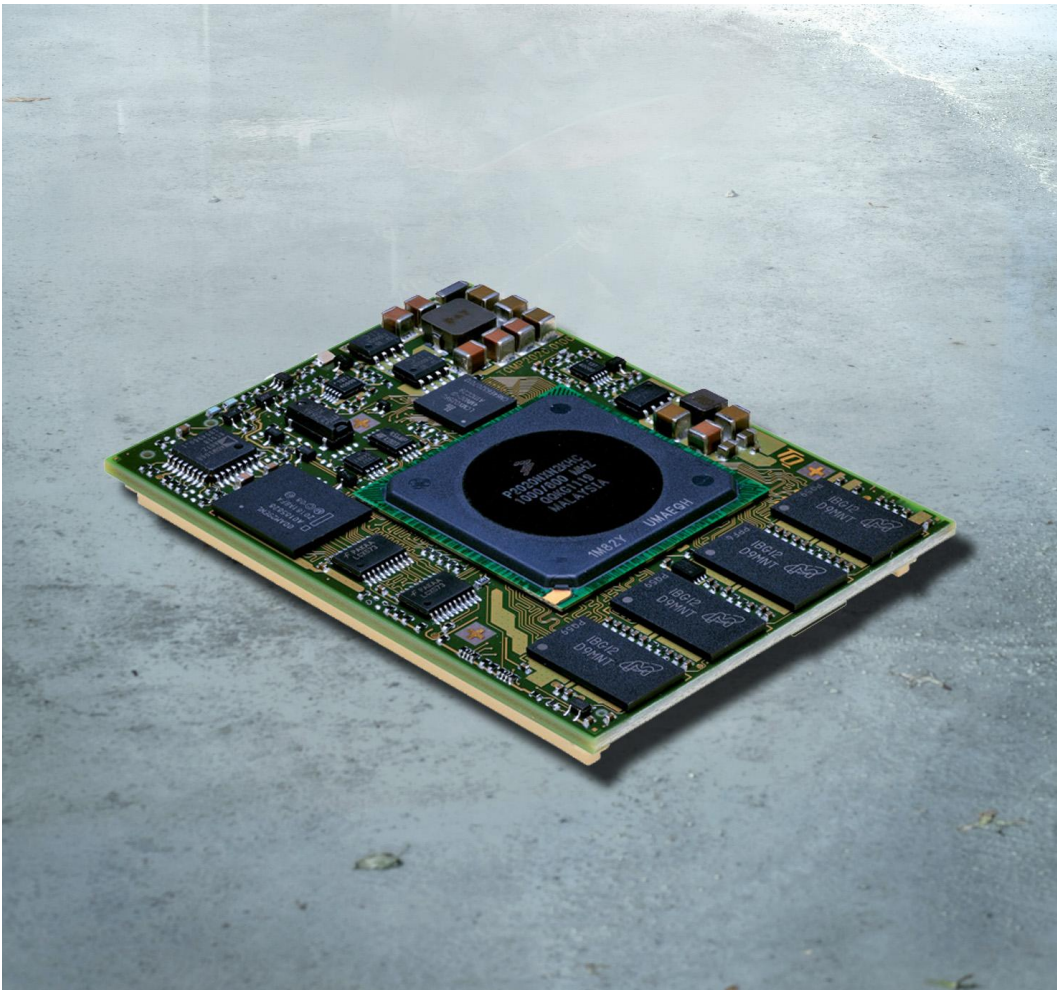

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Revision history

Rev.	Date	Name	Pos.	Modification
100	07.07.2011	Petz		Document created
101	03.01.2012	Petz	3.2.3 Table 7 3.2.3.6 3.2.4.6 Illustration 6 3.2.4.6 Table 17	CPU configuration legend updated ”Meaning P2020” for values “10” and “11” of signals PORDEVSR[20:21] corrected Warning added “100 MHz” for TQMP1xxx removed Added Explanation for Illustration 6 added Type of signal HRESET# specified more precisely
102	24.05.2012	Petz	3.2.3.2 3.7	Typo Link to Wiki added

1. ABOUT THIS MANUAL

1.1 Copyright

1.2 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.3 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol / Visual Cue	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	This specification is used to state the complete file name with its corresponding extension.

1.4 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the module and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.5 Registered trademarks

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TQ-Components GmbH
Gut Delling, Mühlstraße 2
82229 Seefeld
Tel: +49 (0) 8153 9308–0
Fax: +49 (0) 8153 9308–134
Email: info@tqs.de
Web: http://www.tq-group.com/

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1.8 Copyright and licence expenses

The drivers and utilities for the used components as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.
Boot loader licence expenses are paid by TQ-Components GmbH and are included in the price. Licence expenses for the operating system and applications are not taken into consideration and must be separately calculated / declared.

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the used modules:**
  These documents describe the service, functionality and special characteristics of the used module (incl. BIOS).

- **Specifications of the used components:**
  The manufacturer's specifications of the used components, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Components GmbH.

- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.

- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.

- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

1.10 Acronyms and definitions

Table 2: Acronyms

Acronym	Description
BGA	Ball Grid Array
COP	Common On-chip Processor
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DDR	Double Data Rate
DMA	Direct Memory Access
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GP	General Purpose
IP	Ingress Protection
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LSB	Least Significant Bit
LVTTL	Low Voltage Transistor Transistor Logic
MII	Media-Independent Interface
MSB	Most Significant Bit
NAND	Not-and
NC	Not Connected
NOR	Not-or
PHY	Physical (Interface)

Table 2: Acronyms (continued)

Acronym	Description
PLL	Phase Locked Loop
POR	Power-On Reset
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read-Only Memory
RTBI	Reduced Ten-Bit Interface
RTC	Real-Time Clock
RoHS	Restriction of (the use of certain) Hazardous Substances
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media Independent Interface
SMD	Surface-Mounted Device
SPI	Serial Peripheral Interface
SerDes	Serializer/Deserializer
TBI	Ten-Bit Interface
TSEC	Three-Speed Ethernet Controller
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin count Interface
UPM	User Programmable Machine
USB	Universal Serial Bus

2. BRIEF DESCRIPTION

The TQMP2020 is a universal Minimodule based on the Freescale QorIQ processor P2020.
It extends the range of Power-Architecture based modules towards High-End, with reduced size.
The computing performance of the P2020 (dual core CPU) is approximately double of the MPC8548, at significantly lower power dissipation. Alternatively, a P2010 (single core) can be assembled on the module. In this case, the computing performance corresponds to the MPC8548. The power dissipation is reduced further.
A P1020, or P1021 (dual core), or a P1011, or P1012 (single core) can be assembled on the same printed circuit board as an alternative.

The characteristic features of the module are:

- Dual or Single Core, max. 1.2 GHz
- DDR3, 32 or 64 bit with ECC
- 4 × SERDES, configurable as PCI Express, SGMII or Serial Rapid/IO
- 3 × Gbit-Ethernet

The Starterkit STKP2020 is used as an Eval-Board for the TQMP2020.
All function relevant pins of the CPU are routed to the module plug connectors.
Even when using the module, the user has complete freedom, as in a design-in solution.

3. TECHNICAL DATA

3.1 Overview

3.1.1 TQMP2020 block diagram

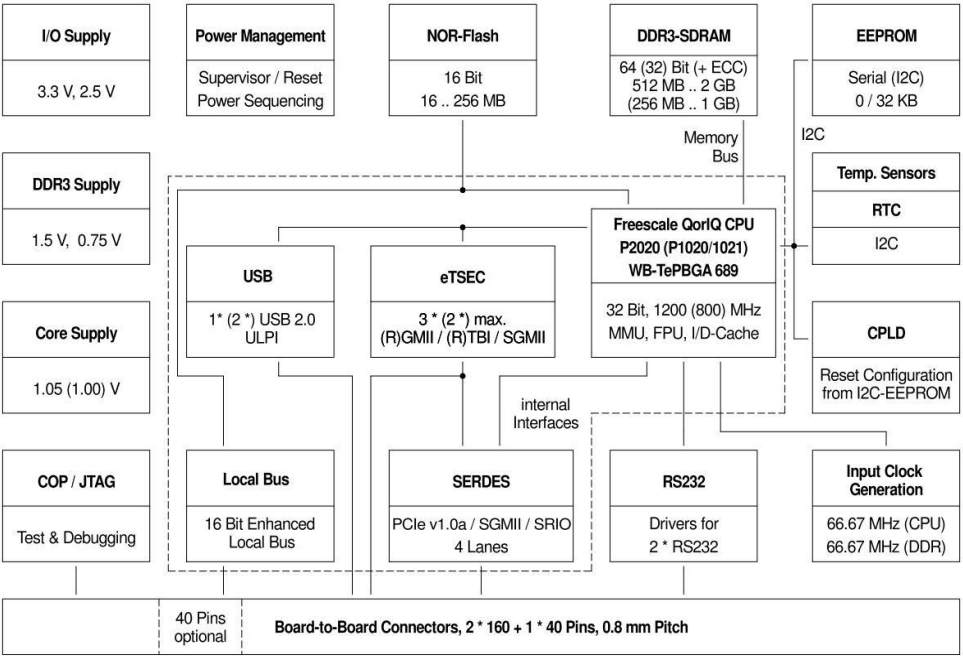

Illustration 1: TQMP2020 block diagram

3.1.2 System components

- QorIQ processor P2020 or P2010, optional P1020/11 and P1021/12
- Oscillator for CPU clocks
- Reset generator and power fail logic
- CPLD for reset configuration
- Voltage regulator for 2.5 V, 1.8 V, 1.5 V, core voltage VDD, VTT, VREF
- Switch for 3.3 V
- DDR3 SDRAM
- NOR Flash
- Serial EEPROM (data + configuration)
- RTC
- Temperature sensors
- RS232 driver for two serial interfaces
- Board-to-board plug connector system

3.2 Electronics

3.2.1 CPU

As an alternative to the P2020, (dual core) a P2010 (single core) can be assembled on the same module. Unless otherwise noted, the name P2020 also stands for the P2010 in the following, and equally for derivatives with and without encryption.
The P2020 offers a large number of interfaces. On account of the high data rates special attention is to be paid to the interfaces mentioned in the following.

3.2.1.1 Parallel Modes of the Enhanced Three Speed Ethernet Controller (eTSEC)

The three gigabit Ethernet interfaces TQMP2020 are implemented via eTSECs. All relevant pins are routed to the module plug connectors, to enable the user to use all possible interface modes supported by the CPU. PHY and transformer have to be integrated on the baseboard for RF-technical reasons.

- MII mode
  - Highest frequency to be transmitted: 25 MHz (Tx- and Rx clock 100 Mbit/s)

- RMII mode
  - Highest frequency to be transmitted: 50 MHz (Tx- and Rx clock @ 100 Mbit/s)
  - Lower number of signals than with MII
  - Timing is tighter than with MII, because both clock edges are used

- GMII-and TBI mode
  - Highest frequency to be transmitted: 125 MHz (Tx- and Rx clock @ 1 Gbit/s)
  - Transmit clock changes signal of GTX_CLK to TX_CLK as well as direction with fallback to 10/100 Mbit/s (MII)

- RGMII-and RTBI mode
  - Highest frequency to be transmitted: 125 MHz (Tx- and Rx clock @ 1 Gbit/s)
  - Lower number of signals than with (G)MII or TBI
  - Timing tighter than with (G)MII and TBI, because both clock edges are used
  - Source clocking

The configuration of the interface modes is carried out via the CPLD, which reads the configuration from the configuration EEPROM. See also 3.2.3.
The above-described interfaces, except RGMII, are supported by the P2020 as well as P2010. With all other CPUs, (P1020/11 as well as P1021/12) only two eTSECs (eTSEC1 / 3) can be operated in the parallel mode with RGMII. The following table shows the possible eTSEC-configurations.

Table 3: eTSEC configuration possibilities P2020/10 (P1020/11, P1021/12)

eTSEC1	eTSEC2	eTSEC3
Standard interface	Standard interface	
	SGMII	SGMII
Inactive	Inactive	Inactive
Reduced interface	Reduced interface	
	SGMII	SGMII
Inactive	Inactive	Inactive
	SGMII	SGMII
Inactive	Inactive	Inactive
Reduced interface	Reduced interface	Reduced interface
	SGMII	SGMII
Inactive	Inactive	Inactive

Underlined: also P1020/11 and P1021/12

Standard interfaces: GMII, TBI, MII
Reduced interfaces: RGMII, RTBI, RMII

If the parallel mode is used the IO voltages at the CPU (= LVDD) and at the PHYs must be the same. See also 3.3.2.3.

3.2.1.2 Serializer/Deserializer (SerDes)

The SerDes controller can be operated as a SGMII, PCI Express or Serial Rapid/IO:

- SGMII Highest frequency to be transmitted: 625 MHz (1.25 Gbit/s)
- PCI Express Highest frequency to be transmitted: 1.25 GHz (2.5 Gbit/s)
- Serial Rapid/IO Highest frequency to be transmitted: 1.563 GHz (3.125 Gbit/s)

Serial Rapid/IO (SRIO) is only supported by the P2020 and the P2010.
The following table shows the possible configurations of the SerDes controllers.

Table 4: SerDes configuration possibilities P2020/10 (P1020/11, P1021/12)

SerDes lanes				Gbaud	
0	**1**	**2**	**3**	**0 & 1**	**2 & 3**
PEX1: × 1	Off	Off	Off	2.5	–
PEX1: × 1	PEX2: × 1	PEX3: × 2		2.5	2.5
PEX1: × 2		PEX3: × 2		2.5	2.5
PEX1: × 4				2.5	
SRIO2: × 1	SRIO1: × 1	Off	Off	3.125	–
SRIO2: × 4				1.25 / 2.5 / 3.125	
SRIO2: × 1	SRIO1: × 1	SGMII2	SGMII3	1.25 / 2.5	1.25
PEX1: × 1	SRIO1: × 1	SGMII2	SGMII3	2.5	1.25
PEX1: × 1	PEX2: × 1	SGMII2	SGMII3	2.5	1.25
PEX1: × 2		SGMII2	SGMII3	2.5	1.25
Off	Off	Off	Off	–	–

Underlined: also P1020/11 and P1021/12

The configuration of the SerDes controller is carried out via the CPLD, which reads the configuration from the configuration EEPROM. See also 3.2.3, considering Table 3.

3.2.1.3 USB

In contrast to P2020/10 and the P1021/12, the P1020/11 possesses two USB controllers. Because Local Bus and USB2 are multiplexed with the P1020/11, the second USB-PHY (ULPI) must be connected at the Local Bus. This means that the second USB-PHY is almost completely limited in its function, or the NOR flash can only be partly used.

3.2.2 Reset logic and supervisor

The reset logic contains the following functions:

- Supervision of the following voltages used on module:
  - 3.3 V, 2.5 V, 1.8 V, 1.5 V
  - VDD (core voltage)
  - VREF (reference voltage for DDR3 SDRAM)
  - VTT (termination voltage for DDR3 SDRAM)
- External reset input (debounced with 200 ms delay)
- PGOOD output (e.g., for power sequencing of an external PHY)
- Indication of the reset state by a LED (HRESET# low ⇨ LED lights up)

3.2.2.1 Supervision 3.3 V

Tolerance range of the fed supply voltage:
VCC3V3ID = 3.201 V to 3.465 V = 3.3 V –3% / +5%

Permitted voltage range for CPU and 3.3 V logic:
VCC3V3 = 3.135 V to 3.465 V

Tolerance of the voltage supervision, voltage drop in VCC3V3 taken into account:
V_{Reset} = 3.135 V to 3.201 V

3.2.2.2 Supervision 2.5 V

This supply voltage is generated and monitored internally.

3.2.2.3 Supervision 1.8 V

This supply voltage is generated and monitored internally.

3.2.2.4 Supervision 1.5 V

This supply voltage is generated and monitored internally.

3.2.2.5 Supervision VDD

The required core voltage depends on the CPU (P2 or P1). It is set at the voltage regulator by component placement, and in the supervisor by the configuration.
The user cannot change this setting.

3.2.2.6 Supervision VREF

The DDR3 reference voltage VREF is monitored internally.

3.2.2.7 Supervision VTT

The DDR3 termination voltage VTT is generated and monitored internally.

3.2.2.8 Reset LED

- LED is controlled via the HRESET#-Signal; HRESET# low ⇨ LED lights up
- The supervisor provides duration for at least 200 ms of the HRESET# pulse.
  The reset is thereby visible even if the reset pulse at RESIN# is very short.

3.2.2.9 Self-reset

The P2020 can request a hardware reset by software. The signal HRESET_REQ# signals the reset requirement. It can be triggered by software by writing to register bit RSTCR[HRESET_REQ].
The following participants can also trigger HRESET_REQ#:

- Boot sequencer error (Preamble, CRC)
- eSDHC boot loader error (e.g., boot signature)
- eSPI boot loader error (e.g., boot signature)
- Not correctable eLBC ECC Error during boot phase of NAND flash
- Rapid/IO
- e500 watchdog

RESIN# is connected to HRESET_REQ# with a resistor on the module (Illustration 2).

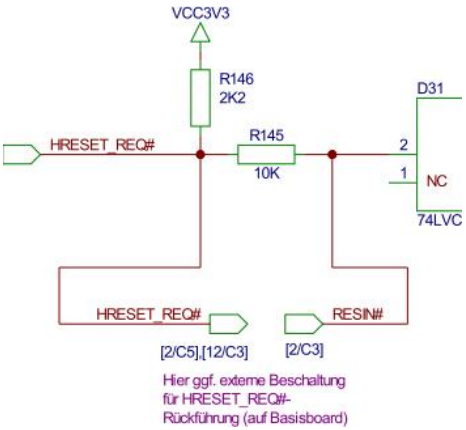

Illustration 2: Feedback HRESET_REQ#

This enables a self-reset trigger. The self-reset can be prevented, or be linked to other conditions depending on the external wiring on the baseboard (see Table 5).

The following table shows the reset options, depending on the wiring of the RESIN#-Signals.

Table 5: Reset options

External wiring at RESIN# input	Reset function
None	Self-reset is possible (HRESET_REQ# is switched through to RESIN# on the module)
Pull-up ≤ 2k2 to VCC3V3	No self-reset possible (HRESET_REQ# cannot trigger a reset on the module)
Open-Drain-/Open Collector output or push button to DGND	Self-reset is possible In addition, an external reset can be triggered by applying a low level at RESIN#
Push-Pull output or Open-Drain-/Open Collector output with pull-up ≤ 2k2 to VCC3V3	No self-reset, but only external reset possible (HRESET_REQ# cannot trigger a reset on the module)

3.2.2.10 JTAG reset TRST#

TRST# will be pulled low by HRESET#, it can still however be triggered separately (COP/JTAG-Debugging). This is achieved with the following circuit on the module.

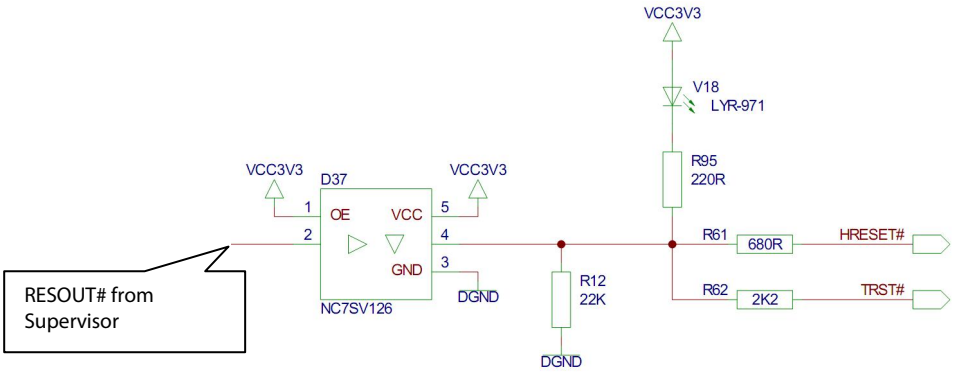

Illustration 3: Wiring of TRST#

3.2.3 CPU configuration

Table 6: Legend for Table 7, Table 8 and Table 9

Binary value in bold	"Default" (Freescale) ⇨ internal value if nothing is connected (internal pull-up)
Binary value greyed out	"Reserved" ⇨ do not use
Light green highlighted	Value is fixed in the design (not alterable)
Dark green highlighted	Value is set in the design by comparators (not by CPLD / EEPROM)
Blue highlighted	Default values of CPLD

3.2.3.1 Reset configuration of the hardware

The signals listed in Table 7 (column 2) are used to define the reset configuration of the CPU on the module.

Table 7: Reset configuration

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_boot_seq[0:1]	LGPL3/LFWP#, LGPL5	PORBMSR[10:11]	00	Reserved	Reserved
			01	Boot sequencer is enabled on I²C1 with normal I²C addressing mode.	Boot sequencer is enabled on I²C1 with normal I²C addressing mode.
			10	Boot sequencer is enabled on I²C1 with extended I²C addressing mode.	Boot sequencer is enabled on I²C1 with extended I²C addressing mode.
			11	**Boot sequencer is disabled. No I²C ROM is accessed.**	**Boot sequencer is disabled. No I²C ROM is accessed.**
cfg_sys_pll[0:2]	LA[29:31]	PORPLLSR[26:30]	000	4:1	4:1
			001	5:1	5:1
			010	6:1	6:1
			011	8:1	Reserved
			others	Reserved	Reserved
cfg_core0_pll[0:2]	LBCTL, LALE, LGPL2/LOE#/LFRE#	PORPLLSR[10:15]	000	4:1	Reserved
			001	9:2 (4.5:1)	Reserved
			010	1:1	1:1
			011	3:2 (1.5:1)	3:2 (1.5:1)
			100	2:1	2:1
			101	5:2 (2.5:1)	5:2 (2.5:1)
			110	3:1	3:1
			111	7:2 (3.5:1)	Reserved

Table 7: Reset configuration (continued)

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_core1_pll[0:2]	LWE0#, UART_SOUT1, READY_P1	PORPLLSR[2:7]	000	4:1	Reserved
			001	9:2 (4.5:1)	Reserved
			010	1:1	1:1
			011	3:2 (1.5:1)	3:2 (1.5:1)
			100	2:1	2:1
			101	5:2 (2.5:1)	5:2 (2.5:1)
			110	3:1	3:1
			111	7:2 (3.5:1)	Reserved
cfg_ddr_pll[0:2]	TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT[1:2]	PORPLLSR[18:22]	000	Reserved	3:1
			001	4:1	4:1
			010	6:1	6:1
			011	8:1	8:1
			100	10:1	10:1
			101	12:1	Reserved
			110	Reserved	Reserved
			111	Synchronous mode	Synchronous mode
cfg_srds_pll_toe	TRIG_OUT/READY_P0	PORDEVSR2[10]	0	Enable PLL lock time-out counter, POR-sequence waits for SerDes PLL to lock while time-out counter has not expired	Not used
			1	**Disable PLL lock time-out counter, POR-sequence waits for SerDes PLL to lock**	Not used
cfg_plat_speed	LA23	PORDEVSR2[14]	0	Platform clock <333 MHz	Platform clock <300 MHz and >267 MHz
			1	**Platform clock ≥333 MHz**	**Platform clock ≥300 MHz**

Table 7: Reset configuration (continued)

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_core0_speed	LA24	PORDEVSR2[12]	0	Core 0 clock ≤1 GHz	Core 0 clock ≤450 MHz
			1	**Core 0 clock >1 GHz**	**Core 0 clock >450 MHz**
cfg_core1_speed	LA25	PORDEVSR2[13]	0	Core 1 clock ≤1 GHz	Core 1 clock ≤450 MHz
			1	**Core 1 clock >1 GHz**	**Core 1 clock >450 MHz**
cfg_ddr_speed	LA26	PORDEVSR2[15]	0	DDR clock <500 MHz	DDR clock <450 MHz
			1	**DDR clock ≥500 MHz**	**DDR clock ≥450 MHz**
cfg_sys_speed	LA28	PORDEVSR2[21]	0	System clock <66 MHz	Reserved
			1	**System clock ≥66 MHz**	**System clock ≥66 MHz**
cfg_cpu[0:1]_boot	LA27, LA16	PORBMSR[0:1]	00	CPU boot holdoff mode for both cores. The e500 cores are prevented from booting until configured by an external master.	CPU boot holdoff mode for both cores. The e500 cores are prevented from booting until configured by an external master.
			01	e500 core 1 is allowed to boot without waiting for configuration by an external master, while e500 core 0 is prevented from booting until configured by an external master or the other core.	e500 core 1 is allowed to boot without waiting for configuration by an external master, while e500 core 0 is prevented from booting until configured by an external master or the other core.
			10	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core.	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core.
			11	Both e500 cores are allowed to boot without waiting for configuration by an external master.	**Both e500 cores are allowed to boot without waiting for configuration by an external master.**

Table 7: Reset configuration (continued)

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_ddr_debug	DMA2_DDONE0#	PORDBGMSR[7]	0	ECC pins driven Debug info instead of normal ECC I/O. (disconnect memory devices)	ECC pins driven Debug info instead of normal ECC I/O. (disconnect memory devices)
			1	**ECC pins in normal mode**	**ECC pins in normal mode**
cfg_device_ID[7:5]	TSEC2_TXD[4:2]	PORDEVSR[29:31]	xxx-----	Device ID LSBs for Rapid/IO hosts	Not used
cfg_dram_type	TSEC2_TXD1	PORDEVSR[25]	0	DDR2 1.8 V, CKE low @ reset	DDR2 1.8 V, CKE low @ reset
			1	**DDR3 1.5 V, CKE low @ reset**	**DDR3 1.5 V, CKE low @ reset**
cfg_elbc_ecc	MSRCID0	PORDEVSR[15]	0	eLBC ECC checking disabled	eLBC ECC checking disabled
			1	**eLBC ECC checking enabled**	**eLBC ECC checking enabled**
cfg_eng_use[0:7]	LA[20:22], UART_SOUT0, *TRIG_OUT/READY_P0*, MSRCID1, MSRCID4, DMA1_DDONE#	PORDEVSR2	000x0000	Reserved for engineering use	Not used
			...	Reserved for engineering use	Not used
			111x1110	Reserved for engineering use	Not used
			111x1111	**Default (see cfg_srds_pll_toe)**	Not used

Table 7: Reset configuration (continued)

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_host_agt[0:2]	LWE1#/LBS1, LA[18:19]	PORBMSR[13:15]	000	Agent on all PCIe and SRIO	Agent on all PCIe
			001	Agent on PCIe 1 or host SRIO 2, Host on PCIe 2 / SRIO 1, Host on PCIe 3	Agent on PCIe 1, Host on PCIe 2
			010	Host on PCIe 1 or agent SRIO 2, Agent on PCIe 2 / SRIO 1, Host on PCIe 3	Host on PCIe 1, Agent on PCIe 2
			011	Host on PCIe 1 / SRIO 2, Host on PCIe 2 / SRIO 1, Agent on PCIe 3	Reserved
			100	Agent on PCIe 1 / SRIO 2, Agent on PCIe 2 / SRIO 1, Host on PCIe 3	Reserved
			101	Agent on PCIe 1 or host SRIO 2, Host on PCIe 2 / SRIO 1, Agent on PCIe 3	Reserved
			110	Host on PCIe 1 or agent SRIO 2, Agent on PCIe 2 / SRIO 1, Agent on PCIe 3	Reserved
			111	**Host processor / root complex for all PCIe / SRIO**	**Host processor / root complex for all PCIe**

Table 7: Reset configuration (continued)

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_io_ports[0:3]	TSEC1_TXD[3:1], TSEC2_TX_ER	PORDEVSR[9:12]	0000	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, SerDes lanes 1-3 powered down	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, SerDes lanes 1-3 powered down
			0001	SerDes lanes 0-3 powered down	SerDes lanes 0-3 powered down
			0010	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, PCIe 2 (x1) (2.5 Gbps) → SerDes lane 1, PCIe 3 (x2) (2.5 Gbps) → SerDes lane 2-3	Reserved
			0011	Reserved	Reserved
			0100	PCIe 1 (x2) (2.5 Gbps) → SerDes lane 0-1, PCIe 3 (x2) (2.5 Gbps) → SerDes lane 2-3	Reserved
			0101	Reserved	Reserved
			0110	PCIe 1 (x4) (2.5 Gbps) → SerDes lane 0-3	PCIe 1 (x4) (2.5 Gbps) → SerDes lane 0-3
			0111	SRIO 2 (1x) (3.125 Gbps) → SerDes lane 0, SRIO 1 (1x) (3.125 Gbps) → SerDes lane 1, SerDes lanes 2-3 powered down	Reserved
			1000	SRIO 2 (4x) (1.25 Gbps) → SerDes lane 0-3	Reserved
			1001	SRIO 2 (4x) (2.5 Gbps) → SerDes lane 0-3	Reserved
			1010	SRIO 2 (4x) (3.125 Gbps) → SerDes lane 0-3	Reserved
			1011	SRIO 2 (1x) (1.25 Gbps) → SerDes lane 0, SRIO 1 (1x) (1.25 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	Reserved
			1100	SRIO 2 (1x) (2.5 Gbps) → SerDes lane 0, SRIO 1 (1x) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	Reserved
			1101	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, SRIO 1 (1x) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	Reserved
			1110	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, PCIe 2 (x1) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, PCIe 2 (x1) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3
			1111	**PCIe 1 (x2) (2.5 Gbps) → SerDes lane 0-1 SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2 SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3**	**PCIe 1 (x2) (2.5 Gbps) → SerDes lane 0-1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3**

Table 7: Reset configuration (continued)

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_mem_debug	DMA2_DACK0#	PORDBGMSR[5]	0	Debug info from eLBC is driven on MSRCID and MDVAL	Debug info from eLBC is driven on MSRCID and MDVAL
			1	**Debug info from DDR is driven on MSRCID and MDVAL**	**Debug info from DDR is driven on MSRCID and MDVAL**
cfg_rio_sys_size	LGPL0/LFCLE	PORDEVSR[28]	0	Large system size (up to 65536 devices)	Not used
			1	**Small system size (up to 256 devices)**	Not used
cfg_rom_loc[0:3]	TSEC1_TXD[6:4], TSEC1_TX_ER	PORBMSR[4:7]	0000	PCIe 1	PCIe 1
			0001	PCIe 2	PCIe 2
			0010	SRIO 1	Reserved
			0011	SRIO 2	Reserved
			0100	DDR	DDR
			0101	PCIe 3	Reserved
			0110	On-Chip boot ROM - SPI config	On-Chip boot ROM - SPI config
			0111	On-Chip boot ROM - eSDHC config	On-Chip boot ROM - eSDHC config
			1000	eLBC FCM - 8-bit NAND small page	eLBC FCM - 8-bit NAND small page
			1001	Reserved	Reserved
			1010	eLBC FCM - 8-bit NAND large page	eLBC FCM - 8-bit NAND large page
			1011	Reserved	Reserved
			1100	Reserved	Reserved
			1101	eLBC GPCM - 8-bit ROM	eLBC GPCM - 8-bit ROM
			1110	eLBC GPCM - 16-bit ROM	eLBC GPCM - 16-bit ROM
			1111	**eLBC GPCM - 16-bit ROM (formerly probably GPCM - 32-bit)**	**eLBC GPCM - 16-bit ROM (formerly probably GPCM - 32-bit)**
cfg_sgmii2	LGPL1/LFALE	PORDEVSR[3]	0	eTSEC2 (SGMII) → SGMII SerDes lane 2 pins	Not used
			1	**eTSEC2 (Std.) → TSEC2_* pins**	Not used
cfg_sgmii3	TSEC_1588_ALARM_OUT2	PORDEVSR[4]	0	eTSEC3 (SGMII) → SGMII SerDes lane 3 pins	eTSEC3 → SGMII
			1	**eTSEC3 (Std.) → TSEC3_* pins**	**eTSEC3 → RGMII**

Table 7: Reset configuration (continued)

Config signal	IO signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_srds_refclk	TSEC_1588_ALARM_OUT1	PORDEVSR2[18]	0	SerDes Ref Clock = 125 MHz	SerDes Ref Clock = 125 MHz
			1	**SerDes Ref Clock = 100 MHz**	**SerDes Ref Clock = 100 MHz**
cfg_tsec_reduce	EC_MDC	PORDEVSR[0]	0	eTSEC1 & eTSEC2 in reduced pin mode (RTBI, RGMII, RMII)	eTSEC1 in reduced mode (RGMII)
			1	**eTSEC1 & eTSEC2 in std. width (TBI, GMII, MII)**	**Reserved**
cfg_tsec1_prtcl[0:1]	TSEC1_TXD0, TSEC1_TXD7	PORDEVSR[6:7]	00	Reserved	Reserved / eTSEC1 → SGMII
			01	ETSEC1 → MII / RMII	Reserved / eTSEC1 → SGMII
			10	ETSEC1 → GMII / RGMII	eTSEC1 → RGMII
			11	**ETSEC1 → TBI / RTBI**	**Reserved** / eTSEC1 → SGMII
cfg_tsec2_prtcl[0:1]	TSEC2_TXD0, TSEC2_TXD7	PORDEVSR[18:19]	00	Reserved	Not used
			01	ETSEC2 → MII / RMII (if not configured to SGMII)	Not used
			10	ETSEC2 → GMII / RGMII (if not configured to SGMII)	Not used
			11	**eTSEC2 → TBI / RTBI (if not configured to SGMII)**	Not used
cfg_tsec3_prtcl[0:1]	UART_RTS[0:1]#	PORDEVSR[20:21]	00	Reserved	Reserved / eTSEC3 → SGMII
			01	eTSEC3 → RMII (if not configured to SGMII)	Reserved / eTSEC3 → SGMII
			10	eTSEC3 → RGMII (if not configured to SGMII)	eTSEC3 → RGMII
			11	**eTSEC3 → RTBI (if not configured to SGMII)**	**Reserved / eTSEC3 → SGMII**
cfg_sdhc_cd_pol_sel	TSEC2_TXD5/TSEC3_TX_EN	PORDEVSR[23]	0	**eSDHC Card-detect polarity is not inverted**	Not used
			1	**eSDHC Card-detect polarity is not inverted**	**Not used**

3.2.3.2 Freely available reset configuration

The signals listed in the following table are not used on the module. The baseboard can pass additional configuration data to the CPU on these signals, if desired. These do not influence the configuration of the CPU by hardware after a reset, but can merely be utilised by software.

Table 8: Free reset configuration (general purpose)

Config signal	IO-Signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_gpinput[0:15]	LAD[0:15]	GPPORCR[0:15]	0x nnnn_0000	General-purpose POR config → not used	General-purpose POR config → not used

3.2.3.3 Other configuration signals

The module generates the signals listed in the following table. They are not read during reset, but must be applied permanently.

Table 9: Static configuration signals

Config signal	IO-Signal at the P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
LVDD_VSEL	LVDD_VSEL	IOVSELSR[30:31]	0	3.3 V: eTSEC[1:3], Eth. Management, 1588	3.3 V: eTSEC[1:3], Eth. Management, 1588
			1	2.5 V: eTSEC[1:3], Eth. Management, 1588	2.5 V: eTSEC[1:3], Eth. Management, 1588
BVDD_VSEL[0:1]	BVDD_VSEL[0:1]	IOVSELSR[26:27]	00	3.3 V: Local Bus, GPIO[8:15]	3.3 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
			01	2.5 V: Local Bus, GPIO[8:15]	2.5 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
			10	1.8 V: Local Bus, GPIO[8:15]	1.8 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
			11	3.3 V: Local Bus, GPIO[8:15]	3.3 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
CVDD_VSEL[0:1]	CVDD_VSEL[0:1]	IOVSELSR[22:23]	00	3.3 V: USB, eSDHC, SPI	3.3 V: USB, eSDHC, SPI
			01	2.5 V: USB, eSDHC, SPI	2.5 V: USB, eSDHC, SPI
			10	1.8 V: USB, eSDHC, SPI	1.8 V: USB, eSDHC, SPI
			11	3.3 V: USB, eSDHC, SPI	3.3 V: USB, eSDHC, SPI

3.2.3.4 Configuration data in the EEPROM

Table 10 shows how the configuration data is stored in the EEPROM. The single fields with configuration data consist of an Enable bit and the actual data field in each case:

Enable 0 = Tri-State 1 = Actively driven during Reset	Configuration data see Table 7

Table 10: Configuration data in EEPROM

Address	Content							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Fixed Configuration ID							
	0	0	1	0	1	0	1	0
1	Enable | cfg_boot_seq[0:1]			Enable | cfg_sys_pll[0:2]				Enable
2	cfg_core0_pll[0:2]			Enable | cfg_core1_pll[0:2]				Enable
3	cfg_ddr_pll[0:2]			Enable | cfg_srds_pll_toe		Enable | cfg_plat_speed		Enable
4	cfg_core0_speed	Enable | cfg_core1_speed		Enable | cfg_ddr_speed		Enable | cfg_sys_speed		Enable
5	cfg_cpu[0:1]_boot		Enable | cfg_ddr_debug		Enable | cfg_device_ID[7:5]			
6	Enable | cfg_dram_type		Enable | cfg_elbc_ecc		Enable | cfg_eng_use[0:2]			
7	cfg_eng_use[3:7]					Enable | cfg_host_agt[0:1]		
8	cfg_host_agt[2]	Enable | cfg_io_ports[0:3]					Enable | cfg_mem_debug	
9	Enable | cfg_rio_sys_size		Enable | cfg_rom_loc[0:3]					Enable
10	cfg_sgmii2	Enable | cfg_sgmii3		Enable | cfg_srds_refclk		Enable | cfg_tsec_reduce		Enable
11	cfg_tsec1_prtcl[0:1]		Enable | cfg_tsec2_prtcl[0:1]			Enable | cfg_tsec3_prtcl[0:1]		
12	Enable | cfg_sdhc_cd_pol_sel		*unused*	*unused*	*unused*	*unused*	*unused*	*unused*
13	CRC checksum							

3.2.3.5 Error handling and default configuration

The CPLD transmits a reset sequence on the I^2C bus (IIC1) before the real access.
This ensures that accesses still running at the time of the reset are completed and the EEPROM is ready to be read.
To ensure the system integrity, the configuration mechanism handles the following errors:

- I^2C protocol error
- Configuration ID missing
- CRC incorrect

In these cases, the CPLD starts another attempt. If this also fails, the default configuration will be passed to the CPU (highlighted in blue in Table 7). This guarantees that the system boots, but with certain functional limitations (lower clock, interfaces partly not available).
The CRC used the polynomial $x^8 + x^2 + x + 1$ and the start value 0xFF. A tool, which calculates the CRC, can be made available, if required.

Tip 1

Damaged or deleted configuration data generates a CRC error and causes the use of the default configuration. With the again bootable system, the EEPROM can be rewritten. Another possibility is, to pull IIC1_SDA "low". This leads to a protocol error (NACK) and therefore the default configuration to be used. In this manner a system with two different boot configurations can be operated: e.g., a normal operation (config-EEPROM) with boot process via PCIe or eSDHC and a service or emergency operation (default-config) with boot loader in the NOR flash.

Tip 2

The enable-bits enable the configuration of single fields not via the module, but via the baseboard without reprogramming the EEPROM. Thus, e.g., the field "cfg_device_ID" can be configured with different Device-IDs depending on the baseboard. Pull-ups / pull-downs or active drivers (driver conflicts possible) must be provided for this on the baseboard.
During the reset phase respective, power-up the corresponding signals are driven by the CPLD. As these signals are outputs of the CPU or the module, a possible driver's conflict must be taken into account in the design of the baseboard. The signals UART_SOUT0# (cfg_eng_use3), UART_SOUT1# (cfg_core1_pll1) and TSEC2_TXD5/TSEC3_TX_EN (cfg_sdhc_cd_pol_sel) are an exception. These signals are separated from the plug connector during the reset phase of the module to improve the system integrity.

3.2.3.6 Settings via the boot sequencer

The CPU configuration with CPU specific boot sequencer cannot replace the configuration via the CPU pins, but only complement. Because it runs before the software starts, it can carry out additional settings, which cannot or should not be set by software.
The standard software delivered with the module (U-Boot) does not depend on the boot sequencer.
The standard software (U-Boot) delivered with the module does not rely on the boot sequencer.
The configuration with the boot sequencer starts after the end of the reset. In certain cases, the configuration via the boot sequencer is indispensable:

- Multiprocessor environments
- Preconfiguration to boot via other systems or interfaces (e.g., PCIe, Rapid/IO, SDRAM...)
- Fixing of incompatibilities with reset values (e.g., preset functionality of the bus driver control LBCTL)

	Wrong data can lead to an unbootable system! This condition can be fixed by temporary activation of the default configuration, because the boot sequencer is deactivated then. See also tip 2 under 3.2.3.5.

	The CPU operates the I^2C bus at about 160 kHz when the boot sequencer is used. Devices, which can only work at a maximum of 100 kHz may not be connected to IIC1, when the boot sequencer is enabled. This only affects the baseboard as all I^2C bus devices on the TQMP2020 can operate at 400 kHz.

3.2.4 Clock

3.2.4.1 Internal clock structure of the P2020/2010

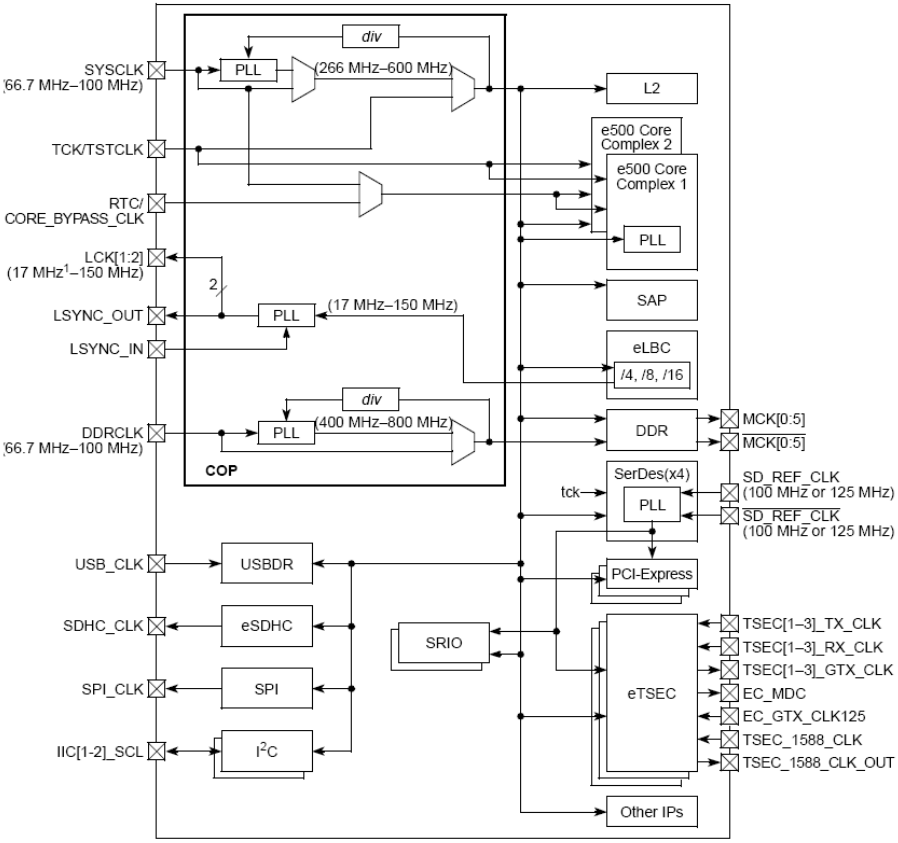

Illustration 4: P2020/2010 clock subsystem, block diagram (Source: Freescale)

3.2.4.2 Internal clock structure of the P1020/1011 and P1021/1012

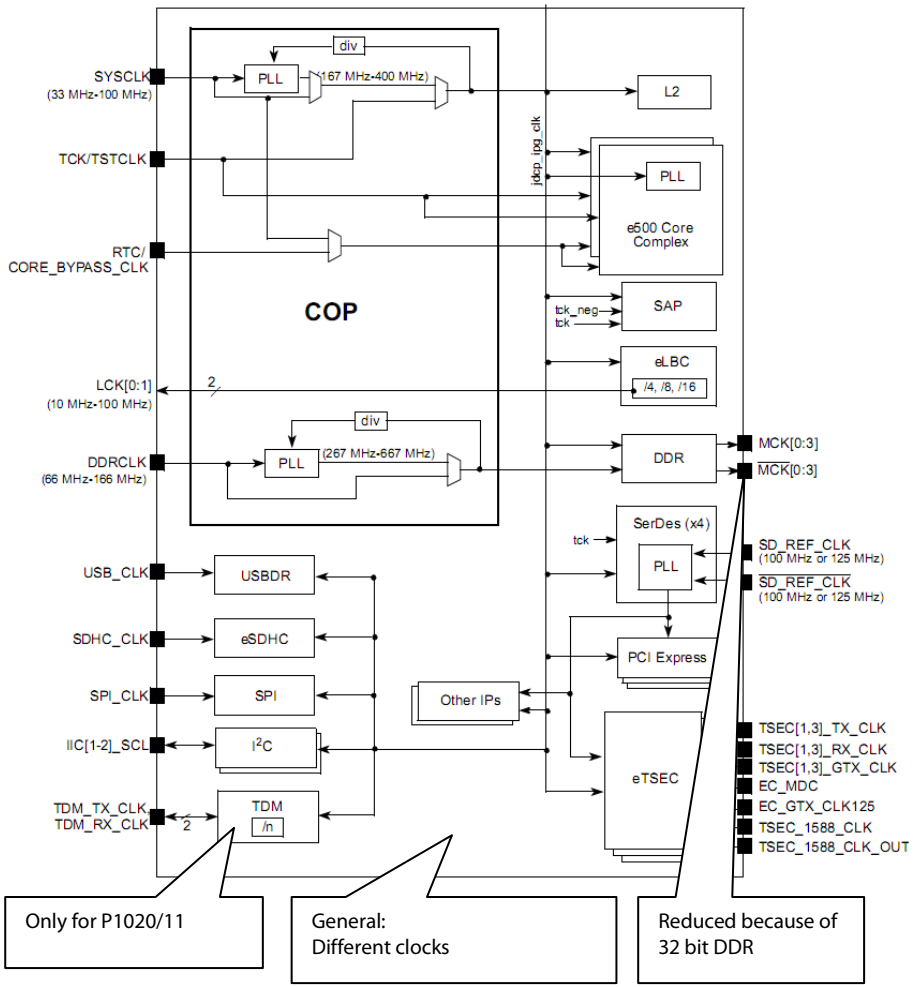

Illustration 5: P1020/1011 and P1021/1012 clock subsystem, block diagram (Source: Freescale)

3.2.4.3 System clock SYSCLK

In normal operation, SYSCLK is generated on the module.
The Platform- or Core-Complex-Bus clock (see 3.2.4.4) is generated by multiplication from this.
The Memory bus clock (see 0) can also be generated.
The frequency is 66.666 MHz.
Spread spectrum clocking is possible on request, but not standard.

3.2.4.4 Core-Complex-Bus clock CCB_CLK

The Platform- or Core-Complex-Bus clock CCB_CLK is generated from the system clock signal SYSCLK by multiplication. The multiplication factor is fixed by the reset configuration. The signal merely exists CPU internally. It is used for the L2 cache (internal) as well as for the Local Bus and other interfaces.
The frequency is set to 400 MHz by default.
Core frequencies of 600, 800, 1000 and 1200 MHz are possible with it, see 3.2.4.5.

TQMP1xxx: 266 / 333 / 400 / 533 MHz = 0.5 × frequency CORE_CLK or constant 266 MHz.

3.2.4.5 Processor Core clock CORE_CLK

The core clock CORE_CLK is generated by multiplication from CCB_CLK.
The multiplication factor is fixed by the reset configuration.
The signal merely exists CPU internally and is used for the e500v2 core(s).
Possible frequencies are 600, 800, 1000 or 1200 MHz.

TQMP1020, TQMP1021: 333 to 800 MHz, gradation depending on CCB_CLK and multiplication factors.

3.2.4.6 Local Bus clock LCLK

The Local Bus clock LCLK is generated from CCB_CLK divided by LCRR[CLKDIV] (values 4, 8 or 16).
The division factor LCRR[CLKDIV] is configurable at run time.
The signal is used for the Local Bus.
Possible frequencies with CCB_CLK = 400 MHz are 25, 50, 100 MHz.
The maximum possible frequency LCLK for the P2020 is 150 MHz.

TQMP1xxx:

- *with CCB_CLK = 400 MHz: 25, 50 MHz*
- *with CCB_CLK = 267 MHz: 17, 33, 66 MHz*

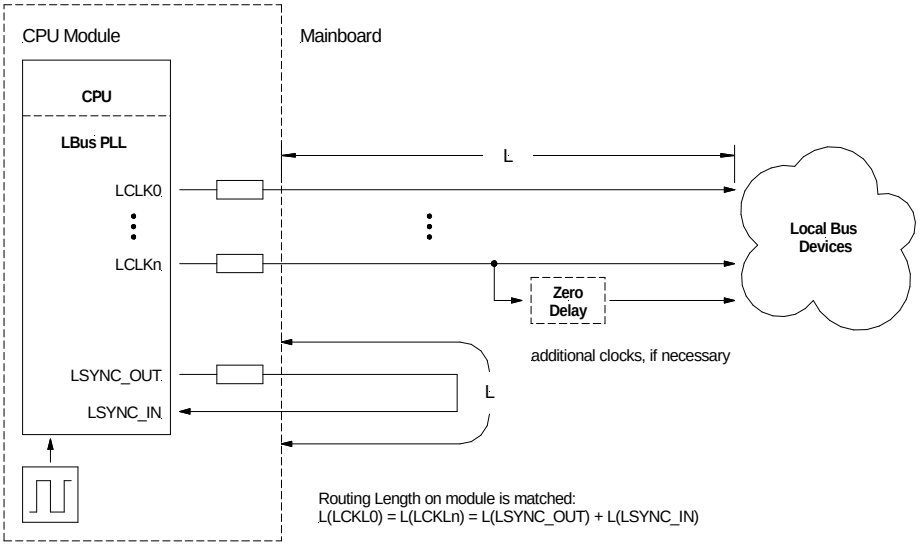

Illustration 6: Length alignment Local Bus

Two clock outputs LCKL[0:1] are provided externally. A zero-delay buffer has to be provided on the baseboard, if more participants have to be supplied as clock outputs are available.
The following applies for the feedback:

- A feedback is only required if the Local Bus is used in PLL Enable mode.
- No feedback is required, however, if the PLL Bypass mode is used (it may be present).
- The adjustment of the cable length is only required if participants, which use the clock are connected to the Local Bus on the baseboard. If this is not the case, the length of the feedback is unimportant. On the module are no bus participants, which require the clock.

3.2.4.7 Memory bus clocks: DDRCLK, DDR_CLK, MCKx, MCK#

The Platform clock CCB_CLK can be used as an alternative to the Memory Bus clock DDR_CLK, or be generated by an own PLL from DDRCLK (= SYSCLK).
The frequency of the Memory Bus clock DDR_CLK corresponds to the DDR data rate.
It is twice as high as the frequency of the signals MCKx and MCK#.
Favourite frequency: DDR_CLK = 800 MHz, multiplied from DDRCLK (66.666 MHz) × 12.

TQMP1xxx: 666 MHz from DDRCLK (66.666 MHz) × 10.

3.2.4.8 Real time clock RTC

The signal RTC is a clock input, through which a time base can be created which is independent of the system clock. The signal RTC is available at the connector but not connected on the module.
More detailed information can be found in the hardware specification of the CPU (1).

3.2.4.9 USB clock USB_CLK

The signal USB_CLK is required for the interface to the external USB-PHY. (The USB controller runs synchronically to CCB_CLK). If USB is used, a 60-MHz clock must be fed at this signal.
More detailed information can be found in the hardware specification of the CPU (1).

3.2.4.10 SERDES clock SD_REF_CLK/SD_REF_CLK#

The signal pair SD_REF_CLK/SD_REF_CLK# is required for the SERDES interface. (The system side runs synchronically to CCB_CLK). If the SERDES interface is used, depending on protocol and data rate, a clock of 100 or 125 MHz must be supplied here.
If no SERDES clock is supplied, the reset configuration has to prevent that the CPU waits for the SERDES-PLL to lock after a reset. See also cfg_srds_pll_toe under 3.2.3.1.
More detailed information can be found in the hardware specification of the CPU (1).

3.2.4.11 Standard clock frequencies

Table 11: Standard clock frequencies (with P2020)

Clock	Frequency [MHz]	Remark
SYSCLK	66.666	Input clock system-PLL
CCB_CLK	400	Platform clock
CORE_CLK	1,200	Core clock
LCLK	25 / 50 / 100	Standard frequency underlined
DDRCLK	66.666	Input clock DDR-PLL, frequency identical with SYSCLK
DDR_CLK	800	= Data rate
MCKx/MCKx#	400	= half data rate = physical clock
RTC	Freely selectable	Not connected on module
USB_CLK	60	When required externally
SD_REF_CLK/SD_REF_CLK#	100 / 125	When required externally, frequency depending on protocol and data rate

3.2.5 Local Bus

The available chip selects are assigned as follows:

Table 12: Assignment chip selects at the Local Bus

Chip select	Usage on TQMP2020
LCS0#/CS_NOR#	NOR flash (boot)
LCS1#	Free
LCS2#	Free
LCS3#	Free
LCS4#	Free
LCS5#/DMA2_DREQ1#	Free, if not used for DMA
LCS6#/DMA2_DACK1#	Free, if not used for DMA
LCS7#/DMA2_DDONE1#	Free, if not used for DMA

3.2.6 NOR flash

- 3.3-V flashes Micron PC28FxxxM29EW,
  alternatively EON EN29GL, 16 bit wide
- Connected at the Local Bus
  because of multiplexed addresses and data ⇨ addresses via a latch
- One bank with 16 bit bus width
- 16 to 256 Mibyte
- Access time 100 ns
- Chip-select LCS0#

The status signal RY/BY# of the flash is not used by the CPU.
The event of write and erasure cycles must be monitored by polling.

3.2.7 DDR3 SDRAM

- DDR3 SDRAMs, 64 bit wide, alternatively with / without ECC
  P10xx: 32 bit wide, with / without ECC
- 512 Mibyte to 1 Gibyte (2 Gibyte announced)
  P10xx: 256 to 512 Mibyte (1 Gibyte announced)
- DDR3-800 (400 MHz clock)
  P10xx: DDR3-667 (333 MHz clock)
- Chip select MCS0#, with stacked DDR also MCS1#
- BGA package, 96 balls

3.2.8 I²C bus

All I²C bus devices on the module are connected to the I²C controller IIC1 of the CPU.
Table 13 shows the used addresses.
All devices are designed for a maximum I²C clock frequency of 400 kHz.
The pull-ups available on the module are sufficient for the bus loads on the module.
If required that more devices are connected to the bus, additional pull-ups must be connected in parallel on the baseboard, to achieve sufficient low-high edges.

Table 13: IIC1 device addresses

Device	MSB							LSB
Data EEPROM	1	0	1	0	0 (A2)	0 (A1)	0 (A0)	R/W
Configuration EEPROM SE97B (*)	1	0	1	0	1 (A2)	1 (A1)	1 (A0)	R/W
Configuration EEPROM SE97B Write Protect (*)	0	1	1	0	1 (A2)	1 (A1)	1 (A0)	R/W
Temperature Sensor SE97B (*)	0	0	1	1	1 (A2)	1 (A1)	1 (A0)	R/W
Temperature Sensor SA560004EDP	1	0	0	1	1	0	0	R/W
Real Time Clock DS1337	1	1	0	1	0	0	0	R/W
Power Manager ADM1068	1	0	0	0	1	0 (A1)	0 (A0)	R/W

(*) Combined in one device

3.2.8.1 Data EEPROM

The serial EEPROM can store, e.g., characteristics of the module and customer specific parameter data. In the EEPROM single memory cells can be deleted and be overwritten in contrast to flash. At delivery the EEPROM is erased. It can, e.g. save application parameters permanently.

- 32 Kibyte = 256 Kibit or not assembled
- Is freely available for user's data
- Can be used for boot sequencer when required
- Controlled via I^2C controller IIC1, device address see Table 13

3.2.8.2 Configuration EEPROM

At delivery the configuration-EEPROM contains a standard reset configuration (see 3.2.3.5).

- Combined device SE97B
- 256 bytes = 2 Kibit
- Used for reset configuration
- Update by the CPU is possible
- Temporary or permanent write protection possible
- Controlled via I^2C controller IIC1, device address see Table 13

An altered reset configuration can lead under certain circumstances to an unbootable system. In this case there are several possibilities to get back to a functioning reset configuration:

- It is possible to connect an external master (programming unit) at the I^2C bus.
  The support of TQ-Components can recommend a suitable tool.
- Recovery by module software: It is a prerequisite that the software in the NOR flash on the module runs with the default reset configuration, and that the I^2C bus can be accessed.
  For a "how to" see 3.2.3.5, tip 1.

3.2.8.3 RTC (real time clock)

As the CPU does not contain an internal bufferable RTC, it was connected externally.

- RTC DS1337U, controlled via I²C bus of the CPU
- Battery buffering possible (battery on baseboard at VBAT)
- Alarm outputs INTA# and SQW/INTB# (Open Drain) are routed to a common pin
- Controlled via I²C controller IIC1, device address see Table 13
- 30 ppm oscillator tolerance over the whole temperature range

3.2.8.4 Temperature supervision

- Control of all sensors via I²C controller IIC1, device addresses see Table 13
- Measuring point 1: chip temperature of the CPU by internal measuring diode
  P10xx: availability of the internal diode unclear
  Implemented by remote channel SA560004EDP
- Measuring point 1a (assembly option):
  External sensor alternatively to CPU internal measuring diode, implemented by remote channel SA560004EDP on top side between CPU and switching regulator
- Measuring point 2: PCB bottom side close to DDR3
  Implemented by local channel SA560004EDP
- Measuring point 3: PCB top side between DDR3 devices
  Implemented by combined device SE97B

3.2.9 General-Purpose-I/O

- 16 GPIOs, 9 of it multiplexed with other interface signals
  P1020 16 GPIOs; P1021 no GPIOs
- Configured as input after power-on reset
- Open drain capable
- Interrupt capable

3.3 Supply

3.3.1 Power sequencing

The module is supplied with 3.3 V only. All other voltages are generated on the module.
The integrated power manager ensures valid power sequencing.
For that reason the external supplied 3.3 V are routed via a switch.
To guarantee the correct power sequencing for the variable I/O voltages LVDD and CVDD as well, LVDD and CVDD may not be supplied by an external supply voltage. LVDD and CVDD must be fed via the provided pins VCC3V3OUT, VCC2V5OUT or VCC1V8OUT (see Illustration 7).

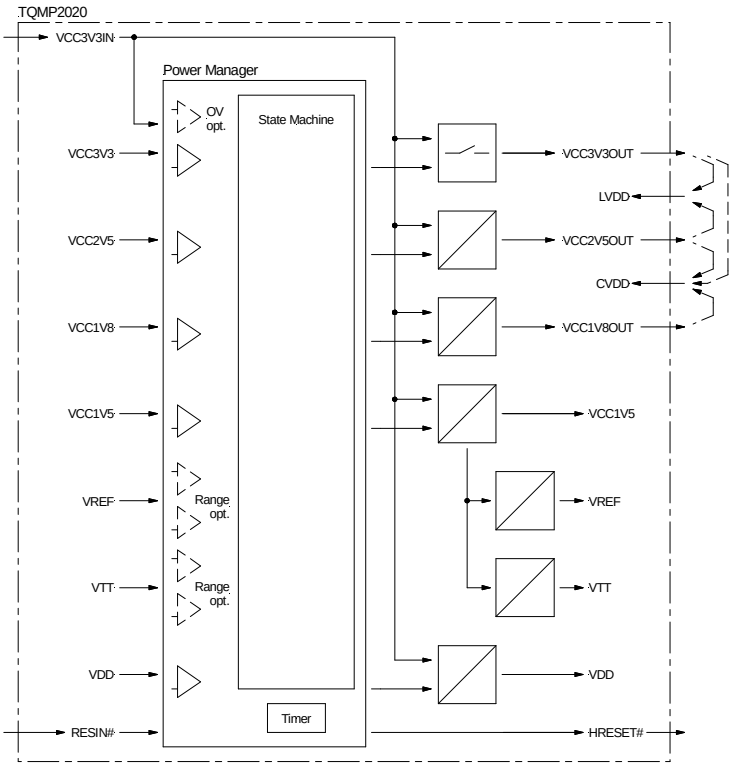

Illustration 7: Supply structure (simplified)

3.3.2 Supply inputs

For the supply voltages to be fed the following limits apply:

3.3.2.1 VCC3V3IN / main supply

Table 14: Requirements for 3.3 V external

VCC3V3IN	3.201 V to 3.465 V (3.3 V –3 % / +5 %)	Determined by voltage range of components and supervisor threshold (see 3.2.2.1)
Ripple max.	30 mV	Peak to peak
Current consumption	5 A	TQMP2020 @ 400 / 1200 / 800 MHz (CCB / Core / DDR3)

3.3.2.2 VBAT / RTC supply

- Supply of the RTC
- Current consumption only, if VBAT >VCC3V3
  (Connection via Schottky diode to VCC3V3 is present on module.)

Table 15: Requirements for VBAT

Voltage VBAT	1.8 V to 5.5 V	Determined by voltage range of RTC (see 3.2.8.3)
Ripple max.	1 %	Peak to peak
Timekeeping current	2 µA	VCC3V3IN = 0 V, Oscillator running

3.3.2.3 LVDD / Ethernet-I/O supply

LVDD is generated by feedback of the voltages VCC3V3OUT or VCC2V5OUT, which are monitored and generated on the module. In this way the necessary specifications are observed automatically.
The driver's configuration LVDD_VSEL is done on the module automatically, based on the supplied voltage, see 3.2.3.3.

3.3.2.4 BVDD / Local Bus supply

BVDD always operates at 3.3 V. BVDD cannot be changed and is not accessible externally.
The driver's configuration BVDD_VSEL[0:1] is done on the module, see 3.2.3.3.

3.3.2.5 CVDD / supply USB, SDHC and SPI

CVDD is generated by feedback of the voltages VCC3V3OUT, VCC2V5OUT or VCC1V8OUT, which are monitored and generated on the module. In this way the necessary specifications are observed automatically.
The driver's configuration CVDD_VSEL[0:1] is done on the module automatically, based on the supplied voltage, see 3.2.3.3.

3.3.3 Supply outputs

3.3.3.1 VCC3V3OUT

VCC3V3OUT exclusively supplies the variable I/O voltages LVDD or CVDD.
An additional load is not permitted.
Voltage: 3.3 V

3.3.3.2 VCC2V5OUT

VCC2V5OUT exclusively supplies the variable I/O voltages LVDD or CVDD.
An additional load is not permitted.
Voltage: 2.5 V

3.3.3.3 VCC1V8OUT

VCC1V8OUT exclusively supplies the variable I/O voltage CVDD.
An additional load is not permitted.
Voltage: 1.8 V

3.4 Interfaces to other systems and devices

3.4.1 Serial interfaces

- Two internal UARTs: UART1 and UART2
- Max. 115,200 baud (limited by driver / level shifter)
- Transceiver for TxD and RxD with RS232compatible levels
- Additionally all signals are also available unbuffered at the module plug connectors
- Default assembly: driver for 2 × RxD and 2 × TxD;
  the control signals RTS and CTS are only available unbuffered

3.4.2 COP/JTAG interface

All signals of the Freescale COP/JTAG interfaces (debugging interface) are made available externally. The COP/JTAG interface encloses the following signals.
(Signal direction seen from the module or Starterkit):

Table 16: Signals COP/JTAG interface

Pin*	Signal name	Type	Function
1	TDO	O	Test Data Output
2	NC	–	–
3	TDI	I	Test Data Input
4	TRST#	I	Test Reset
5	NC	–	–
6	VDD_SENSE	O	Voltage Sense of Debugger (3.3 V, 10 mA max.)
7	TCK	I	Test Clock
8	CKSTP_IN#**	I	Checkstop In
9	TMS	I	Test Mode Select
10	NC	–	–
11	SRESET#	I	Soft Reset
12	NC	–	(Optional Ground)
13	RESIN#	I	Reset In, connects to HRESET# on module
14	(Key pin)	–	–
15	CKSTP_OUT#**		Checkstop Out
16	GND	–	Ground

* on Starterkit STKP2020
** or'ed on the STKP2020, see (1)

The wiring necessary on the baseboard can be taken from the circuit diagram of the STKP2020.

The COP/JTAG interface uses the same signals as the JTAG interface.
A CPLD type LCMXO256C is after the CPU in the JTAG chain on the module.
This information must be passed on to the debugger.

Lauterbach Trace32:
SYStem.CONFIG IRPRE 8
SYStem.CONFIG DRPRE 1

Abatron BDI2000:
SCANSUCC 1 8 ; 1 device with instruction register length 8 for MachXO device

A corresponding setting should also exist at all other usable debuggers.

3.4.3 External bus / other interfaces

The interfaces described here are routed to the plug connectors leading to the baseboard:

2×160 pins + 1×40 pins

3.4.3.1 Treatment of unused pins

The module is designed in such a way, that only a minimum number of signals are required to run the module. Therefore many signals do not need external wiring if their function is not required.

- Pure outputs (type = O):
  no wiring necessary
- Inputs and I/Os with pull-up / pull-down (type = O, I/O, with pull-ups or pull-downs):
  no wiring necessary
- I/Os which can be configured as an output (e.g., GPIO_5):
  it is generally sufficient to configure unused pins as an output during initialisation
- Continuing notes are found in (1)

3.4.3.2 Pinout according to functional groups

The wiring on the module is referred to under "Description".
If necessary notes for the handling on the baseboard are supplied.

Table 17: Pinout according to functional groups

GPIO / DMA / Timer				
Signal	CPU Pin	Type	Description	Module Pin
GPIO_0/IRQ7	R28	I/O	General Purpose I/O 0 / External Interrupt 7	X2-2
GPIO_1/IRQ8	R26	I/O	General Purpose I/O 1 / External Interrupt 8	X2-4
GPIO_2/IRQ9	P29	I/O	General Purpose I/O 2 / External Interrupt 9	X2-6
GPIO_3/IRQ10	N24	I/O	General Purpose I/O 3 / External Interrupt 10	X2-10
GPIO_4/IRQ11	U29	I/O	General Purpose I/O 4 / External Interrupt 11	X2-12
GPIO_5	R24	I/O	General Purpose I/O 5	X2-11
GPIO_6	R29	I/O	General Purpose I/O 6	X2-14
GPIO_7	R25	I/O	General Purpose I/O 7	X2-13
GPIO_8/SDHC_CD#	F22	I/O	General Purpose I/O 8 / eSDHC card detection	X2-16
GPIO_9/SDHC_WP	A24	I/O	General Purpose I/O 9 / eSDHC card write protect	X2-17
GPIO_10/USB_PCTL0	A25	I/O	General Purpose I/O 10 / USB Port control 0	X2-18
GPIO_11/USB_PCTL1	D24	I/O	General Purpose I/O 11 / USB Port control 1	X2-19
GPIO_12	F23	I/O	General Purpose I/O 12	X2-20
GPIO_13	E23	I/O	General Purpose I/O 13	X2-21
GPIO_14	F24	I/O	General Purpose I/O 14	X2-22
GPIO_15	E24	I/O	General Purpose I/O 15	X2-23

USB				
Signal	CPU Pin	Type	Description	Module Pin
USB_NXT	B26	I	USB Next data	X2-41
USB_DIR	A28	I	USB Direction	X2-43
USB_STP	B29	O	USB Stop	X2-44
USB_PWRFAULT	C29	I	USB VBUS power fault	X2-46
USB_CLK	D27	I	USB PHY clock	X2-45
USB_D7	C28	I/O	USB Data 7	X2-55
USB_D6	C25	I/O	USB Data 6	X2-54
USB_D5	B28	I/O	USB Data 5	X2-53
USB_D4	B25	I/O	USB Data 4	X2-52
USB_D3	D26	I/O	USB Data 3	X2-51
USB_D2	A27	I/O	USB Data 2	X2-50
USB_D1	A26	I/O	USB Data 1	X2-49
USB_D0	C26	I/O	USB Data 0	X2-48

Table 17: Pinout according to functional groups (continued)

Power Management				
Signal	CPU Pin	Type	Description	Module Pin
ASLEEP	U25	O	Sleep State, ↑ 4k7 to VCC3V3 on module	X1-82

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Debug / Test				
Signal	CPU Pin	Type	Description	Module Pin
TCK	V29	I	Test Clock, ↑ 4k7 to VCC3V3 on module	X2-102
TDI	T25	I	Test Data In	X2-96
TDO	(V28)	O	CPU Test Data Out via CPLD, see 3.4.2	X2-98
TMS	U26	I	Test Mode Select, ↑ 10k to VCC3V3 on module	X2-100
TRST#	V26	I	Test Reset	X2-104
TRIG_IN	AB28	I	Watchpoint Trigger in, ↓ 4k7 to DGND on module	X2-99
TRIG_OUT/READY _P0/QUIESCE#	U28	O	Watchpoint Trigger Out / Processor 0 ready / quiescent state	X2-101
READY_P1	W26	O	Processor 1 ready	X2-103
MSRCID0	P28	O	Memory Debug Source ID 0	X2-87
MSRCID1	R27	O	Memory Debug Source ID 1	X2-89
MSRCID2	P27	O	Memory Debug Source ID 2	X2-91
MSRCID3	P26	O	Memory Debug Source ID 3	X2-93
MSRCID4	N26	O	Memory Debug Source ID 4	X2-95
MDVAL	M24	O	Memory Debug data valid	X2-88
SCAN_MODE#	W27	I	Scan Mode, ↑ 1k to VCC3V3 on module	X2-92
TEST_SEL#	AA28	I	Test Select P2020, P1020, P1021: ↑ 4k7 to VCC3V3 on module P2010, P1011, P1012: ↓ 1k to DGND on module	X2-94

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

Interrupt Controller / DMA				
Signal	CPU Pin	Type	Description	Module Pin
DMA1_DREQ#	Y28	I	DMA1 request, ↑ 4k7 to VCC3V3 on module	X2-108
DMA2_DREQ0#	W28	I	DMA2 request 0, ↑ 4k7 to VCC3V3 on module	X2-114
DMA1_DACK#	T28	O	DMA1 acknowledge	X2-110
DMA2_DACK0#	T29	O	DMA2 acknowledge 0	X2-116
DMA1_DDONE#	T26	O	DMA1 done	X2-112
DMA2_DDONE0#	Y29	O	DMA2 done 0	X2-118
UDE0#	J27	I	Unconditional debug event 0, ↑ 4k7 to VCC3V3 on module	X2-109
UDE1#	K28	I	Unconditional debug event 1, ↑ 4k7 to VCC3V3 on module	X2-111
MCP0#	AA27	I	Machine check processor 0, ↑ 4k7 to VCC3V3 on module	X2-105
MCP1#	M25	I	Machine check processor 1, ↑ 4k7 to VCC3V3 on module	X2-107
IRQ0#	L24	I	External interrupt 0, ↑ 4k7 to VCC3V3 on module	X2-115
IRQ1#	K26	I	External interrupt 1, ↑ 4k7 to VCC3V3 on module	X2-117
IRQ2#	K29	I	External interrupt 2, ↑ 4k7 to VCC3V3 on module	X2-119
IRQ3#	N25	I	External interrupt 3, ↑ 4k7 to VCC3V3 on module	X2-121
IRQ4#	L26	I	External interrupt 4, ↑ 4k7 to VCC3V3 on module	X2-123
IRQ5#	L29	I	External interrupt 5, ↑ 4k7 to VCC3V3 on module	X2-125
IRQ6#	K27	I	External interrupt 6, ↑ 4k7 to VCC3V3 on module	X2-127
IRQ_OUT#	N29	O	Interrupt output, ↑ 4k7 to VCC3V3 on module	X2-120

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Clocks				
Signal	CPU Pin	Type	Description	Module Pin
CLK_OUT	T24	O	Clock Out, → 22 Ω on module	X2-81
RTC	K24	I	Real time clock	X2-85
DDRCLK	AC9	O	DDR clock, driven on module Do not connect, for test use only	X2-75
SYSCLK	W29	O	System clock, driven on module Do not connect, for test use only	X2-79

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

I²C				
Signal	CPU Pin	Type	Description	Module Pin
IIC1_SDA	H28	I/O	I²C1 Serial data, ↑ 2k4 to VCC3V3 on module	X2-133
IIC1_SCL	G27	I/O	I²C1 Serial clock, ↑ 2k4 to VCC3V3 on module	X2-131
IIC2_SDA	H26	I/O	I²C2 Serial data, ↑ 4k7 to VCC3V3 on module	X2-134
IIC2_SCL	H25	I/O	I²C2 Serial clock, ↑ 4k7 to VCC3V3 on module	X2-132

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Reset				
Signal	CPU Pin	Type	Description	Module Pin
HRESET#	W25	I	Hard reset, driven on module (P2020: input; TQMP2020: output; see Illustration 7)	X2-137
HRESET_REQ#	U24	O	Hard reset request, ↑ 2k2 to VCC3V3 on module, connected to RESIN# via 10k on module	X2-139
SRESET#	W24	I	Soft reset, ↑ 4k7 to VCC3V3 on module	X2-141
CKSTP_IN0#	AA29	I	Checkstop in 0, ↑ 4k7 to VCC3V3 on module	X2-135
CKSTP_IN1#	AB29	I	Checkstop in 1, ↑ 4k7 to VCC3V3 on module	X2-136
CKSTP_OUT0#	V25	O	Checkstop Out 0, ↑ 4k7 to VCC3V3 on module	X2-142
CKSTP_OUT1#	Y27	O	Checkstop Out 1, ↑ 4k7 to VCC3V3 on module	X2-140

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Non-CPU Signals				
Signal	CPU Pin	Type	Description	Module Pin
RTC_INT#	–	O	Real time clock interrupt outputs INTA# and SQW/INTB# (DS1337) connected together, ↑ 10k via Schottky diode to VCC3V3 on module	X2-148
TEMP_OS#	–	O	Temperature sensor alarm outputs EVENT# (SE97B), ALERT# and T_CRIT# (SA56004E) connected together, ↑ 10k to VCC3V3	X2-146
RESIN#	–	I	Reset Input (Reset input of voltage supervisor), ↑ and connection to HRESET_REQ# on module	X2-143
CLKOE	–	I	Internal 66.666 MHz driver enable, ↑ 4k7 to VCC3V3 on module	X2-144
PGOOD	–	O	Power good output, ↓ 22k to DGND on module, use for baseboard power sequencing	X1-158

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

SPI				
Signal	CPU Pin	Type	Description	Module Pin
SPI_MISO	F28	I	SPI Master-in slave-out, ↑, 2 to 10k to CVDD on baseboard if not used	X2-25
SPI_MOSI	F25	I/O	SPI Master-out slave-in, ↑, 2 to 10k to CVDD on baseboard if not used	X2-27
SPI_CS0#/ SDHC_DATA4	D28	I/O	SPI slave select 0 / SDHC data line 4, ↑, 2 to 10k to CVDD on baseboard if not used	X2-26
SPI_CS1#/ SDHC_DATA5	E26	I/O	SPI slave select 1 / SDHC data line 5	X2-28
SPI_CS2#/ SDHC_DATA6	F29	I/O	SPI slave select 2 / SDHC data line 6	X2-30
SPI_CS3#/ SDHC_DATA7	E29	I/O	SPI slave select 3 / SDHC data line 7	X2-32
SPI_CLK	D29	O	SPI clock, ↓, 1k to DGND on baseboard if not used	X2-29

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

ESDHC				
Signal	CPU Pin	Type	Description	Module Pin
SDHC_DATA0	G28	I/O	SDHC data line 0	X2-33
SDHC_DATA1	F27	I/O	SDHC data line 1	X2-35
SDHC_DATA2	G25	I/O	SDHC data line 2	X2-37
SDHC_DATA3	G26	I/O	SDHC data line 3	X2-39
SDHC_CMD	F26	I/O	SDHC CMD line	X2-36
SDHC_CLK	G29	O	SDHC clock	X2-38

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

RS232 (via transceiver)				
Signal	CPU Pin	Type	Description	Module Pin
RS232_SIN0	–	I	UART0 serial in data, RS232 level	X2-147
RS232_SOUT0	–	O	UART0 serial out data, RS232 level	X2-149
RS232_SIN1	–	I	UART1 serial in data, RS232 level	X2-150
RS232_SOUT1	–	O	UART1 serial out data, RS232 level	X2-152

UARTs				
Signal	CPU Pin	Type	Description	Module Pin
UART_SIN0	H29	I	UART0 serial in data, LVTTL level, ↑ 10k to VCC3V3 on module if RS232 transceiver is not assembled Do not connect if RS232 transceiver on module is used	X2-151
UART_SOUT0	J26	O	UART0 serial out data, LVTTL level	X2-153
UART_CTS0#	J28	I	UART0 clear to send, LVTTL level, ↑ 10k to VCC3V3 on module	X2-157
UART_RTS0#	J29	O	UART0 request to send, LVTTL level	X2-155
UART_SIN1	G24	I	UART1 serial in data, LVTTL level, ↑ 10k to VCC3V3 on module if RS232 transceiver is not assembled Do not connect if RS232 transceiver on module is used	X2-159
UART_SOUT1	J25	O	UART1 serial out data, LVTTL level	X2-160
UART_CTS1#	H24	I	UART1 clear to send, LVTTL level, ↑ 10k to VCC3V3 on module	X2-156
UART_RTS1#	J24	O	UART1 request to send, LVTTL level	X2-158

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

Local Bus				
Signal	CPU Pin	Type	Description	Module Pin
LAD0	B18	I/O	Local Bus address / data 0	X2-60
LAD1	E20	I/O	Local Bus address / data 1	X2-62
LAD2	A19	I/O	Local Bus address / data 2	X2-64
LAD3	B20	I/O	Local Bus address / data 3	X2-66
LAD4	D19	I/O	Local Bus address / data 4	X2-68
LAD5	A18	I/O	Local Bus address / data 5	X2-70
LAD6	B17	I/O	Local Bus address / data 6	X2-69
LAD7	C20	I/O	Local Bus address / data 7	X2-71
LAD8	F19	I/O	Local Bus address / data 8	X3-14
LAD9	E10	I/O	Local Bus address / data 9	X3-16
LAD10	B16	I/O	Local Bus address / data 10	X3-18
LAD11	D14	I/O	Local Bus address / data 11	X3-20
LAD12	D17	I/O	Local Bus address / data 12	X3-22
LAD13	E11	I/O	Local Bus address / data 13	X3-24
LAD14	A16	I/O	Local Bus address / data 14	X3-26
LAD15	C15	I/O	Local Bus address / data 15	X3-30
LDP0	E18	I/O	Local Bus data parity 0, ↑ 4k7 to VCC3V3 on module	X3-8
LDP1	B19	I/O	Local Bus data parity 1, ↑ 4k7 to VCC3V3 on module	X3-10
LA16	B21	O	Local Bus burst address 16	X3-32
LA17	A22	O	Local Bus burst address 17	X3-34
LA18	C21	O	Local Bus burst address 18	X3-36
LA19	F21	O	Local Bus burst address 19	X3-38
LA20	E12	O	Local Bus burst address 20	X3-40
LA21	A21	O	Local Bus burst address 21	X3-31
LA22	D11	O	Local Bus burst address 22	X3-29
LA23	E22	O	Local Bus burst address 23	X3-27
LA24	F20	O	Local Bus burst address 24	X2-73
LA25	E21	O	Local Bus burst address 25	X2-74
LA26	B22	O	Local Bus burst address 26	X2-76
LA27	F18	O	Local Bus burst address 27	X2-78
LA28	A23	O	Local Bus burst address 28	X2-80
LA29	B23	O	Local Bus burst address 29	X2-82
LA30	C23	O	Local Bus burst address 30	X2-84
LA31	D23	O	Local Bus burst address 31	X2-86

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

Local Bus (continued)				
Signal	CPU Pin	Type	Description	Module Pin
LCS0#/CS_NOR#	D20	O	Local Bus chip select 0, Used internally for NOR flash, ↑ 4k7 to VCC3V3 on module	X3-15
LCS1#	A12	O	Local Bus chip select 1, ↑ 4k7 to VCC3V3 on module	X3-17
LCS2#	E19	O	Local Bus chip select 2, ↑ 4k7 to VCC3V3 on module	X3-21
LCS3#	D21	O	Local Bus chip select 3, ↑ 4k7 to VCC3V3 on module	X3-23
LCS4#	F11	O	Local Bus chip select 4, ↑ 4k7 to VCC3V3 on module	X3-25
LCS5#/DMA2_DREQ1#	D15	I/O	Local Bus chip select 5 / DMA2 request 1, ↑ 4k7 to VCC3V3 on module	X3-4
LCS6#/DMA2_DACK1#	D13	O	Local Bus chip select 6 / DMA2 acknowledge 1, ↑ 4k7 to VCC3V3 on module	X3-6
LCS7#/DMA2_DDONE1#	A17	O	Local Bus chip select 7 / DMA2 done 1, ↑ 4k7 to VCC3V3 on module	X2-59
LWE0#/LFWE#/LBS0#	F12	O	Local Bus write enable 0 / NAND flash write enable / byte (lane) select 0	X2-57
LWE1#/LBS1#	D12	O	Local Bus write enable 1 / byte (lane) select 1	X3-2
LBCTL	E17	O	Local Bus data buffer control	X2-67
LALE	C17	O	Local Bus address latch enable Signal integrity and timing is critical - do not connect if not used on baseboard. If used, keep as short as possible and observe length constraints with respect to LAD[0:15]	X2-65
LGPL0/LFCLE	B12	O	Local Bus UPM general purpose line 0 / NAND flash command latch enable	X3-5
LGPL1/LFALE	C13	O	Local Bus GP line 1 / NAND flash address latch enable	X3-7
LGPL2/LFRE#/LOE#	A20	O	Local Bus GP line 2 / NAND flash read enable / output enable	X3-9
LGPL3/LFWP#	D10	O	Local Bus GP line 3 / NAND flash write protect	X3-11
LGPL4/LGTA#/LFRB/ LUPWAIT/LPBSE	B13	I/O	Local Bus GP line 4 / transaction termination / NAND flash ready-busy / wait / parity byte select, ↑ 4k7 to VCC3V3 on module	X2-61
LGPL5	C19	O	Local Bus GP line 5	X3-13
LCLK0	B15	O	Local Bus clock 0, → 22 Ω on module	X2-58
LCLK1	A15	O	Local Bus clock 1, → 22 Ω on module	X3-33
LSYNC_IN	A13	I	Local Bus PLL synchronization in, → 22 Ω on module, ↑ 4k7 to VCC3V3 on module	X3-37
LSYNC_OUT	A14	O	Local Bus PLL synchronization out, → 22 Ω on module	X3-39

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

(e)TSECs / IEEE1588				
Signal	CPU Pin	Type	Description	Module Pin
TSEC_1588_CLK_IN	AG21	I	IEEE1588 clock in, ↑ 10k to LVDD on module	X1-69
TSEC_1588_TRIG_IN1	AH20	I	IEEE1588 trigger in 1, ↑ 10k to LVDD on module	X1-71
TSEC_1588_TRIG_IN2	AG20	I	IEEE1588 trigger in 2, ↑ 10k to LVDD on module	X1-73
TSEC_1588_ALARM_OUT1	AE20	O	IEEE1588 alarm out 1	X1-77
TSEC_1588_ALARM_OUT2	AJ20	O	IEEE1588 alarm out 2	X1-79
TSEC_1588_CLK_OUT	AG22	O	IEEE1588 clock out	X1-70
TSEC_1588_PULSE_OUT1	AH21	O	IEEE1588 pulse out 1	X1-72
TSEC_1588_PULSE_OUT2	AJ22	O	IEEE1588 pulse out 2	X1-74
EC_MDC	AD20	O	Ethernet management data clock	X1-76
EC_MDIO	AJ21	I/O	Ethernet management data in / out, ↑ 10k to LVDD on module	X1-78
EC_GTX_CLK125	AF24	I	eTSEC Gigabit reference clock, ↓ 10k to DGND on module	X1-80
TSEC1_TXD7/TSEC3_TXD3	AF22	O	eTSEC1 transmit data 7 / eTSEC3 transmit data 3	X1-53
TSEC1_TXD6/TSEC3_TXD2	AD22	O	eTSEC1 transmit data 6 / eTSEC3 transmit data 2	X1-51
TSEC1_TXD5/TSEC3_TXD1	AD23	O	eTSEC1 transmit data 5 / eTSEC3 transmit data 1	X1-49
TSEC1_TXD4/TSEC3_TXD0	AE21	O	eTSEC1 transmit data 4 / eTSEC3 transmit data 0	X1-47
TSEC1_TXD3	AJ25	O	eTSEC1 transmit data 3	X1-45
TSEC1_TXD2	AH28	O	eTSEC1 transmit data 2	X1-41
TSEC1_TXD1	AE25	O	eTSEC1 transmit data 1	X1-39
TSEC1_TXD0	AD24	O	eTSEC1 transmit data 0	X1-37
TSEC1_TX_EN	AH24	O	eTSEC1 transmit enable, ↓ 10k to DGND on module	X1-55
TSEC1_TX_ER	AF23	O	eTSEC1 transmit error	X1-57
TSEC1_TX_CLK	AJ24	I	eTSEC1 transmit clock in, ↑ 10k to LVDD on module	X1-61
TSEC1_GTX_CLK	AG25	O	eTSEC1 transmit clock out	X1-63
TSEC1_CRS/TSEC3_RX_DV	AJ27	I/O	eTSEC1 carrier sense / eTSEC3 receive data valid, ↑ 10k to LVDD on module	X1-65
TSEC1_COL/TSEC3_RX_CLK	AH26	I	eTSEC1 collision detect / eTSEC3 receive clock, ↑ 10k to LVDD on module	X1-67
TSEC1_RXD7/TSEC3_RXD3	AG23	I	eTSEC1 receive data 7 / eTSEC3 receive data 3, ↑ 10k to LVDD on module	X1-29
TSEC1_RXD6/TSEC3_RXD2	AH22	I	eTSEC1 receive data 6 / eTSEC3 receive data 2, ↑ 10k to LVDD on module	X1-25
TSEC1_RXD5/TSEC3_RXD1	AJ23	I	eTSEC1 receive data 5 / eTSEC3 receive data 1, ↑ 10k to LVDD on module	X1-23
TSEC1_RXD4/TSEC3_RXD0	AE24	I	eTSEC1 receive data 4 / eTSEC3 receive data 0, ↑ 10k to LVDD on module	X1-21

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

(e)TSECs / IEEE1588 (continued)				
Signal	CPU Pin	Type	Description	Module Pin
TSEC1_RXD3	AJ28	I	eTSEC1 receive data 3, ↑ 10k to LVDD on module	X1-19
TSEC1_RXD2	AE22	I	eTSEC1 receive data 2, ↑ 10k to LVDD on module	X1-17
TSEC1_RXD1	AD21	I	eTSEC1 receive data 1, ↑ 10k to LVDD on module	X1-15
TSEC1_RXD0	AH25	I	eTSEC1 receive data 0, ↑ 10k to LVDD on module	X1-13
TSEC1_RX_DV	AJ26	I	eTSEC1 receive data valid, ↑ 10k to LVDD on module	X1-31
TSEC1_RX_ER	AH23	I	eTSEC1 receive error, ↑ 10k to LVDD on module	X1-33
TSEC1_RX_CLK	AG26	I	eTSEC1 receive clock, ↑ 10k to LVDD on module	X1-35
TSEC2_TXD7	AE26	O	eTSEC2 transmit data 7	X1-54
TSEC2_TXD6	AF26	O	eTSEC2 transmit data 6	X1-50
TSEC2_TXD5/TSEC3_TX_EN	AB24	O	eTSEC2 transmit data 5 / eTSEC3 transmit enable, ↓ 10k to DGND on module	X1-48
TSEC2_TXD4/ TSEC3_GTX_CLK	AB25	O	eTSEC2 transmit data 4 / eTSEC3 transmit clock out	X1-46
TSEC2_TXD3	AG29	O	eTSEC2 transmit data 3	X1-44
TSEC2_TXD2	AA25	O	eTSEC2 transmit data 2	X1-42
TSEC2_TXD1	AF27	O	eTSEC2 transmit data 1	X1-40
TSEC2_TXD0	Y24	O	eTSEC2 transmit data 0	X1-38
TSEC2_TX_EN	AA26	O	eTSEC2 transmit enable, ↓ 10k to DGND on module	X1-56
TSEC2_TX_ER	AE29	O	eTSEC2 transmit error	X1-58
TSEC2_TX_CLK	AA24	I	eTSEC2 transmit clock in, ↑ 10k to LVDD on module	X1-60
TSEC2_GTX_CLK	AG28	O	eTSEC2 transmit clock out	X1-62
TSEC2_CRS/TSEC3_RX_ER	AD25	I/O	eTSEC2 carrier sense / eTSEC3 receive error, ↑ 10k to LVDD on module	X1-64
TSEC2_COL/TSEC3_TX_CLK	AE27	I	eTSEC2 collision detect / eTSEC3 transmit clock in, ↑ 10k to LVDD on module	X1-66
TSEC2_RXD7	AD27	I	eTSEC2 receive data 7, ↑ 10k to LVDD on module	X1-28
TSEC2_RXD6	AB26	I	eTSEC2 receive data 6, ↑ 10k to LVDD on module	X1-26
TSEC2_RXD5	AC26	I	eTSEC2 receive data 5, ↑ 10k to LVDD on module	X1-24
TSEC2_RXD4	AD26	I	eTSEC2 receive data 4, ↑ 10k to LVDD on module	X1-22
TSEC2_RXD3	AB27	I	eTSEC2 receive data 3, ↑ 10k to LVDD on module	X1-18
TSEC2_RXD2	AD28	I	eTSEC2 receive data 2, ↑ 10k to LVDD on module	X1-16
TSEC2_RXD1	AF29	I	eTSEC2 receive data 1, ↑ 10k to LVDD on module	X1-14
TSEC2_RXD0	AF28	I	eTSEC2 receive data 0, ↑ 10k to LVDD on module	X1-12
TSEC2_RX_DV	AD29	I	eTSEC2 receive data valid, ↑ 10k to LVDD on module	X1-30
TSEC2_RX_ER	AE28	I	eTSEC2 receive error, ↑ 10k to LVDD on module	X1-32
TSEC2_RX_CLK	AC29	I	eTSEC2 receive clock, ↑ 10k to LVDD on module	X1-34

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

SERDES				
Signal	CPU Pin	Type	Description	Module Pin
SD_TX3	AD18	O	SERDES transmit data 3	X1-89
SD_TX3#	AE18	O	SERDES transmit data 3 complement	X1-91
SD_TX2	AE17	O	SERDES transmit data 2	X1-97
SD_TX2#	AF17	O	SERDES transmit data 2 complement	X1-99
SD_TX1	AE13	O	SERDES transmit data 1	X1-105
SD_TX1#	AF13	O	SERDES transmit data 1 complement	X1-107
SD_TX0	AD12	O	SERDES transmit data 0	X1-113
SD_TX0#	AE12	O	SERDES transmit data 0 complement	X1-115
SD_RX3	AH18	I	SERDES receive data 3	X1-94
SD_RX3#	AJ18	I	SERDES receive data 3 complement	X1-96
SD_RX2	AH16	I	SERDES receive data 2	X1-102
SD_RX2#	AJ16	I	SERDES receive data 2 complement	X1-104
SD_RX1	AH14	I	SERDES receive data 1	X1-110
SD_RX1#	AJ14	I	SERDES receive data 1 complement	X1-112
SD_RX0	AH12	I	SERDES receive data 0	X1-118
SD_RX0#	AJ12	I	SERDES receive data 0 complement	X1-120
SD_REF_CLK	AG15	I	SERDES PLL reference clock	X1-86
SD_REF_CLK#	AF15	I	SERDES PLL reference clock complement	X1-88

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 17: Pinout according to functional groups (continued)

Module supply				
Signal	Pin Count	Type	Description	Module Pin
VCC3V3IN	2	Supply	3.3 V supply input	See below
	X1-6, X1-8			
VCC3V3IN	8	Supply	3.3 V supply input	See below
	X1-1, X1-2, X1-3, X1-4, X1-5, X1-7, X1-9, X1-11			
VBAT	1	Supply	Battery Voltage, connected directly to RTC supply pin and or'ed with VCC3V3 via Schottky diode.	X1-10
LVDD	1	Supply	eTSEC, IEEE1588 and Ethernet Management I/O supply voltage Connect to either VCC3V3OUT or VCC2V5OUT, depending on Physical Interface Mode; LVDD_VSEL will be set automatically depending on LVDD voltage.	X2-5
CVDD	1	Supply	USB, eSDHC and eSPI I/O supply voltage Connect to VCC3V3OUT, VCC2V5OUT or VCC1V8OUT, depending on desired I/O voltage; CVDD_VSEL[0:1] will be set automatically depending on CVDD voltage.	X2-3
VCC3V3OUT	1	Supply	3.3 V supply output after power sequencing switch Use for LVDD and/or CVDD supply only!	X2-1
VCC2V5OUT	1	Supply	2.5 V supply output Use for LVDD and/or CVDD supply only!	X2-7
VCC1V8OUT	1	Supply	1.8 V supply output Use for CVDD supply only!	X2-9
DGND	71	Supply	(Digital) Ground For best signal integrity of high-speed lanes connect all of them to baseboard ground plane.	see below
	X1-20, X1-27, X1-36, X1-43, X1-52, X1-59, X1-68, X1-75, X1-84, X1-85, X1-87, X1-90, X1-92, X1-93, X1-95, X1-98, X1-100, X1-101, X1-103, X1-106, X1-108, X1-109, X1-111, X1-114, X1-116, X1-117, X1-119, X1-122, X1-124, X1-125, X1-127, X1-130, X1-132, X1-133, X1-135, X1-138, X1-140, X1-141, X1-143, X1-146, X1-148, X1-149, X1-151, X1-154, X1-156, X1-157			
	X2-8, X2-15, X2-24, X2-31, X2-40, X2-47, X2-56, X2-63, X2-72, X2-77, X2-83, X2-90, X2-97, X2-106, X2-113, X2-122, X2-129, X2-138, X2-145, X2-154			
	X3-3, X3-12, X3-19, X3-28, X3-35			

Table 17: Pinout according to functional groups (continued)

Reserved				
Signal	CPU Pin	Type	Description	Module Pin
RSVD4080/SD_3	–	I	Reserved input 3, connect to ground	X1-150
RSVD4080/SD_3#	–	I	Reserved input 3 complement, connect to ground	X1-152
RSVD4080/SD_2	–	I	Reserved input 2, connect to ground	X1-142
RSVD4080/SD_2#	–	I	Reserved input 2 complement, connect to ground	X1-144
RSVD4080/SD_1	–	O	Reserved output 1, do not connect	X1-153
RSVD4080/SD_1#	–	O	Reserved output 1 complement, do not connect	X1-155
RSVD4080/SD_0	–	O	Reserved output 0, do not connect	X1-145
RSVD4080/SD_0#	–	O	Reserved output 0 complement, do not connect	X1-147
RSVD1022/SD2_TX1	–	O	Reserved SERDES2 transmit data 1, do not connect	X1-129
RSVD1022/SD2_TX1#	–	O	Reserved SERDES2 transmit data 1 complement, do not connect	X1-131
RSVD1022/SD2_TX0	–	O	Reserved SERDES2 transmit data 0, do not connect	X1-137
RSVD1022/SD2_TX0#	–	O	Reserved SERDES2 transmit data 0 complement, do not connect	X1-139
RSVD1022/SD2_RX1	–	I	Reserved SERDES2 receive data 1, connect to ground	X1-126
RSVD1022/SD2_RX1#	–	I	Reserved SERDES2 receive data 1 complement, connect to ground	X1-128
RSVD1022/SD2_RX0	–	I	Reserved SERDES2 receive data 0, connect to ground	X1-134
RSVD1022/SD2_RX0#	–	I	Reserved SERDES2 receive data 0 complement, connect to ground	X1-136
RSVD1022/SD2_REF_CLK	–	I	Reserved SERDES PLL reference clock, connect to ground	X1-121
RSVD1022/SD2_REF_CLK#	–	I	Reserved SERDES PLL reference clock complement, connect to ground	X1-123
RSVD4080/EMI2_MDC	–	O	Reserved Ethernet management clock 2, do not connect	X1-81
RSVD4080/EMI2_MDIO	–	I/O	Reserved Ethernet management data in / out 2, do not connect	X1-83
RSVD1022/POWER_OK/ GPIO3_19	–	I/O	Reserved power ok, do not connect	X1-159
RSVD1022/POWER_EN	–	O	Reserved power enable, do not connect	X1-160
RSVD1022/SDHC_CD/ GPIO1_28	–	I/O	Reserved eSDHC card detection, do not connect	X2-34
RSVD1022/SDHC_WP/ GPIO1_29	–	I/O	Reserved eSDHC card write protect, do not connect	X2-42
RSVD1022/IRQ7	–	I	Reserved external interrupt 7, do not connect	X2-124
RSVD1022/IRQ8	–	I	Reserved external interrupt 8, do not connect	X2-126
RSVD1022/IRQ9	–	I	Reserved external interrupt 9, do not connect	X2-128
RSVD1022/IRQ10	–	I	Reserved external interrupt 10, do not connect	X2-130
RSVD1022/IRQ11	–	I	Reserved external interrupt 11, do not connect	X3-1

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

3.5 Cooling

3.5.1 Power dissipation

The maximum power dissipation at 400 / 1200 / 800 MHz CCB / Core / DDR is 16 W, cf. 3.3.2.1.
This value applies to the design of the supply and includes short-term peak loads.

The thermal design power at 400 / 1200 / 800 MHz CCB / Core / DDR is 12 W.
This value applies to the design of the cooling. Because of the thermal inertia of the system, a lower power loss is valued in average.

3.5.2 Heat sink

The Starterkit STKP2020 shows a cooling solution with active cooling (fan) which is sufficient for many applications. Regardless of the shown solution, the cooling solution has to be adapted to each specific case. (Clock frequency, stack height, available airflow etc.).

	The operation without heat sink, is also temporarily prohibited! This also applies to laboratory use and operation at room temperature!

3.6 Mechanics

3.6.1 General information

- Double-sided SMD component placement
- High pin count SMD plug connectors with 0.8 mm pitch
- Mating plugs with different heights enable customisation of the stacks heights to the component placement of the base board

	The RF suitability of the module plug connectors was verified with the stack height 5 mm. The results indicate however that sufficient reserves are available to use higher plug connectors for the given data rates of up to 3.125 Gbit/s (6 mm, possibly even 7 mm).

3.6.2 Notes of treatment

To avoid damages caused by mechanical stress, the TQMP2020 may only be extracted from the baseboard by using the extraction tool MOZIP2020. It can also be obtained separately.

3.6.3 Dimensions

- Board dimensions 74 × 54 mm² (Illustration 9)
- Stack height see Table 18

Table 18: Stack heights, overview

Expansion stage DDR SDRAM	Stack height without heat sink max. a + b + c	Free stack height under module min. a – d
All	10.3 mm	3.0 mm

2.5 mm should be kept free on the baseboard, along the longitudinal edges on both sides of the module for the extraction tool MOZIP2020, respective the universal mount TQMP2020 -HAL1.

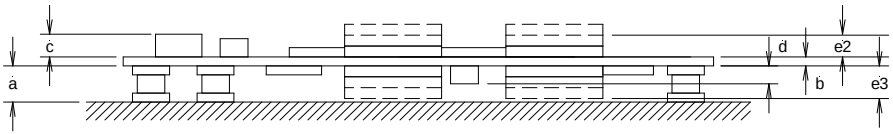

Illustration 8: Stack heights (not to scale)

Table 19: Stack heights, detailed

Dim.	Value [mm]	Remark
a	5.0 ±0.2	Combination module connector with mating plug; 6, 7 and 8 mm are also possible with different connectors on baseboard
b	2.0 ±0.1	PC-board
c	3.0 +0 / –x	Coil L2 (highest stack height top side)
d	1.6 ±0.2	Ferrite L8 (highest stack height bottom side)
f	2.46 +0 / –0.46	CPU (top side, not drawn)

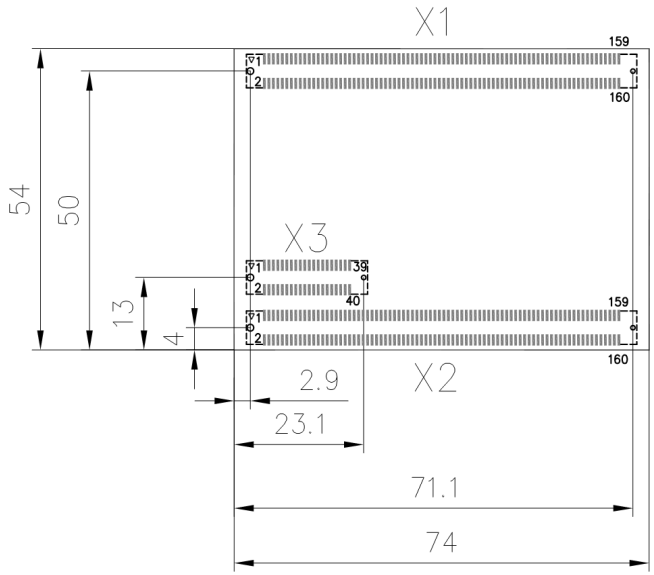

Illustration 9: Overall dimensions (top view through board)

3.7 Boot loader

The boot loader U-Boot is the basic software delivered with the TQMP2020.
More information can be found in the Support Wiki for the TQMP2020.

4. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

4.1 EMC

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board; Contacting of all DGND pins of the module.
- With metal casings, a good (at least according to RF) connection of the PCB ground to the housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding; do not route tracks via separating trenches
- Filtering of all signals which can be connected externally (also "slow" and DC can radiate RF indirectly) this also applies for the power supply

4.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the baseboard, no special preventive measures were planned on the TQMP2020. According to the data sheets, the used devices already have some protection; however, this is generally not sufficient to meet the legal requirements without any further measures.
Following measures are recommended for a baseboard:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, in certain circumstances Zener diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays) with the smallest possible capacity

5. CLIMATIC AND OPERATIONAL CONDITIONS

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection), hence, no fixed value can be given for the whole assembly. In general, a reliable operation is given when following conditions are met:

- Standard temperature range
  Chip temperature of CPU: 0 °C to +125 °C
  Package temperature of the DDR3 SDRAMs: 0 °C to +95 °C
  Package temperature of the remaining ICs: 0 °C to +70 °C
- Extended temperature range
  Chip temperature of CPU: –40 °C to +125 °C
  Package temperature of the DDR3 SDRAMs: –40 °C to +95 °C
  Package temperature of the remaining ICs: –40 °C to +85 °C

Detailed information to the thermal characteristics of the CPU can be found in (1).
Information about example configurations with active and passive cooling can be obtained from the TQ-Components support.

As an embedded module, it is not protected against dust, external impact and contact (IP00). An adequate protection has to be guaranteed by the surrounding system.

5.1 Reliability and service life

The module is designed for a typical service life of 10 years.
It was designed to be insensitive to vibration and impact.

5.2 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at present there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes.
Tests or certifications regarding this were not carried out.

5.3 RoHS compliance

The TQMP2020 is manufactured RoHS compliant.
TQ-Components GmbH issues the RoHS conformity declaration.

6. APPENDIX

6.1 References

Table 20: Further applicable documents

No.	Name	Date	Company
(1)	P2020 QorIQ Integrated Processor Hardware Specifications	04/2011 Rev. 0	Freescale
(2)	P1020 QorIQ Integrated Processor Hardware Specifications Product Preview / Preliminary, Freescale Confidential Proprietary P1020EC	05/2010 Rev. H Draft	Freescale
(3)	P1021 QorIQ Integrated Processor Hardware Specifications Product Preview / Preliminary, Freescale Confidential Proprietary P1021EC	05/2010 Rev. H Draft	Freescale
(4)	P1022/13 QorIQ Integrated Processor Hardware Specifications Preliminary, Freescale Confidential Proprietary	12/2009 Rev .D	Freescale
(5)	P2020 QorIQ Integrated Processor Reference Manual P2020RM	03/2011 Rev. 1	Freescale

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
info@tq-group.com I www.tq-group.com

Technology in Quality