

PALMiCE FPGA

User's Manual (Forth edition)

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Chapter 1

Introduction

1.1 Introduction

The PALMiCE FPGA is a emulator that makes it possible to debug applications based on Xilinx large-scale FPGA devices. It consists of the PALMiCE unit and original debugger CSIDE.

The PALMiCE unit has a palm-sized body and requires no power supply (supports Vbus). The use of the USB as an interface with a host provides excellent portability, permitting to perform debugging anywhere by carrying PALMiCE with the notebook computer.

Its main features are as follows.

- Analyzer monitor signal registration and automatic wiring can be performed from the HDL source window (Probing function)
- Display of the values of arbitrary signals from the FPGA internal circuits in the HDL source window (Quick inspection function)
- Implements all functions without using FPGA internal resources (slice/block RAM).
- Displays the block RAM content
- 16-channel state analyzer function
- Supports JTAG chain devices
- High-speed processing support for FPGA configuration (one million gates in a mere 1.8 seconds)
- Supports various devices
- Usable as a simple logic analyzer
- Has a palm-sized, light and compact body
- Enables latest CSIDE to be downloaded from the Internet (Only for the registered users.)

Note The user logic is stopped by a shutdown operation when accessing the FPGA internal signals.

This manual describes the set-up and the connections for PALMiCE FPGA.

The PALMiCE FPGA is available as the FPGA380 model, which uses a 38-pin connector (MICTOR connector) for connection to the target system.

Before using your PALMiCE FPGA, first read this chapter.

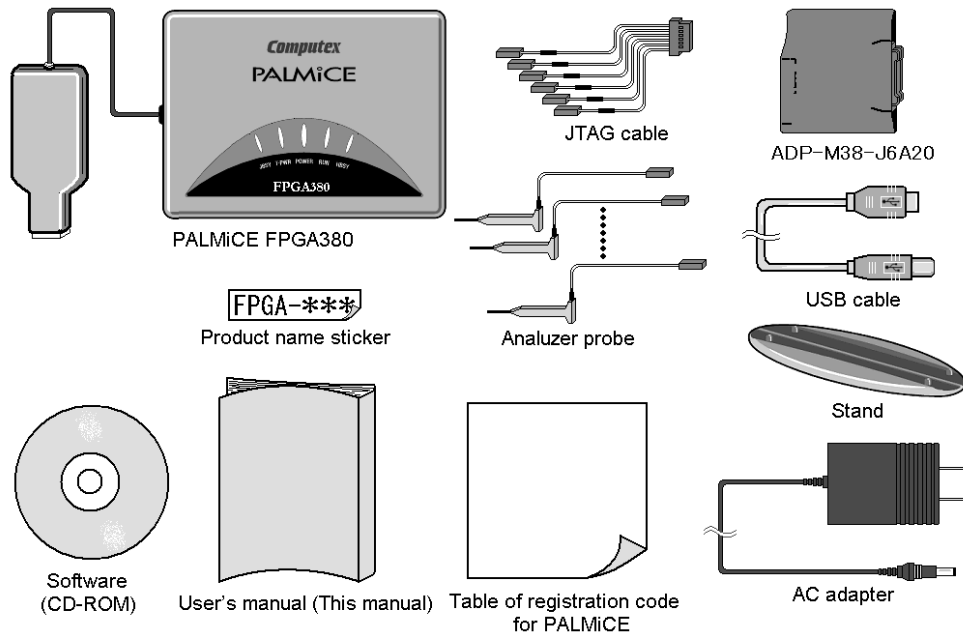
If a connector has already been prepared in the target system, you can prepare to use CSIDE by reading “**Chapter 3 Setting PALMiCE**” and “**Chapter 4 Setting CSIDE**”.

Refer to “**Chapter 6 Troubleshooting**” if CSIDE cannot be started. (If either CSIDE cannot recognize PALMiCE or CSIDE starts up but does not correctly recognize the FPGA in the target system.)

1.2 Product structure

The product structure of PALMiCE is as follows.

● PALMiCE FPGA380	1
● Software(CD-ROM)	1
● PALMiCE FPGA User's manual (This manual)	1
● Table of registration code for PALMiCE	1
● AC adapter	1
● USB cable(2m)	1
● ADP-M38-J6A20 (38pins →6pins/20pins)	1
● JTAG cable (6pins 15cm)	1
● Analyzer probe	20
● Stand	1
● Product name sticker	1



1.3 Requirements

Requirements for using PALMiCE are as follows.

Minimum requirements

Device	Condition
Host PC	IBM PC/AT compatibles
CPU	Pentium 166MHz or more
Installed memory	64Mbytes or more
Hard disk	Free space of 50Mbytes or more
USB	USB1.1 compliant

Recommended requirements

Device	Condition
Host PC	IBM PC/AT compatibles
CPU	Pentium III 667MHz
Installed memory	256Mbytes
OS	Windows2000 Professional
USB	USB1.1 compliant

USB devices are classified into either a “high-powered device” or a “low-powered device” according to the necessary power supply capacity.

A low-powered device requires the power supply of 100mA or less while a high-powered device requires the power supply of 500mA or less.

PALMiCE is a high-powered device.

It does not operate with the USB hub which supports only a low-powered device.

For example, some USB hubs attached to the USB keyboard support only a low-powered device, with which PALMiCE is disabled to operate. To ensure a type of your hub, see the manual for the used PC or that for the USB hub.

Supported OS

OS (English)	Note
Windows 98SE/Me	Internet Explorer4.01 or above
Windows 2000 Professional Windows XP Professional/Home Edition	Intel version only supported

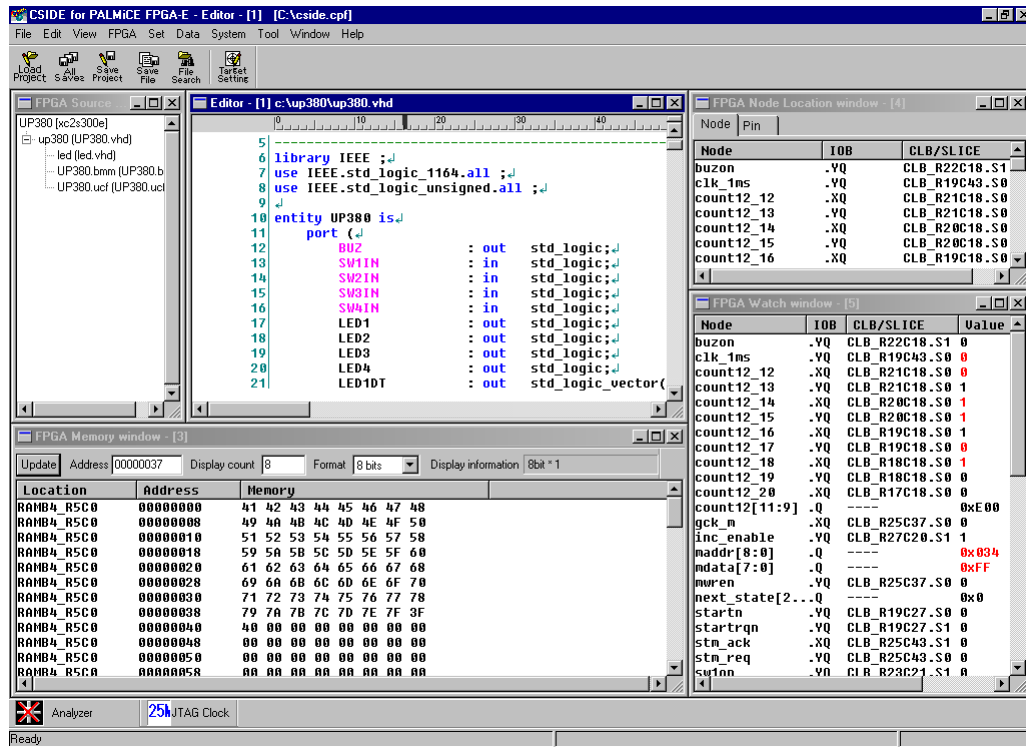
The operation with WindowsNT and Windows 95 are not guaranteed.

An error message, such as “The entry point is not found,” is indicated and CSIDE does not start up, if Internet Explorer 4.01 or above has not been installed.

For the latest information on the supported OS, see our homepage or README.TXT of CSIDE.

1.4 CSIDE

CSIDE is provided on CD-ROM. It contains its main unit and the interface driver. A CSIDE operation manual is provided online. The online manual is created in HTML so that it can be browsed with a HTML browser (such as Internet Explorer).

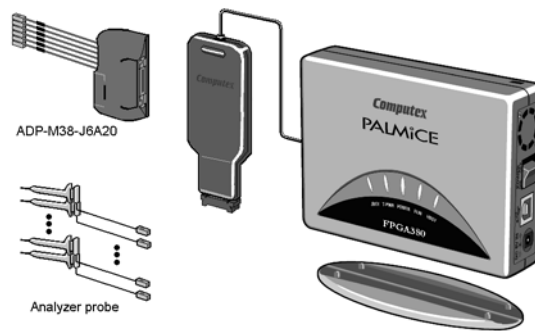


1.5 Product specifications

1.5.1 PALMiCE

The PALMiCE unit is provided with the USB port and the MICTOR connector to connect with the PC and with the target system.

For the MICTOR connector, see “**Chapter 2 Hardware specifications for PALMiCE FPGA**”.



1.5.2 Functions

Devices supported		Xilinx Spartan- II ,Spartan- II E,Spartan-3 Virtex,Virtex-E,Virtex- II , Virtex- II Pro *1
The place and route tools supported		Xilinx ISE5.x, ISE6.1i, ISE6.2i *2
Language supported		VHDL, Verilog
Target I/F	Specification	JTAG I/F
	Connector	38 pins MICTOR connector *3
	Voltage	Auto trace (bet, 2.3V and 3.6V)
	JTAG clock	150KHz, 1MHz, 5MHz, 10MHz pr 25MHz
Reference function		All internal nodes, sampling of block RAM contents *4
Chain devices supported		Up to 20 (The sum of the JTAG instruction lengths must be no more than 128 bits.)
Linkage function		Starts ISE in the background and synthesizes circuits.
Probing function		Automatically routes FPGA internal nodes to FPGA pins.
State analyzer fuction *5		• Capacity - External synchronous mode : 256K cycles - Internal asynchronous mode : 512K cycles • Sampling clock - External synchronous mode: MAX 100MHz - Internal asynchronous mode :200MHz to 2KHz • Trigger specification - AND specification of signal • Trigger position 5 positions between START and END • Channel 16 channels MAX • Time stamp function 16bits clock 10nS, 100nS, 1uS or1mS
Others		FPGA configuration

*1 Processor is not supported.

*2 ISE WebPack is not supported. Certain functions are restricted if the Synplicity Synplify logic synthesis tool is used instead of the Xilinx XST tool for logic synthesis.

*3 Usable even with the already developed target using the flying lead cable or the clip connection method.

*4 The FPGA is stopped (shut down) when the readback function is used.

*5 Usable also as a simple logic analyzer when not connecting with FPGA.

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Chapter 2 Hardware specifications for PALMiCE FPGA

2.1 Part names and functions

2.1.1 General specifications

Item	Specifications
I/F	Connector in the target system :MICTOR 2-767004-2, 767054-1 or 767061 of AMP make
LED	- POWER (Green) · T-PWR (Red) - RUN (Green) · JBSY (Orange) · HBSY (Orange)
Outside dimension	106mm(W) × 78mm(D) × 29.5mm(H) Except the connector
Usage environment	- Operating temperature :5°C to 40°C - operating humidity :35% to 85%RH no condensation
Host Interface	·USB (Ver1.1)
AC adapter	·5V 1.6A
Main unit current consumption	DC5V ±5% 800mA MAX

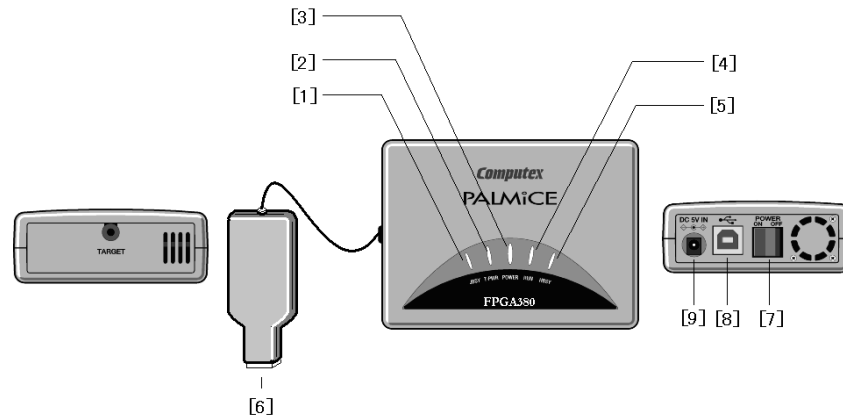
2.1.2 Functional specifications

Item	Specifications
Target system voltage	Auto trace (bet, 2.3V to 3.6V)
JTAG clock	150KHz, 1MHz, 5MHz, 10MHz, or 25MHz
FPGA supported	Xilinx Spartan- II , Spartan- II E, Spartan-3 Virtex, Virtex-E, Virtex- II , Virtex- II Pro *1
Analyzer clock	External synchronous mode : MAX 100MHz Internal asynchronous mode :200MHz to 2KHz
Analyzer memory	256K/512K cycles (depends on mode)
Time stamp	10ns, 100ns, 1μs or 1ms

*1 Processor is not supported.

2.1.3 Outside view

The following figure shows PALMiCE FPGA380.

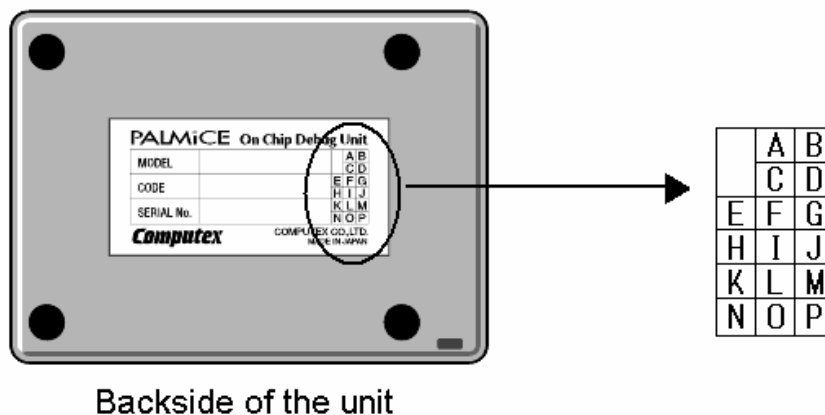


PALMiCE FPGA380

- [1] JBSY (Orange)
Lights in JTAG communication.
- [2] T-PWR (Red)
Lights when the power is supplied to connected target system
- [1] POWER (Green)
Lights when the power is supplied to PALMiCE. The power is supplied from the original AC adapter.
- [3] RUN (Green)
FPGA380 is not used.
- [4] HBSY (Orange)
Lights in communication between the host PC and PALMiCE.
- [5] Analyzer connector
Is a 38-pin connector to connect the target system and the PALMiCE.
- [6] Power switch
Turns on and off the PALMiCE power. The power input state is checked with POWER LED as described in [3].
- [7] USB connector
Connects with the USB cable.
- [8] Power
Connects with the original AC adapter.

2.1.4 Hardware revision

A sticker showing information on the PALMiCE unit is put on the backside of the unit.



< Revision sticker >

Example 1)

1	A	B
	C	D
E	F	G
H	I	J
K	L	M
N	O	P

Example 2)

2	A	B
	C	D
E	F	G
H	I	J
K	L	M
N	O	P

Read the number in the upper left and the last alphabetical character blacked out.

In example 1) shown above, the hardware revision of the unit is read as 1-~~B~~.

In example 2), in which the alphabetical characters are not blacked out, it is read as 2-~~0~~.

The number is updated each time the board of the PALMiCE unit is changed. When the version is upgraded with the same board, the alphabetical character is changed starting at 0 and then alphabetically.

For example, assume that the board is changed after the revision has been updated up to 1-D. At this time, it is updated to 2-0. Then each time the version is upgraded, the character (the latter part) is changed alphabetically (e.g. 2-A, 2-B).

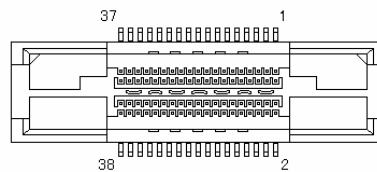
2.2 Target interface (38 pins)

2.2.1 Shape of 38 pin connector

The following figure shows the shape of the AUD connector mounted on the target system.
(For detailed dimensions, see information provided by the manufacturer.)

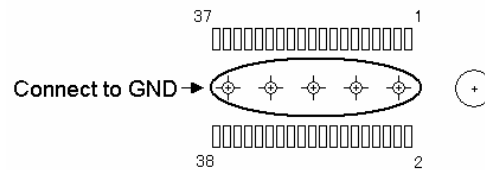
MICTOR connector of AMP make

- 2-767004-2
- 767054-1
- 767061



Attach the MICTOR connector as close to the FPGA as possible, so that the wire pattern length is short.

Also Grand Bus leads of the MICTOR connector must be connected to GND.



Signals and circuit diagram for MICTOR connector

This table shows signals of the connector mounted on the target system.

(Target basis)

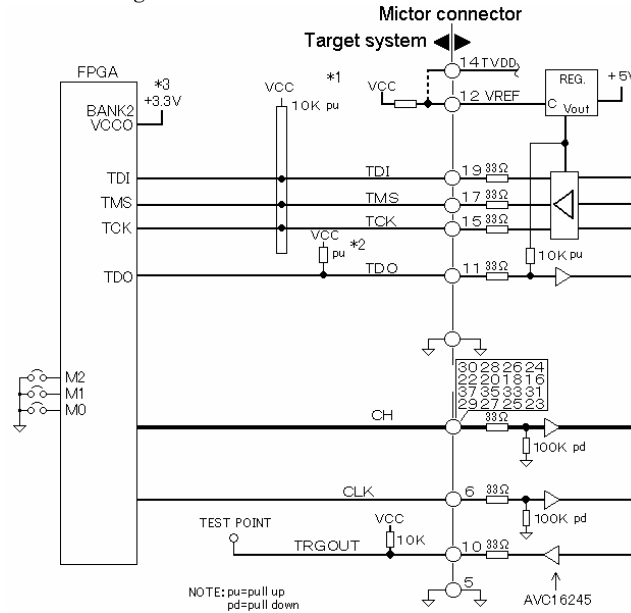
No.	Signal	Note	No.	Signal	Note
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	CLK	Output
7	NC		8	NC	
9	NC		10	TRGOUT	Input
11	TDO* ¹	Output	12	VREF* ²	Output
13	NC		14	NC	
15	TCK	Input	16	CH7	Output
17	TMS	Input	18	CH6	Output
19	TDI	Input	20	CH5	Output
21	NC		22	CH4	Output
23	CH15	Output	24	CH3	Output
25	CH14	Output	26	CH2	Output
27	CH13	Output	28	CH1	Output
29	CH12	Output	30	CH0	Output
31	CH11	Output	32	NC	
33	CH10	Output	34	NC	
35	CH9	Output	36	NC	
37	CH8	Output	38	NC	

Note1: *1 : If the Virtex-Pro 200 is used, we recommend pulling up with a resistor of 200 Ω or greater.

Note2: *2: This is for detecting the potential. A signal pulled up in 1K Ω is also permissible. The voltage level conforms to 2.3V to 3.6V.

Note3: Do not connect anything to the NC pins.

The target interface circuit diagram is shown as follows for reference.



Generally the pull-up resistance of the TDO signal is 10K Ω , but 200 Ω or more is recommended for Virtex-II Pro since the signal is open drain output.

Devices	VCC *1	TDO pull-up resistor *2	BANK2 VCCO *3
SpartanII, Spartan-IIE Virtex, Virtex-E	2.5V to 3.3V	Not required	Required (3.3V)
Virtex-II	2.5V to 3.3V	Not required	Not regulated
Virtex-IIPro	2.5V to 3.3V	Required (200 Ω or more)	Not regulated
Spartan-3	2.5V	Not required	Not regulated

The FPGA may not be configured properly when PROM is on a chain. Set the M2, M1 and M0 terminals to 1, 0 and 1 respectively when using PALMiCE FPGA.

Analyzer probe signal specifications

Output voltage level

- Not in connecting with target : 0.2V or less
- In connecting with target : Conforms to target voltage (2.3V to 3.6V)

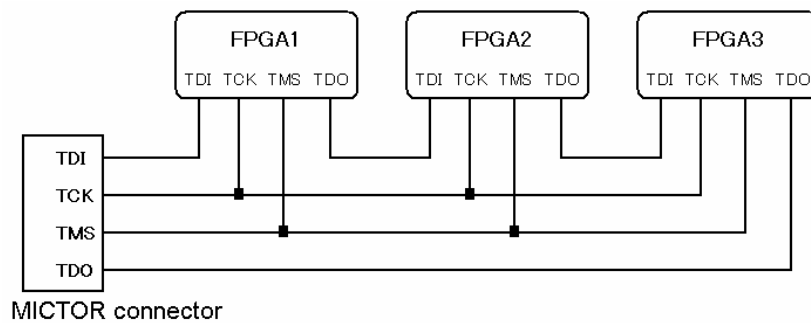
Note Do not apply a voltage of 3.6V or more to the target voltage (VREF).

Input voltage level

- Target voltage :when 2.3V to 2.7V :when 3.0V to 3.6V
- VIH :1.7V to VREF :2.0V to VREF
- VIL :0.7V :0.8V or less

JTAG signal (TCK, TMS, TDI, TDO)

These must be connected to the target system FPGA for communication with the FPGA.
If multiple FPGAs are daisy chained together, Connect the TDO signal from the last stage to the JTAG connector.



VREF signal

This signal is connected to the power supply. (2.3V to 3.6V)

The target interface of PALMiCE conforms to connected potential.

The VREF signal is not used as the power supply but for detecting potential. A signal pulled up in 1K Ω is permissible.

Supply this as the reference voltage if you are only using the PALMiCE FPGA state analyzer function.

CH0 to CH15 signals

This channel is for use by the state analyzer.

We recommend reserving these as FPGA analyzer pins and routing them in advance.

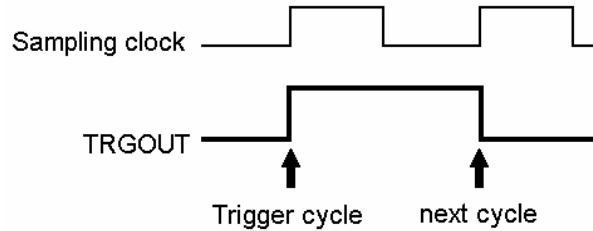
Although a full 16 lines are not absolutely required, the more lines available, the wider the range of analyses that can be performed.

An FPGA internal signal is output to this pin using the probing function or the logic synthesis tool, and then that FPGA internal signal is analyzed.

TRGOUT signal

The TRGOUT signal is provided so that a single trigger pulse (active high) can be output from PALMiCE when the specified trigger condition is matched. There is no need to connect this signal if it is not used.

The TRGOUT output signal is output with the following timing.



CLK signal

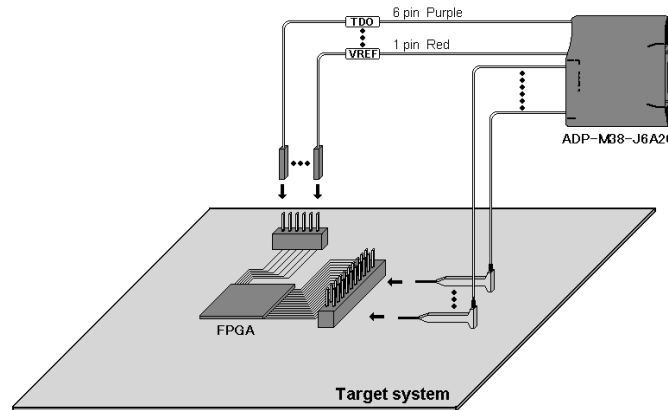
The state analyzer function sampling operation is performed with this clock by connecting to an arbitrary clock in the target system. (Up to 100 MHz)

Sampling is also possible without using this clock by using a PALMiCE FPGA380 internal clock.

2.2.2 ADP-M38-J6A20 (38pin to 6pin / 20pin)

With the PALMiCE FPGA, we recommend connecting to the target system using a standard 38-pin MICTOR connector. However, if it is not possible to provide a MICTOR connector on the target system, conversion adapters are available for connecting with already completed target systems.

However, using a conversion adapter increases the cable length and makes the system more susceptible to noise. If this is a problem, set the JTAG clock to a lower frequency in the CSIDE “Target System Settings”.



Connection with the target system consists of two parts: the 6 pins used for JTAG and the 20 pins used for the analyzer.

Connect the 6 JTAG pins to the connector that extracts the FPGA JTAG pins.

Waveforms can be acquired using the state analyzer by connecting the 20 pins used for the analyzer to the connector that extracts the FPGA I/O pins or to arbitrary signal in the target system.

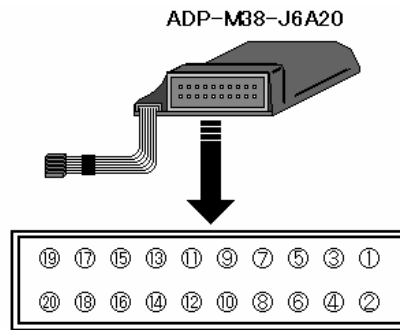
The 6 JTAG pins are acquired by connecting to the connector that matches the label with the connector that extracts the FPGA JTAG signals.

Make all possible efforts to assure that signal lines are never connected incorrectly.

Incorrect signal connections may result in damage to the hardware.

6pins signal table for JTAG

No.	Wire color	Signal line (Label)
1	Red	VREF
2	Black	GND
3	White	TCK
4	Green	TMS
5	Yellow	TDI
6	Purple	T D O



20pin signal table for analyzer (Target basis)

No.	Signal	Input/Output	No.	Signal	Input/Output
1	CH8	Output	2	CH0	Output
3	CH9	Output	4	CH1	Output
5	CH10	Output	6	CH2	Output
7	CH11	Output	8	CH3	Output
9	CH12	Output	10	CH4	Output
11	CH13	Output	12	CH5	Output
13	CH14	Output	14	CH6	Output
15	CH15	Output	16	CH7	Output
17	TRGOUT	Input	18	GND	—
19	VREF	Output	20	CLK	Output

CH0~CH15 : This channel is for use by the state analyzer.

TRGOUT : When the trigger conditions match, a single active-high pulse is output from the PALMiCE FPGA. When not required, handle this pin as an NC pin.

VREF : The same signal as the VREF in the 6 JTAG pins.

Not required if the 6 JTAG pins are connected to the target system.

Do not supply a potential that differs from the potential of the 6 JTAG pins.

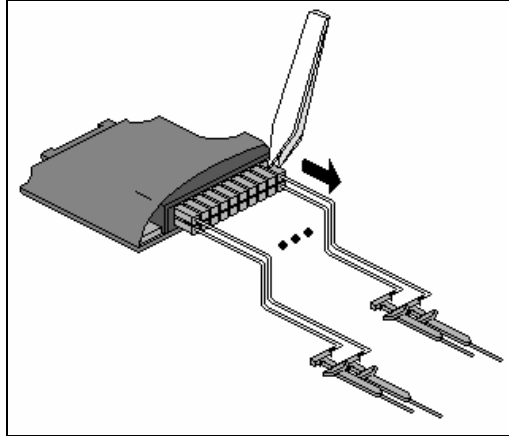
Supply this as the reference voltage if you are only using the PALMiCE FPGA state analyzer function.

CLK : The state analyzer function sampling operation is performed with this clock by connecting to an arbitrary clock in the target system.
Sampling is also possible without using this clock by using a PALMiCE FPGA internal clock.

The 20 analyzer pins can be removed individually in one-pin units.

When removing these lines to minimize wire tangles and noise, always remove the line by grasping the connector with tweezers or a similar tool. If you pull on the wire, it may come off the connector.

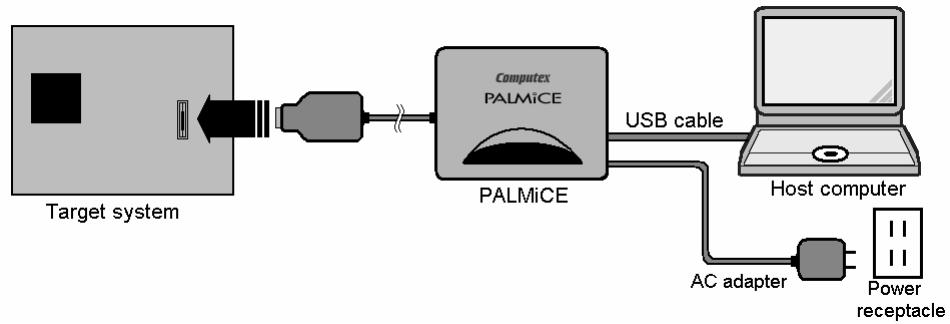
When reconnecting these lines, do not mismatch the clip tip signal name with the connector pin. An incorrectly matched connection can result in damage to the hardware.



Chapter 3 Setting PALMiCE

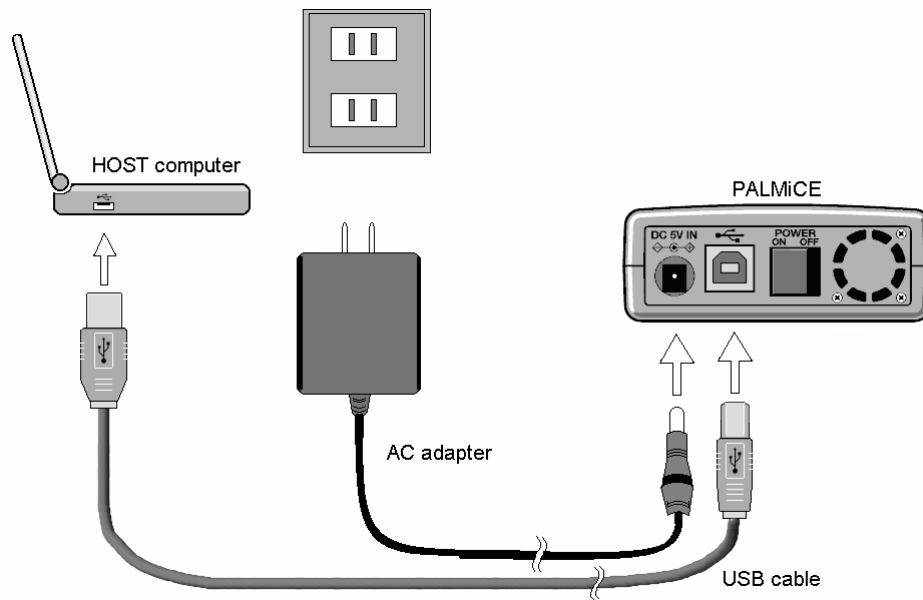
This chapter describes a connection between PALMiCE and the target system and that between PALMiCE and the host PC.

PALMiCE is connected as follows.



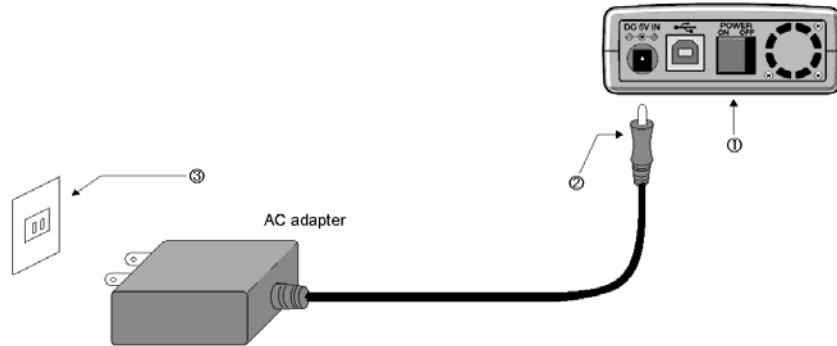
Following sections explain the connections respectively.

3.1 Connecting with host PC



3.2 Connecting with AC adapter

Connect PALMiCE with the USB before connecting the AC adapter. The connection is made to PALMiCE.



Follow the following steps to connect.

- ① Ensure that the power switch of the PALMiCE unit is off.
- ② Connect the DC connector to the main unit.
- ③ Connect the AC adapter to the outlet (100VAC). (Take care because it is constantly electrified.)

3.3 Setting PC

The installation of the driver to the host PC is required for using PALMiCE. The installation method varies according to Windows to be used.

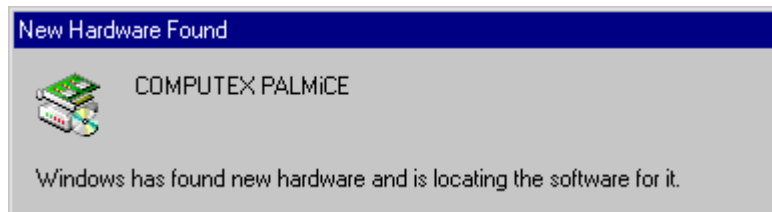
The following sections give the methods for Windows98SE, WindowsMe, Windows2000 and WindowsXP respectively.

When the USB port is used also for a CD-ROM drive or a floppy disk drive, it is not usable for it while PALMiCE is being connected. In this case, copy the CD-ROM contents onto the local hard disk etc. in advance.

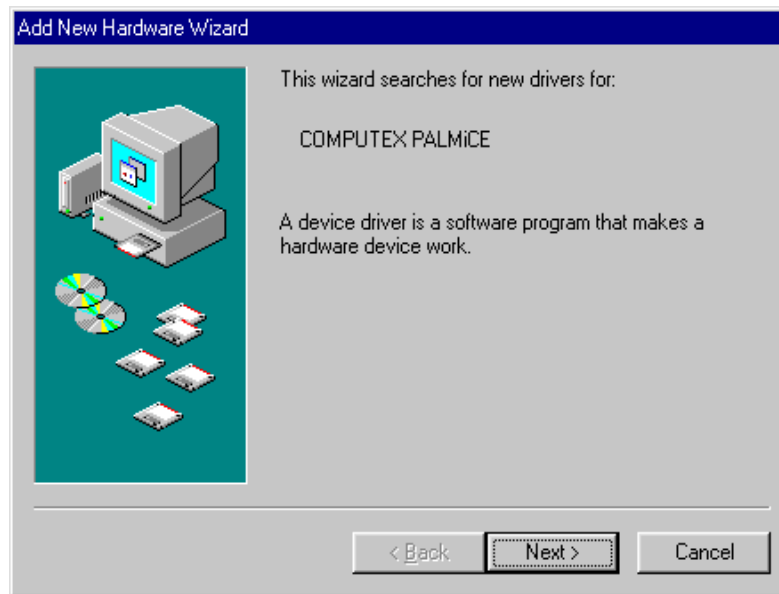
Ctexusb1.sys, Ctexusb2.sys and PALMiCE.inf are required to install the PALMiCE driver. These files are stored in the root of the CSIDE CD-ROM.

3.3.1 For Windows98SE

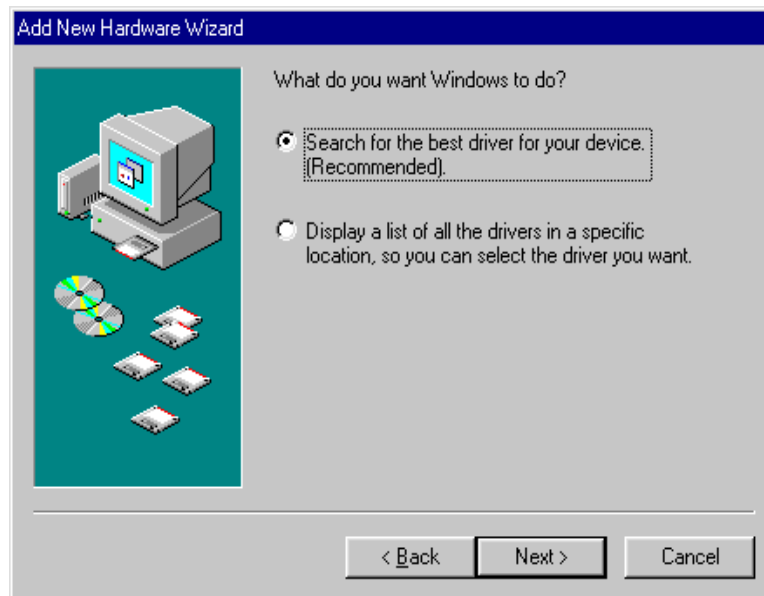
1. Connect PALMiCE with the USB port of the host PC.
2. Turn on the PALMiCE power switch.
3. The OS recognizes PALMiCE by plug & play.
If the OS does not recognize it automatically, ensure that the USB controller of the host PC operates properly.



4. The “Add New Hardware Wizard” appears. Click the **[Next>]** button.



5. Select “Search for the best driver for your device. (Recommended)” and click the **[Next>]** button.



6. Insert the CSIDE CD-ROM into the CD-ROM drive. Check “CD-ROM drive” and click the **[Next>]** button.



7. Click the **[Next>]** button if [PALMiCEdx.INF] has been found from the CD-ROM by driver file searches.

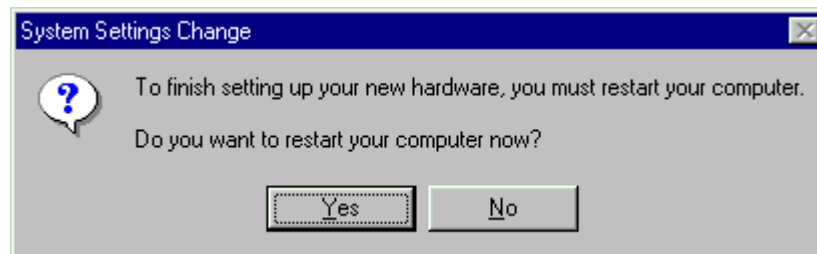
In Windows98SE, the device driver in the CD-ROM may not be found. In this case, click the **[<Back]** button. Set up Windows98SE according to “**About recognition of device driver for Windows98SE**” and then restart setting from Step 6.



8. The following dialog appears. The installation of the PALMiCE device driver is complete. Click the **[Finish]** button.



9. Ensure to click **[Yes]** to restart the host PC if the following message appears.



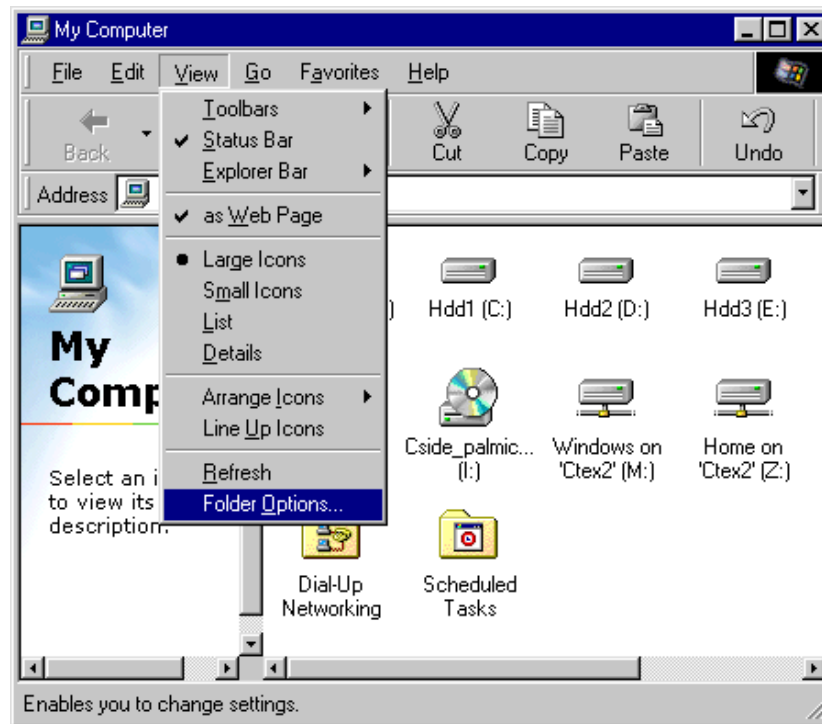
About recognition of device driver for Windows98SE

In Windows98, the PALMiCE device driver may not be found from the CD-ROM of CSIDE.

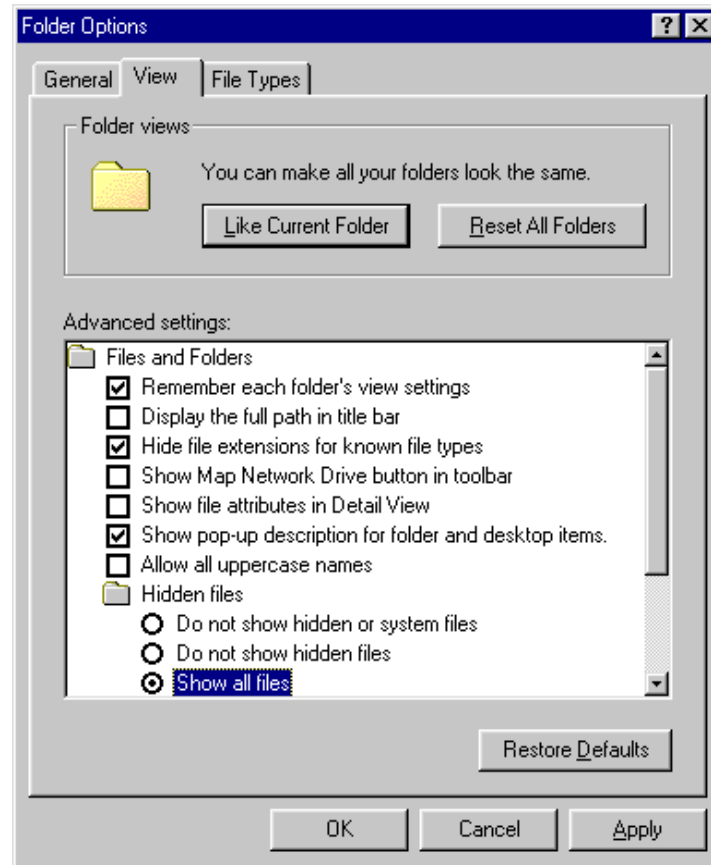
In this case, follow the following steps to set up Windows98.

Or, save “PALMICEdx.INF” and “CTEXUSB1.SYS” files in the root of the CD-ROM onto a floppy disk and check “Floppy disk drives” in Step 6.

1. Select **[View - Folder options]** of My Computer.



2. Open the **[View]** tab of the “Folder Options” dialog. Select “Show all files” from “Hidden files” and click the **[OK]** button.

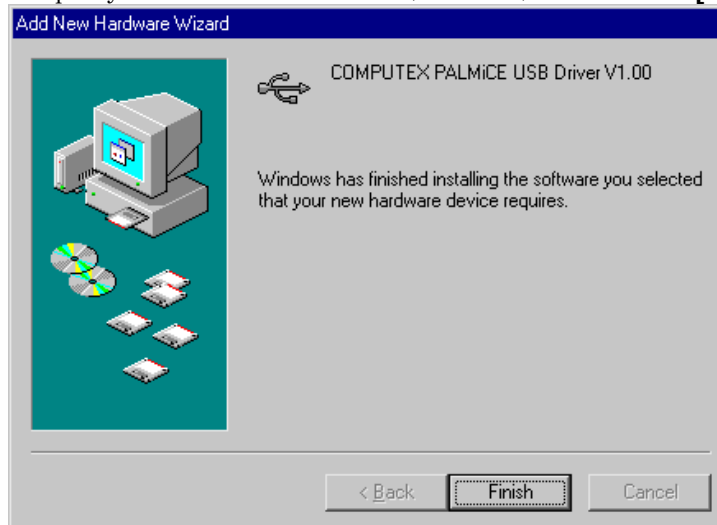


3.3.2 For Windows98ME

1. Connect PALMiCE with the USB port of the host PC.
2. Turn on the PALMiCE power switch.
3. The OS recognizes PALMiCE by plug&play.
Insert the CSIDE CD-ROM into the CD-ROM drive and click **[Next>]** button.

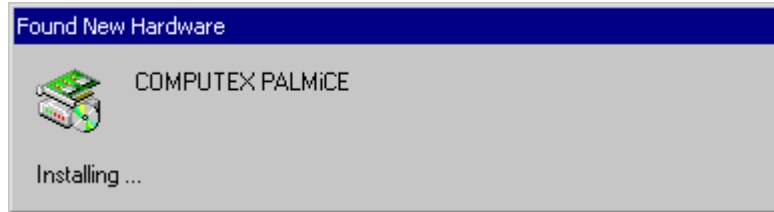


4. The following dialog appears. The installation of the PALMiCE device driver is complete. Click the **[Finish]** button.
If the device driver has not been found, click the **[<Back]** button to return to Step 3.
Then select "Specify the location of the driver (Advanced)" and click the **[Next>]** button.

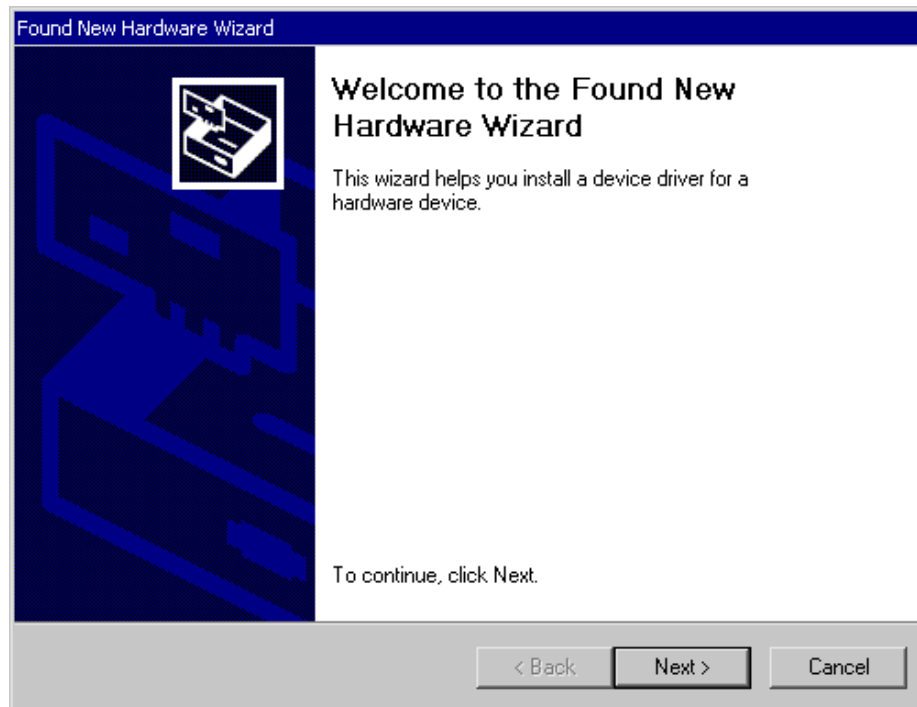


3.3.3 For Windows 2000

1. Connect PALMiCE with the USB port of the host PC.
2. Turn on the PALMiCE power switch.
3. The OS recognizes PALMiCE by plug&play.
If the OS does not recognize it automatically, ensure that the USB controller of the host PC operates properly



4. The “Found New Hardware wizard” dialog opens. Click the **[Next>]** button.



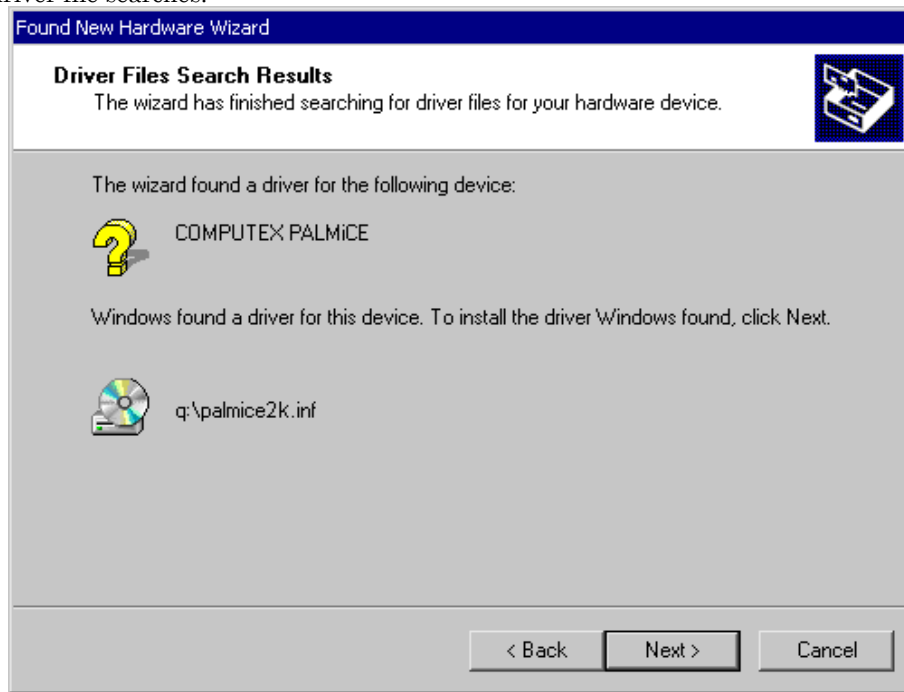
5. Select **[Search for a suitable driver for my device (recommended)]**.



6. Insert the CD-ROM of CSIDE for PALMiCE into the CD-ROM drive. Then check [CD-ROM drives] and click the **[Next>]** button.



7. Click the **[Next>]** button when [palmice2k.inf] has been found from the CD-ROM by driver file searches.



8. The following dialog appears. The installation of the PALMiCE device driver is complete.



3.3.4 For Windows XP

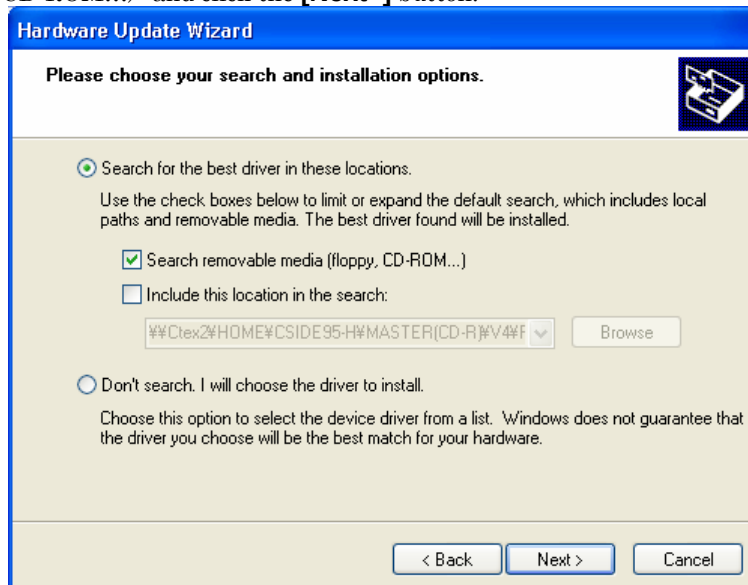
1. Connect PALMiCE with the USB port of the host PC.
2. Turn on the PALMiCE power switch.



3. The OS recognizes PALMiCE by plug&play.

If the OS does not recognize it automatically, ensure that the USB controller of the host PC operates properly

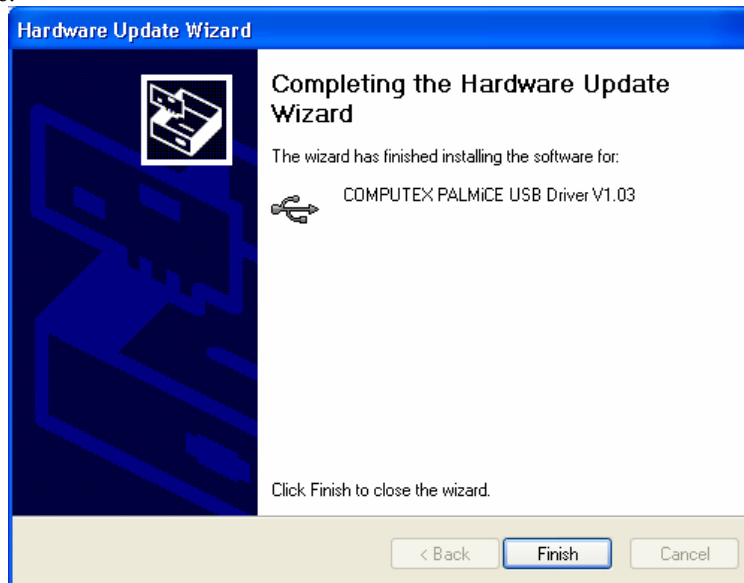
The “Hardware Update Wizard” dialog opens. Then check “Search removable media (floppy, CD-ROM...)” and click the **[Next>]** button.



4. For the following display, click the **[Continue Anyway]** button.



5. The following dialog appears. The installation of the PALMiCE device driver is complete.



Chapter 4 Setting CSIDE

This chapter covers the settings of CSIDE.

4.1 Installing CSIDE

CSIDE is provided on CD-ROM. Upon inserting the CD-ROM, an installer starts up automatically.



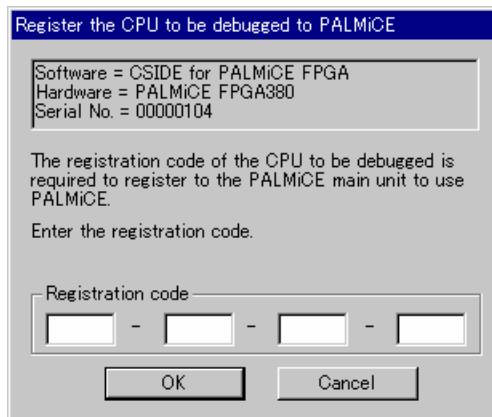
Start up SETUP.EXE of the CD-ROM if an installer does not start. SETUP.EXE is in folder\CSIDE\DISK1.

Click **[CSIDE for PALMiCE FPGA-E]** and install it to any drive.

4.2 Starting CSIDE

Icons for CSIDE are registered after the installation. Select and execute the icon of its main unit. The following dialog box opens when CSIDE starts up for the first time.

If an error message appears without opening the dialog box, see **Chapter 6 Troubleshooting**.



For the PALMiCE FPGA, the registration code must be registered in the PALMiCE unit when starting it for the first time. This process is essential to use debug mode. Not that use with a device other than one supported for the registered code is not possible. It may be hard to distinguish the corresponding device when using more than one PALMiCE. Product name sticker is provided to make easy to distinguish. It is recommended to put the sticker in a prominent place after the registration.

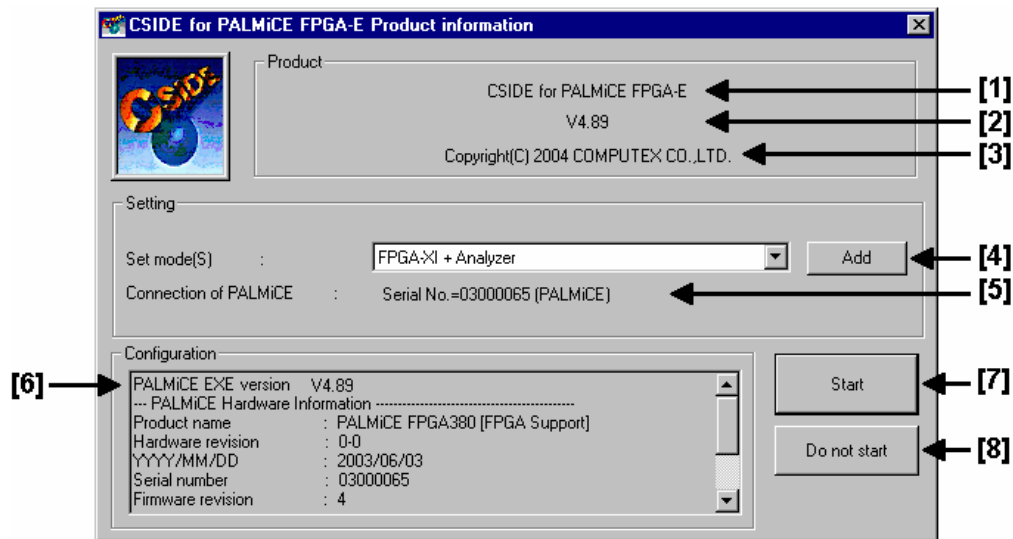
The contents registered here are used for confirmation when the version of CSIDE is upgraded after purchase.

Latest CSIDE is downloadable from our homepage. To download, the registration for our user support system (charged) is required. It is strongly recommend to register for it.

We issue the code for the registration. Enter the code and click the **[OK]** button.

After completion of the code registration, the above dialog box is not viewed any more at start-up of CSIDE. Also, it is not viewed when the CPU registration code has been already registered in the unit.

The following dialog box appears if proper processing has been performed.



Set the following items.

- Mode setting : Set the start mode.

After completing the settings, go on to the next setting by clicking **[Start]**.

The meaning of each item in PALMiCE product information is as follows.

- [1] Name of CSIDE.
- [2] Version of CSIDE.
- [3] Copyright of CSIDE.
- [4] Debug mode setting
Select the start mode.
 - FPGA-XI+Analyzer
Startup with FPGA and the state analyzer function supported
 - Analyzer only
Startup with only the state analyzer function supported. In this mode, it is not necessary for the JTAG signals to be connected.
- [5] Connection of PALMiCE
Whether or not PALMiCE is being connected is viewed. Something like “Serial No.=000000001 (PALMiCE Rev.0-1)” is displayed if it is connected properly. If not, “PALMiCE cannot be recognized” is viewed. In the case, check the USB driver settings, the connection between the host PC and PALMiCE, etc. This item is related only to PALMiCE and the host PC, not being affected by the connection of the target system.

[6] Configuration

A structure of PALMiCE is viewed.

- PALMiCE EXE version
The EXE version of CSIDE is displayed. While the version mentioned in [2] means the product version, this item shows the internal version.
- Product name
The model name of PALMiCE recognized by CSIDE is viewed.
- Hardware revision
The revision of PALMiCE unit is viewed.
- YYYY/MM/DD
The date of manufacture is viewed.
- Serial number
The individual serial number is viewed.
- Firmware revision
This is the program revision written in PALMiCE.
- Control revision
This is the program revision written in PALMiCE. The program is mainly changed according to FPGA to be debugged.
- Firmware rewrite count
The number of counts the firmware has been rewritten is viewed.

[7] Clicking the **[Start]** button starts up CSIDE after checking the set contents.

[8] Clicking the **[Do not start]** button terminates CSIDE.

It is required to set the target system to start up CSIDE. In the next section, “**Setting target system**” is described.

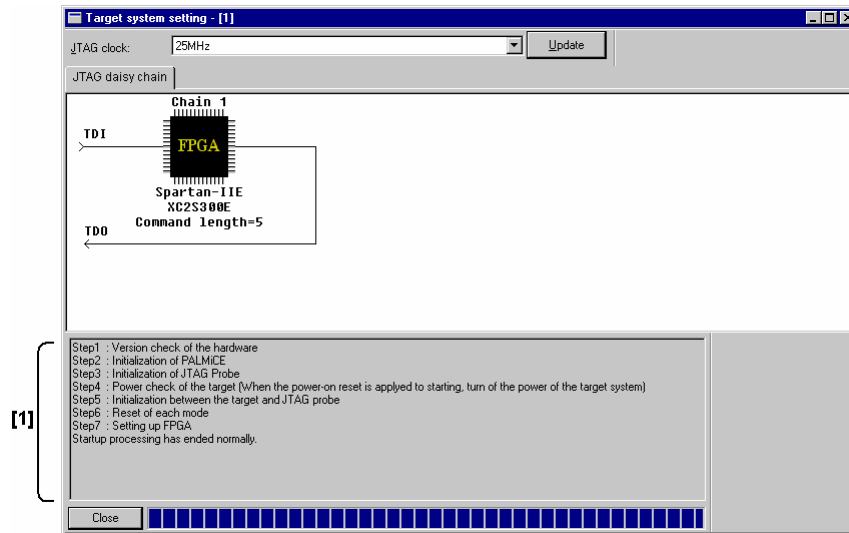
4.3 Setting target system

Set up the target system first after starting CSIDE.

The JTAG probe, device connection and JTAG daisy chain are set here.

Click the **[Update]** button in the upper right of the dialog box after completing the settings.

Then CSIDE checks the set contents and performs start-up processing of PALMiCE.



By clicking the **[Update]** button, screen [1] is viewed to indicate the progress of start-up processing step by step. Processing may stop if the settings have been made incorrectly. In the following sections, the contents of the target system settings are described.

4.3.1 Operating setting window of target system

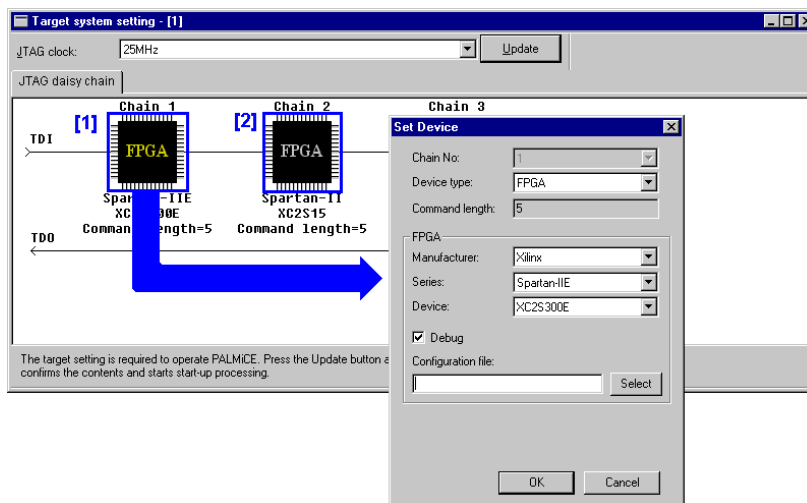
CSIDE expands its functions to improve its operability as a debugger while it conforms to Windows basically. The main functions are as follows;

- Double-click action
- Pop-up menu

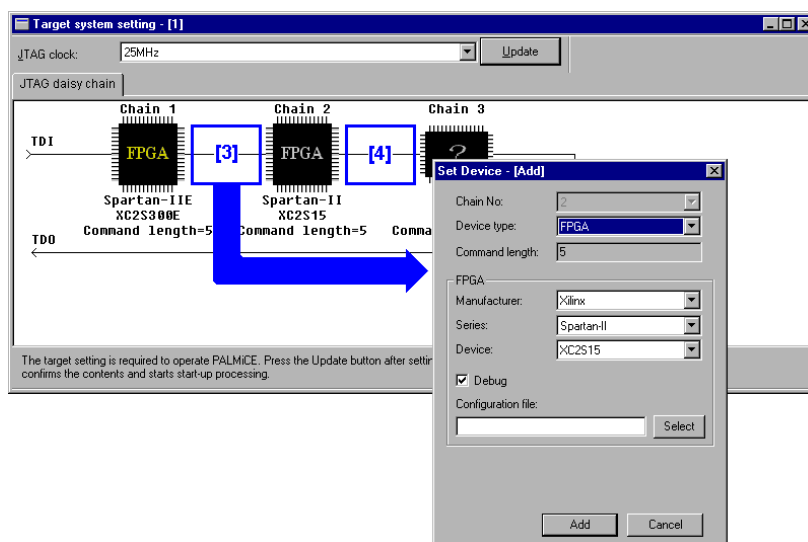
These functions are adopted anywhere in CSIDE and are also available outside the target system setting window. The next sections describe the functions.

Double-click action

By moving the mouse cursor to the item to be changed and by double-clicking it, a setting dialog box opens and the set contents can be changed easily.



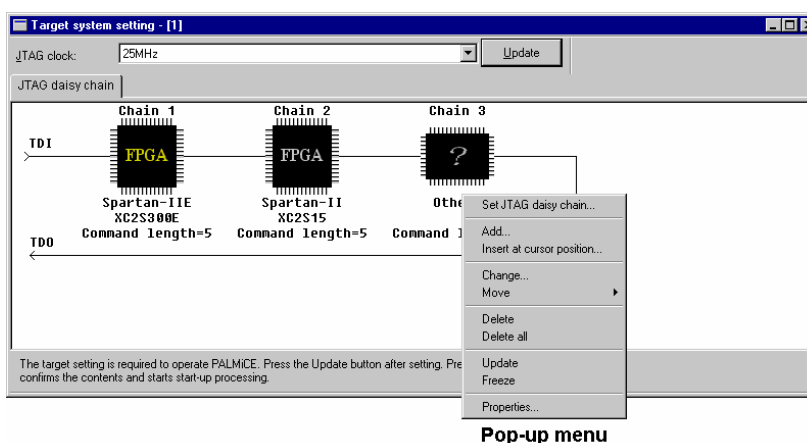
For example, double click at position 1 in the Target System Settings window. This opens a dialog box to change the chain 1 items as shown above. Similarly, a dialog box to change chain 2 items is opened by double clicking at position 2.



Also, double clicking at position 3 opens a dialog box for insertion at the cursor position relative to the position of chain 2. Similarly, double clicking at position 4 opens a dialog box for insertion at the cursor position relative to the position of chain 3.

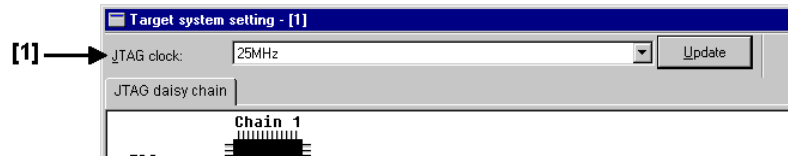
Pop-up menu

While a double-click action and a direct data change are allocated to the most frequently used functions, the pop-up menu is allocated to the all the functions of the window. The menu opens by clicking the right mouse button or by pressing **[Shift]** and **[F10]** simultaneously when the window is active.



4.3.2 JTAG probe related

Set the following JTAG-related items.



[1] JTAG clock

The next section describe the above mentioned items in details.

JTAG clock

The JTAG clock is the TCK clock signal used by the JTAG interface. In CSIDE, clocks with frequencies of 150KHz, 1, 5, 10, and 25 MHz can be selected.

With the Virtex-II Pro, since the TDO output signal is an open-drain output, there are limits on the clock selection due to the value of the pull-up resistor in the target system.

Select a frequency of 10 MHz or lower if a 1 K Ω pull-up resistor is used in the target system.

4.4 Setting JTAG daisy chain

If the JTAG signal lines are cascade connected in the target system, daisy chains of up to 8 elements can be handled.

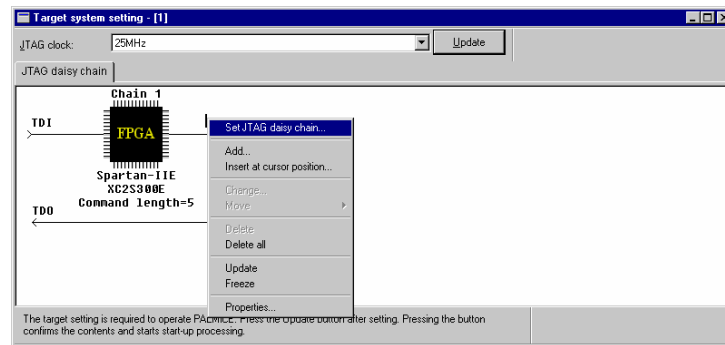
The connection position and Bypass command bit length must be set for each device.

See section “4.4.1 Setting in dialog box” and “4.4.2 Settings in window” for details on the setting procedures.

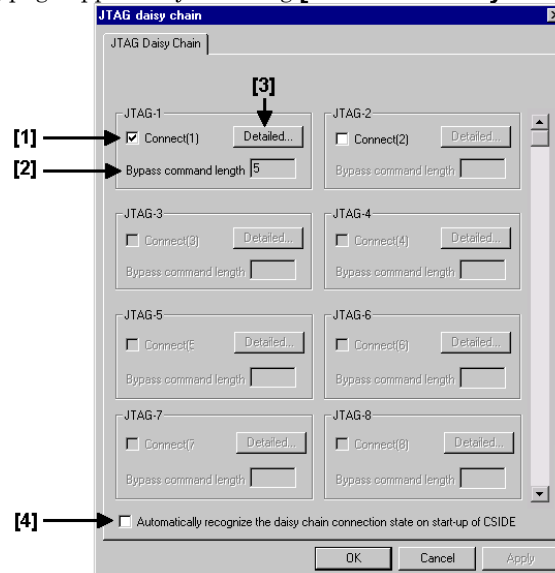
Note that when started in state analyzer function only mode (Analyzer only), there are no JTAG daisy chain settings. (FPGA380 only)

4.4.1 Setting in dialog box

The setting method uses **[Set JTAG daisy chain]** on pop-up menu in the JTAG daisy chain window.



The following setting page appears by selecting **[Set JTAG daisy chain]**.



Use the following procedure to set the various values for the devices that are daisy chained together.

[1] Connect

Insert a number of checks that corresponds to the devices daisy chained together.

[2] Bypass command length

Set the bit length for the Bypass command for the connected devices.

This is allocated automatically if FPGA, CPLD PROM or System ACE are selected as the device type.

(Example: Spartan-II XC2S15: 5 bits)

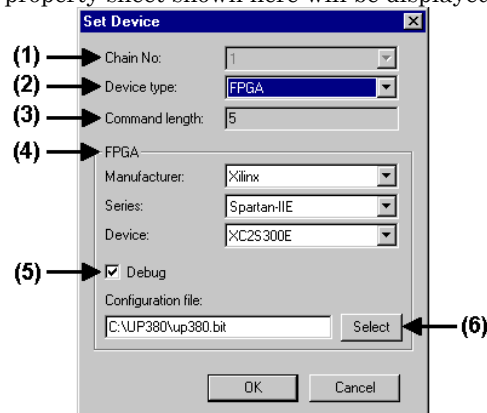
The Bypass command bit length for other devices is specified in the manual for the connected device.

(Example: The register length of the JTAG instruction register is 5 bits)

[3] Detailed

This set sets the detailed settings for the connected device.

Click **[Detailed]**. The property sheet shown here will be displayed.



(1) Chain No

The chain number of the device currently being set up will be displayed.

(2) Device type

Select the type of the connected device.

If the device is a Xilinx product that CSIDE supports, select FPGA, CPLD, PROM, or SystemACE. Select "Other" for an unsupported device or other device.

(3) Command length

Set the bit length for the Bypass command for the connected devices.

This is allocated automatically if FPGA is selected as the device type.

(Example: Spartan-II XC2S15: 5 bits)

(4) FPGA (CPLD, PROM, System ACE)

Select the FPGA device name in the order manufacturer, series, and device name. This item can only be selected if FPGA CPLD, PROM or System ACE are selected as the device type.

(5) Debug

Make the device the object of debugging.

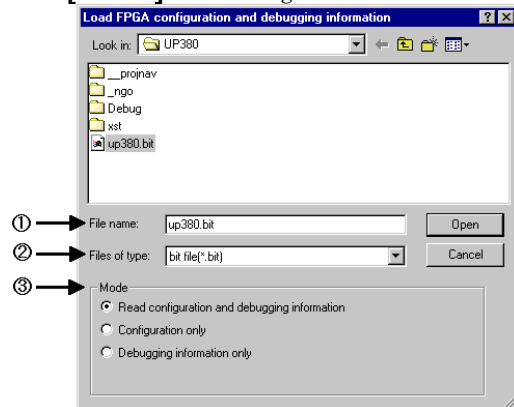
When the connected device is an object of debugging, check this item and specify a configuration file. For a device that is not the object of debugging, remove the check if present. In this case, the configuration file and related items are not needed in any way. This item is only enabled when FPGA is selected as the device type.

(6) Select

The item reads in the FPGA configuration and location information.

This item is only enabled when FPGA is selected as the device type.

Click **[Select]**. The dialog box shown here will be displayed.



A configuration file is a bitstream .BIT file that was created by the logic synthesis tool. This .BIT file is used in FPGA configuration.

The location information files have the same file name as the configuration file, but the files read in have the extensions .LL and .PAD. If the location information files are not in the same directory as the configuration file, a file specification dialog box will be displayed.

Also, if a location information file of the form "filename_BD.BMM" generated from the block RAM placement information .BMM file is present, that file will also be read in at the same time.

① File name

Specifies the file name for FPGA configuration.

② File of type

Displays the file type.

③ Mode

Displays the file type.

- Read configuration and debugging information

After configuring the FPGA for which the location information is read in.

Select this mode if configuration and debugging will be performed using PALMiCE FPGA.

- Configuration only

Only performs an FPGA configuration. The location information is not

read in.

Select this mode if only configuration will be performed using PALMiCE FPGA.

- Debugging information only

The FPGA configuration is not performed. Only the debugging information is read in.

Select this mode if configuration is performed in the serial ROM provided for a separate target and only internal monitoring will be performed without having PALMiCE FPGA perform configuration operation.

[4] Automatically recognize the daisy chain connection state on start-up of CSIDE

This is a mode in which the settings described in steps [1] to [3] above are acquired from the target system by automatic recognition.

If the daisy chain state of the target system used is not known, enable this mode and start CSIDE.

However, if an unsupported device is connected, the daisy chaining may not be recognized correctly.

If the daisy chaining is not recognized correctly, correct the settings manually after automatic recognition.

Note Perform the **[Automatically recognize the daisy chain connection state on start-up of CSIDE]** in the state where the FPGA has not been configured.

4.4.2 Settings in window

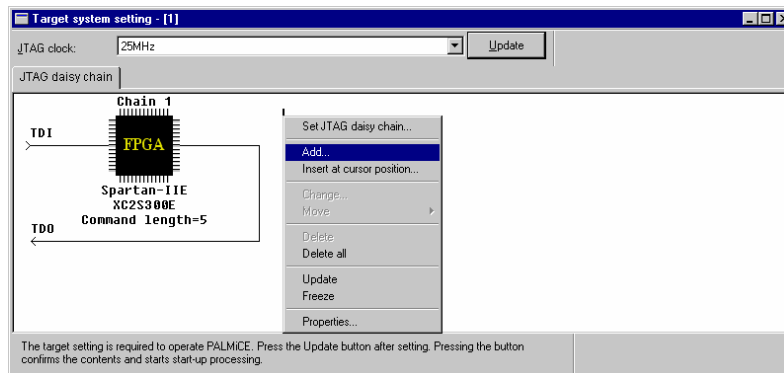
This setting method makes settings in the JTAG Daisy Chain window.

[Add], **[Insert at cursor position]**, **[Change]**, **[Move]**, **[Delete]** and **[Delete All]** are available on the pop-up menu.

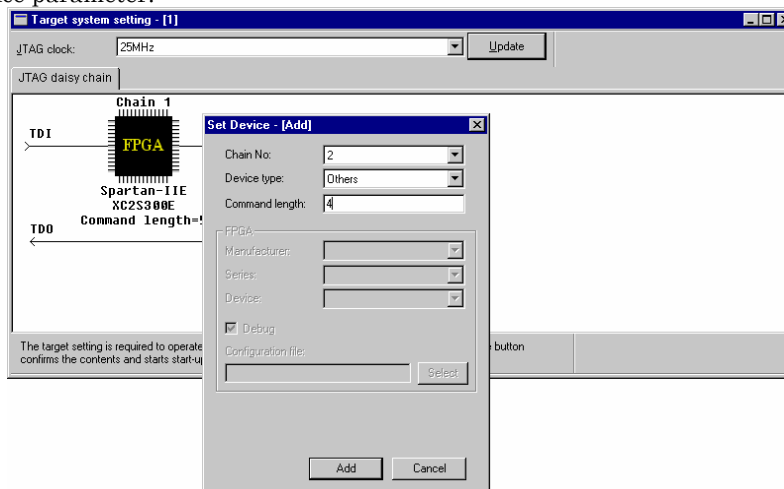
The following sections explain each function with an example.

Add

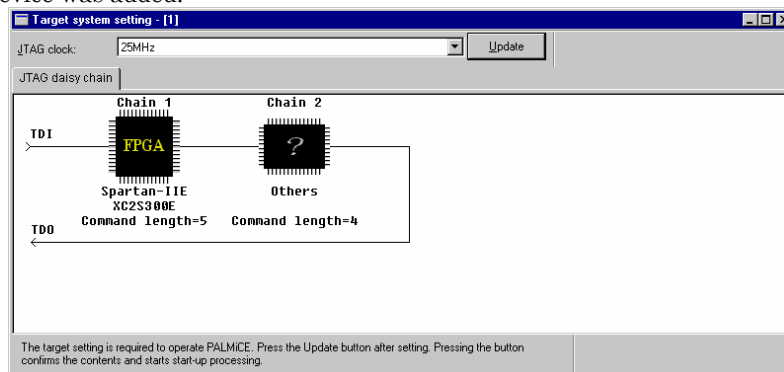
A device is added using **[Add]** on the pop up menu.



A double-click at the both ends of the chain devices also performs the same operation.
Set a device parameter.

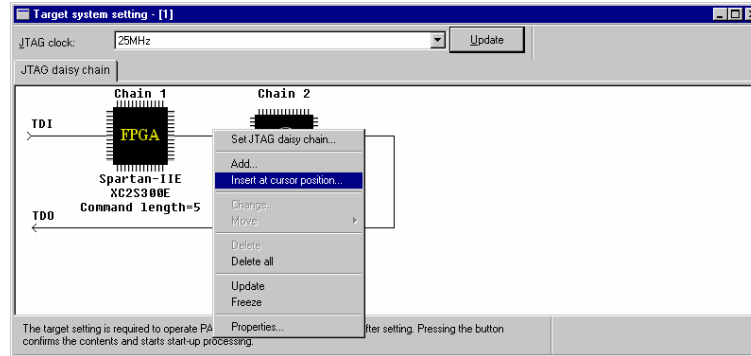


A chain device was added.



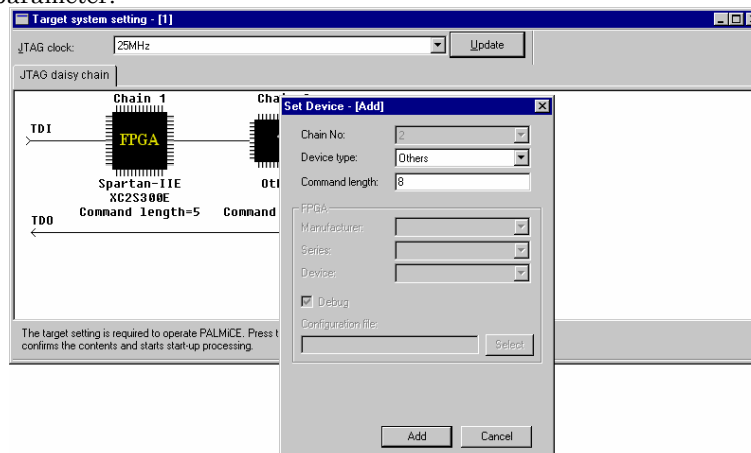
Insert at cursor position

A chain device is added between Chain 1 and Chain 2 using **[Insert at cursor position]** on the pop-up menu.

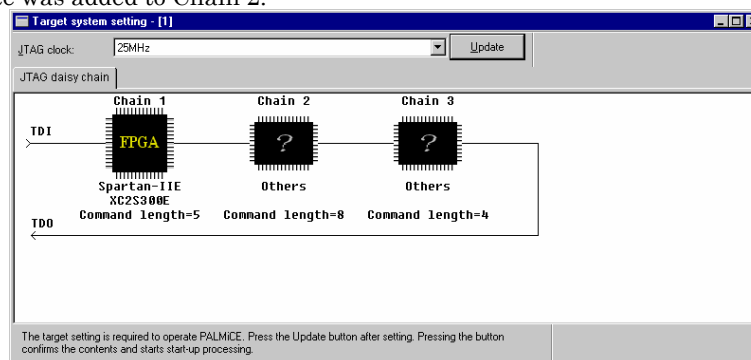


A double-click between the chain devices can perform the same operation.

Set a device parameter.

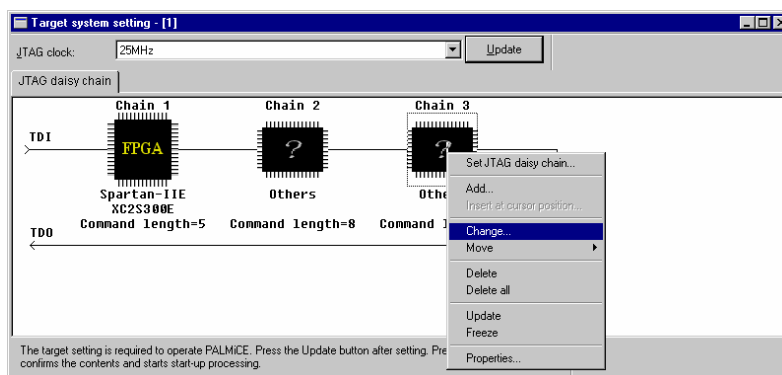


A chain device was added to Chain 2.



Change

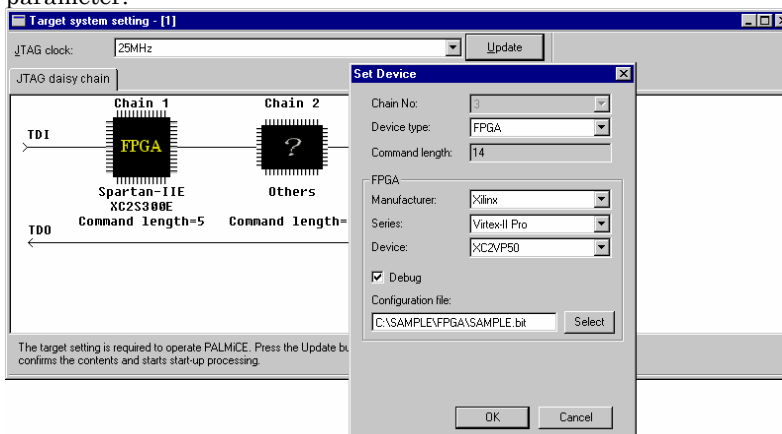
A device parameter at the cursor position is changed using **[Change]** on the pop-up menu.



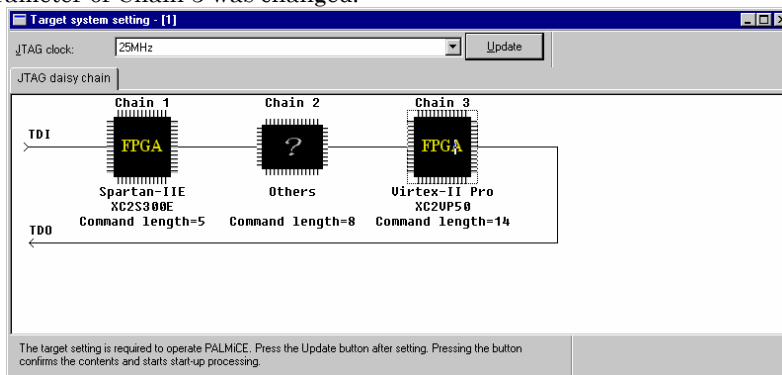
A double-click on a device to be changed also performs the same operation.

Also direct key input at the cursor position can also change devices.

Set a device parameter.

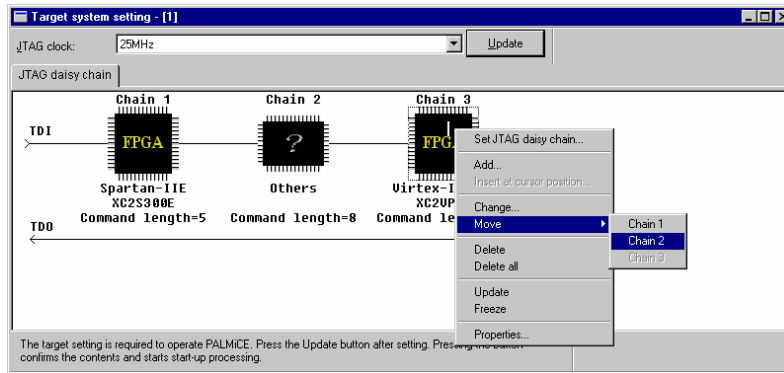


A device parameter of Chain 3 was changed.

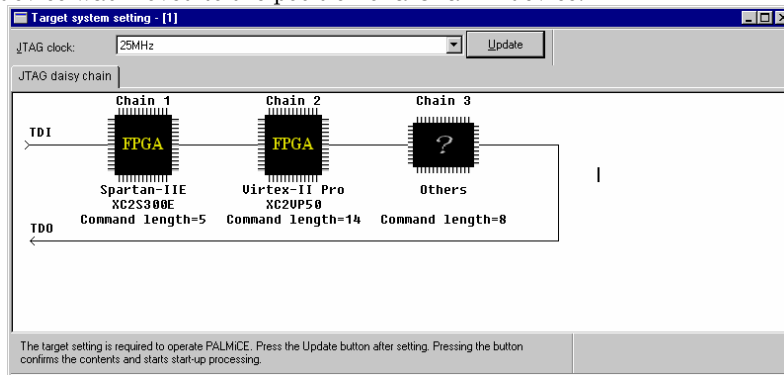


Move

A Chain 3 device is moved to the position of a Chain 2 device using **[Move]** on the pop-up menu.

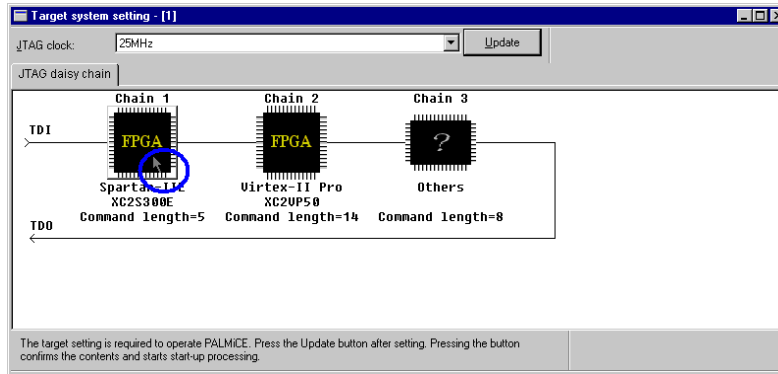


A Chain 3 device was moved to the position of a Chain 2 device.



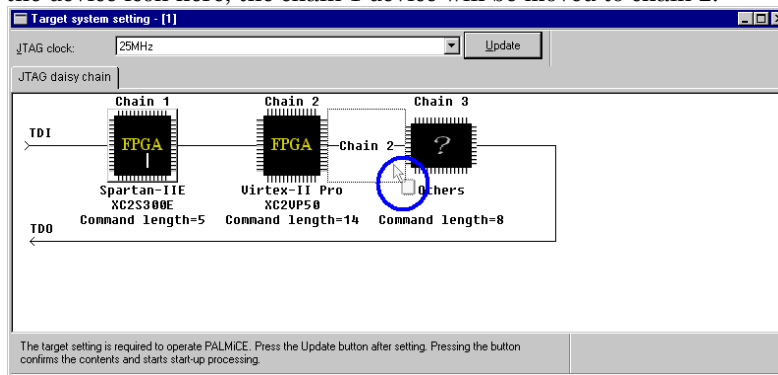
The **[Move]** operation can also be performed by dragging and dropping the chain device to be moved.

When the device icon is moved, the outline of the device being dragged changes and the drag starts.



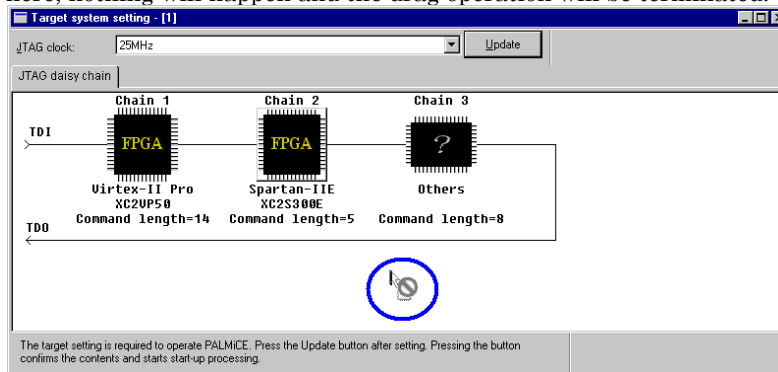
When the device icon is moved, the outline of the device being dragged changes and the drag starts.

If you drop the device icon here, the chain 1 device will be moved to chain 2.



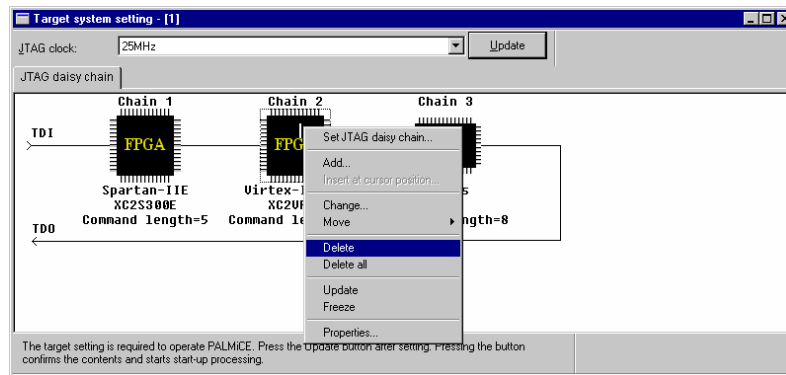
If you move the cursor over an area where the device icon cannot be dropped, the cursor will switch to a No Entry mark.

If you drop here, nothing will happen and the drag operation will be terminated.



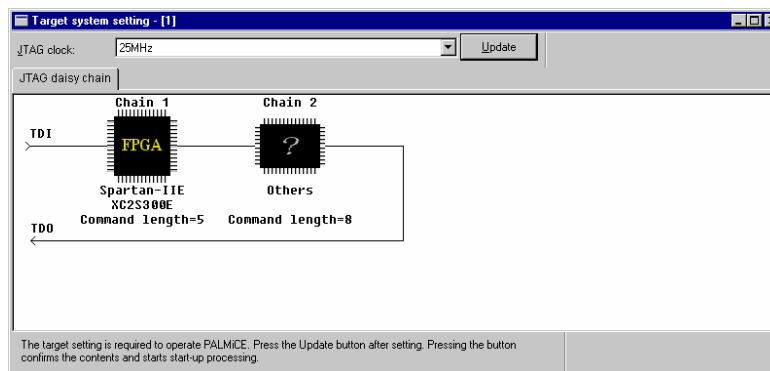
Delete

A Chain 2 device at the cursor position is deleted using **[Delete]** on the pop-up menu.



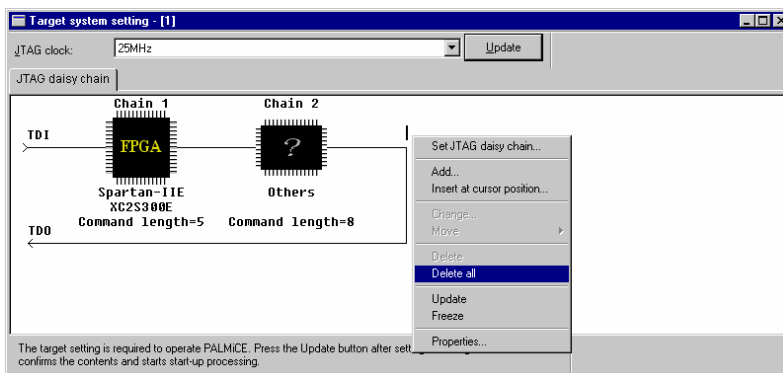
[Delete] key input after moving the cursor to a device chain to be deleted performs the same operation.

A Chain 2 device was deleted.

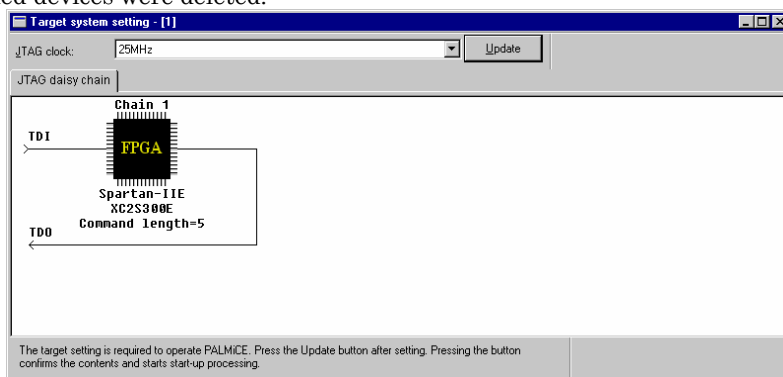


Delete All

All the added chain devices are deleted using **[Delete all]** on the pop-up menu.



All the added devices were deleted.



Update

The contents to be displayed are updated.

Always top

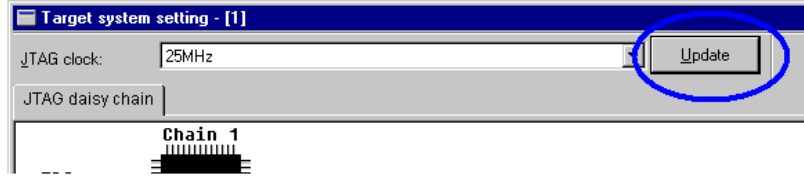
The window constantly appears in front of the others.

Properties

The character color, background color and font are changed here.

4.5 Starting PALMiCE (Update)

Click **[Update]** to start the PALMiCE operation after completing the settings.



By clicking **[Update]**, the settings made for the target system are displayed. An error message indicating possible causes is viewed for reference if PALMiCE has unsuccessfully started up for some reason.

(Blank)

Chapter 5

FPGA Debugging Function Preparations

This chapter describes the settings that are required for FPGA debugging using PALMiCE FPGA.

- Capture component instantiation
- Configuration file option settings

There are two methods for performing these settings: they can be made when starting CSIDE, or they can be set up in advance by the user.

Although the method performed at CSIDE startup in which settings are performed simply by selection from a displayed menu may be used, note that the CSIDE preparation processing will be performed at startup.

See sections “**5.1 Capture Component Instantiation**” and “**5.2 Configuration File Option Settings**” for details on how the user can set these items in advance.

When the settings required to debug an FPGA as set in advance before CSIDE startup, the CSIDE preparation processing can be omitted and the startup time shortened.

5.1 Capture Component Instantiation

To sample FPGA internal nodes and display the results in CSIDE, the components to be captured in the user circuit must be instantiated (embedded).

The following is a necessary condition for this operation.

- A sampling clock is required

Set up any one of the FPGA internal user clocks to be used as this clock. (We recommend using a clock pulse signal with a frequency of a few kHz or higher.)

Specify the components to be instantiated in the FPGA source program.

The following presents example in VHDL and Verilog.

Example

- The FPGA node is always sampled.
- A Xilinx SPARTAN II E is used.
(Use a capture component that matches the device. For example, if a Virtex II is used, specify CAPTURE_VIRTEX2 as the underlined section.)

●VHDL

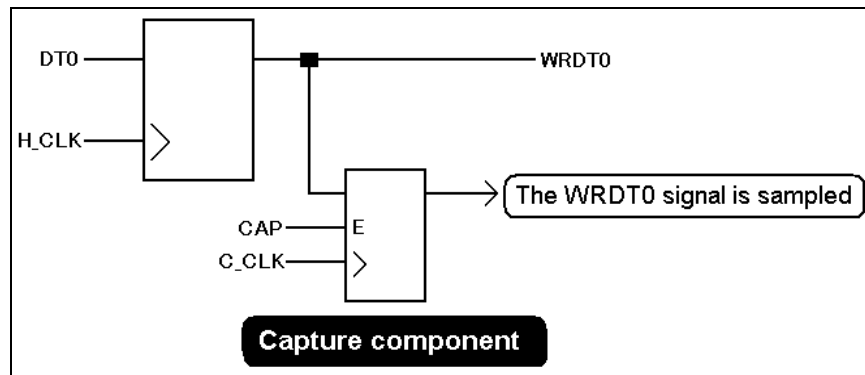
```
<Architecture declaration part (architecture)>
component CAPTURE_SPARTAN2
  port(
    CAP:in std_logic;
    CLK:in std_logic
  );
end component;

begin

  UC:CAPTURE_SPARTAN2 port map(CAP=>'1',CLK=>C_CLK);
```

●Verilog

```
CAPTURE_SPARTAN2 UC ( .CAP (1'b1), .CLK (C_CLKG));
```



Capture Component Image

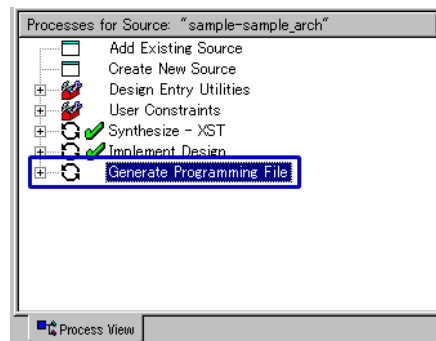
The FPGA node can be sampled at all times by setting the enable signal (the CAP signal in the previous example) to the "1" state at all times.

Use of capture components consumes no user resources whatsoever.

5.2 Configuration File Option Settings

After completing design layout using a logic synthesis tool, the user must set the options required for FPGA configuration in JTAG and must also set up generation of the "LL file," the location information file required for debugging.

The following example shows these settings using the Xilinx ISE 6.2i FPGA development tool.



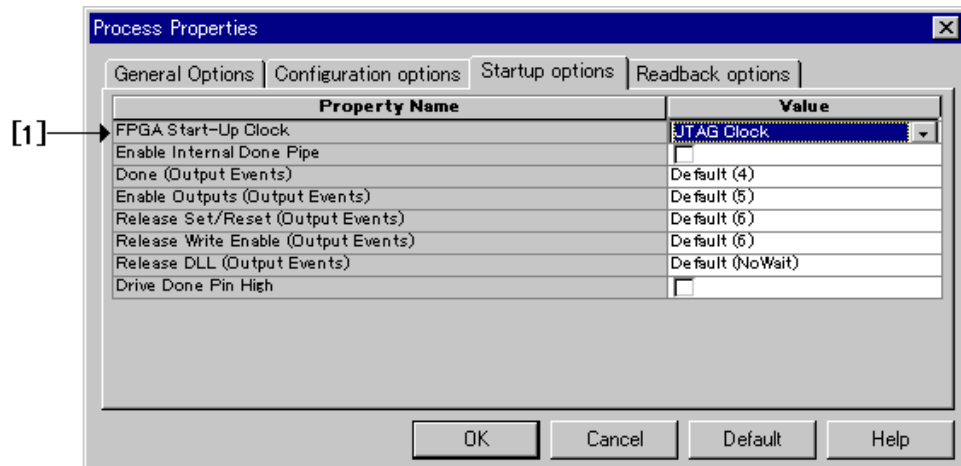
When executing the **[Generate Programming File]** operation, set all the property option items.

- Startup Options
- Readback Options

Select **[Generate Programming File]** and then select **[Properties]** in the pop-up menu.
The Property Settings dialog box will open.

5.2.1 Startup Options

Set the items required to configure the FPGA in JTAG mode.
Select the property's **[Startup Options]**. The following property page will be displayed.

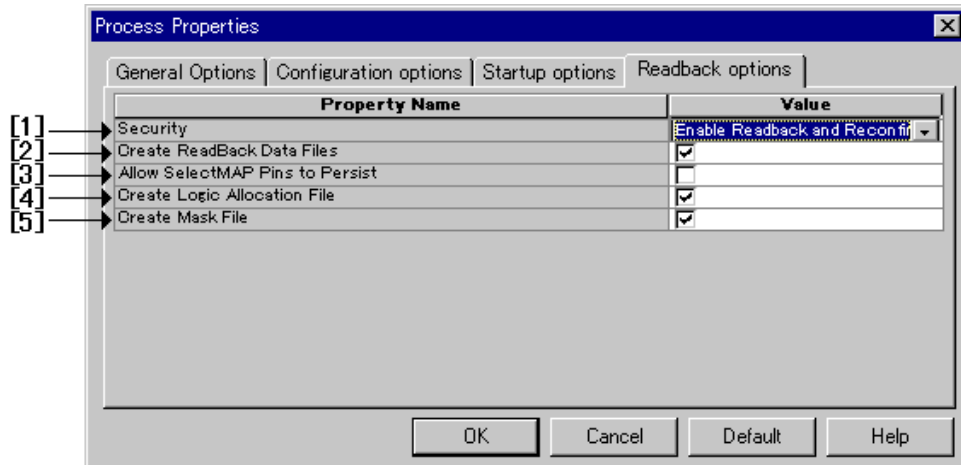


- [1] FPGA Start-Up Clock
Select the "JTAG Clock".

5.2.2 Readback Options

Set the items required to generate the .LL file.

Select the property's **[Readback Options]**. The following property page will be displayed.



- [1] Security
Select the "Enable Readback and Recoufiguration".
- [2] Create Readback Data Files
Check the box.
- [3] Allow SelectMAP Pins to Persist
Uncheck the box.
- [4] Create Logic Allocation File
Check the box.
- [5] Create Mask File
Check the box.

Chapter 6

Troubleshooting

6.1 CSIDE does not start up

This section gives possible causes of and solutions to failure in start-up.

6.1.1 Connecting PALMiCE to the host personal computer

If CSIDE terminates with an error, it may not be possible to restart CSIDE. If that happens turn the PALMiCE main power off and then on again.

6.1.2 Initialization Between the FPGA and the JTAG Probe

The following are possible causes of failures of the initialization between the FPGA and the JTAG probe after clicking Update in the Target System Settings window.

- 1) The target system JTAG connector or MICTOR connector is not connected.
- 2) The target system power supply is not applied.
- 3) The JTAG chain is not routed correctly.
- 4) There is no pull-up resistor on the TDO pin. (Virtex-II Pro)

PALMiCE FPGA

User's manual

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