

TWR-MC-LV3PH

User's Manual

Rev. 1.0





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1 Overview

The 3-phase Low Voltage Motor Control board (TWR-MC-LV3PH) is a peripheral Tower System Module with one of the available MCU tower module, accommodating a selected microcontroller, it provides a ready-made, software-development platform for one-third horsepower off-line motors. Feedback signals are provided that allow a variety of algorithms to control 3-phase PMSM and BLDC motors.

The TWR-MC-LV3PH module features:

- Power supply voltage input 12-24VDC, extended up to 50V (see chapter 3.2 Electrical Characteristics for details)
- Output current up to 8 Amps
- Power supply reverse polarity protection circuitry
- 3-phase bridge inverter (6-MOSFET's)
- 3-phase MOSFET gate driver with over current and under voltage protection
- 3-phase and d.c. bus-current-sensing shunts
- DC bus-voltage sensing
- 3-phase back-EMF voltage sensing circuitry
- Low-voltage on-board power supplies
- Encoder/Hall sensor sensing circuitry
- Motor power and signal connectors
- User LED, power-on LED, 6 PWM LED diodes

A block diagram for the TWR-MC-LV3PH is shown in the figure below.



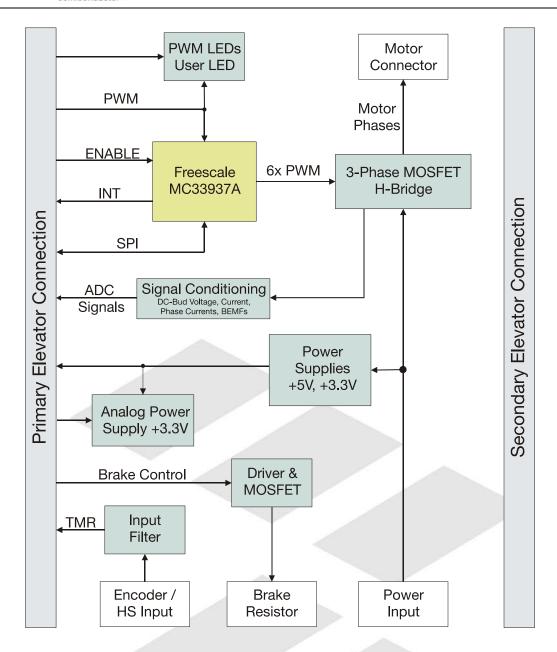


Figure 1 - TWR-MC-LV3PH Block Diagram



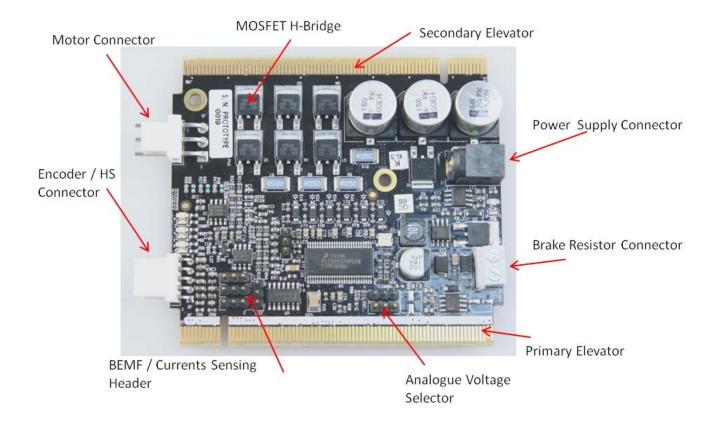


Figure 2 - TWR-MC-LV3PH Image

2 Reference Documents

The documents listed below should be referenced for more information on the Freescale Tower system and the TWR-MC-LV3PH. Refer to http://www.freescale.com/tower for the latest revision of all released Tower documentation.

- TWR-MC-LV3PH Schematics
- TWR-MC-LV3PH Quick Start Guide
- Freescale MC33937A Three Phase Field Effect Transistor Pre-driver

3 Hardware Features

This section provides more details about the features and functionality of the TWR-MC-LV3PH.



3.1 Power Supply

Freescale's 3-phase Low Voltage Motor Control Tower Module is a 3-phase power stage that will operate off d.c. input voltages of 12 to 24 volts, 8 amps. The module contains reverse polarity protection circuitry.

It is intended that the TWR-MC-LV3PH be powered from an external power supply of 12 to 24 volts, 4 to 8 amps depending on used motor. The module includes 5.0V and 3.3V supplies which are capable to provide power to entire Tower System.

3.1.1 +5V Power Supply

The +5V level is generated by means of the LM2594HVM switching step-down regulator (see TWR-MC-LV3PH schematic), which generates this level from bus voltage. This converter can supply up to 500 mA. This voltage level serves the MC33269D linear regulator, encoder and optionally entire tower system. If the LM2594HVM converter operates properly, the D7 green LED is lit.

3.1.2 +3.3V Power Supply

An important voltage level for this board is +3.3V. This voltage level is obtained from the MC33269D linear voltage regulator and can supply up to 800 mA.

3.1.3 +1.65V Voltage Reference

Current sensing operational amplifiers use 1.65V voltage level connected to non-inverted inputs. This level is obtained from a precision voltage reference LM4041 (D6).

3.1.4 Analog Power Supply and Grounding

For analog quantities sensing (currents and voltages) is used separated analog voltage 3.3V and ground. This voltage level can be chosen from two sources. One is separated from 3.3V digital power supply using an LC filter and the second source is from the primary elevator port. A source selection is done via jumpers J2 and J3.

3.2 Electrical Characteristics

The electrical characteristics in table below apply to operations at 25°C with a 24-Vd.c. power- supply voltage. Input voltage maximal value can be higher than 24V. A 50V maximal input voltage value is allowed, but the DC bus and BEMF sensing circuits need to be modified. The divider resistors in these circuits need to be changed to increase sensing range up to 50V if required. It prevents scaled quantities exceeding the maximally allowed input voltage value on the controller input pins.

If an input voltage higher than 24V is applied, the plugged TWR modules might be damaged.



Characteristic	Symbol	Min	Тур	Max	Units
DC input voltage	V_{dc}	12	_	24	V
Quiescent Current	I_{CC}	_	TBD	_	mA
Logic 1 Input Voltage	V_{IH}	1.5	_	1.7	V
Logic 0 Input Voltage	V_{IL}	0.9	_	1	V
Input Resistance	R_In	_	10	_	kΩ
Analogue Output Range	V_{Out}	0	_	3.3	V
Bus Current Sense Voltage	I _{Sense}	_	412	_	mV/A
Bus Current Sense Offset	I _{offset}		+1.65		V
Bus Voltage Sense Voltage*	V_{Bus}	_	91	_	mV/V
Bus Voltage Sense Offset	V_{offset}		0		V
Bus Continuous Output Current **	I_{C}	_	_	8	Α
Total Power Dissipation (per MOSFET) ***	P_D	_	_	TBD	W
Dead-time (set by SW MC33937) ****	t _{off}	0	_	15	us

Table 1 - Electrical Characteristics

3.3 Three Phase Field Effect Transistor Pre-driver

The TWR-MC-LV3PH module utilizes Freescale MC33937A Three Phase Field Effect Transistor Predriver. The 33937 is a Field Effect Transistor (FET) pre-driver designed for three phase motor control and similar applications. The integrated circuit (IC) uses SMARTMOS™ technology. The IC contains three High Side FET pre-drivers and three Low Side FET pre-drivers. Three external bootstrap capacitors provide gate charge to the High Side FETs. The IC interfaces to a MCU via six direct input control signals, an SPI port for device setup and asynchronous reset, enable and interrupt signals.

Features:

- Fully specified from 8.0V to 40V covers 12V and 24V automotive systems
- Extended operating range from 6.0V to 58V covers 12V and 42V systems
- Greater than 1.0A gate drive capability with protection
- Protection against reverse charge injection from CGD and CGS of external FETs
- Includes a charge pump to support full FET drive at low battery voltages
- Dead time is programmable via the SPI port
- Simultaneous output capability enabled via safe SPI command
- MC33937A supports very high current loads



3.4 SPI communication

Freescale MC33937A driver uses SPI communication for operating parameter, mode and interrupt setting. Driver command and registers are described in a driver manual. The selection between two Chip Select signals is available on the board via two 0-ohm resistors R95, R96 (see 5.1).

3.5 3-Phase Bridge

The output stage is configured as a 3-phase bridge with MOSFET-output transistors. It is simplified considerably by an integrated-gate driver that has an over-current, under voltage and other safety features.

At the input, pull-down resistor R26 sets logic low in the absence of a signal for the low side transistor. Open input pull-down is important because the power transistors must stay off in the case of a broken connection or an absence of power on the daughter board. Gate driver inputs are 3.3V compatible. A Freescale device, an MC33937A, supplies the gate drive. The MC33937A also provides under voltage hold-off and over-current. Under voltage hold-off threshold value is 8V. MC33937A has an implemented dead-time insertion which can be configured using SPI. The default dead-time value is typically 15µs.

One important design decision in a motor drive is the selection of gate-drive impedance for the output transistors. Resistor R14, R15, diode D8, and the MC33937A nominal 100mA current sinking capability determine gate-drive impedance for the lower half-bridge transistor. A similar network is used on the upper half-bridge. These networks set the turn-on gate drive impedance at approximately 100Ω and the turn-off gate drive to approximately 100mA. These values produce transition times of approximately 285 ns.

Transition times of this length represent a carefully weighed compromise between power dissipation and noise generation. Generally, transition times longer than 250 ns tend to get power hungry at non-audible PWM rates; transition times under 50 ns create di/dts so large that proper operation is difficult to achieve. The 3-phase Low Voltage Motor Control Tower Module is designed with switching times at the higher end of this range to minimize noise.

Anti-parallel diode softness is also a primary design consideration. If the anti-parallel diodes in an offline motor drive are allowed to snap, the resulting di/dts can cause noise management problems difficult to solve. In general, the peak to zero di/dt should be approximately equal to the di/dt applied to turning off the anti-parallel diodes. The IRFR540Z MOSFETs used in this design are targeted at this kind of reverse recovery.

3.6 Bus Voltage and Current Feedback

Bus voltage is scaled down by a voltage divider consisting of R74, R77 and R79. The values are chosen such that a 36.3-volt bus voltage corresponds to 3.3V at output V_SENSE_DCB. V_SENSE_DCB is scaled at 91mV per volt of the DC bus voltage and is terminated on the main elevator port. An additional output, V_SENSE_DCB_HALF, provides a reference used in zero-crossing detection.

V_SENSE_DCB_HALF is scaled at 45.5mV per volt of the DC bus voltage and is also terminated on the main port.



Bus current is sampled by resistor R10 and amplified in either the MC33937A's operational amplifier or external operational amplifier U6B. This circuit provides a voltage output suitable for sampling on A/D (analogue-to-digital) inputs. Both operational amplifiers are connected as differential amplifiers for bus-current sensing with the equal gain given by:

A = R40/(R38+R39)

The output voltage is shifted up by ± 1.65 V_REF to accommodate positive and negative current swings. A ± 400 -mV voltage drop across the sense resistor corresponds to a measured current range of ± 8 amps. AMP_OUT signal is internally connected to the over current comparator of the MC33937A and provides an over-current triggering function.

The shunt resistor is represented by a 0.05-ohm resistance WELWYN SMD precision resistor, the same as the phase current measurement resistors.

3.7 Safety Functions

The MC33937A provides over-current and under voltage functions. Bus current feedback is filtered to remove spikes, and this signal is fed into the MC33937A current comparator input ITRIP. Therefore, when bus current exceeds reference value (set by trimmer R37), all six output transistors are switched off. Once a fault state has been detected, all six gate drivers are off until the fault state is cleared in by the CLINTO command or by switching the board off. Then you can switch the power stage on. The under voltage function is implemented internally. The MC33937A's supply voltage is sensed internally. If this voltage is lower than 8V, the hold off circuit is evaluated and an interrupt is generated if set

The MC33927 safety functions keep the driver operating properly and within safe limits. Current limiting by itself, however, does not necessarily ensure that a board is operating within safe thermal limits. The MC33927 has a thermal warning feature. If the temperature rises above 170°C on one of the three detectors, then an interrupt is generated if set.

The MC33927 driver has also other safety features such as desaturation detection, phase error, framing error, write error after the lock and exiting RST. All these features can be configured through SPI to trigger interrupts. Detail information is available in the driver datasheet.

3.8 Back EMF Signals

Back EMF signals are included to support sensorless algorithms for brushless d.c. motors and dead time distortion correction for sinusoidal motors. The raw phase voltage is scaled down by a voltage divider consisting of R47 and R48 (phase A). Output from this divider produces back EMF sense voltage BEMF_SENSE_A. Resistor values are chosen such that a 36.3-volt of phase voltage corresponds to a 3.3-volt A/D input. BEMF_SENSE_A is terminated to the elevator main port.

3.9 Phase Current Sensing

Sampling resistors provide phase current information for all three phases. Because these resistors sample current in the lower phase legs, they do not directly measure phase current. However, given



phase voltages for all three phases, phase current can be constructed mathematically from the lower phase leg values. This information can be used in vector-control algorithms for AC induction motors.. Referencing the sampling resistors to the negative motor rail makes the measurement circuitry straightforward and inexpensive. Current is sampled by resistor R7 (phase A) and amplified by the differential amplifier U5A. This circuit provides a voltage output suitable for sampling on A/D inputs. An AD8656 is used as a differential amplifier. With R38 = R41 and R39 = R42 and R40 = R46, the gain is given by:

A = R40/(R39+R38)

The input voltage is shifted up by +1.65V_REF to accommodate both positive and negative current swings. A ± 400 -mV voltage drop across the shunt resistor corresponds to a measured current range of ± 8 amps. As a source for $\pm 1.65V$ _REF, a precision shunt voltage reference LM4041.

3.10 LED Indication

This module also contains 8 LEDs as indicators:

- D5 User LED diode for user defined purposes, activated on high level..
- D7 Indicates that the +5V level is properly generated.
- D14 PWM AT indication LED, activated on low level.
- D16 PWM AB indication LED, activated on high level.
- D18 PWM BT indication LED, activated on low level.
- D15 PWM_BB indication LED, activated on high level.
- D17 PWM CT indication LED, activated on low level.
- D19 PWM CB indication LED, activated on high level.

3.11 Encoder / Hall-Effect Interace

The TWR-MC-LV3PH contains an Encoder/Hall-Effect interface. The circuit is designed to accept +3.3V to +5.0V encoder or Hall-Effect sensor inputs. Input noise filtering is supplied on the input path for the Encoder/Hall-Effect interface. Filtered signals are then connected to the elevator main port.

3.12 Brake

An external brake resistor can be connected to dissipate re-generative motor energy during periods of active deceleration or rapid reversal. Under these conditions, motor back EMF adds to the dc bus voltage. Without a means to dissipate excess energy, an overvoltage condition could easily occur. With an external dissipative resistor connected to J4, it serves to dissipate energy across the dc bus. MOSEFET Q8 is turned on by software when the bus voltage sensing circuit exceeds level set in software.

Power dissipation capability depends, of course, on the capability of the externally connected dissipative resistor.

The MIC4127YME is a dual MOSFET pre-driver 5.0V tolerant. This board uses its A channel to drive the braking resistance MOSFET.



4 Signal Description

This section provides more details about signals of input / output connectors and jumpers of the TWR-TWR-MC-LV3PH.

4.1 Power Supply Input Connector J1

The power supply input connector, labeled J1, accepts d.c. voltages from 12V to 50V/8A max. The J1 connector is a 2.1mm power jack for plug-in type DC power supply connections. The board has reverse polarity protection.

Power applied to the board is indicated by a green color +5V LED.

4.2 External Brake Resistor Interface J4

A brake resistor can be connected to brake-resistor connector J4. The brake resistor allows power dissipation and can be controlled through the Brake control signal.

4.3 Motor Connector J5

Power outputs to the motor are located on connector J1. Phase outputs are labeled A, B, and C. Table 2 contains pin assignments. On a permanent magnet synchronous motor, any one of the three phase windings can be connected here. For brushless d.c. motors, you must connect the wire colour coded for phase A into the connector terminal labeled A, and so on for phase B and phase C.

Pin #	Signal Name	Description
1	Α	Supplies power to motor phase A
2	В	Supplies power to motor phase B
3	С	Supplies power to motor phase C

Table 2 – Motor Connector J5 – Signal Description

4.4 Encoder / Hall-effect Interface J8

The Encoder/Hall-Effect interface J8 is located on the right edge of the board. The circuit is designed to accept +3.3V to +5V encoder or Hall-Effect sensor inputs. Input noise filtering is supplied on the input path to the Encoder/Hall-Effect interface. Table 3 shows the Encoder/Hall-Effect interface pin description.

Pin #	Signal Name	Description
1	+5.0V	Supplies power from the board to either ENCODER or Hall sensors



2	GND	ENCODER or Hall sensors ground
3	Phase A	ENCODER or Hall Phase A input
4	Phase B	ENCODER or Hall Phase B input
5	Phase C	ENCODER or Hall Phase C input

Table 3 – Encoder / Hall-effect Interface J8 – Signal Description

4.5 Elevator Connections

The TWR-MC-LV3PH features two expansion card-edge connectors that interface to Elevator boards in a Tower System: the Primary and Secondary Elevator connectors. Table provides the pinout for the Primary and Secondary Elevator Connector. An "X" in the "Used" column indicated that there is a connection from the TWR-MC-LV3PH to that pin on the Elevator connector. An "X" in the "Jmp" column indicates that a jumper is available that can configure or isolate the connection from the Elevator connector.

Table 4 - TWR-MC-LV3PH Primary Elevator Connector Pinout

		TV	WR-MC-LV3	PH Pr	imary (Connector			
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B1	5V	5.0V Power	Х		A1	5V	5.0V Power	Х	
B2	GND	Ground	х		A2	GND	Ground	х	
В3	3.3V	3.3V Power	х		А3	3.3V	3.3V Power	х	
B4	ELE_PS_SENSE	Elevator Power Sense	х		A4	3.3V	3.3V Power	х	
B5	GND	Ground	х		A5	GND	Ground	х	
В6	GND	Ground	х		A6	GND	Ground	х	
В7	SDHC_CLK / SPI1_CLK				A7	SCL0			
B8	SDHC_D3 / SPI1_CS1_b				A8	SDA0			
В9	SDHC_D3 / SPI1_CSO_b				A9	GPIO9 / CTS1			
B10	SDHC_CMD / SPI1_MOSI				A10	GPIO8 / SDHC_D2			
B11	SDHC_D0 / SPI1_MISO				A11	GPIO7 / SD_WP_DET			
B12	ETH_COL				A12	ETH_CRS			
B13	ETH_RXER				A13	ETH_MDC			
B14	ETH_TXCLK				A14	ETH_MDIO			
B15	ETH_TXEN				A15	ETH_RXCLK			
B16	ETH_TXER				A16	ETH_RXDV			
B17	ETH_TXD3				A17	ETH_RXD3			
B18	ETH_TXD2				A18	ETH_RXD2			
B19	ETH_TXD1				A19	ETH_RXD1			
B20	ETH_TXD0				A20	ETH_RXD0			
B21	GPIO1 / RTS1	USER_LED	Х		A21	SSI_MCLK			
B22	GPIO2 / SDHC_D1	BRAKE_CONTROL	Х		A22	SSI_BCLK			
B23	GPIO3				A23	SSI_FS			
B24	CLKIN0				A24	SSI_RXD			
B25	CLKOUT1				A25	SSI_TXD			
B26	GND	Ground	х		A26	GND	Ground	х	



		TWR	-MC-LV3	BPH Pr	imary (Connector			
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B27	AN7				A27	AN3			
B28	AN6	I_SENCE_C / I_SENSE_DCB	х	х	A28	AN2	I_SENSE_C / BEMF_SENSE_C	х	х
B29	AN5	I_SENCE_A / V_SENSE_DCB_HALF	х	х	A29	AN1	I_SENSE_B / BEMF_SENSE_B	х	х
B30	AN4	V_SENSE_DCB	х		A30	AN0	I_SENSE_A / BEMF_SENSE_A	х	х
B31	GND	Ground	Х		A31	GND	Ground	х	
B32	DAC1				A32	DAC0			
B33	TMR3				A33	TMR1	ENC_PHASE_B	х	
B34	TMR2	ENC_INDEX	х		A34	TMR0	ENC_PHASE_A	х	
B35	GPIO4				A35	GPIO6			
B36	3.3V	3.3V Power	Х		A36	3.3V	3.3V Power	х	
B37	PWM7				A37	PWM3	PWM_BB	х	
B38	PWM6				A38	PWM2	PWM_BT	х	
B39	PWM5	PWM_CB	Х		A39	PWM1	PWM_AB	х	
B40	PWM4	PWM_CT	Х		A40	PWM0	PWM_AT	х	
B41	CANRX0				A41	RXD0			
B42	CANTX0				A42	TXD0			
B43	1WIRE				A43	RXD1			
B44	SPI0_MISO (IO1)	MISO	Х		A44	TXD1			
B45	SPI0_MOSI (IO0)	MOSI	Х		A45	VSS	GNDA_ELV	х	х
B46	SPIO_CSO_b	/SS	Х		A46	VDDA	VDDA_ELV	х	Х
B47	SPIO_CS1_b	/SS	Х		A47	VREFA1	_		
B48	SPIO_CLK	SCLK	Х		A48	VREFA2			
B49	GND	Ground	х		A49	GND	Ground	х	
B50	SCL1	- Ground			A50	GPIO14			
B51	SDA1				A51	GPIO15			
B52	GPIO5 / SPIO HOLD (IO3)	DRV EN	х		A52	GPIO16 / SPIO_WP (IO2)			
B53	USB0_DP_PDOWN				A53	GPIO17			
B54	USB0_DM_PDOWN				A54	USB0_DM			
B55	IRQ_H				A55	 USB0_DP			
B56	IRQ_G				A56	USBO_ID			
B57	IRQ_F				A57	USBO_VBUS			
B58	IRQ_E				A58	TMR7			
B59	IRQ_D				A59	TMR6			
B60	IRQ_C				A60	TMR5			
B61	IRQ_B	DRV_INT	х	х	A61	TMR4			
B62	IRQ_A	DRV_OC	X	X	A62	RSTIN_b			
B63	EBI_ALE / EBI_CS1_b				A63	RSTOUT_b	RESET	х	
B64	EBI_CSO_b				A64	CLKOUT0		^	
B65	GND	Ground	х		A65	GND	Ground	х	
B66	EBI_AD15	Ground	^		A66	EBI_AD14	Ground	^	
B67	EBI_AD15				A67	EBI_AD14			
B68	EBI_AD17				A67	EBI_AD13			
B69	EBI_AD18				A69	EBI_AD11			



	TWR-MC-LV3PH Primary Connector								
Pin	Name	Usage	Used	Jmp	Pin	Name	Usage	Used	Jmp
B70	EBI_AD19				A70	EBI_AD10			
B71	EBI_R/W_b				A71	EBI_AD9			
B72	EBI_OE_b				A72	EBI_AD8			
B73	EBI_D7				A73	EBI_AD7			
B74	EBI_D6				A74	EBI_AD6			
B75	EBI_D5				A75	EBI_AD5			
B76	EBI_D4				A76	EBI_AD4			
B77	EBI_D3				A77	EBI_AD3			
B78	EBI_D2				A78	EBI_AD2			
B79	EBI_D1				A79	EBI_AD1			
B80	EBI_D0				A80	EBI_AD0			
B81	GND	Ground	х		A81	GND	Ground	х	
B82	3.3V	3.3V Power	Х		A82	3.3V	3.3V Power	х	

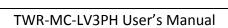




Table 5 - TWR-MC-LV3PH Secondary Elevator Connector Pinout

	TWR-SER2 Secondary Connector								
Pin	Name		Jm	p Pin	Name	Usage	Used	Jmp	
D1	5V			C1	5V				
D2	GND	Ground	х	C2	GND	Ground	х		
D3	3.3V			C3	3.3V				
D4	ELE_PS_SENSE			C4	3.3V				
D5	GND	Ground	х	C5	GND	Ground	х		
D6	GND	Ground	х	C6	GND	Ground	х		
D7	SPI2_CLK			C7	SCL2				
D8	SPI2_CS1_b			C8	SDA2				
D9	SPI2_CS0_b			C9	GPIO25				
D10	SPI2_MOSI			C10	ULPI_STOP				
D11	SPI2_MISO			C11	ULPI_CLK				
D12	ETH_COL			C12	GPIO26				
D13	ETH_RXER			C13	ETH_MDC				
D14	ETH_TXCLK			C14	ETH_MDIO				
D15	ETH_TXEN			C15	ETH_RXCLK				
D16	GPIO18			C16	ETH_RXDV				
D17	GPIO19 / SDHC_D4			C17	GPIO27 / SDHC_D6				
D18	GPIO20 / SDHC_D5			C18	GPIO28 / SDHC_D7				
D19	ETH_TXD1			C19	ETH_RXD1				
D20	ETH_TXD0			C20	ETH_RXD0				
D21	ULPI_NEXT / USB1_DM			C21	ULPI_DATA0 / USB3_DM				
D22	ULPI_DIR / USB1_DP			C22	ULPI_DATA1 / USB3_DP				
D23	UPLI_DATA5 / USB2_DM			C23	ULPI_DATA2 / USB4_DM				
D24	ULPI_DATA6 / USB2_DP			C24	ULPI_DATA3 / USB4_DP				
D25	ULPI_DATA7			C25	ULPI_DATA4				
D26	GND	Ground	х	C26	GND	Ground	х		
D27	LCD_HSYNC / LCD_P24			C27	AN11				
D28	LCD_VSYNC / LCD_P25			C28	AN10				
D29	AN13			C29	AN9				
D30	AN12			C30	AN8				
D31	GND	Ground	х	C31	GND	Ground	х		
D32	LCD_CLK / LCD_P26			C32	GPIO29				
D33	TMR11			C33	TMR9				
D34	TMR10			C34	TMR8				
D35	GPIO21			C35	GPIO30				
D36	3.3V			C36	3.3V				
D37	PWM15			C37	PWM11				
D38	PWM14			C38	PWM10				
D39	PWM13			C39	PWM9				
D40	PWM12			C40	PWM8				
D41	CANRX1			C41	RXD2 / TSI0				
D42	CANTX1			C42	TXD2 / TSI1				



	TWR-SER2 Secondary Connector									
Pin	Name			Jmp	Pin	Name	Usage	Used	Jmp	
D43	GPIO22				C43	RTS2 / TSI2				
D44	LCD_OE / LCD_P27				C44	CTS2 / TSI3				
D45	LCD_D0 / LCD_P0				C45	RXD3 / TSI4				
D46	LCD_D1/LCD_P1				C46	TXD3 / TSI5				
D47	LCD_D2 / LCD_P2				C47	RTS3 / TSI6				
D48	LCD_D3 / LCD_P3				C48	CTS3 / TSI7				
D49	GND	Ground	х		C49	GND	Ground	х		
D50	GPIO23				C50	LCD_D4 / LCD_P4				
D51	GPIO24				C51	LCD_D5 / LCD_P5				
D52	LCD_D12 / LCD_P12				C52	LCD_D6 / LCD_P6				
D53	LCD_D13 / LCD_P13				C53	LCD_D7 / LCD_P7				
D54	LCD_D14 / LCD_P14				C54	LCD_D8 / LCD_P8				
D55	IRQ_P / SPI2_CS2_b				C55	LCD_D9 / LCD_P9				
D56	IRQ_O / SPI2_CS3_b				C56	LCD_D10 / LCD_P10				
D57	IRQ_N				C57	LCD_D11 / LCD_P11				
D58	IRQ_M				C58	TMR16				
D59	IRQ_L				C59	TMR15				
D60	IRQ_K				C60	TMR14				
D61	IRQ_J				C61	TMR13				
D62	IRQ_I				C62	LCD_D15 / LCD_P15				
D63	LCD_D18 / LCD_P18				C63	LCD_D16 / LCD_P16				
D64	LCD_D19 / LCD_P19				C64	LCD_D17 / LCD_P17				
D65	GND	Ground	х		C65	GND	Ground	Х		
D66	EBI_AD20 / LCD_P42				C66	EBI_BE_32_24_b / LCD_P28				
D67	EBI_AD21 / LCD_P43				C67	EBI_BE_23_16_b / LCD_P29				
D68	EBI_AD22 / LCD_P44				C68	EBI_BE_15_8_b / LCD_P30				
D69	EBI_AD23 / LCD_P45				C69	EBI_BE_7_0_b / LCD_P31				
D70	EBI_AD24 / LCD_P46				C70	EBI_TSIZEO / LCD_P32				
D71	EBI_AD25 / LCD_P47				C71	EBI_TSIZE1 / LCD_P33				
D72	EBI_AD26 / LCD_P48				C72	EBI_TS_b / LCD_P34				
D73	EBI_AD27 / LCD_P49				C73	EBI_TBST_b / LCD_P35				
D74	EBI_AD28 / LCD_P50				C74	EBI_TA_b / LCD_P36				
D75	EBI_AD29 / LCD_P51				C75	EBI_CS4_b / LCD_P37				
D76	EBI_AD30 / LCD_P52				C76	EBI_CS3_b / LCD_P38				
D77	EBI_AD31 / LCD_P53				C77	EBI_CS2_b / LCD_P39				
D78	LCD_D20 / LCD_P20				C78	EBI_CS1_b / LCD_P40				
D79	LCD_D21 / LCD_P21				C79	GPIO31 / LCD_P41				
D80	LCD_D22 / LCD_P22				C80	LCD_D23 / LCD_P23				
D81	ETH_COL	Ground	х		C81	GPIO26	Ground	х		
D82	ETH_RXER				C82	ETH_MDC				



5 Configuration Settings

There are several jumpers provided for isolation, configuration, and feature selection. Refer to the following table for details. The default installed jumper settings are shown in *bold*.

5.1 Zero-Ohm Resistors

Resistor C	ptions	Setting	Description
R61	MC33937A VPWR	Placed	Enables DCB_POS voltage to MC33937A
KOI	MC33937A VPVVK	Unplaced	Disables DCB_POS voltage to MC33937A
R86	U6B output	Placed	Enables I_SENSE_DCB signal as output of U6B
Noo	OOB Output	Unplaced	Disables I_SENSE_DCB signal as output of U6B
R88	MC33937A AMP OUT	Placed	Enables I_SENSE_DCB signal as output of MC33937A
Koo	INIC33937A AMIF_OUT	Unplaced	Disables I_SENSE_DCB signal as output of MC33937A
R89	MC33937A INT output	Placed	Enables DRV_INT connection to elevator
Koa	MC33937A INT Output	Unplaced	Disables DRV_INT connection to elevator
R89	MC33937A over current output	Placed	Enables DRV_OC connection to elevator
Ros	MC33937A over current output	Unplaced	Disables DRV_OC connection to elevator
R95	SPI0 CS0	Placed	Enables Chip Select 0 connection to elevator
1,90	3510_030	Unplaced	Disables Chip Select 0 connection to elevator
R96	SPI0 CS1	Placed	Enables Chip Select 1 connection to elevator
K90	3F10_C31	Unplaced	Disables Chip Select 1 connection to elevator

Table 5 - TWR-MC-LV3PH Jumper Settings

5.2 Jumper Settings

Jumper O	ptions	Setting	Description
10	VDDA Source Select	1-2	Internal on-board source of analog 3.3V
J2	VDDA Source Select	2-3	Elevator source of analog 3.3V
J3	VSSA Source Select	1-2	Internal on-board source of analog GND
J3	V33A 3001Ce Select	2-3	Elevator source of analog GND
J10	AN6 Signal Select	1-2	Phase C current signal
310	And Signal Select	2-3	DC-Bus current signal
J11	AN5 Signal Select	1-2	Phase A current signal
JII	ANS Signal Select	2-3	DC-Bus_half voltage signal
J12	AN2 Signal Select	1-2	Phase C current signal
J12	ANZ Signal Select	2-3	Back EMF phase C
J13	AN1 Signal Select	1-2	Phase B current signal
010	ANT Signal Select	2-3	Back EMF phase B
J14	AN0 Signal Select	1-2	Phase A current signal
314	ANO Signal Select	2-3	Back EMF phase A

Table 6 - TWR-MC-LV3PH Jumper Settings

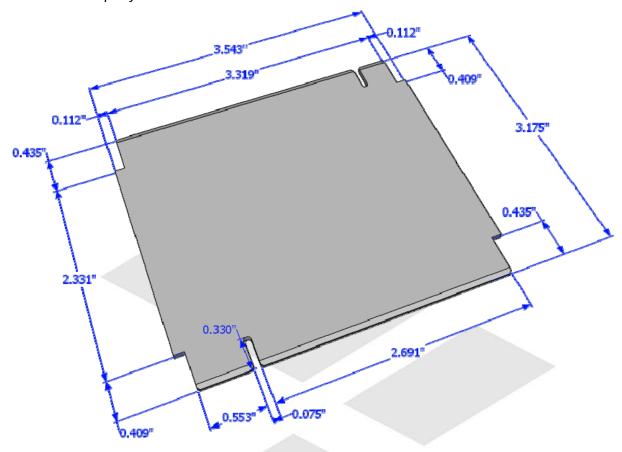






6 Mechanical Form Factor

The TWR-MC-LV3PH is designed for the Freescale Tower System as a side mounting peripheral and complies with the electrical and mechanical specification as described in *Freescale Tower Electromechanical Specification*.





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