56F807

Evaluation Module User Manual

56F800
16-bit Digital Signal Controllers

DSP56F807EVMUM
Rev. 3
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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Preface

This reference manual describes in detail the hardware on the 56F807 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F807 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction -** provides an overview of the EVM and its features.
- **Chapter 2, Technical Summary -** describes in detail the 56F807EVM hardware.
- **Appendix A, 56F807EVM Schematics -** contains the schematics of the 56F807EVM.
- **Appendix B, 56F807EVM Bill of Material -** provides a list of the materials used on the 56F807EVM board.

Suggested Reading

More documentation on the 56F807 and the 56F807EVM kit may be found at URL:

http://www.freescale.com

Notation Conventions

This manual uses the following notational conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{WE}$ $\overline{OE}$	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a “$” symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter “b” attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Bold	Reference sources, paths, emphasis	...see: **http://www.freescale.com**...	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

A/D	Analog-to-Digital
CAN	Controller Area Network; serial communications peripheral and method
CiA	CAN in Automation, an international CAN user's group that coordinates standards for CAN communications protocols
D/A	Digital-to-Analog
EVM	Evaluation Module
GPIO	General Purpose Input and Output Port
IC	Integrated Circuit
JTAG	Joint Test Action Group, a bus protocol/interface used for test and debug
LQFP	Low-profile Quad Flat Pack
MPIO	Multi Purpose Input and Output Port ; shares package pins with other peripherals on the chip and can function as a GPIO
OnCE™	On-Chip Emulation, a debug bus and port created by Freescale to enable designers to create a low-cost hardware interface for a professional-quality debug environment
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface Port
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter

References

The following sources were referenced to produce this manual:

[1] *DSP56800 Family Manua*l, DSP56800FM, Freescale Semiconductor

[2] *DSP56F801/803/805/807 User's Manual*, DSP56F801-7UM, Freescale Semiconductor

[3] *56F807 Technical Data*, DSP56F807, Freescale Semiconductor

[4] *CiA Draft Recommendation DR-303-1, Cabling and Connector Pin Assignment*, Version 1.0, CAN in Automation

[5] *CAN Specification 2.0B*, BOSCH or CAN in Automation

Chapter 1
Introduction

The 56F807EVM is used to demonstrate the abilities of the 56F807 and to provide a hardware tool allowing the development of applications that use the 56F807.

The 56F807EVM is an evaluation module board that includes a 56F807 part, peripheral expansion connectors, external memory and a CAN interface. The expansion connectors are for signal monitoring and user feature expandability.

The 56F807EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800 architecture. The tools and examples provided with the 56F807EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/OnCE™ port. The breakpoint features of the OnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full-speed, until the break conditions are satisfied. The ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the hybrid controller's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the chip are available to the user.

1.1 56F807EVM Architecture

The 56F807EVM facilitates the evaluation of various features present in the 56F807 part and can be used to develop real-time software and hardware products based on the

56F807. The 56F807EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the customer's application-specific device(s). The 56F807EVM is flexible enough to allow a user to fully exploit the 56F807's features to optimize the performance of their product, as shown in **Figure 1-1**.

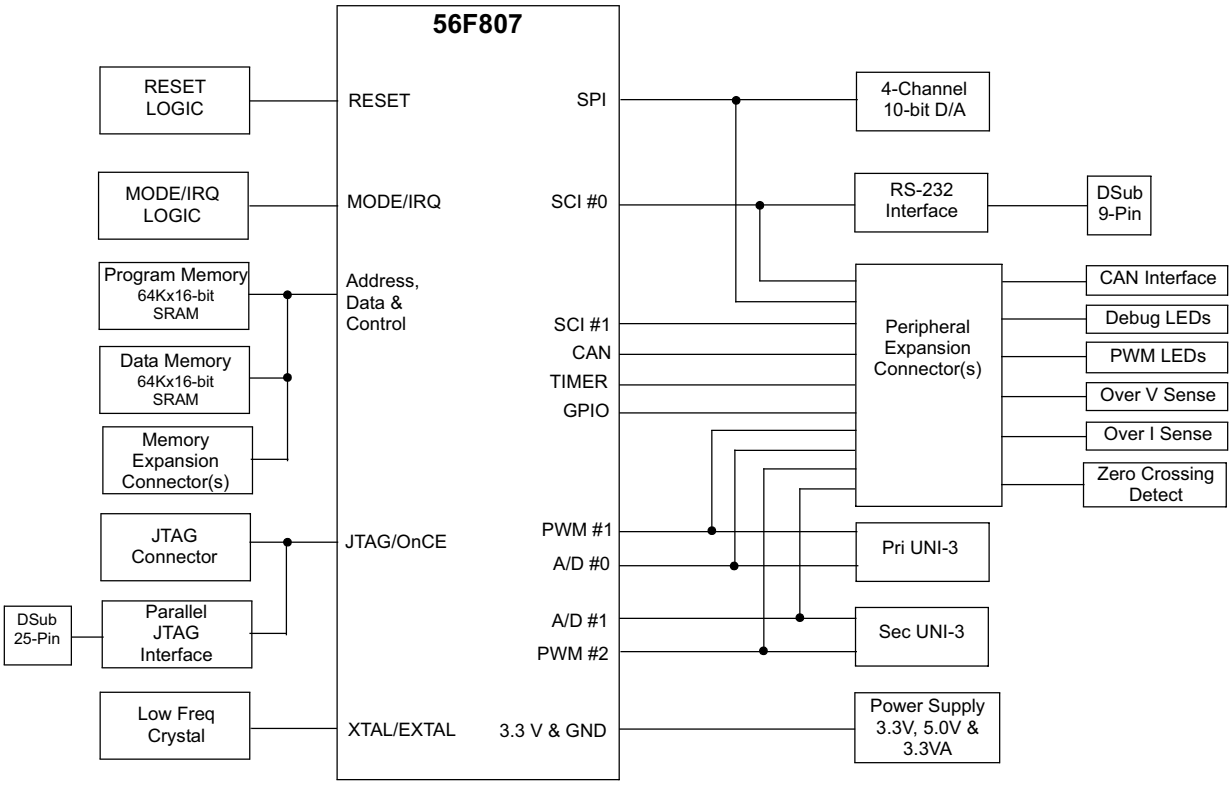

Figure 1-1. Block Diagram of the 56F807EVM

1.2 56F807EVM Configuration Jumpers

Seventeen jumper groups, (JG1-JG17), shown in **Figure 1-2**, are used to configure various features on the 56F807EVM board. **Table 1-1** describes the default jumper group settings.

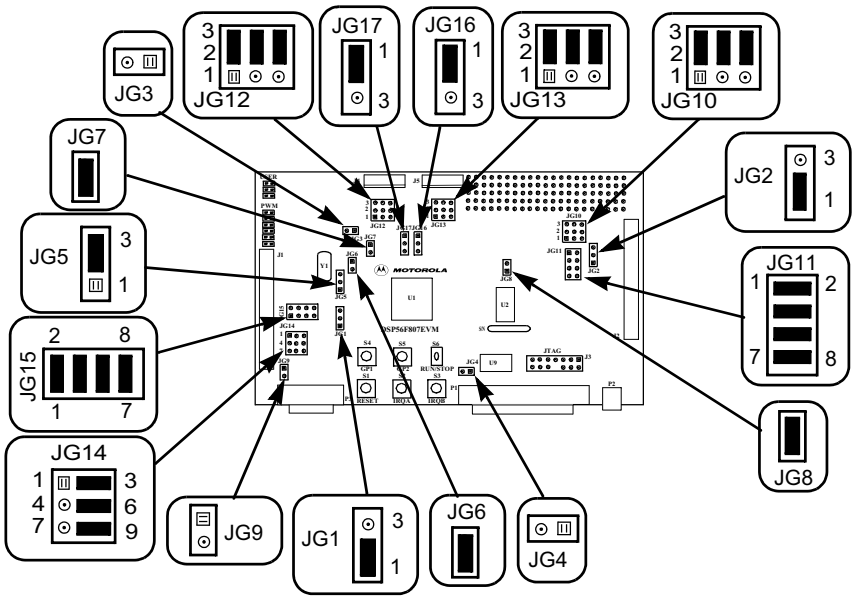

Figure 1-2. 56F807EVM Jumper Reference

Table 1-1. 56F807EVM Default Jumper Options

Jumper Group	Comment	Jumper Connections
JG1	Primary UNI-3 Phase A Over-Current Selected for FAULTA1	1–2
JG2	Secondary UNI-3 Phase A Over-Current Selected for FAULTB1	1–2
JG3	CAN termination unselected	NC
JG4	Enable on-board Parallel JTAG Host/Target Interface	NC
JG5	Use on-board EXTAL crystal input for oscillator	2–3
JG6	Use on-board XTAL crystal input for oscillator	1–2
JG7	Selects device's Mode 0 operation upon exit from reset	1-2
JG8	Enable on-board SRAM	1–2
JG9	Disable RS-232 output	NC
JG10	Secondary UNI-3 3-Phase Current Sense Selected as inputs to A/D	2–3, 5–6 & 8–9
JG11	Secondary UNI-3 serial selected	1–2, 3–4, 5–6 & 7–8
JG12	Primary Encoder Input Selected	2–3, 5–6 & 8–9
JG13	Secondary Encoder Input Selected	2–3, 5–6 & 8–9
JG14	Primary UNI-3 3-Phase Current Sense Selected as inputs to A/D	2–3, 5–6 & 8–9
JG15	Primary UNI-3 serial selected	1–2, 3–4, 5–6 & 7–8
JG16	PD0 input selected as a high input	1–2
JG17	PD1 input selected as a high input	1–2

1.3 56F807EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12V DC power supply to the 56F807EVM board.

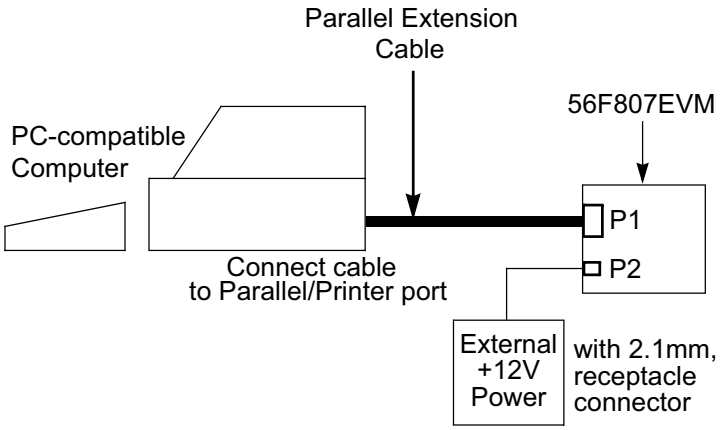

Figure 1-3. Connecting the 56F807EVM Cables

. Perform the following steps to connect the 56F807EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer
2. Connect the other end of the parallel extension cable to P1, shown in **Figure 1-3**, on the 56F807EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12V DC, 4.0A power supply is not plugged into a 120V AC power source
4. Connect the 2.1mm output power plug from the external power supply into P2, shown in **Figure 1-3**, on the 56F807EVM board.
5. Apply power to the external power supply. The green Power-On LED, LED10, will illuminate when power is correctly applied.

Chapter 2
Technical Summary

The 56F807EVM is designed as a versatile hybrid controller development card for developing real-time software and hardware products to support a new generation of applications in digital and wireless messaging, servo and motor control, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F807 controller, combined with the on-board 64K × 16-bit external program static RAM (SRAM), 64K × 16-bit external data SRAM, CAN interface, Hall-Effect/Quadrature Encoder interface, motor zero crossing logic, motor bus over-current logic, motor bus over-voltage logic and parallel JTAG interface, makes the 56F807EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F807 processor.

The main features of the 56F807EVM, with board and schematic reference designators, include:

- 56F807 16-bit +3.3V hybrid controller operating at 80MHz [U1]
- External fast static RAM (FSRAM) memory [U2], configured as:
  - 64K×16 bits of Program memory with 0 wait states at 70MHz
  - 64K×16 bits of Data memory with 0 wait states at 70MHz
- 4-Channel 10-bit Serial D/A, SPI for real-time user data display [U14]
- 8.00MHz crystal oscillator for frequency generation [Y1]
- Optional external oscillator frequency input connector [JG5 and JG6]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J3]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P1]
- RS-232 interface for easy connection to a host processor [U13 and P3]
- CAN interface for high speed, 1.0Mbps, communications [U8 and J24]
- CAN bypass and bus termination [J25 and JG3]
- Connector to allow the user to connect his own SCI0 / MPIO-compatible peripheral [J15]

- Connector to allow the user to connect his own SCI1 /MPIO-compatible peripheral [J14]
- Connector to allow the user to connect his own SPI / MPIO-compatible peripheral [J13]
- Connector to allow the user to connect his own PWMA or MPIO-compatible peripheral [J10]
- Connector to allow the user to connect his own PWMB / MPIO-compatible peripheral [J11]
- Connector to allow the user to connect his own CAN physical layer peripheral [J16]
- Connector to allow the user to connect his own Timer A / MPIO-compatible peripheral [J18]
- Connector to allow the user to connect his own Timer B / MPIO-compatible peripheral [J21]
- Connector to allow the user to connect his own Timer C / MPIO-compatible peripheral [J19]
- Connector to allow the user to connect his own Timer D / MPIO-compatible peripheral [J22]
- Connector to allow the user to attach his own Port B GPIO-compatible peripheral [J20]
- Connector to allow the user to attach his own Port D GPIO-compatible peripheral [J23]
- Connector to allow the user to attach his own Port E GPIO-compatible peripheral [J17]
- Connector to allow the user to attach their own A/D Port A-compatible peripheral [J9]
- Connector to allow the user to attach his own A/D Port B-compatible peripheral [J12]
- 56F807's external memory expansion connectors [J6, J7 and J8]
- On-board power regulation from an external +12V DC-supplied power input [P2]
- Light Emitting Diode (LED) power indicator [LED10]
- Three on-board real-time user debugging LEDs [LED1-3]
- Six on-board Primary PWM monitoring LEDs [LED4-9]
- Primary UNI-3 Motor interface [J1]
  - Encoder/Hall-Effect interface and selector [JG12]
  - Over-Voltage sensing [U16]
  - Over-Current sensing [U3]
  - Phase Current sensing [U3 and U4]
  - Back-EMF sensing and selector [JG14]

  - Temperature sensing
  - Zero Crossing detection and selector [JG14]
  - Pulse Width Modulation
- Secondary UNI-3 Motor interface [J2]
  - Encoder/Hall-Effect interface and selector [JG13]
  - Over-Voltage sensing [U16]
  - Over-Current sensing [U6]
  - Phase Current sensing [U5 and U6]
  - Back-EMF sensing and selector [JG10]
  - Temperature sensing
  - Zero Crossing detection and selector [JG10]
  - Pulse Width Modulation
- Manual RESET push-button [S1]
- Manual interrupt push-button for $\overline{\text{IRQA}}$ [S2]
- Manual interrupt push-button for $\overline{\text{IRQB}}$ [S3]
- General purpose push-button on GPIO PD3 [S4]
- General purpose push-button on GPIO PD4 [S5]
- General purpose toggle switch for RUN/STOP control(PD5) [S6]
- General purpose jumper on GPIO PD0 [JG16]
- General purpose jumper on GPIO PD1 [JG17]

2.1 56F807

The 56F807EVM uses a Freescale DSP56F807FV80 part, designated as U1 on the board and in the schematics. This part will operate at a maximum speed of 80MHz. A full description of the 56F807, including functionality and user information, is provided in these documents:

- *DSP56800 Family Manual*, (DSP56800FM): Provides a detailed description of the core processor, including internal status and control registers and a detailed description of the family instruction set.
- *DSP56F801/803/805/807 User's Manual*, (DSP56F801-7UM): Provides an overview description of the hybrid controller and detailed information about the on-chip

components including the memory and I/O maps, peripheral functionality, and control/status register descriptions for each subsystem.

- *56F807 Technical Data*, (DSP56F807)**:** Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements and available packaging.

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

http://www.freescale.com

2.2 Program and Data Memory

The 56F807EVM uses one bank of 128K×16-bit Fast Static RAM (GSI GS72116, labeled U2) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-1**. This physical memory bank is split into two logical memory banks of 64Kx16-bits: one for Program memory and the other for Data memory. By using the controller's program strobe, $\overline{PS}$, signal line along with the memory chip's A0 signal line, half of the memory chip is selected when Program memory accesses are requested and the other half of the memory chip is selected when Data memory accesses are requested. This memory bank will operate with zero wait-state accesses while the 56F807 is running at 70MHz. However, when running at 80MHz, the memory bank operates with four wait-state accesses. This memory bank can be disabled by removing the jumper at JG8.

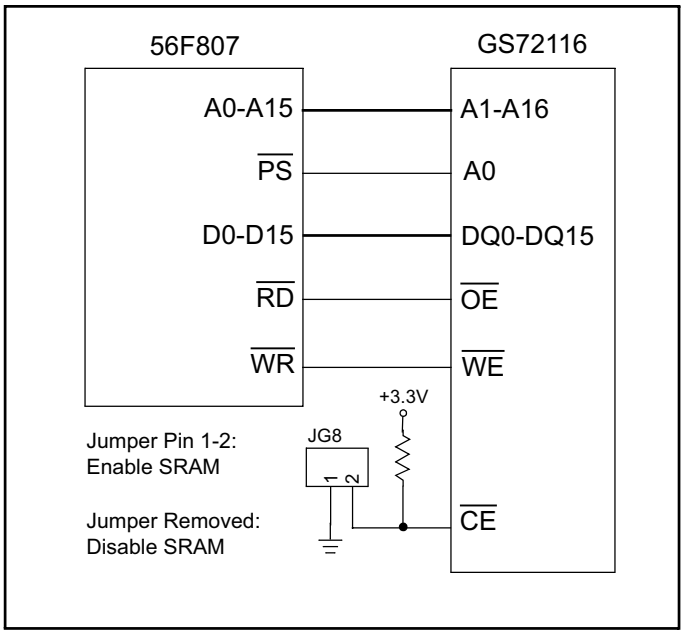

Figure 2-1. Schematic Diagram of the External Memory Interface

2.3 RS-232 Serial Communications

The 56F807EVM provides an RS-232 interface by the use of an RS-232 level converter, (Maxim MAX3245EEAI, designated as U13). Refer to the RS-232 schematic diagram in **Figure 2-2**. The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232-compatible signal levels and connects to the host's serial port via connector P3. Flow control is not provided, but could be implemented using uncommitted GPIO signals. The pin-out of connector P3 is listed in **Table 2-1**. The RS-232 level converter/transceiver can be disabled by placing a jumper at JG9.

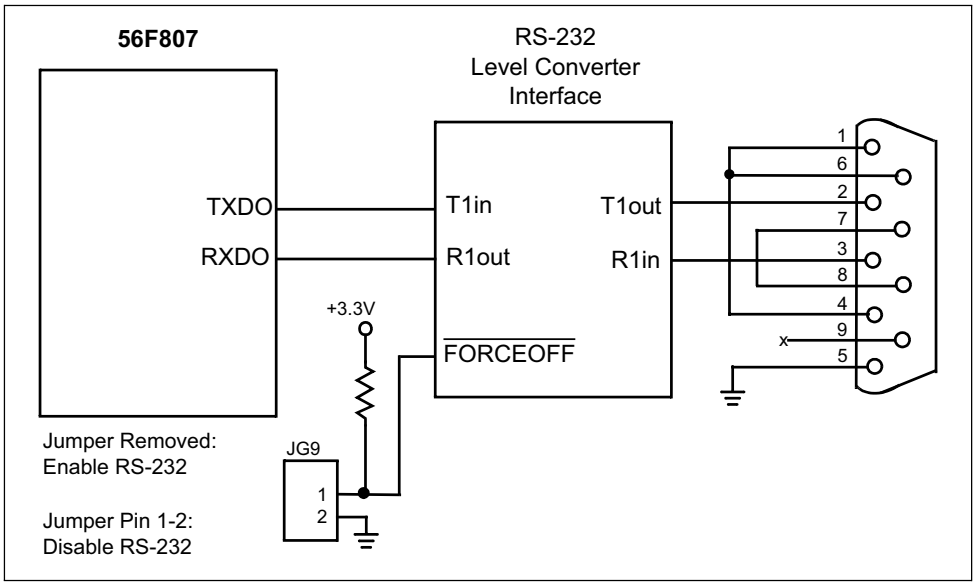

Figure 2-2. Schematic Diagram of the RS-232 Interface

Table 2-1. RS-232 Serial Connector Description

P3			
Pin #	**Signal**	**Pin #**	**Signal**
1	Jumper to 6 & 4	6	Jumper to 1 & 4
2	TXD	7	Jumper to 8
3	RXD	8	Jumper to 7
4	Jumper to 1 & 6	9	N/C
5	GND		

2.4 Clock Source

The 56F807EVM uses an 8.00MHz crystal, Y1, connected to its External Crystal Inputs, EXTAL and XTAL. The 56F807 uses its internal PLL to multiply the input frequency by 10, to achieve its 80MHz maximum operating frequency. An external oscillator source can be connected to the controller by using the oscillator bypass connector, JG6 and JG18; see **Figure 2-3**.

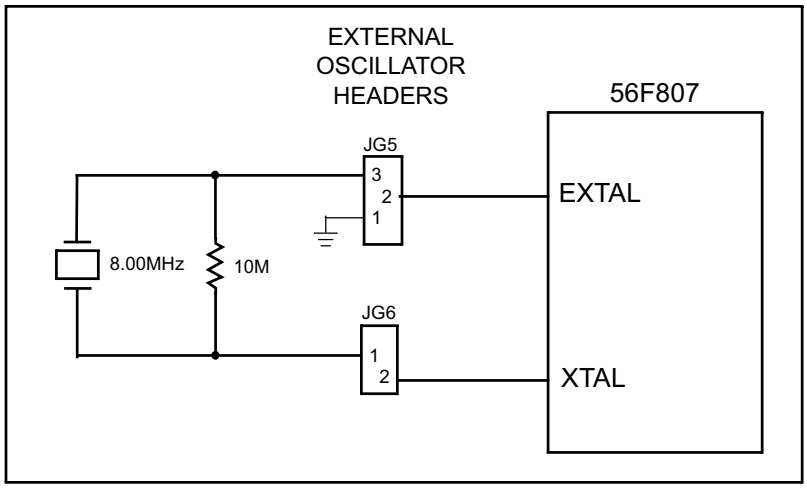

Figure 2-3. Schematic Diagram of the Clock Interface

2.5 Operating Mode

The 56F807EVM provides a boot-up MODE selection jumper, JG7. This jumper is used to select the operating mode of the hybrid controller as it exits RESET. Refer to the DSP56F801/803/805/807 User's Manual for a complete description of the chip's operating modes. **Table 2-2** shows the two operation modes available on the 56F807.

Table 2-2. Operating Mode Selection

Operating Mode	JG7	Comment
0	1–2	Bootstrap from internal memory (GND)
3	No Jumper	Bootstrap from external memory (3.3V)

2.6 Debug LEDs

Three on-board Light-Emitting Diodes, (LEDs), are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-4**. User LED1 is controlled by Port B's PB0 signal. User LED2 is controlled by PB1. User LED3 is controlled by PB2. Setting PB0, PB1 or PB2 to a Logic One value will turn on the associated LED.

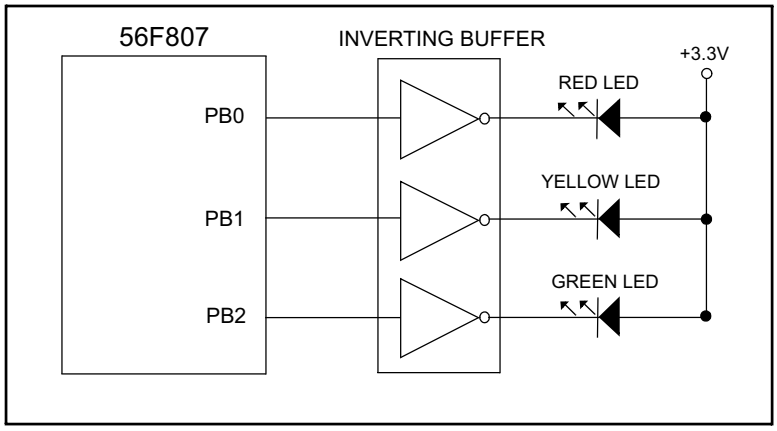

Figure 2-4. Schematic Diagram of the Debug LED Interface

2.7 Debug Support

The 56F807EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

2.7.1 JTAG Connector

The JTAG connector on the 56F807EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F807's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. **Table 2-3** shows the pin-out for this connector.

Table 2-3. JTAG Connector Description

J3			
Pin #	**Signal**	**Pin #**	**Signal**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NC
13	NC	14	$\overline{\text{TRST}}$

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG4. Reference **Table 2-4** for this jumper's selection options.

Table 2-4. Parallel JTAG Interface Disable Jumper Selection

JG4	Comment
No jumpers	On-board Parallel JTAG Interface Enabled
1–2	Disable on-board Parallel JTAG Interface

2.7.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P1, allows the 56F807 to communicate with a Parallel Printer Port on a Windows PC; reference **Figure 2-5**. By using this connector, the user can download programs and work with the 56F807's registers. **Table 2-5** shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG4 should be removed, as shown in **Table 2-4**.

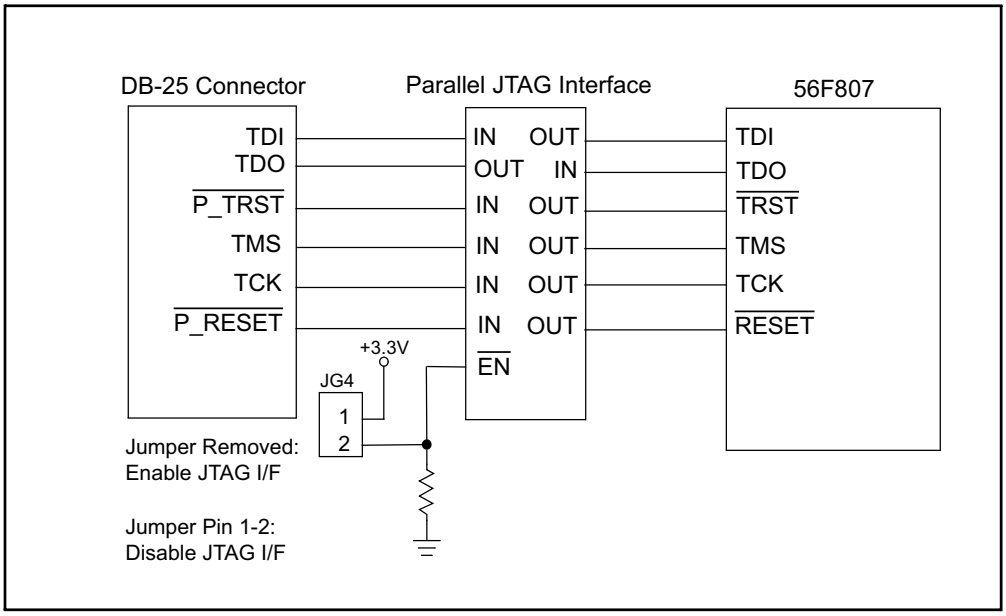

Figure 2-5. Block Diagram of the Parallel JTAG Interface

Table 2-5. Parallel JTAG Interface Connector Description

P1			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	14	NC
2	PORT_RESET	15	PORT_IDENT
3	PORT_TMS	16	NC
4	PORT_TCK	17	NC
5	PORT_TDI	18	GND
6	$\overline{\text{PORT\_TRST}}$	19	GND

Table 2-5. Parallel JTAG Interface Connector Description (Continued)

P1			
Pin #	**Signal**	**Pin #**	**Signal**
7	NC	20	GND
8	PORT_IDENT	21	GND
9	PORT_VCC	22	GND
10	NC	23	GND
11	PORT_TDO	24	GND
12	NC	25	GND
13	PORT_CONNECT		

2.8 External Interrupts

Two on-board push-button switches are provided for external interrupt generation, as shown in **Figure 2-6**. S2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. S3 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQB}}$. These two switches allow the user to generate interrupts for his user-specific programs.

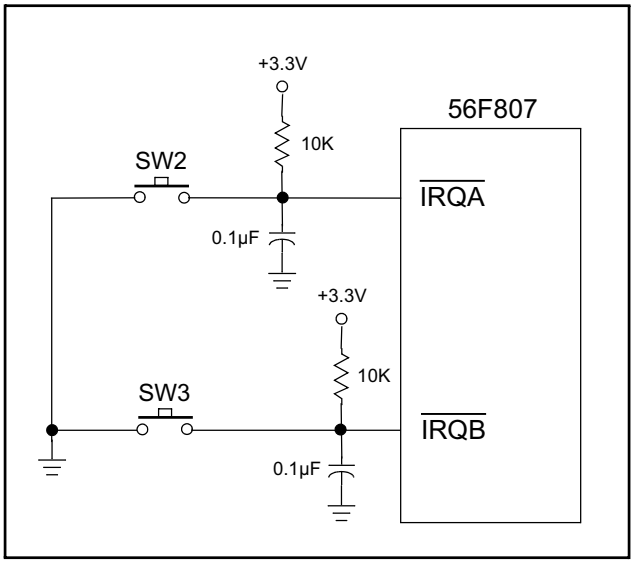

Figure 2-6. Schematic Diagram of the User Interrupt Interface

2.9 Reset

Logic is provided on the 56F807 to generate a clean Power-On RESET signal. Additional, reset logic is provided to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button; refer to **Figure 2-7**.

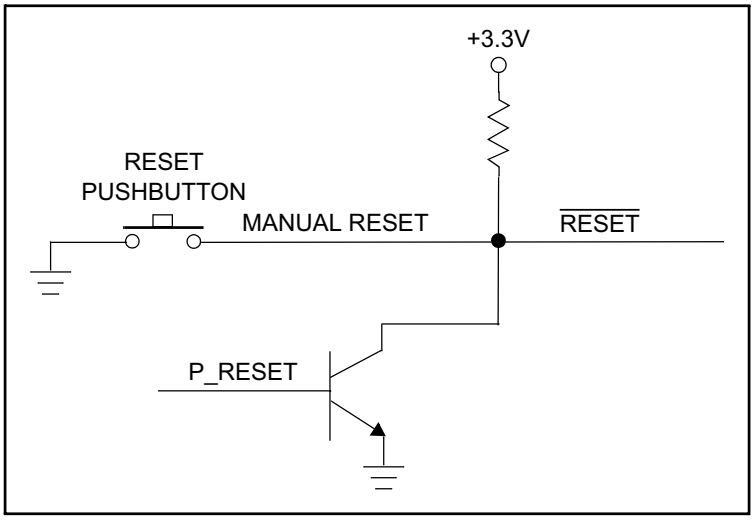

Figure 2-7. Schematic Diagram of the RESET Interface

2.10 Power Supply

The main power input, +12V DC at 4.0A, to the 56F807EVM is through a 2.1mm coax power jack. A 4.0A power supply is provided with the 56F807EVM; however, less than 500mA is required by the EVM. The remaining current is available for user motor control applications when connected to an optional motor power stage board. The 56F807EVM provides +3.3V DC voltage regulation for the hybrid controller, memory, D/A, CAN, parallel JTAG interface and supporting logic; refer to **Figure 2-8**. Power applied to the 56F807EVM is indicated with a Power-On LED, referenced as LED10.

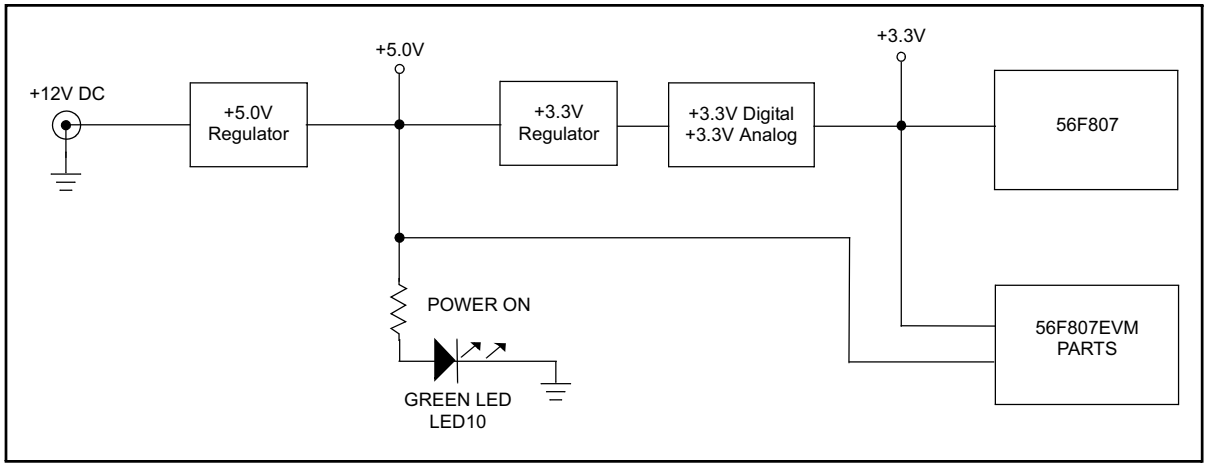

Figure 2-8. Schematic Diagram of the Power Supply

2.11 Primary UNI-3 Interface

Motor control signals from a family of motor driver boards can be connected to the EVM board via the Primary UNI-3 connector/interface. The Primary UNI-3 connector/interface contains all of the signals needed to drive and control the motor drive boards. These signals are connected to various groups of the hybrid controller's input and output ports: A/D, TIMER and PWM Port A. The header, JG14, is used to select between the Back-EMF and Motor Phase Current signals. Refer to **Table 2-6** for the pin-out of the Primary UNI-3 connector, J1.

Table 2-6. Primary UNI-3 Connector Description

J1			
Pin #	**Signal**	**Pin #**	**Signal**
1	PWM_AT	2	Shield
3	PWM_AB	4	Shield
5	PWM_BT	6	Shield
7	PWM_BB	8	Shield
9	PWM_CT	10	Shield
11	PWM_CB	12	GND
13	GND	14	+5.0V DC
15	+5.0V DC	16	Analog +3.3V DC
17	Analog GND	18	Analog GND
19	Analog +15V DC	20	Analog -15V DC
21	Motor DC Bus Voltage Sense	22	Motor DC Bus Current Sense
23	Motor Phase A Current Sense	24	Motor Phase B Current Sense
25	Motor Phase C Current Sense	26	Motor Drive Temperature Sense
27	NC	28	Shield
29	Motor Drive Brake Control	30	Serial COM
31	PFC PWM	32	PFC Inhibit
33	PFC Zero Cross	34	Zero Cross A
35	Zero Cross B	36	Zero Cross C
37	Shield	38	Back-EMF Phase A Sense
39	Back-EMF Phase B Sense	40	Back-EMF Phase C Sense

2.12 Secondary UNI-3 Interface

A Secondary UNI-3 Motor Drive interface is available on the EVM board. Motor control signals from a family of motor driver boards can be connected to the EVM board via the Secondary UNI-3 connector/interface. The Secondary UNI-3 connector/interface contains all of the signals needed to drive and control the motor drive boards. These signals are connected to various groups of the controller's input and output ports: A/D, TIMER and PWM Port B. The header, JG10, is used to select between the Back-EMF and Motor Phase Current signals. Refer to **Table 2-7** for the pin-out of the Secondary UNI-3 connector, J2.

Table 2-7. Secondary UNI-3 Connector Description

J2			
Pin #	**Signal**	**Pin #**	**Signal**
1	PWM_AT	2	Shield
3	PWM_AB	4	Shield
5	PWM_BT	6	Shield
7	PWM_BB	8	Shield
9	PWM_CT	10	Shield
11	PWM_CB	12	GND
13	GND	14	NC
15	NC	16	NC
17	Analog GND	18	Analog GND
19	NC	20	NC
21	Motor DC Bus Voltage Sense	22	Motor DC Bus Current Sense
23	Motor Phase A Current Sense	24	Motor Phase B Current Sense
25	Motor Phase C Current Sense	26	Motor Drive Temperature Sense
27	NC	28	Shield
29	Motor Drive Brake Control	30	Serial COM
31	PFC PWM	32	PFC Inhibit
33	PFC Zero Cross	34	Zero Cross A
35	Zero Cross B	36	Zero Cross C
37	Shield	38	Back-EMF Phase A Sense
39	Back-EMF Phase B Sense	40	Back-EMF Phase C Sense

2.13 General Purpose Switches and Run/Stop Switch

Two general-purpose user pushbutton switches are connected to Port D GPIO signals, PD3 and PD4. A Run/Stop toggle switch is connected to GPIO signal PD5. Refer to **Figure 2-9**.

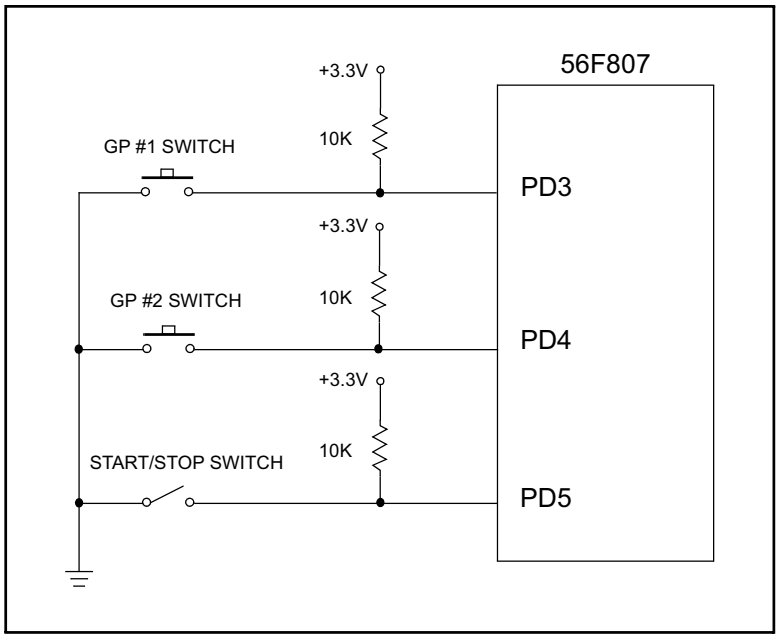

Figure 2-9. Run/Stop and General Purpose Switches

2.14 Serial 10-bit 4-channel D/A Converter

The 56F807EVM board contains a serial 10-bit, 4-channel D/A converter connected to the 56F807's SPI port. The output pins are uncommitted and are connected to a 4X2 header, J26, to allow easy user connections. Refer to **Figure 2-10** for the D/A connections and **Table 2-8** for the header's pin-out. The D/A's output full-scale range value can be set to a value from 0.0V to 2.4V by a trimpot, R97. This trimpot is preset to +2.05V, which provides approximately 2mV per step.

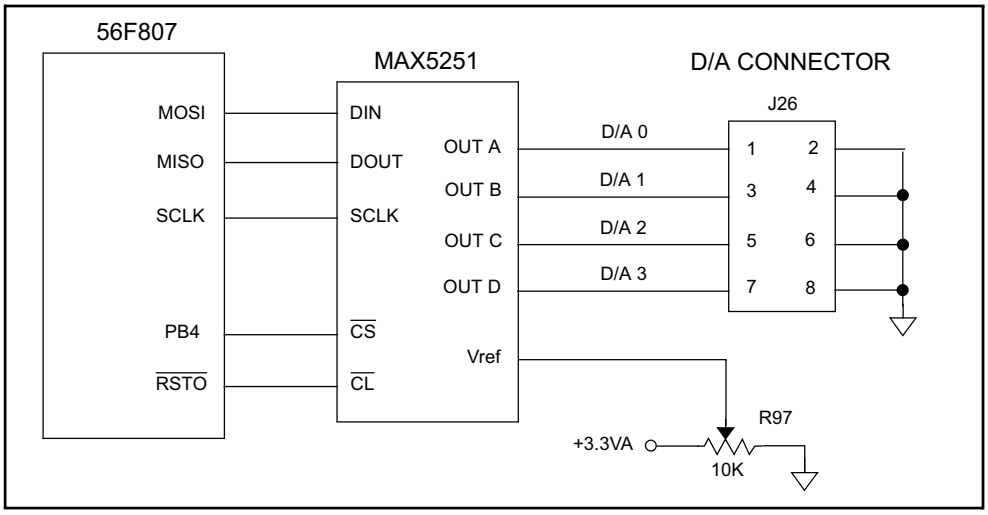

Figure 2-10. Serial 10-bit, 4-Channel D/A Converter

Table 2-8. D/A Header Description

J20			
Pin #	**Signal**	**Pin #**	**Signal**
1	D/A Channel 0	2	AGND
3	D/A Channel 1	4	AGND
5	D/A Channel 2	6	AGND
7	D/A Channel 3	8	AGND

2.15 Motor Control PWM Signals and LEDs

The 56F807 has two independent groups of dedicated PWM units. Each unit contains six PWM, three Phase Current sense and four Fault input lines. PWM group A's PWM lines are connected to the UNI-3 interface connector and to a set of six PWM LEDs via inverting buffers. The inverting buffers are used to isolate and drive the controller's PWM group A's outputs to the PWM LEDs. The secondary PWM signals are routed to the Secondary UNI-3 connector. The PWM LEDs indicate the status of PWM group A signals, as shown in **Figure 2-11**. PWM Group A and B signals are routed out to headers, J10 and J11 respectively, and are available for use by the end user.

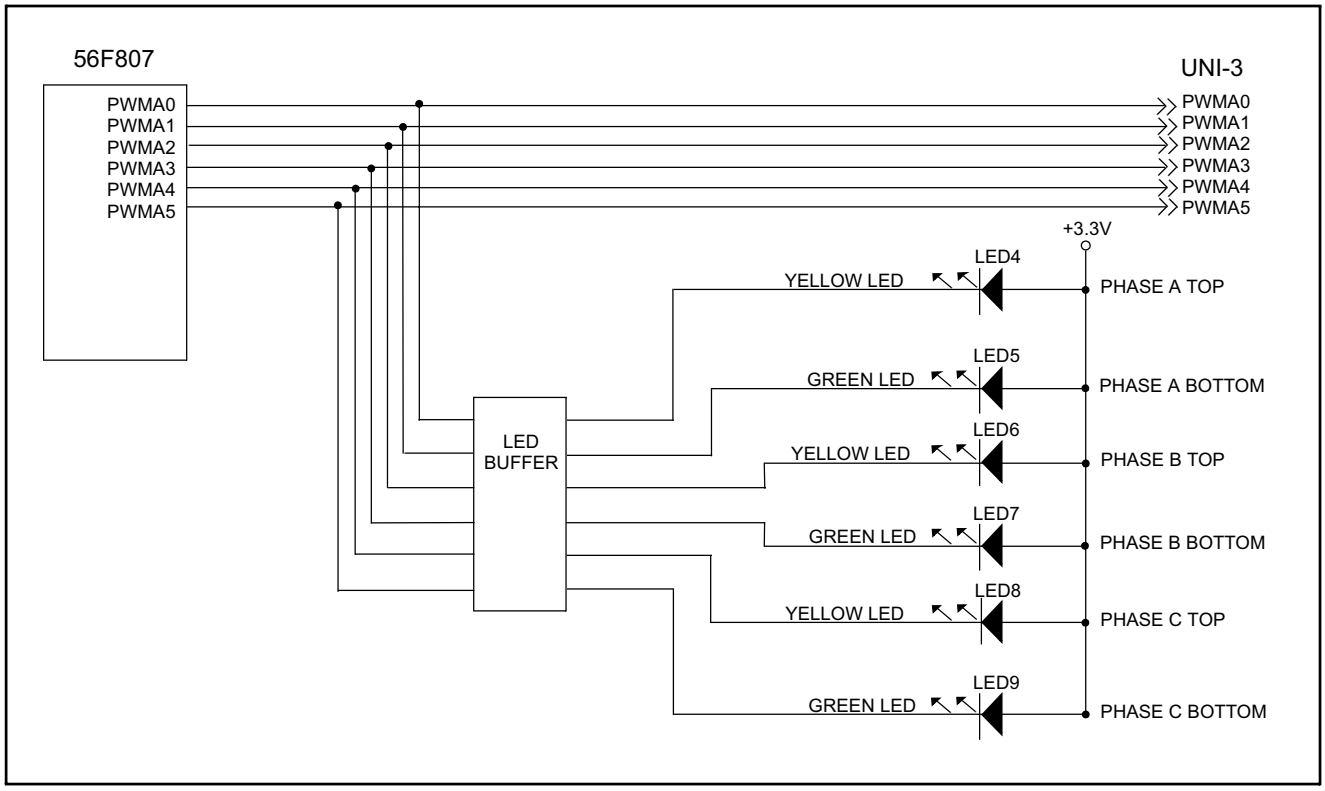

Figure 2-11. PWM Group A Interface and LEDs

2.16 Motor Protection Logic

The 56F807EVM contains two UNI-3 connectors that interface with various motor drive boards, Primary UNI-3 and Secondary UNI-3. The device can sense error conditions generated by the motor power stage boards via signals on the UNI-3 connector. The motor driver board's Motor Supply DC Bus Voltage, Current and Motor Phase Currents are sensed on the power stage board. The conditioned signals are transferred to the board via the UNI-3 connector. These analog input signals are compared to a limit set by trimpots. If the input analog signals are greater than the limit set by the trimpot, a controller digital voltage-compatible +3.3V DC fault signal is generated.

2.16.1 Primary UNI-3 Motor Protection Logic

The Primary UNI-3 DC Bus Over-Voltage signal is connected to the hybrid controller's PWM group A fault inputs. The three Primary UNI-3 Phase Over-Current signals are connected to the device's PWM group A's fault inputs, i.e., FAULTA1, FAULTA2 and FAULTA3. **Figure 2-13** contains the diagram of the Over-Voltage and one phase of the Phase Over-Current circuit for the UNI-3 interface. The FAULTA1 input can be sourced from the Phase A Over-Current circuit or the DC Bus Over-Current circuit. Jumper JG1, provides the selection; reference **Figure 2-12** and **Table 2-9**.

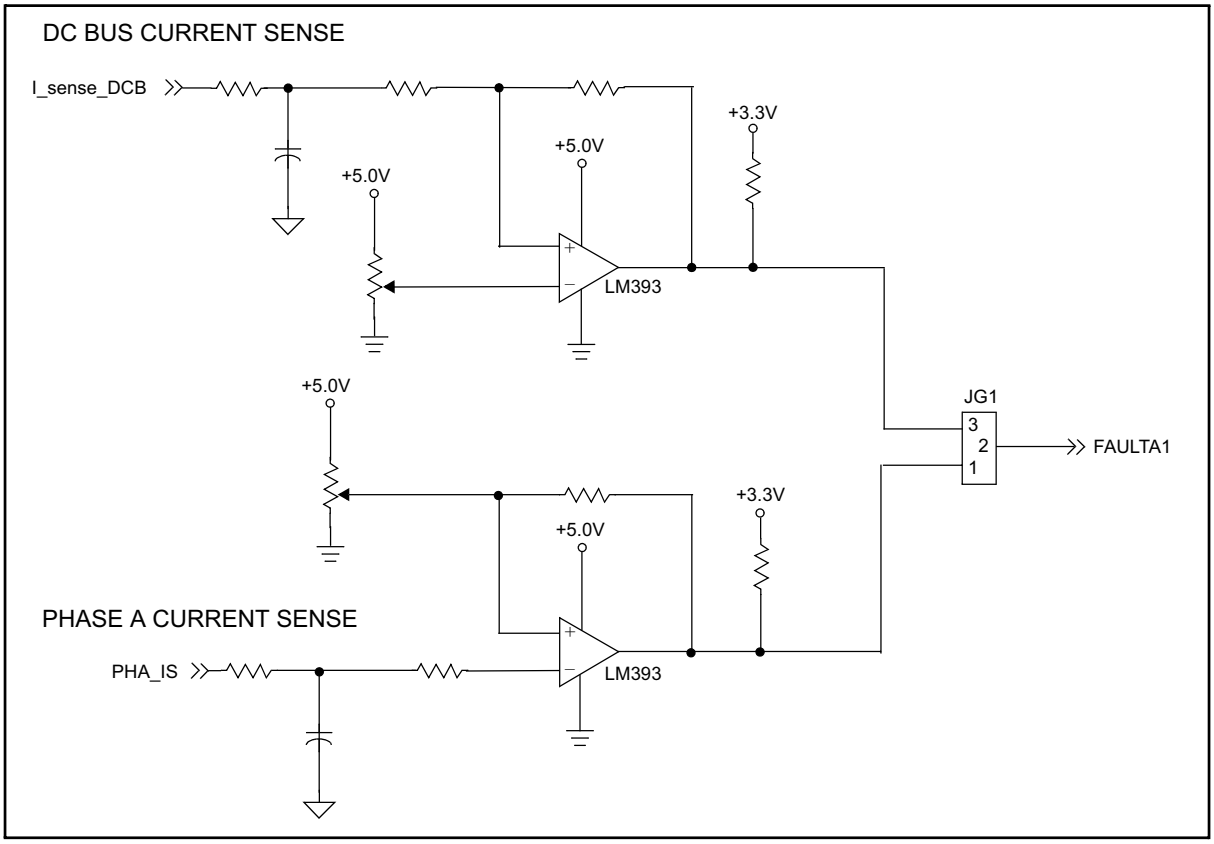

Figure 2-12. FAULTA1 Selection Circuit

Table 2-9. FAULTA1 Source Selection Jumper

JG1	Comment
1–2	Phase A Over-Current Sense input
2–3	DC Bus Over-Current Sense input

2.16.2 Secondary UNI-3 Motor Protection Logic

The Secondary UNI-3 interface is similar to the Primary UNI-3 interface. The Secondary UNI-3 Over-Voltage signal is connected to the hybrid controller's PWM group B's fault input, FAULTB1. The three Secondary UNI-3 Phase Over-Current signals are connected to the device's PWM group B fault inputs, i.e., FAULTB1, FAULTB2 and FAULTB3. The Secondary UNI-3 interface is similar to the circuits contained in **Figure 2-13**. The FAULTB1 input can be sourced from the Phase A Over-Current circuit or the DC Bus Over-Current circuit. Jumper JG16, provides the selection; reference **Figure 2-14** and **Table 2-10**.

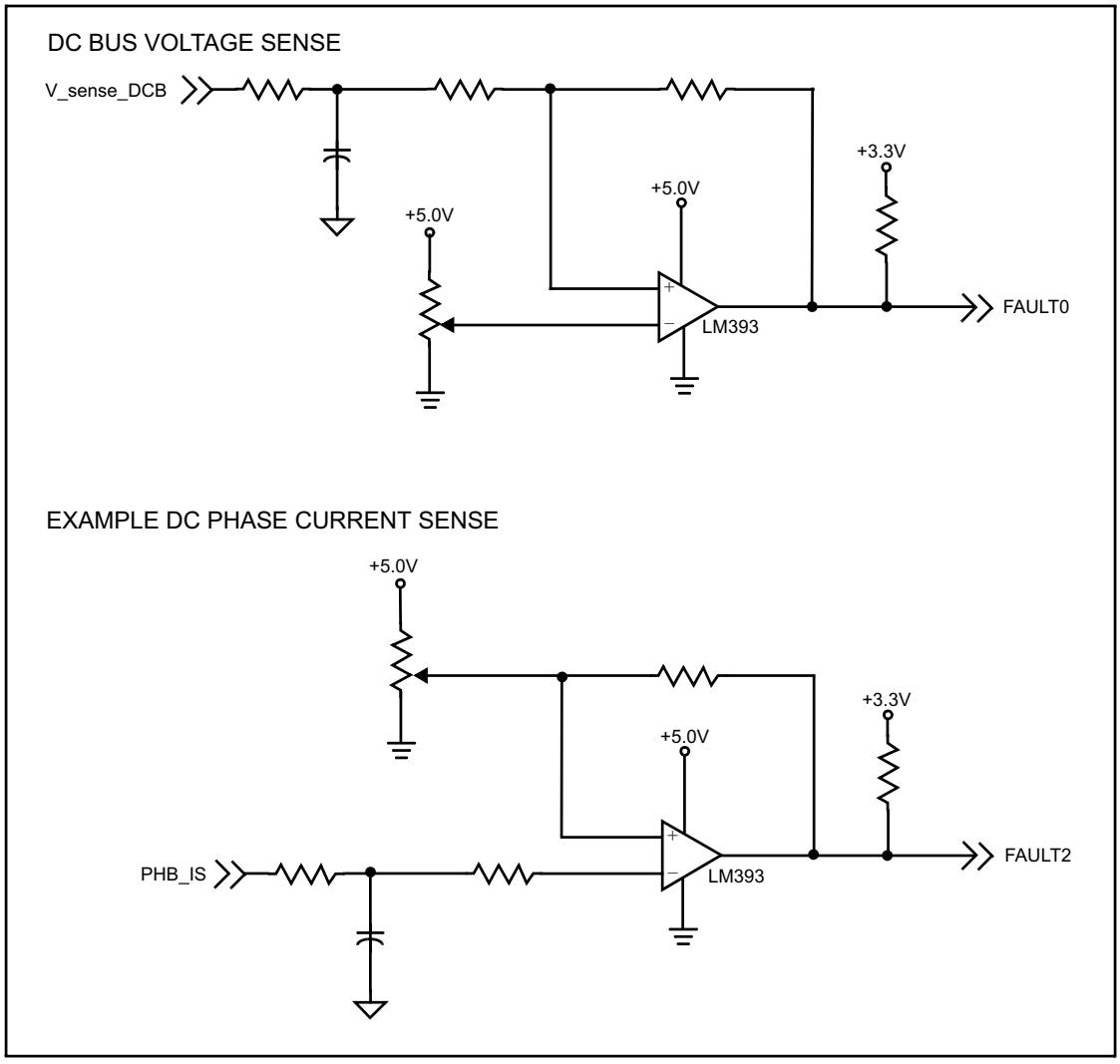

Figure 2-13. DC-Bus Over-Voltage and Phase Over-Current Detection Circuits

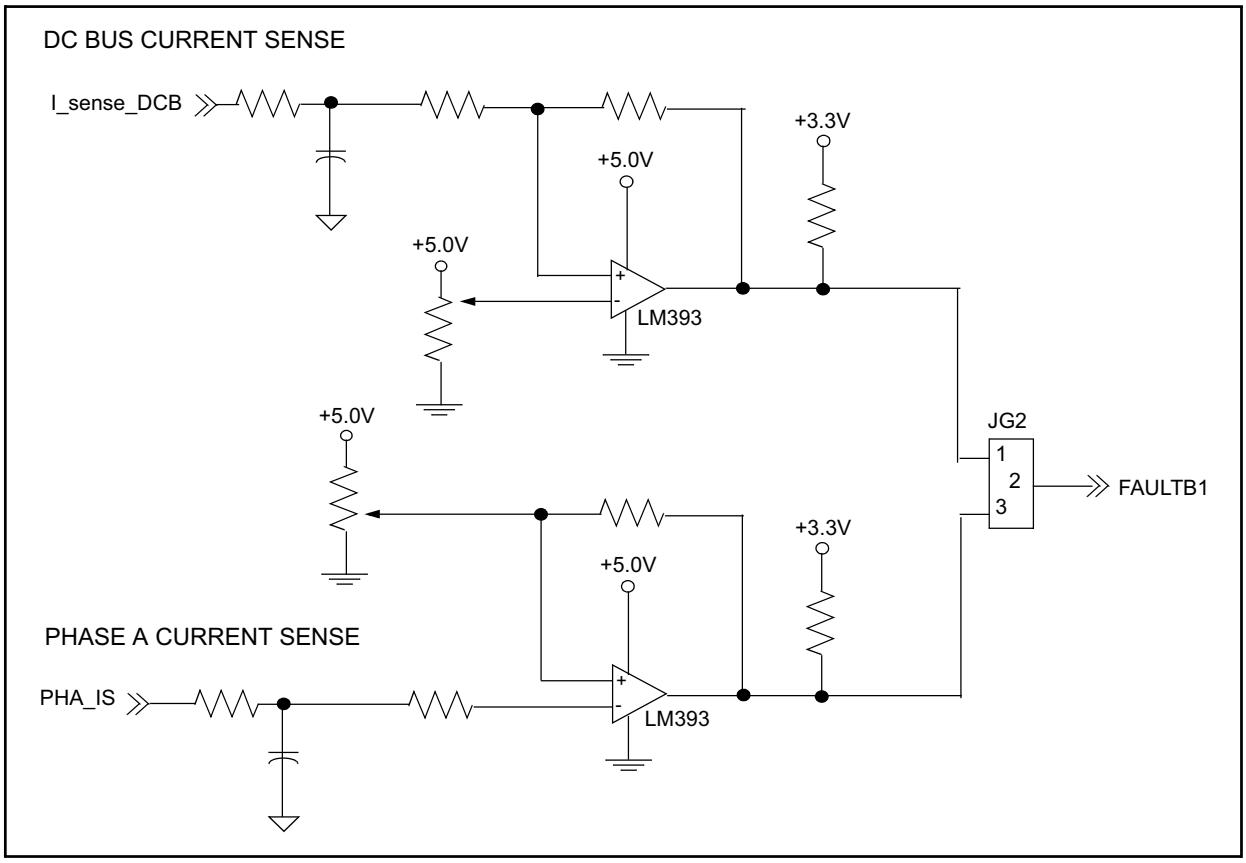

Figure 2-14. FAULTB1 Selection Circuit

Table 2-10. FAULTB1 Source Selection Jumper

JG2	Comment
1–2	Phase A Over-Current Sense input
2–3	DC Bus Over-Current Sense input

2.17 Back-EMF and Motor Phase Current Sensing

The primary and secondary UNI-3 connectors supply Back-EMF and Motor Phase Current signals from the three phases of a motor attached to a motor drive unit. The Back-EMF signals on the UNI-3 connectors are derived from a resistor divider network contained in the motor drive unit. These resistors divide down the attached motor's Back-EMF voltages to a 0 to +3.3V level. The Motor Phase Current signals are derived from current sense resistors. Both of these signal groups are then routed to a group of header pins, JG14, that allow the end user to select which signal group the device's A/D will monitor. Refer to **Figure 2-15** for the design of a single channel. The Secondary UNI-3's Back-EMF signals are simularly derived and routed to a group of header pins, JG10, that allow the end user to select which signal group the controller's A/D will monitor; reference **Table 2-8**.

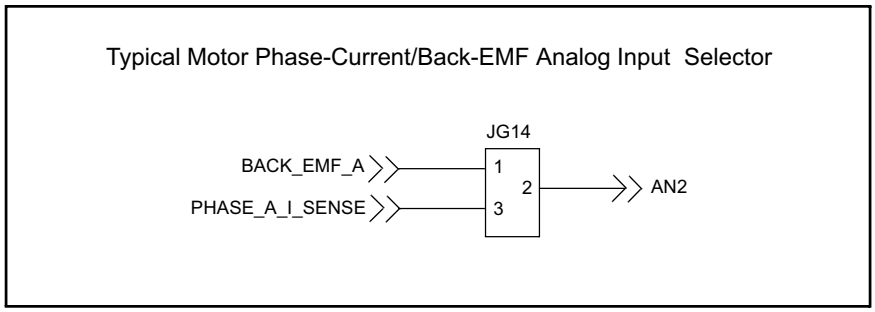

Figure 2-15. Primary Back-EMF or Motor Phase Current Sense Signals

2.18 Quadrature Encoder/Hall-Effect Interface

The 56F807EVM board contains a Primary and Secondary Quadrature Encoder/Hall-Effect interface connected to the hybrid controller's first and second Quad Encoder input ports. The circuit is designed to accept +3.0V to +5.0V encoder or Hall-Effect sensor inputs. Input noise filtering is supplied on the input path for the Quadrature Encoder/Hall-Effect interface, along with additional noise rejection circuitry inside the device. **Figure 2-16** contains the primary encoder interface. The secondary encoder interface is a duplicate of the primary encoder interface.

2.19 Zero-Crossing Detection

An attached UNI-3 motor drive board contains logic that can send out pulses when the phase voltage of an attached 3-phase motor drops to zero. The motor drive board circuits generate a 0 to +5.0V DC pulse via voltage comparators. The resulting pulse signals are sent to a set of jumper blocks shared with the Encoder/Hall-Effect interface. The jumper blocks allow the selection of Zero-Crossing signals or Quadrature Encoder/Hall-Effect signals. When in operation, the controller will only monitor one set of signals, Encoder/Hall-Effect or Zero-Crossing. **Figure 2-16** contains the Zero-Crossing and Encoder/Hall circuits.

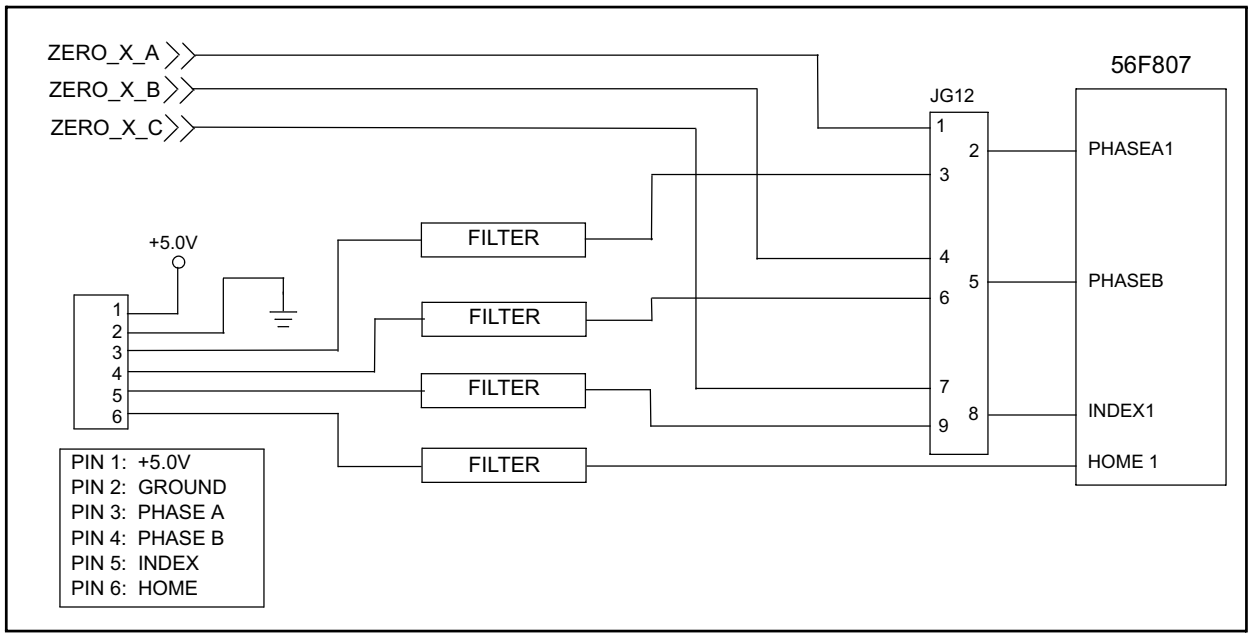

Figure 2-16. Zero-Crossing Encoder Interface

2.20 CAN Interface

The 56F807EVM board contains a CAN physical-layer interface chip that is attached to the MSCAN_RX and MSCAN_TX pins on the 56F807. The EVM board uses a Philips, PCA82C250, high speed, 1Mbps, physical layer interface chip. Due to the +5.0V operating voltage of the CAN chip, a pull-up to +5.0V is required to level shift the Transmit Data output line from the 56F807. A primary, J24, and daisy-chain, J25, CAN connector are provided to allow easy daisy-chaining of CAN devices. CAN bus termination of 120 ohms can be provided by adding a jumper to JG3. Refer to **Table 2-11** for the CAN connector signals, and to **Figure 2-17** for a connection diagram

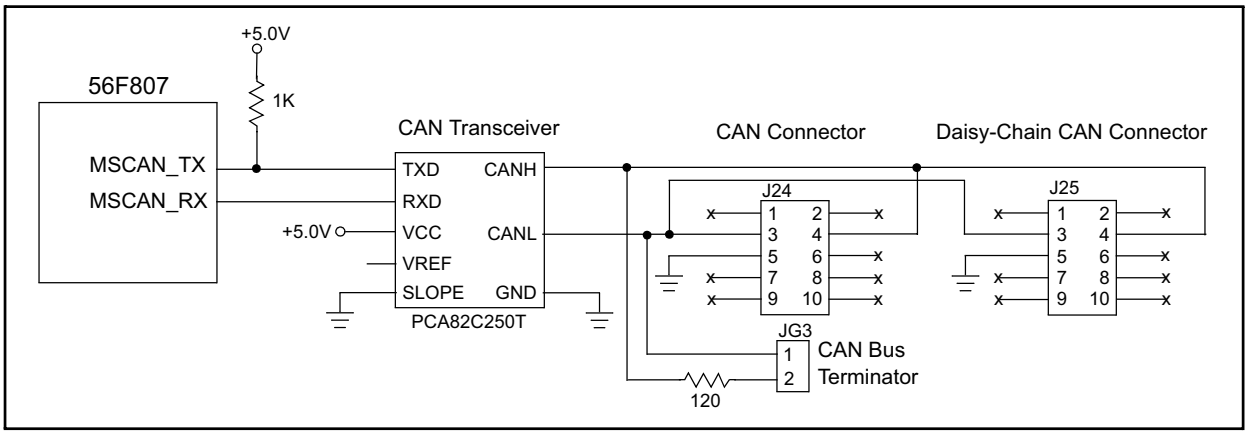

Figure 2-17. CAN Interface

Table 2-11. CAN Header Description

J24 and J25			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	2	NC
3	CANL	4	CANH
5	GND	6	NC
7	NC	8	NC
9	NC	10	NC

2.21 Software Feature Jumpers

The 56F807EVM board contains two software feature jumpers that allow the user to select “User Defined” software features. Two GPIO port pins, PD0 and PD1, are pulled high with 10K ohm resistors on JG16 and JG17. Attaching a jumper will ground the respective Port D signal line; see **Figure 2-18**.

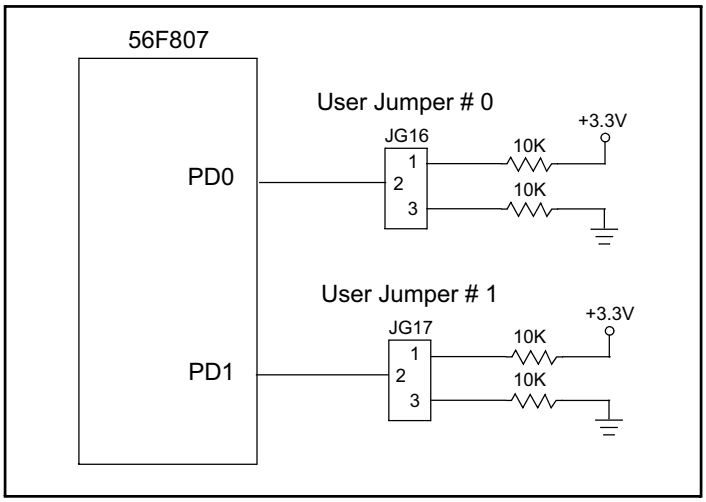

Figure 2-18. Software Feature Jumpers

2.22 Peripheral Connectors

The EVM board contains a group of Peripheral Expansion Connectors used to gain access to the resources of the 56F807. These signal groups have Expansion Connectors:

- Port B
- Port D
- Port E
- External Memory Control
- Encoder A/Timer Channel A
- Encoder B/Timer Channel B
- Timer Channel C
- Timer Channel D
- Port A/Address Bus
- Data Bus
- A/D Input Port A
- A/D Input Port B
- Serial Communications Port 0
- Serial Communications Port 1
- Serial Peripheral Port
- PWM Port A
- PWM Port B

2.22.1 Port B Expansion Connector

Port B is a GPIO port which is connected to the Port B header. The pins of the port, PB0-PB7, are dedicated to general purpose I/O and Interrupt operations. The GPIO port pins may be programmed as inputs, outputs or level-sensitive interrupt inputs. **Table 2-12** shows the port pin to headed connections.

Table 2-12. Port B Connector Description

J20			
Pin #	**Signal**	**Pin #**	**Signal**
1	PB0	2	PB1
3	PB2	4	PB3
5	PB4	6	PB5
7	PB6	8	PB7
9	GND	10	+3.3V

2.22.2 Port D Expansion Connector

Port D is an MPIO port with signal lines attached to various headers. The six pins of the port, PD0-PD5, are dedicated to general purpose operation. The remaining two pins, PD6 and PD7, are shared with the TXD1 and RXD1 signal lines. The GPIO port pins may be programmed as inputs, outputs or level-sensitive interrupt inputs. **Table 2-13** shows the exclusive Port D signals. The shared Port D signals are contained in **Table 2-20**.

Table 2-13. Port D Connector Description

J23			
Pin #	**Signal**	**Pin #**	**Signal**
1	PD0	2	PD1
3	PD2	4	PD3
5	PD4	6	PD5
7	GND	8	+3.3V

2.22.3 Port E Expansion Connector

Port E is an MPIO port with signal lines attached to various headers. The pins of the port are shared with one SCI port, SCI0, two Address bus lines, A6 and A7, and the SPI port. **Table 2-14** shows the shared pins and functions.

Table 2-14. Port E Connector Description

J17					
Pin #	**Signal**	**Alternate Funct**	**Pin #**	**Signal**	**Alternate Funct**
1	PE0	TXD0	2	PE1	RXD0
3	PE2	TXD1	4	PE3	RXD1
5	PE4	SCLK	6	PE5	MOSI
7	PE6	MISO	8	PE7	$\overline{SS}$
9	GND	GND	10	+3.3V	+3.3V

2.22.4 External Memory Control Signal Expansion Connector

The External Memory Control Signal connector contains the device's external memory control signal lines. Refer to **Table 2-15** for the names of these signals.

Table 2-15. External Memory Control Signal Connector Description

J8			
Pin #	**Signal**	**Pin #**	**Signal**
1	$\overline{RD}$	2	$\overline{IRQA}$
3	$\overline{WR}$	4	$\overline{IRQB}$
5	$\overline{PS}$	6	$\overline{RESET}$
7	$\overline{DS}$	8	$\overline{RSTO}$
9	CLKO	10	DE
11	GND	12	+3.3V

2.22.5 Primary Encoder/Timer Channel A Expansion Connector

The Primary Encoder/Timer Channel A port is an MPIO port attached to the Timer A expansion connector. The port can act as a Quadrature Decoder interface port or as a general purpose Timer port. See **Table 2-16** for the signals attached to the connector.

Table 2-16. Timer A Connector Description

J18		
Pin #	**Signal**	**Alternate**
1	TA0	PhaseA0
2	TA1	PhaseB0
3	TA2	INDEX0
4	TA3	HOME0
5	+3.3V	+3.3V
6	GND	GND

2.22.6 Secondary Encoder/Timer Channel B Expansion Connector

The Secondary Encoder/Timer Channel B port is an MPIO port attached to the Timer B expansion connector. The port can act as a Quadrature Decoder interface port or as a general purpose Timer port. Refer to **Table 2-17** for the signals attached to the connector.

Table 2-17. Timer B Connector Description

J21		
Pin #	**Signal**	**Alternate**
1	TB0	PhaseA1
2	TB1	PhaseB1
3	TB2	INDEX1
4	TB3	HOME1
5	+3.3V	+3.3V
6	GND	GND

2.22.7 Timer Channel C Expansion Connector

The Timer Channel C port is an MPIO port attached to the Timer C expansion connector. Refer to **Table 2-18** for the signals attached to the connector.

Table 2-18. Timer C Connector Description

J19	
Pin #	**Signal**
1	TC0
2	TC1
3	+3.3V
4	GND

2.22.8 Timer Channel D Expansion Connector

The Timer Channel D port is an MPIO port attached to the Timer D expansion connector. Refer to **Table 2-19** for the signals attached to the connector.

Table 2-19. Timer D Connector Description

J22	
Pin #	**Signal**
1	TD0
2	TD1
3	TD2
4	TD3
5	+3.3V
6	GND

2.22.9 Address Bus Expansion Connector

The 16-bit Address bus connector contains the hybrid controller's external memory address signal lines. The upper 8 bits, A8 - A15, can also be used as Port A GPIO lines. See **Table 2-20** for the Address bus connector information.

Table 2-20. External Memory Address Bus Connector Description

J6			
Pin #	**Signal**	**Pin #**	**Signal**
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	+3.3V

2.22.10 Data Bus Expansion Connector

The 16-bit Data bus connector contains the device's external memory data signal lines. Refer to **Table 2-21** for the Data bus connector information.

Table 2-21. External Memory Address Bus Connector Description

J7			
Pin #	**Signal**	**Pin #**	**Signal**
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	D8	10	D9
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	GND	18	+3.3V

2.22.11 A/D Port A Expansion Connector

The 8-channel Analog-to-Digital conversion Port A is attached to this connector. See **Table 2-22** for the connection information.

Table 2-22. A/D Port A Connector Description

J9			
Pin #	**Signal**	**Pin #**	**Signal**
1	AN0	2	AN4
3	AN1	4	AN5
5	AN2	6	AN6
7	AN3	8	AN7
9	GNDA	10	+3.3VA

2.22.12 A/D Port B Expansion Connector

The 8-channel Analog-to-Digital conversion Port B is attached to this connector. Refer to **Table 2-23** for the connection information.

Table 2-23. A/D Port B Connector Description

J12			
Pin #	**Signal**	**Pin #**	**Signal**
1	AN8	2	AN12
3	AN9	4	AN13
5	AN10	6	AN14
7	AN11	8	AN15
9	GNDA	10	+3.3VA

2.22.13 Serial Communications Port 0 Expansion Connector

The Serial Communications Port 0, SCI0, is attached to this connector. See **Table 2-24** for the connection information.

Table 2-24. SCI0 Connector Description

J15	
Pin #	**Signal**
1	TXD0
2	RXD0
3	GND

2.22.14 Serial Communications Port 1 Expansion Connector

The Serial Communications Port 1, SCI1, is attached to this connector. Refer to **Table 2-25** for the connection information.

Table 2-25. SCI1 Connector Description

J14	
Pin #	**Signal**
1	TXD1
2	RXD1
3	GND

2.22.15 Serial Peripheral Interface Expansion Connector

The Serial Peripheral Interface, SPI, is attached to this connector. Refer to **Table 2-26** for the connection information.

Table 2-26. SPI Connector Description

J13	
Pin #	**Signal**
1	MOSI
2	MISO
3	SCLK
4	GND

2.22.16 CAN Expansion Connector

The CAN port is attached to this connector. See **Table 2-27** for the connection information.

Table 2-27. CAN Connector Description

J16	
Pin #	**Signal**
1	MSCAN_TX
2	MSCAN_RX
3	GND

2.22.17 PWM Port A Expansion Connector

The PWM Port A is attached to this connector. Refer to **Table 2-28** for the connection information.

Table 2-28. PWM Port A Connector Description

J10			
Pin #	**Signal**	**Pin #**	**Signal**
1	PWMA0	2	PWMA1
3	PWMA2	4	PWMA3
5	PWMA4	6	PWMA5
7	FAULTA0	8	FAULTA1
9	FAULTA2	10	FAULTA3
11	ISA0	12	ISA1
13	ISA2	14	GND

2.22.18 PWM Port B Expansion Connector

The PWM Port B is attached to this connector. Refer to **Table 2-29** for the connection information.

Table 2-29. PWM Port B Connector Description

J11			
Pin #	**Signal**	**Pin #**	**Signal**
1	PWMB0	2	PWMB1
3	PWMB2	4	PWMB3
5	PWMB4	6	PWMB5
7	FAULTB0	8	FAULTB1
9	FAULTB2	10	FAULTB3
11	ISB0	12	ISB1
13	ISB2	14	GND

2.23 Test Points

The 56F807EVM board has a total of eight test points. Four test points are located near the breadboard area: +3.3VA, AGND, +3.3V and GND. Three test points are located near the Primary UNI-3 connector, J1: -15VA, GND and +15VA. The final test point, GND, is located in the upper left corner of the board.

Appendix A
56F807EVM Schematics

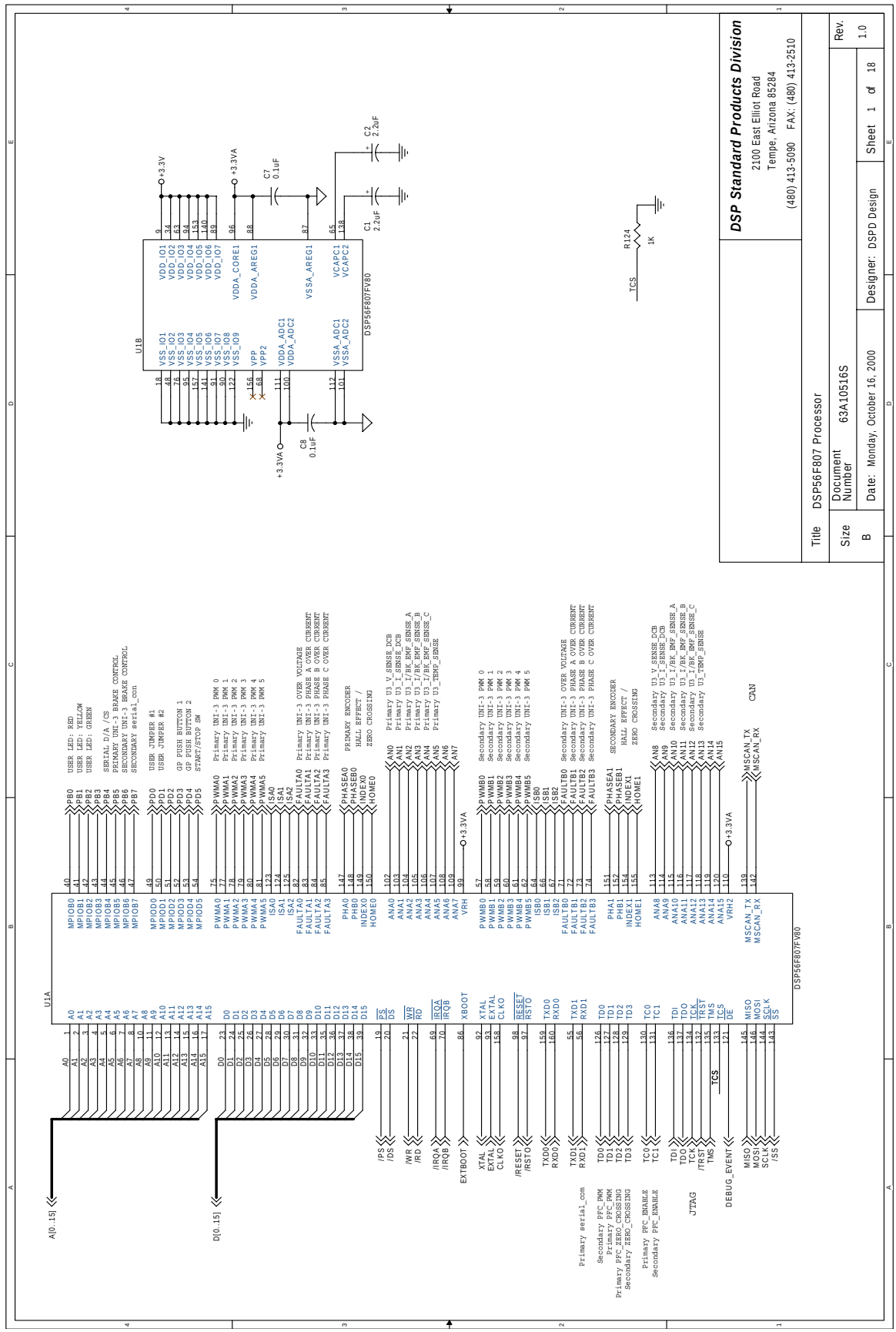

Figure A-1. 56F807 Processor

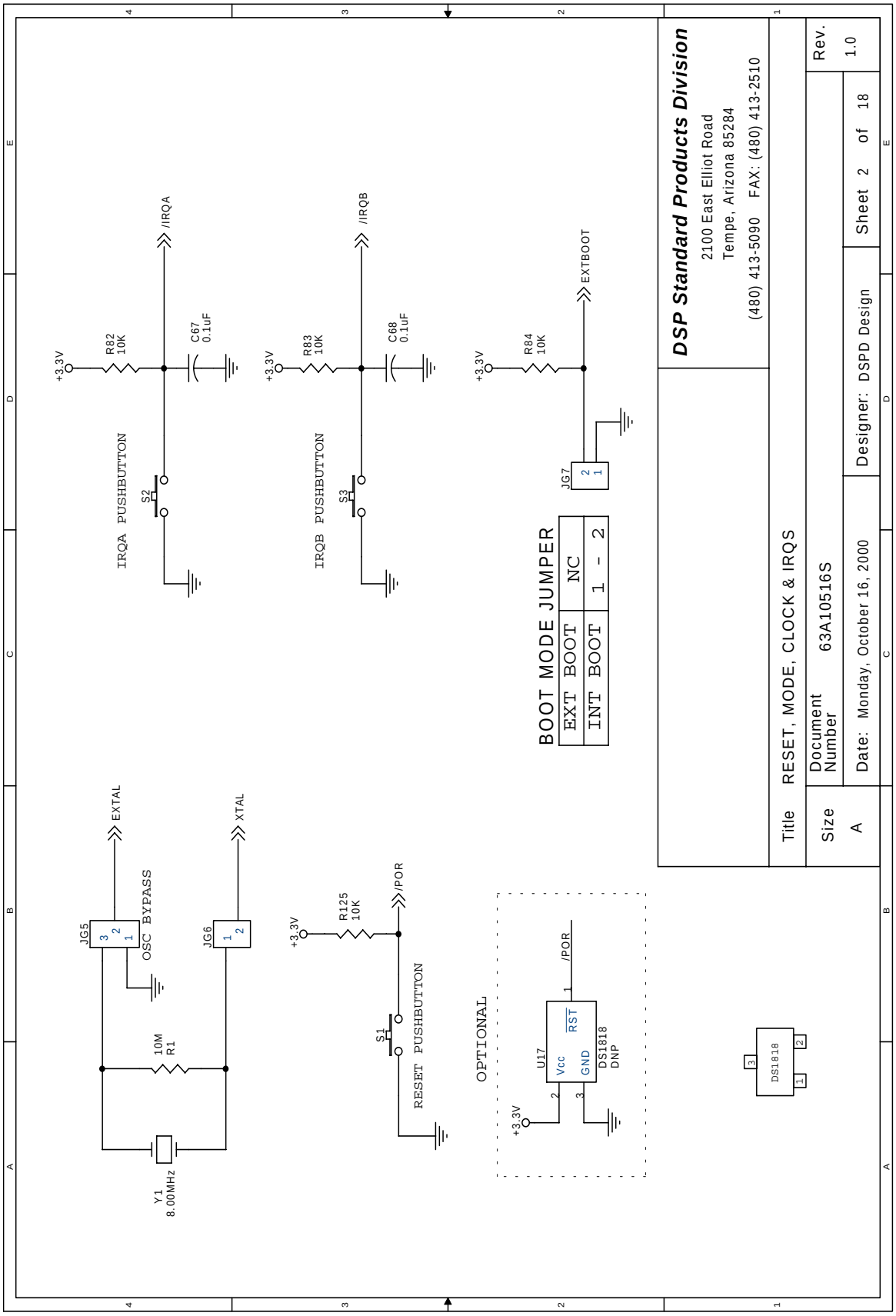

Figure A-2. Reset, Mode,Clock & IRQS

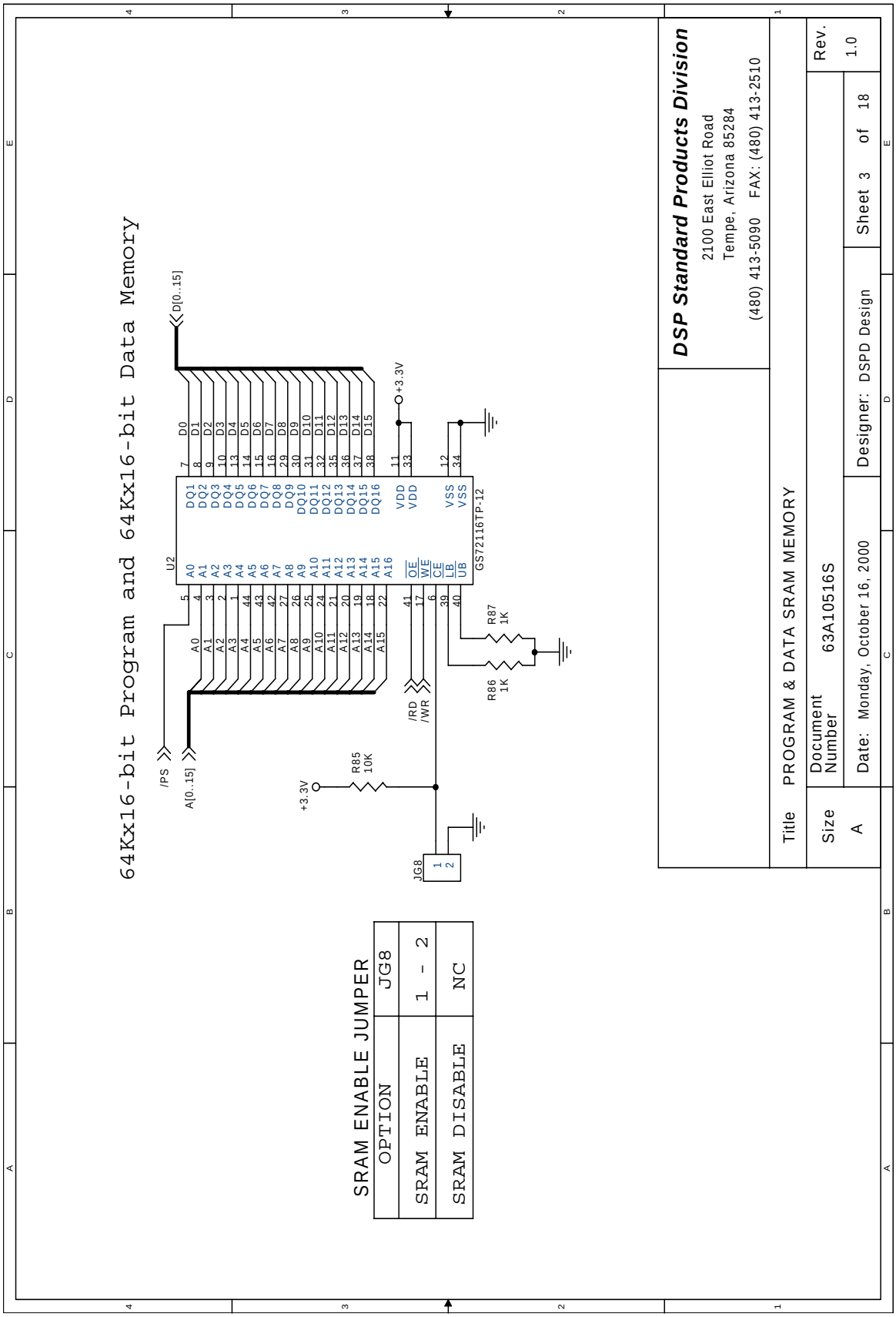

Figure A-3. Program & Data SRAM Memory

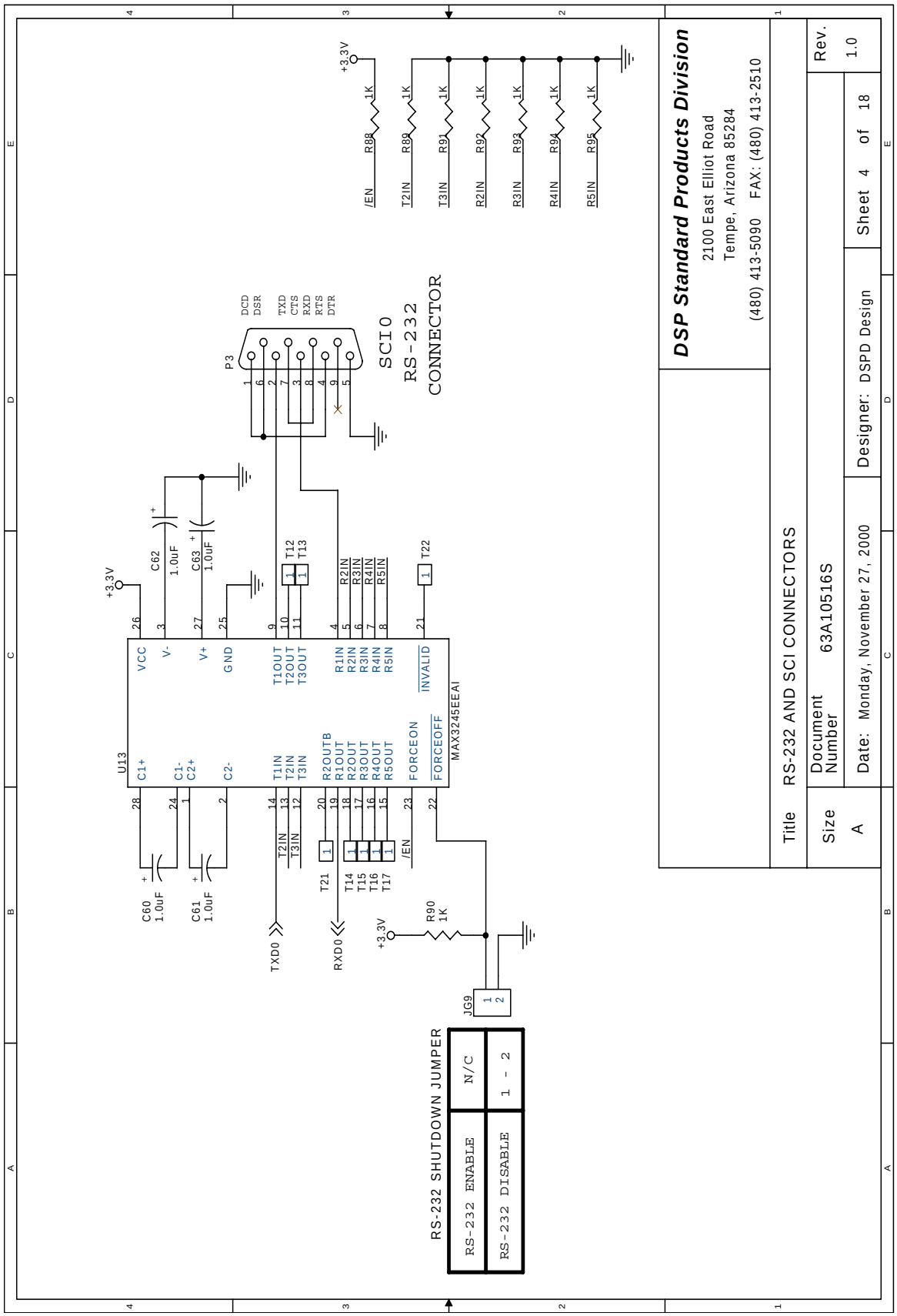

Figure A-4. RS-232 and SCI Connectors

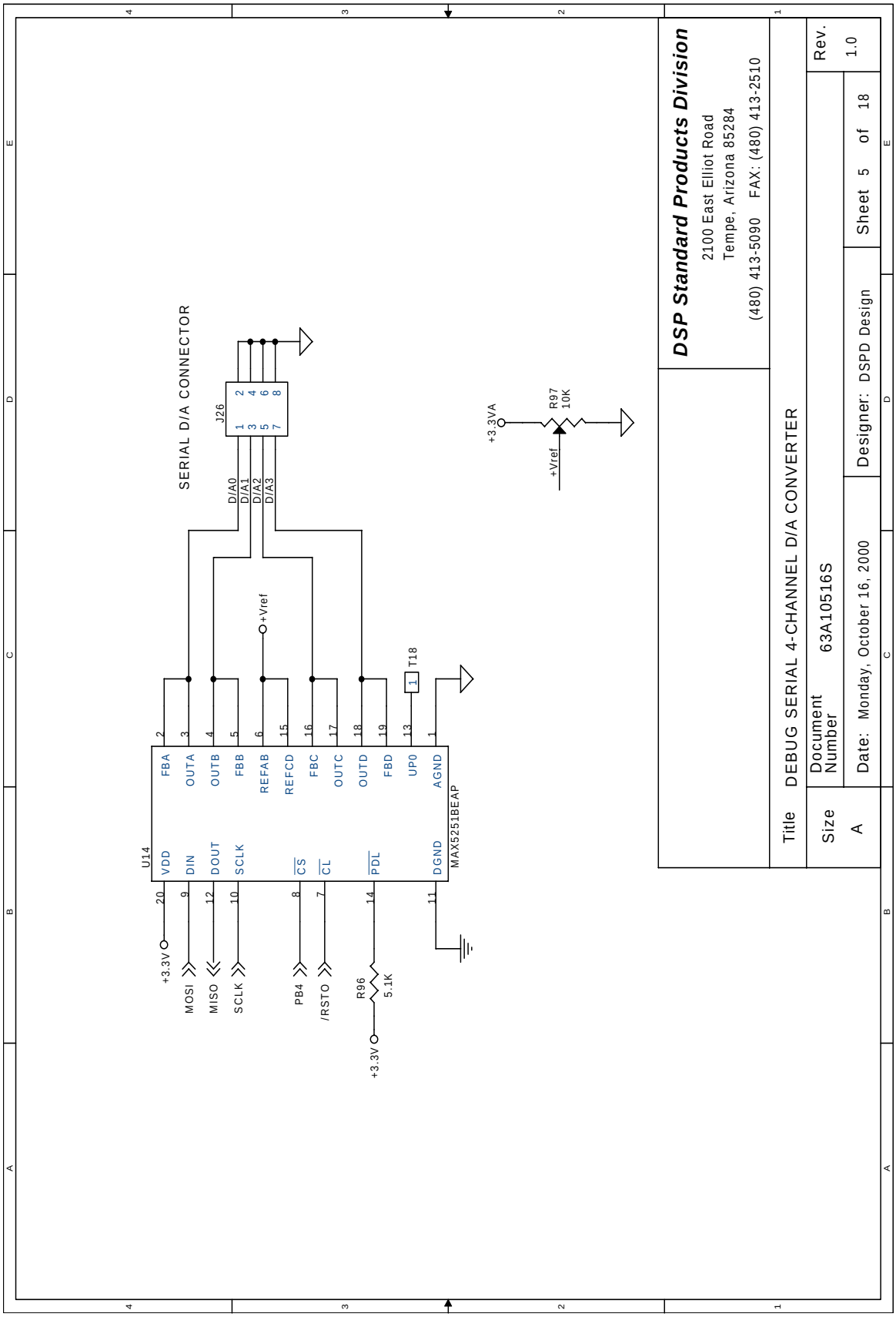

Figure A-5. Debug Serial 4-Channel D/A Converter

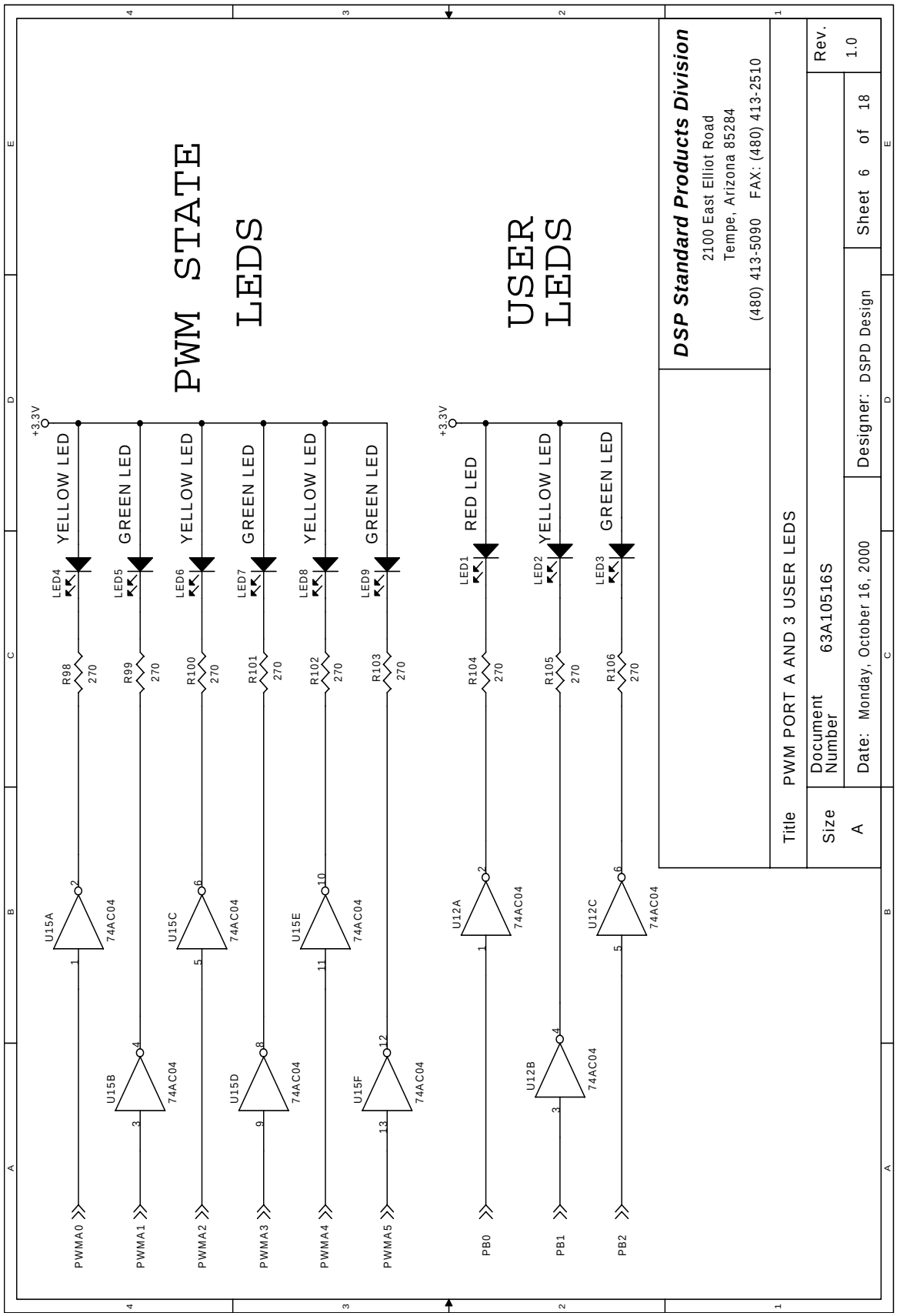

Figure A-6. PWMA and 3 User LEDs

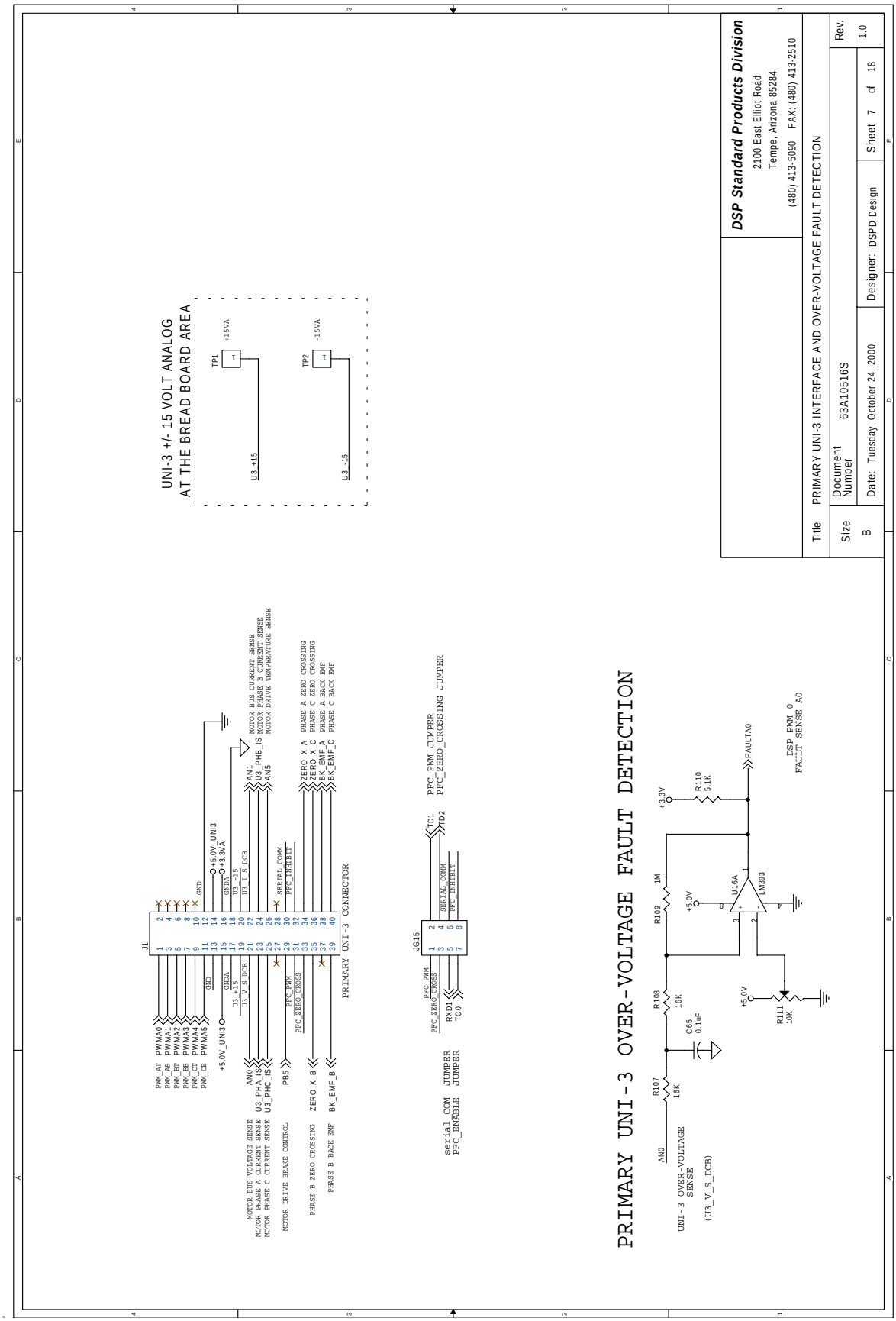

Figure A-7. Primary UNI-3 Interface and Over-Voltage Fault Detection

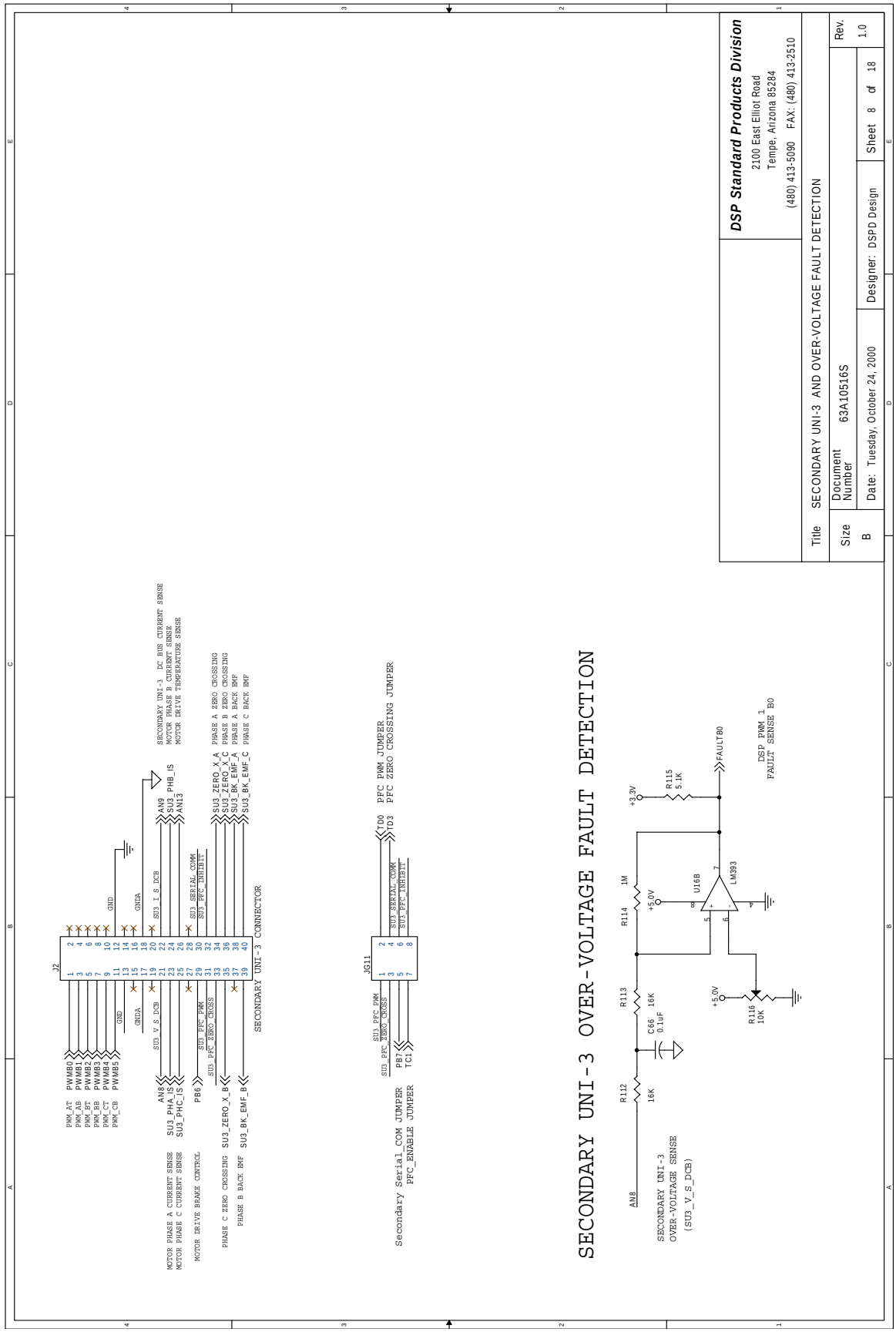

Figure A-8. Secondary UNI-3 and Over-Voltage Detection

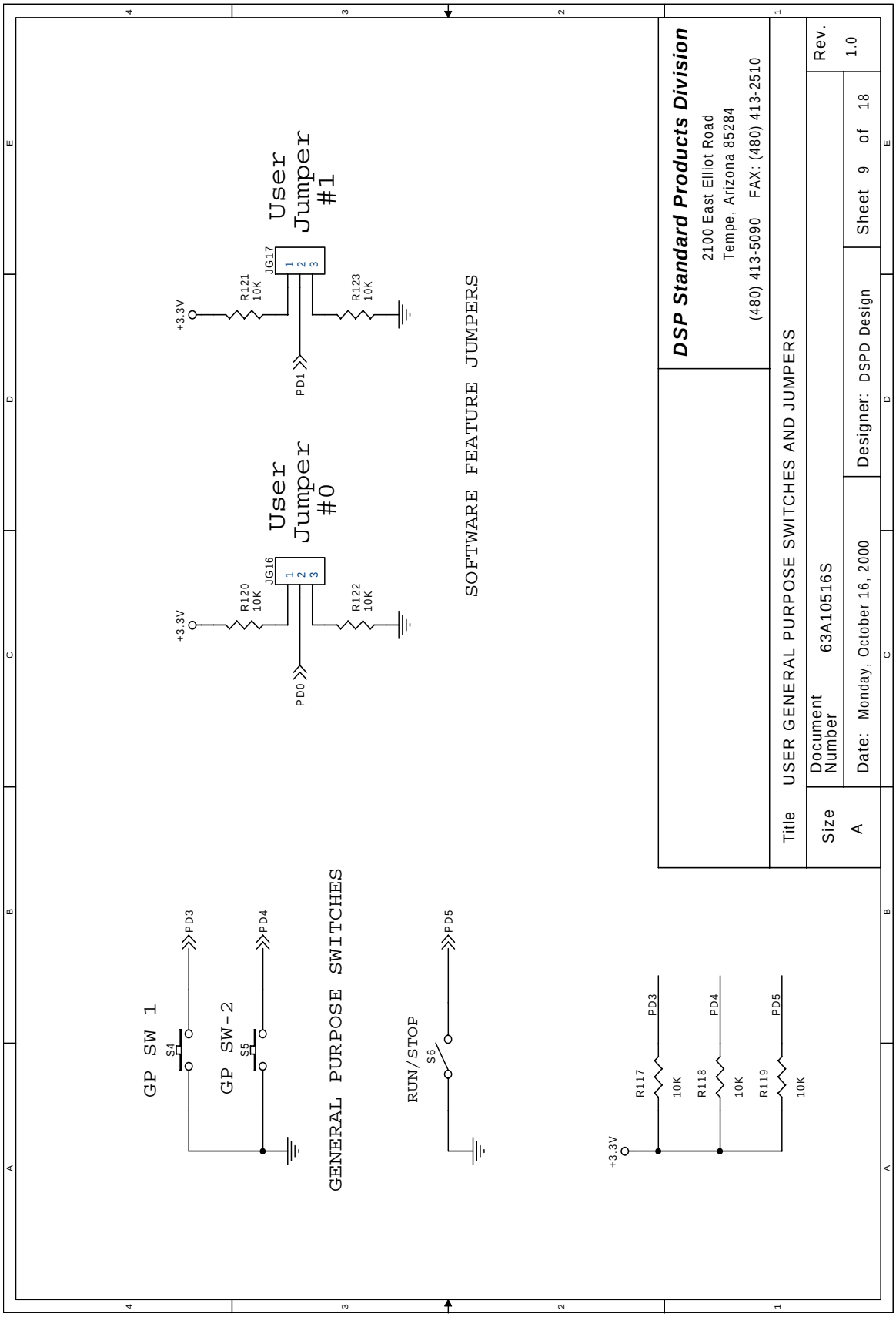

Figure A-9. User General Purpose Switches and Jumpers

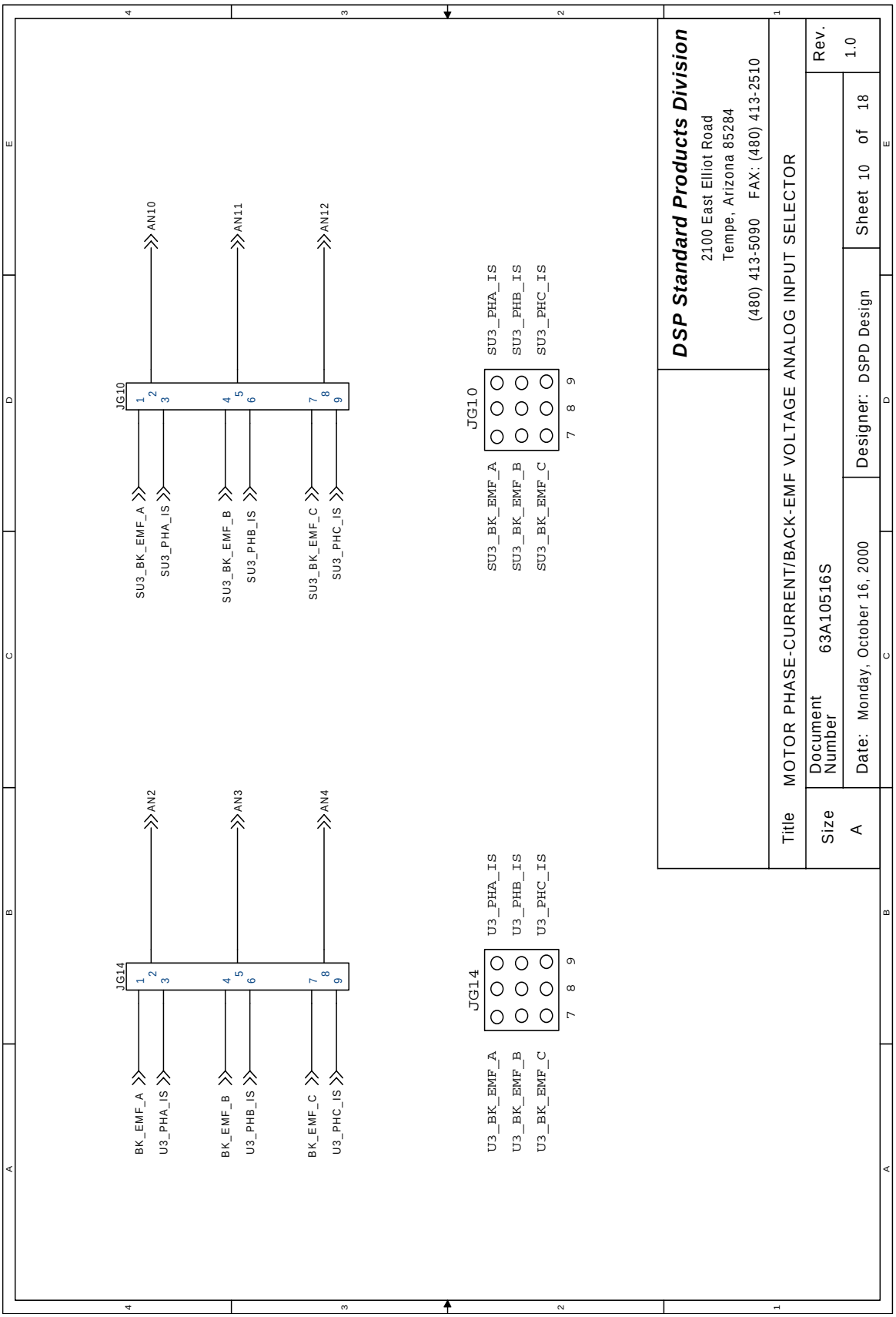

Figure A-10. Motor Phase-Current/Back-EMF Voltage Analog Input Selector

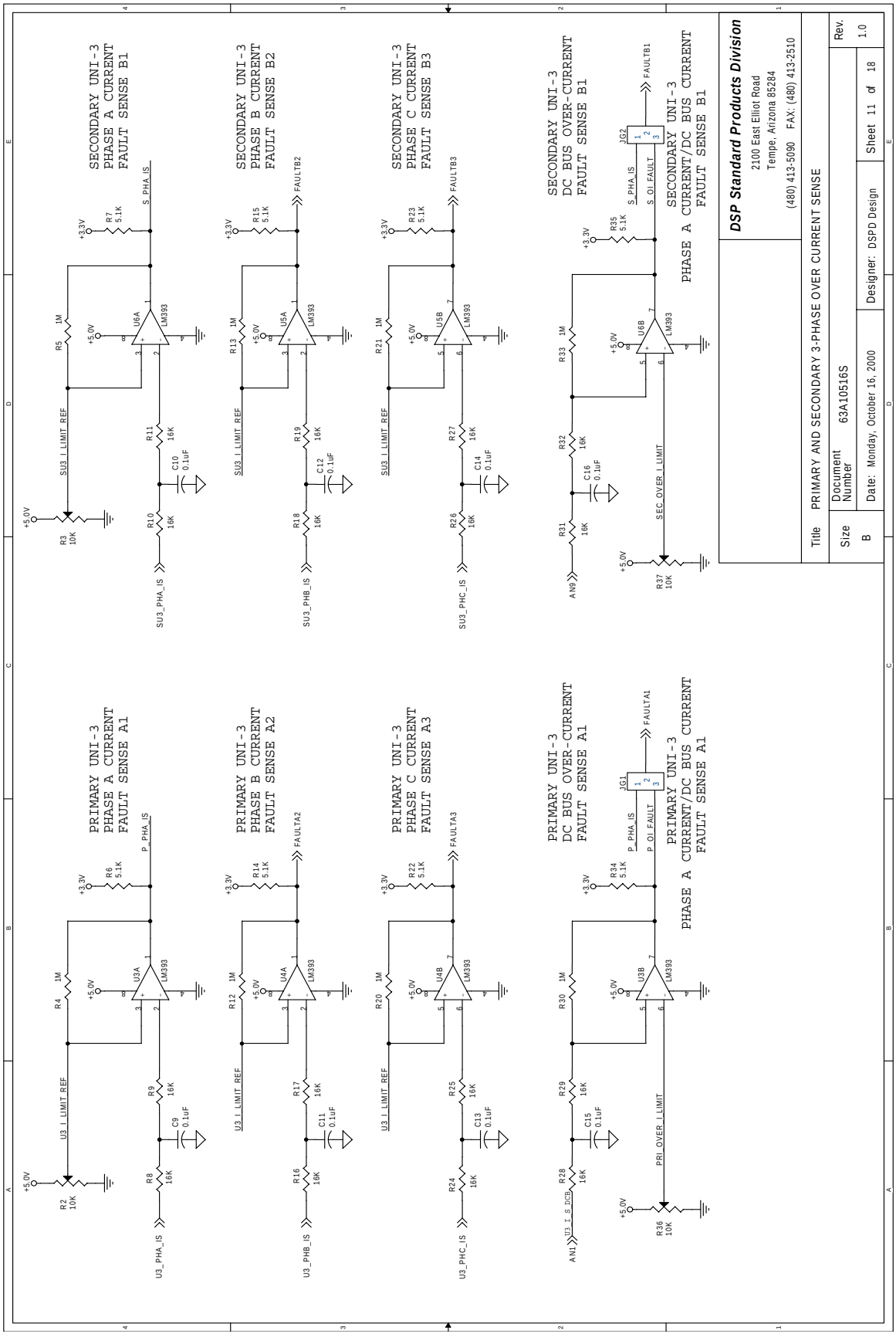

Figure A-11. Primary and Secondary 3-Phase Over-Current Sense

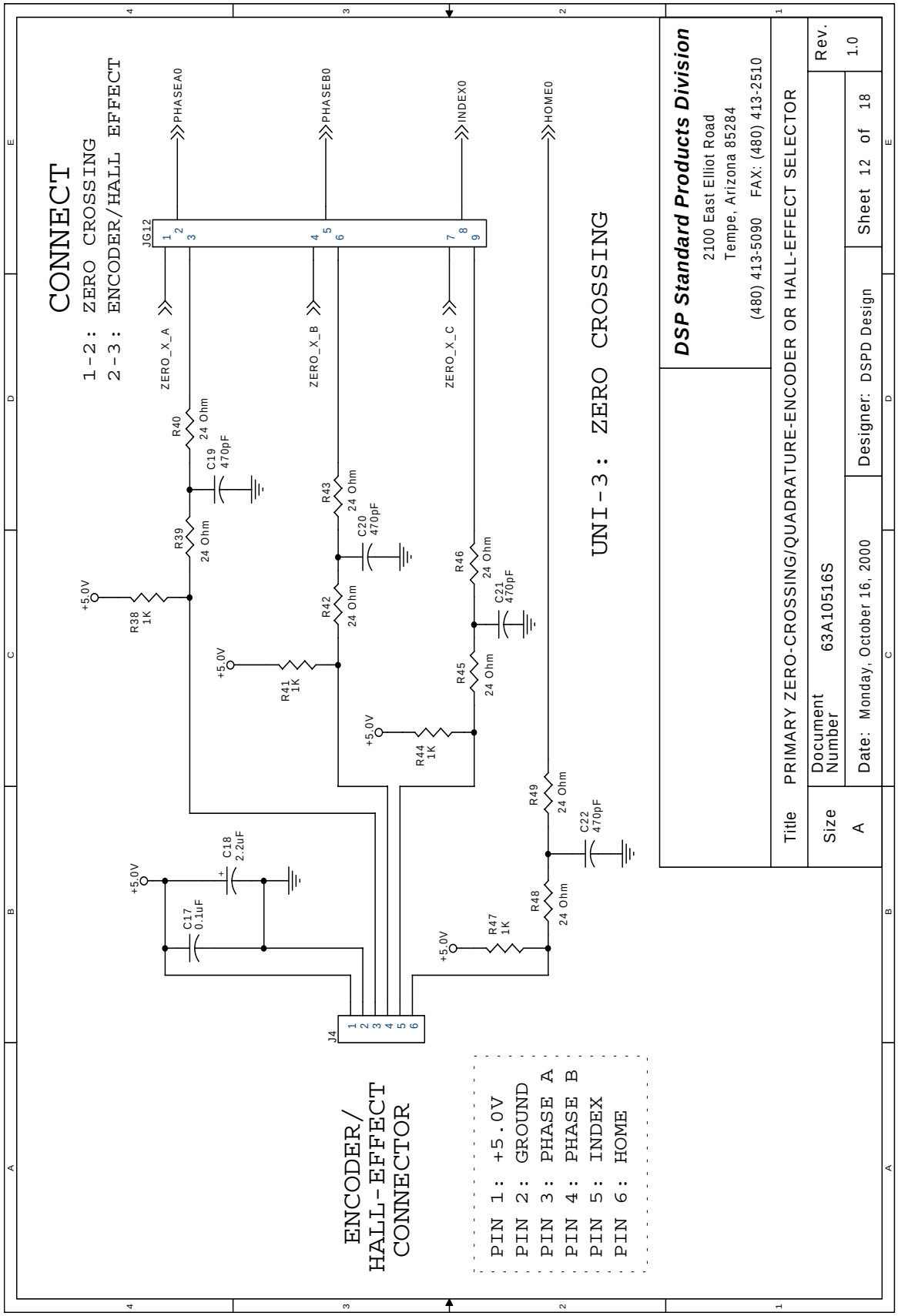

Figure A-12. Primary Zero-Crossing/Quadrature-Encoder or Hall-Effect Selector

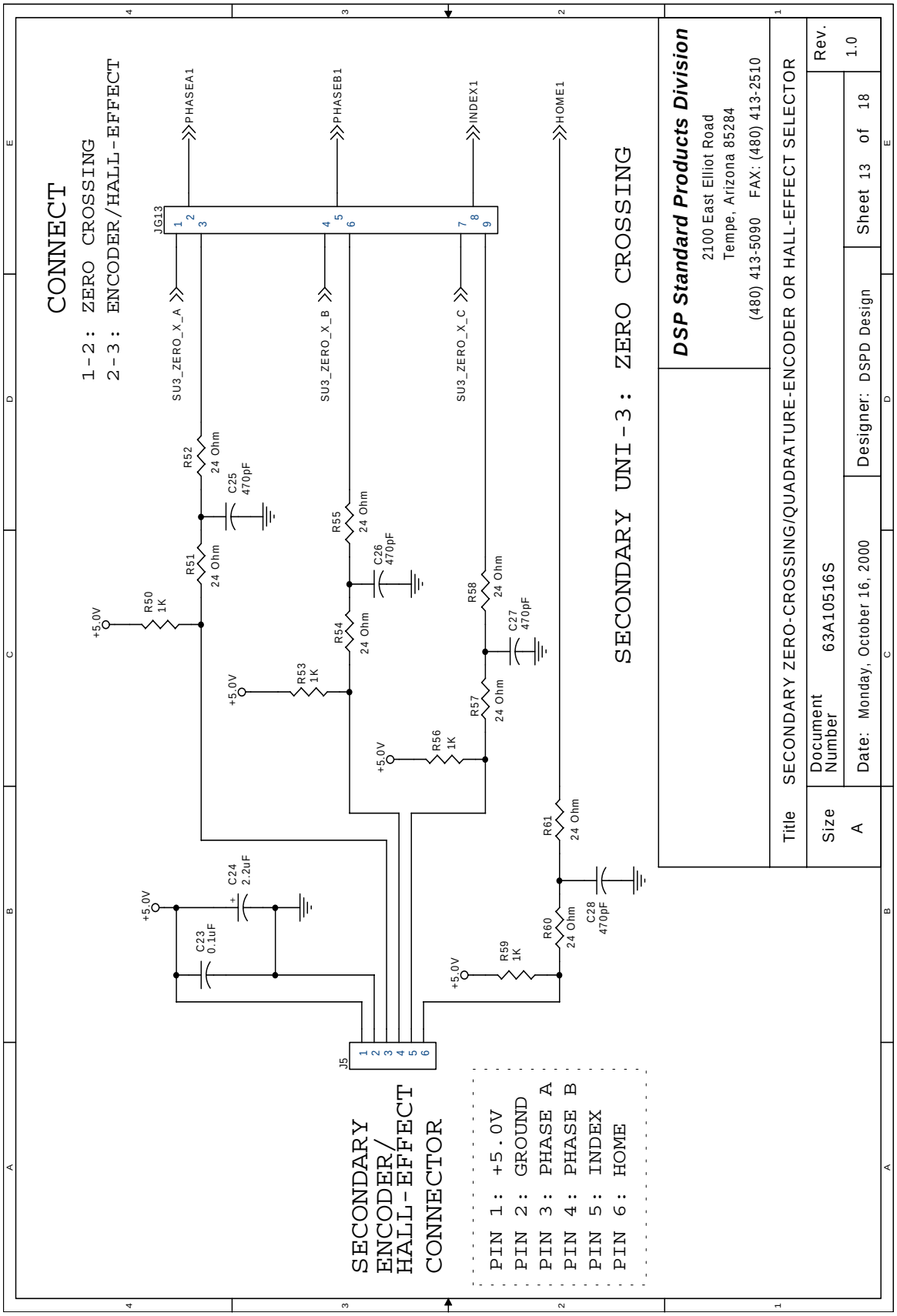

Figure A-13. Secondary Zero-Crossing/Quadrature-Encoder or Hall-Effect Selector

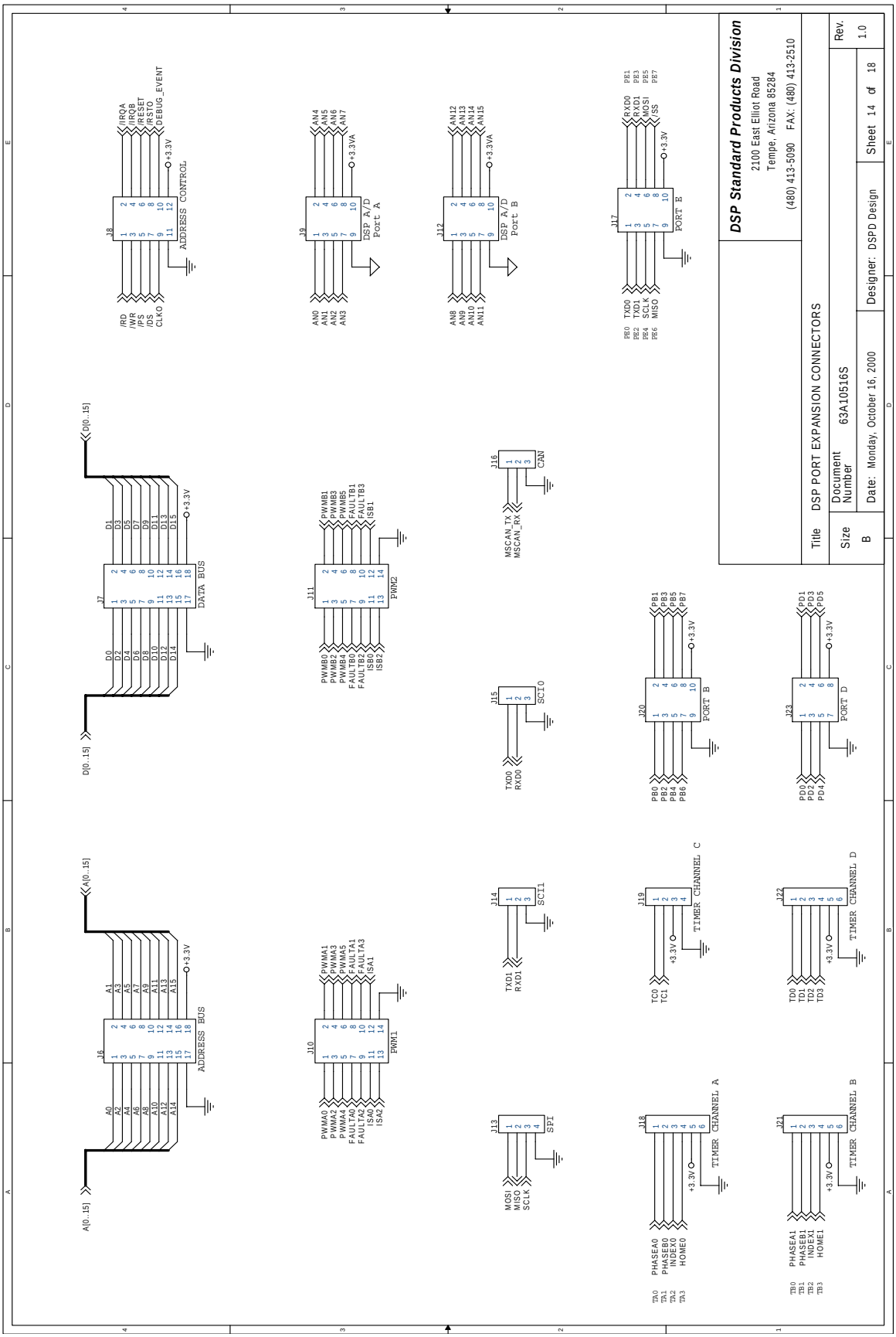

Figure A-14. Port Expansion Connectors

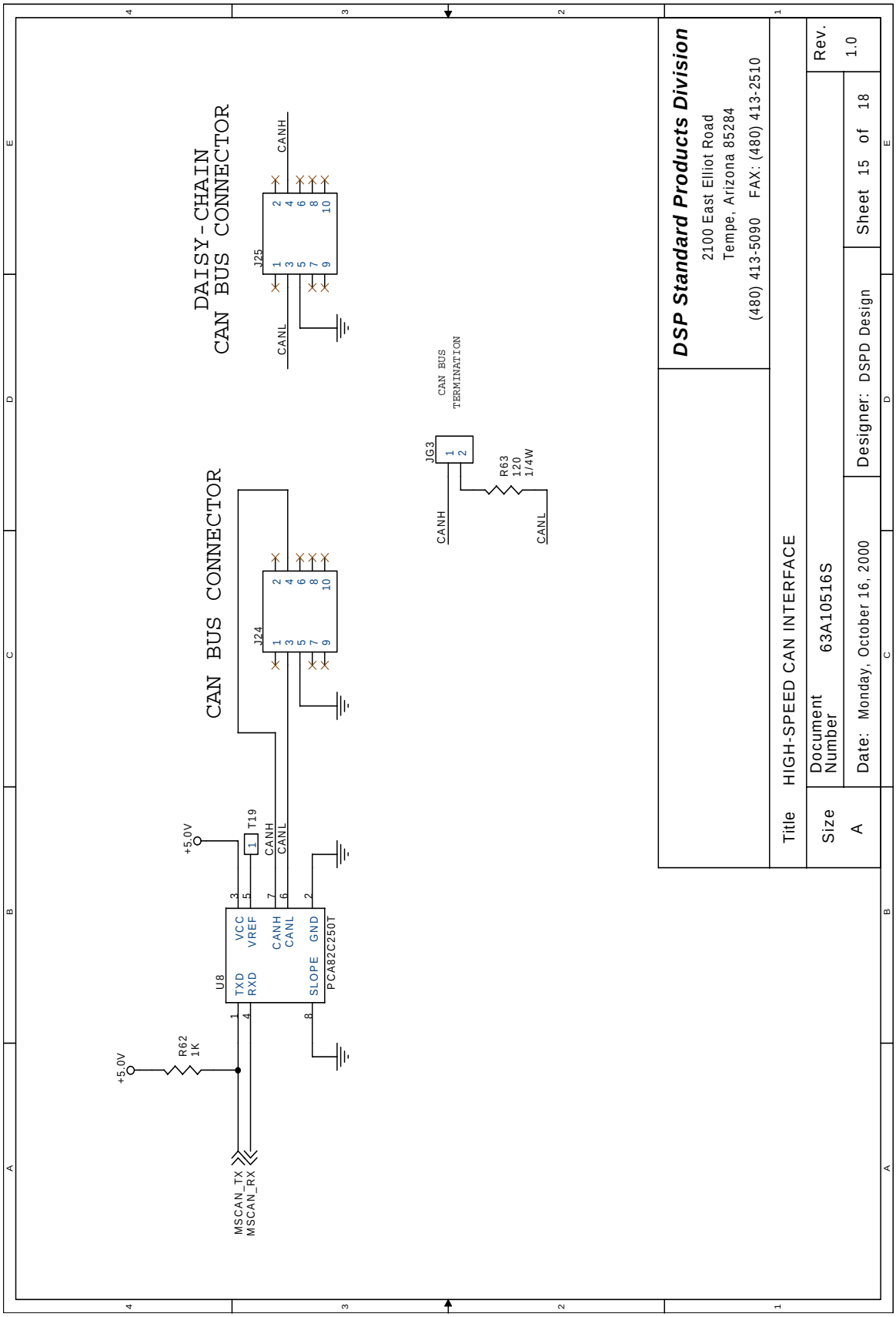

Figure A-15. High-Speed CAN Interface

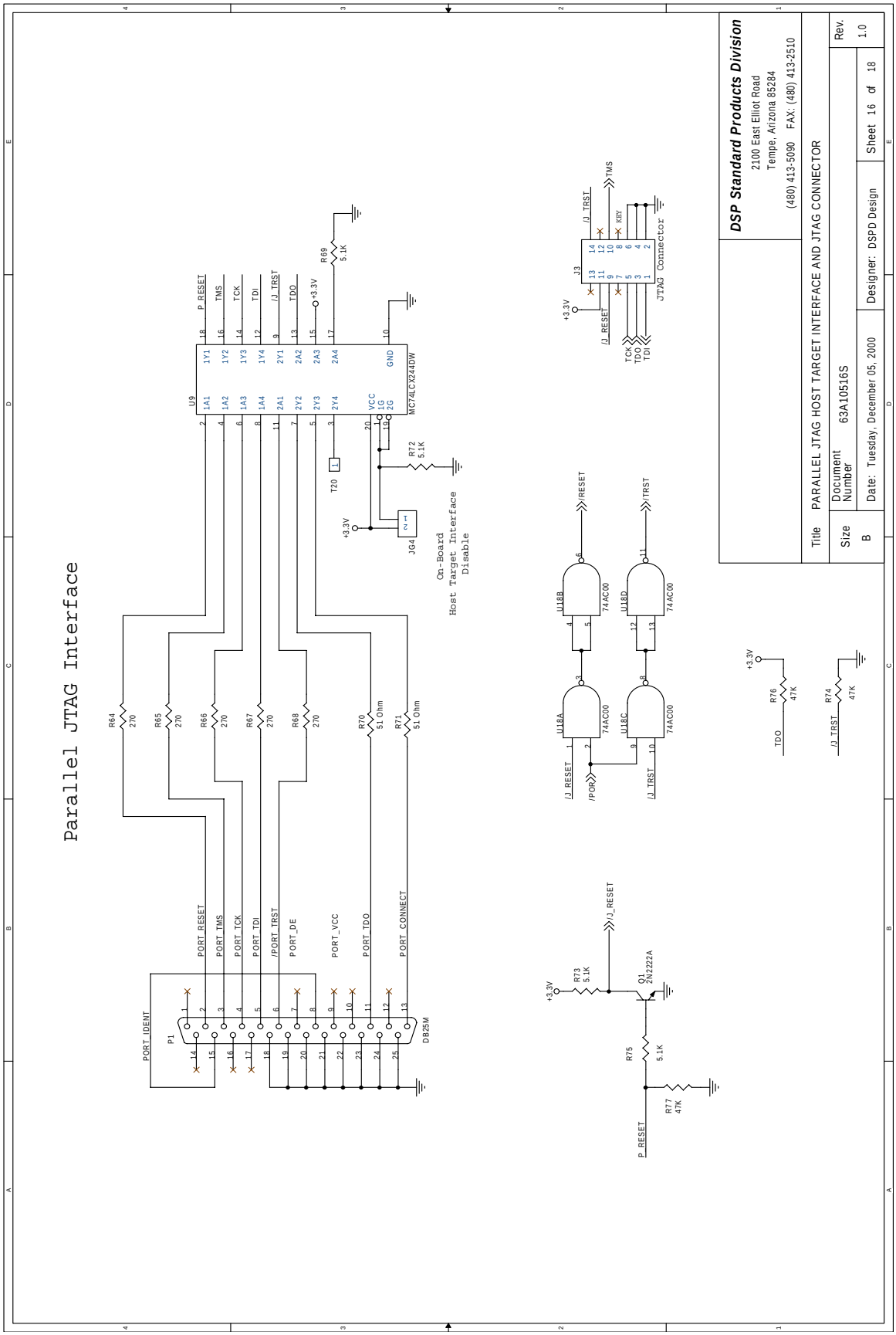

Figure A-16. Parallel JTAG Host Target Interface and JTAG Connector

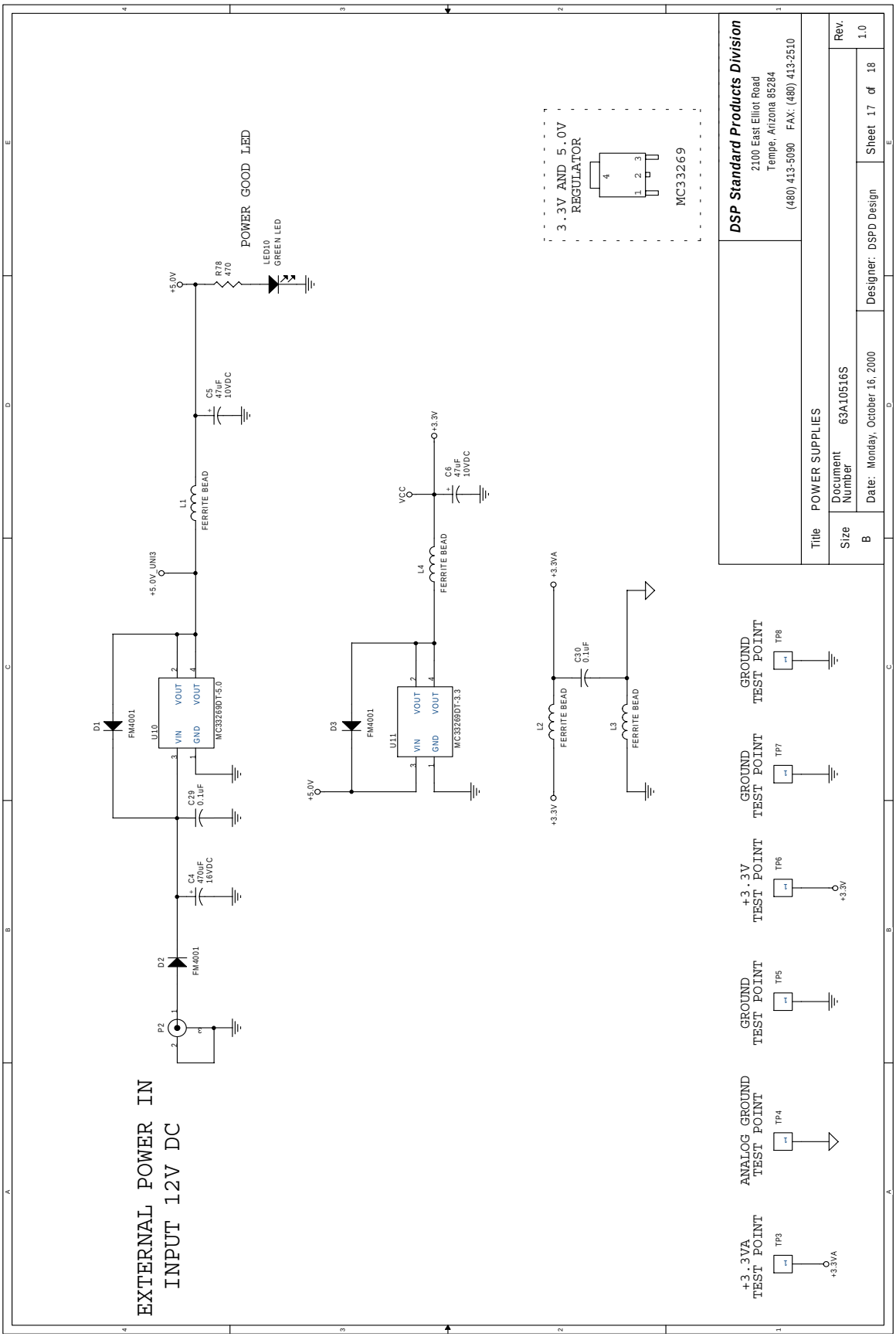

Figure A-17. Power Supplies

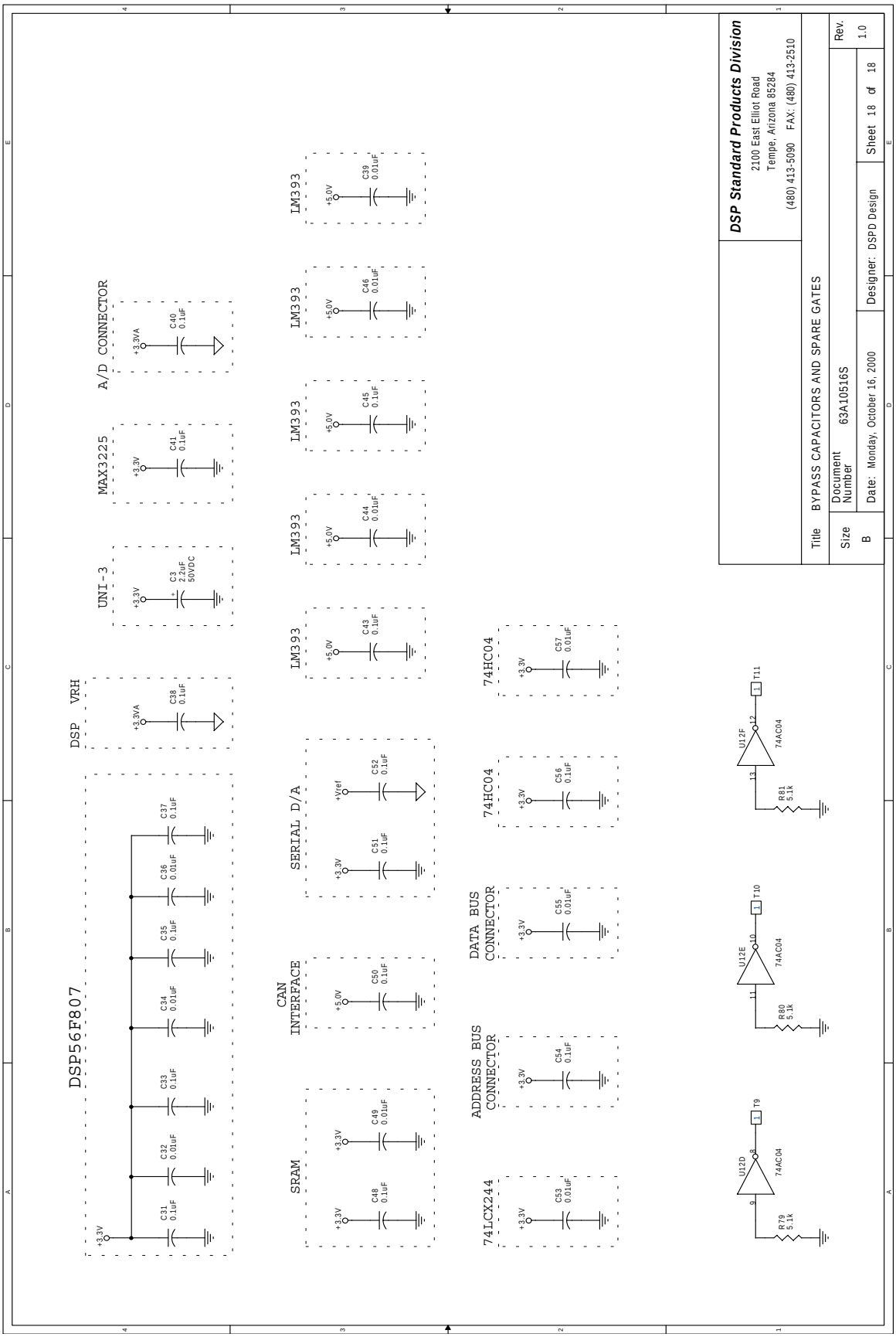

Figure A-18. Bypass Capacitors and Spare Gates

Appendix B
56F807EVM Bill of Material

Qty.	Description	Ref. Designators	Vendor Part #s
Integrated Circuits			
1	DSP56F807FV80	U1	Freescale, DSP56F807FV80
5	LM393	U3—U6, U16	National, LM393M
1	74LCX244	U9	ON Semiconductor, MC74LCX244DW
2	74AC04	U12, U15	Fairchild, 74AC04SC
1	MC33269DT-5.0	U10	ON Semiconductor, MC33269DT-5.0
1	MC33269DT-3.3	U11	ON Semiconductor, MC33269DT-3.3
1	GS72116	U2	GSI, GS72116TP-12
1	MAX3245	U13	Maxim, MAX3245EEAI
1	MAX5251	U14	Maxim, MAX5251BEAP
1	PCA82C250T	U8	Philips Semiconductor, PCA82C250T
1	74AC00	U18	Fairchild, 74AC00SC
Resistors			
20	16K Ω	R8—R11, R16—R19, R24—R29, R31, R32, R107, R108, R112, R113	SMEC, RC73L2A16KOHMJT
10	1M Ω	R4, R5, R12, R13, R20, R21, R30, R33, R109, R114	SMEC, RC73L2A1MOHMJT
18	5.1K Ω	R6, R7, R14, R15, R22, R23, R34, R35, R69, R72, R73, R75, R79—R81, R96, R110, R115	SMEC, RC73L2A5.1KOHMJT
12	10K Ω	R82—R85, R117—R123, R125	SMEC, RC73L2A10KOHMJT
2	51 Ω	R70, R71	SMEC, RC73L2A51OHMJT

Qty.	Description	Ref. Designators	Vendor Part #s
Resistors (Continued)			
3	47K Ω	R74, R76, R77	SMEC, RC73L2A47KOHMJT
1	470 Ω	R78	SMEC, RC73L2A470OHMJT
1	10M Ω	R1	SMEC, RC73L2A10MOHMJT
20	1K Ω	R38, R41, R44, R47, R50, R53, R56, R59, R62, R86—R95, R124	SMEC, RC73L2A1KOHMJT
14	270 Ω	R64—R68, R98—R106	SMEC, RC73L2A270OHMJT
16	24 Ω	R39, R40, R42, R43, R45, R46, R48, R49, R51, R52, R54, R55, R57, R58, R60, R61	SMEC, RC73L2A24OHMJT
1	120 Ω, 1/4W	R63	YAGEO, CFR 120QBK
Potentioneters			
7	10K Ω	R2, R3, R36, R37, R97, R111, R116	BC/MEPCOPAL, ST4B103CT
Inductors			
4	1.0mH	L1, L2, L3, L4	Panasonic, EXC-ELSA35V
LEDs			
1	Red LED	LED1	Hewlett-Packard, HSMS-C650
4	Yellow LED	LED2, LED4, LED6, LED8	Hewlett-Packard, HSMY-C650
5	Green LED	LED3, LED5, LED7, LED9, LED10	Hewlett-Packard, HSMG-C650
Diodes			
3	S2B-FM401	D1, D2, D3	Vishay, DL4001DICT
Capacitors			
5	2.2μF, 50V DC	C1—C3, C18, C24	NICHICON, UWX1H2R2MCR2GB
31	0.1μF	C7—C17, C23, C29—C31, C33, C35, C37, C38, C40, C41, C43, C45, C48, C50—C52, C54, C56, C65, C66	SMEC, MCCE104K2NR-T1
1	470μF, 16V DC	C4	ELMA, RV-16V471MH10R
2	47μF, 16V DC	C5, C6	ELMA, RV2-16V470M-R
8	470pF	C19—C22, C25—C28	SMEC, MCCE471J2NO-T1

Qty.	Description	Ref. Designators	Vendor Part #s
Capacitors (Continued)			
10	0.01μF	C32, C34, C36, C39, C44, C46, C49, C53, C55, C57	SMEC, MCCE103K2NR-T1
4	1.0μF, 50V DC	C60—C63	NICHICON, UWX1H010MCR1GB
Jumpers			
8	3 × 1 Bergstick	JG1, JG2, JG5, J14, J15, JG16, J16, JG17	SAMTEC, TSW-103-07-S-S
4	4 × 2 Bergstick	JG11, JG15, J23, J26	SAMTEC, TSW-104-07-S-D
6	1 × 2 Bergstick	JG3, JG4, JG6, JG7, JG8, JG9	SAMTEC, TSW-102-07-S-S
4	3 x 3 Bergstick	JG10, JG12, JG13, JG14	SAMTEC, TSW-103-07-S-T
2	9 x 2 Bergstick	J6, J7	SAMTEC, TSW-109-07-S-D
3	6 x 1 Bergstick	J18, J21, J22	SAMTEC, TSW-106-07-S-S
6	5 x 2 Bergstick	J9, J12, J17, J20, J24, J25	SAMTEC, TSW-105-07-S-D
2	4 x 1 Bergstick	J13, J19	SAMTEC, TSW-104-07-S-S
3	7 x 2 Bergstick	J3, J10, J11	SAMTEC, TSW-107-07-S-D
2	6 x 1 MTA	J4, J5	AMP, MTA 640456-6
1	6 x 2 Bergstick	J8	SAMTEC, TSW-106-07-S-D
2	20 x 2 Shrouded	J1, J2	3M, 2540-6002UB
Test Points			
8	1 × 1 Bergstick	TP1—TP8	Samtec, TSW-101-07-S-S
Crystals			
1	8.00MHz Crystal	Y1	CTS, ATS08ASM-T
Connectors			
1	DB25M Connector	P1	AMPHENOL, 617-C025P-AJ121
1	2.1mm coax Power Connector	P2	Switch Craft, RAPC-722
1	DE9F Connector	P3	AMPHENOL, 617-C009S-AJ120
Switches			
5	SPST Pushbutton	S1—S5	Panasonic, EVQ-PAD05R
1	SPDT Toggle	S6	C&K, GT11MSCKE

Qty.	Description	Ref. Designators	Vendor Part #s
Transistors			
1	2N2222A	Q1	ZETEX, FMMT2222ACT
Miscellaneous			
28	Shunt	SH1—SH28	Samtec, SNT-100-BL-T
6	Rubber Feet	RF1—RF6	3M, SJ5018BLKC

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S

T

U

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