# ERC Pathchk

Specification statement

Reports nets in the layout that do or do not have a path to power, ground or labeled nets, or that satisfy a combination of these conditions. Used during circuit extraction in Calibre nmLVS, Calibre nmLVS-H, and ICtrace Mask mode.

**Note**

This statement is provided primarily for backward compatibility. The Pathchk layer stat conducting ERC checks.

## Usage

**ERC PATHCHK**
{***labeled_flag*** | ***power_ground_flag*** [*operand power_ground_flag*]}
[POLYGONS NETS | POLYGONS | NETS]
[BY LAYER] [BY CELL | FLAT]
[PORTS ALSO] [NOFLOAT] [EXCLUDE UNUSED]
[EXCLUDE SUPPLY]

## Parameters

- ***labeled_flag***

A required string that specifies how the tool reports a net that does or does not have a path to a top-level labeled net. This option requires top-level connectivity (Text Layer) text objects that are neither power nor ground net labels to be present. Possible choices are:

**LABELED** — Reports nets with a path to a labeled (Text Layer) net.

**! LABELED** — Reports nets with no path to any labeled (Text Layer) net.

where the exclamation mark (!) is synonymous with Boolean NOT.
A ***labeled_flag*** may not be specified with a ***power_ground_flag***.

- ***power_ground_flag***

A required string that specifies how the tool reports a net that does or does not have a path to a top-level supply net. Power and ground nets are top-level nets specified in the LVS Power Name and LVS Ground Name statement. This option requires top-level connectivity (Text Layer) text objects that are power and/or ground net labels to be present. Possible choices are:

**POWER** — Reports nets with a path to a power net.

**! POWER** — Reports nets with no path to a power net.

**GROUND** — Reports nets with a path to a ground net.

**! GROUND** — Reports nets with no path to a ground net.

Where the exclamation mark (!) is synonymous with Boolean NOT.

The ***labeled_flag*** and the ***power_ground_flag*** keywords, when not connected by an *operand*, are called *primitive* conditions.

- *operand*

An optional string of logical symbols that combine two primitive conditions. Possible choices are:

&& — Selects nets that satisfy both primitive conditions: Boolean AND.

|| — Select nets that satisfy the first or second primitive condition, or both: Boolean OR.

- POLYGONS NETS | POLYGONS | NETS

Specifies the type of results file to output. Possible choices are:

POLYGONS — Generates an Calibre nmDRC results database in ASCII format that contains the polygon output of all nets that satisfy the specified conditions.

NETS — Generates a text file that contains a list of all nets that satisfy the specified conditions.

Both are specified by default.

- BY LAYER [BY CELL | FLAT]

An optional keyword set that specifies the type of output to include in the generated ASCII results file. These pertain to the POLYGONS option only. Possible choices are:

BY LAYER — Generates a separate check for each layer. If both BY CELL and BY LAYER are specified, a check is generated for each layer in each cell. Empty checks are not generated.

BY CELL — Causes each cell that has cell-specific results to be checked separately. The check contains nets reported in that cell. The results are reported in top-level coordinate space. BY CELL is ignored in flat execution.

FLAT — Causes cell-specific results to be replicated in every placement. FLAT has no effect in flat execution.

- PORTS ALSO

An optional keyword that specifies to output polygons on nets that are connected only to port objects (nets having Text Layer objects on them are not included). By default, such nets are not included in the output for any request. The PORTS ALSO option removes the special treatment of port nets. This option affects both POLYGONS and NETS output. Note that port objects are specified with the Port Layer Text in Calibre, and the $make_port() command in Pyxis Layout.

- NOFLOAT

An optional keyword that instructs the statement to ignore floating nets. Floating nets are nets that are not connected to any devices.

- EXCLUDE UNUSED

An optional keyword that instructs the statement to exclude *unused* nets from the ERC Pathchk output. Unused nets are connected only to unused devices. Unused devices are specified with LVS Filter Unused Option or equivalent LVS Filter Unused

statements. All options for LVS Filter Unused Option are supported except the INV, P, and Q options.

- EXCLUDE SUPPLY

An optional keyword that instructs the tool to exclude power and ground nets from the results of an ERC Pathchk request containing at least one of the keywords **POWER** or **GROUND** (not preceded by the ! operator). Supply nets are included if EXCLUDE SUPPLY is not specified.

## Description

Reports nets in the layout that do, or do not, have a path to top-level power and/or ground nets, or labeled nets.

By default, a *path* is any route that leads through source/drain pins of built-in MOS devices or pos/neg pins of built-in resistor devices. To qualify, a MOS device (types M, ME, MD, MN, MP, or any of the LDD-type devices) must have at least the following pins: G (or gate), S (or source), and D (or drain). Paths through LDD-type devices are formed in both directions. Capacitor, diode, or bipolar devices can also be added to the path, as specified in ERC Path Also statements.

If you want to enable user-defined devices to participate in ERC Pathchk (user-defined devices do not participate by default), then you must map these devices and their pins to built-in devices and pins. This is done using the LVS Device Type specification statement. See "User-Defined Devices in Path Check Operations" in the *Calibre Verification User's Manual*.

Power and ground nets are specified with LVS Power Name and LVS Ground Name specification statements, respectively. This statement utilizes wildcard characters that appear in LVS Power Name and LVS Ground Name specification statements. Power and ground nets break paths.

The hierarchical level from which text objects are read is controlled by the Text Depth statement.

Power and ground nets are included in the result for the keywords **POWER** and **GROUND**. For example, supply nets are included if you specify:

```
ERC PATHCHK POWER
```

You can exclude supply nets by specifying EXCLUDE SUPPLY. When specifying EXCLUDE SUPPLY, at least one of the **POWER** or **GROUND** keywords must also be specified in the statement. (The EXCLUDE SUPPLY keyword does not apply to the **! POWER** or **! GROUND** keywords.) For example:

```
ERC PATHCHK POWER && ! GROUND EXCLUDE SUPPLY
```

is allowed. However, this form causes a compiler error:

```
ERC PATHCHK ! POWER && ! GROUND EXCLUDE SUPPLY // bad syntax
```

Power and ground nets are not included in the result for **! POWER** and **! GROUND** keywords. The supply net itself is not selected even if there is no path from power to ground. For example:

**ERC PATHCHK ! GROUND**

If a net in the design matches more than one of LVS Power Name or LVS Ground Name name patterns, a warning is issued and conflicts are resolved with power names being given priority over ground names.

The **LABELED** nets are those with connectivity extraction (Text Layer) text, but they are not power or ground nets.

By default, nets that are labeled by port objects alone (no Text Layer objects) are not output. The PORTS ALSO option changes this behavior. All objects from nets connected to top-level nets named by port objects alone are output.

ERC Pathchk statements respect the LVS Compare Case statement. If either the LVS Compare Case YES or LVS Compare Case NAMES statement is specified, then power names and ground names are traced in a case-sensitive manner; otherwise they are case insensitive. These rules on case sensitivity apply to LVS Power Name and LVS Ground Name nets.

ERC Pathchk observes the Layout Preserve Case specification statement for case-sensitivity of net names. See "Case Sensitivity of Supply Net Names" in the *Calibre Verification User's Manual* for more details.

This statement applies to Calibre nmLVS/Calibre nmLVS-H and ICtrace Mask mode. It is executed during circuit extraction and only when the layout is geometric. The following Calibre commands execute this statement:

```
calibre -lvs rules              // executed flat
calibre -lvs -tl ... rules      // executed flat
calibre -lvs -hier ... rules    // executed hierarchically with
                                // geometric Layout System
calibre -spice ... rules
```

The following Pyxis Layout commands execute this statement:

```
$lvs_mask()            // executed flat
$write_mask_cnet()     // executed flat
```

Note the following important considerations:

- The **POWER**, **GROUND**, and **LABELED** options (without the ! operator) are not recommended because they can generate very large files, consume large amounts of memory, and lead to long runtimes. In particular, in hierarchical ERC, such requests essentially flatten the design hierarchy.

- In the default mode, with neither FLAT nor BY CELL specified, the polygon output may contain polygons belonging to a cell in two ways:

- If a net in the cell violates ERC Pathchk requirements in some placements of this cell, the polygons are written out for each placement where the violation occurs in top-level coordinates.

- If, for a given net, a violation appears in every placement of a cell, the polygons are written out once, in the lowest, leftmost placement.

This can lead to confusion because, in the same cell, some polygons may be displayed in many placements and others in only one placement. If the results are difficult to interpret, the BY CELL option can be useful.

The FLAT option can also be used to force Calibre to output cell-specific results in all placements. This increases both memory consumption and the size of the polygon file, but can eliminate potential confusion caused by hierarchical output. However, output using the NETS option is unambiguous in all cases.

ERC Pathchk statements are not executed if the specified net is not present. For example, if there is no power net in the layout, then ERC PATHCHK ! POWER generates an error message and generates no output.

## Results Output Options

The output files are readable by RVE similar to a DRC Results Database.

**POLYGONS —** The POLYGONS option specifies a file named *layout_primary*.*pathchk.erc*. It is placed in the Mask SVDB Directory if that statement is specified, otherwise in the current working directory.
If *layout_primary* is not specified, the word lvs is used instead. The file consists of lines in the format:

```
ERC PATHCHK condition [ in cell cell_name ] [ layer_name ]
```

where *condition* is the specified condition, such as ! POWER or ! POWER && GROUND. By default, results from each ERC Pathchk statement are written to one check in the result file. If the BY CELL option is specified, then the results are classified by cell and the *cell_name* field indicates the cell name. If the BY LAYER option is specified, then the results are classified by layer and the *layer_name* field indicates the layer. Empty checks are not written. If all checks are empty, no file is created.

All polygon results are shown in the top-level coordinate space, and they are written to a Calibre nmDRC results database in ASCII format. By default, hierarchical Calibre shows cell-specific results only once in a representative placement of the cell. The lowest, leftmost placement of each cell serves as its representative. This is similar to Calibre nmDRC-H. Results are cell-specific if they can be generated locally in the cell and occur in all placements of the cell in the design.

Note that polygon results generated by ERC Pathchk are not fully merged. This means that polygons can abut or overlap.

**NETS —** The NETS option specifies a file named *layout_primary*.pathchk.rep. It is placed in the SVDB directory by default, otherwise in the current working directory. If*layout_primary* is not specified, the word lvs is used instead.

In hierarchical execution, the report file format is this:

```
ERC PATHCHK REPORT for layout_primary
  ERC PATHCHK condition:
    cell cell_name (placement): net1, net2, ...
    cell cell_name (placement): net1, net2, ...
```

where *condition* is the specified condition, such as GROUND AND ! POWER, *cell_name* is a cell name where results were found, *placement* is a representative placement of that cell, and net*i* is a net name or number. Cells are listed in bottom-up order. Net names and numbers are in the context of the indicated cells. Cells for which no nets are found by ERC Pathchk are not written to the report file.

In flat execution, the report file format is:

```
ERC PATHCHK REPORT for layout_primary
  ERC PATHCHK condition:
    net1, net2, ...
```

Nothing is reported for requests in which no nets are found in any cell. If all checks are empty, no file is created.

## Requirements and Restrictions

Hierarchical Calibre operations impose a size limit on intermediate data structures generated by ERC Pathchk. The limit is approximately 400 MB. This limit is applied independently to each individual ERC Pathchk statement. Calibre generates incomplete results (some polygons may be omitted from the output) and issues the following warning if Calibre reaches this limit:

```
WARNING: ERC operation exhausted allowed memory allocation.
```

Calibre issues the warning in both the transcript and the circuit extraction report.

This limit applies only to polygon output, for example during the construction of a result layer and when performing the POLYGONS option.

Calibre always completes the net reporting part of this functionality, including the functionality resulting from the NETS option.

You should not reach this limit in normal operations. You see it only in circumstances when a very large net is selected by the ERC Pathchk statement.

See also ERC Summary Report. The search features Find Path and Isolate Path on Layout Net in Calibre RVE for LVS may also be of interest.

## Examples

### Example 1

The following statement outputs a text file listing all the nets with a path to a labeled net:

```
ERC PATHCHK LABELED NETS
```

### Example 2

When not using the [ ! ] LABELED option, the following combinations are possible:

! POWER && GROUND
Nets with no path to power but with a path to ground

! GROUND && POWER
Nets with no path to ground but with a path to power

! GROUND && ! POWER
Nets with no path to ground and no path to power

! GROUND || ! POWER
Nets with no path to ground or no path to power (or both)

POWER && GROUND
Nets with a path to both power and ground

POWER || GROUND
Nets with path to power or a path to ground