SmartLEWIS [™] RX+ TDA5240/35/25 Explorer

Configuration and Evaluation Software B12.6.51

High Sensitivity Receiver with Digital Baseband Processing (TDA5240/35) / Digital Slicer (5225)

USER MANUAL v51

Wireless Control

Infineon Technologies



Never stop thinking.



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1 Introduction

The TDA5240/35/25 Explorer is used to configure the TDA5240, TDA5235 or the TDA5225 and to generate register settings. The tool provides a wizard with a set of pages to configure the TDA5240, TDA5235 or the TDA5240. Each functional block of the TDA5240/35/25 is logically grouped together and represented in a separate dialog. The tool allows the user to save all the changes made in the configuration and retrieve these changes later on.

1.1 Hardware and Software Components

For a fully functional system, the following hardware components are required:

- PC with Microsoft Windows Vista, Microsoft Windows 7 (32-bit or 64-bit vesion), Microsoft Windows XP or Windows 2000 operating system
- Minimum graphical screen resolution 1024 x 768

Additionally, the following software components are needed:

 Microsoft .Net Framework Version 2 or above. Make sure it is installed on your computer correctly, if it is not you can download it from <u>http://www.microsoft.com/downloads/details.aspx?displaylang=de&FamilyID=0856</u> eacb-4362-4b0d-8edd-aab15c5e04f5

Optional are the following software components:

- Infineon SIB Server Package.

1.2 Installation of Software

Before installing the software please remove all previous versions of it.

It is recommended to uninstall the TDA5240/35/25 Explorer via the start menu link "Uninstall Configuration Utility" in the "Infineon Technologies" start menu group.

If uninstalling fails for some reason please try following options to remove the Windows Installer entry for the TDA5240/35/25 Explorer:

- 1. Uninstall by using the "Add/Remove Programs" function in the control panel.
- **2.** Use the Windows Install Clean Up tool. This tool is provided by Microsoft and can be downloaded from their homepage for free. Select the TDA5240-35-25 entry of the product list and press remove.
- If none of the proposed methods work please open the Windows registry (regedit.exe) and navigate to the folder
 "HKEY_CURRENT_USER\Software\Microsoft\Installer\Products". Find the subfolder that
 contains the ProductKey "TDA5240-35-25 Explorer" and delete the folder. Then remove
 the folder "Infineon Technologies\TDA Explorer" in the program files folder of your system.

Please follow the sequence below to install the **Software**:

- 4. Start your PC and Microsoft Windows.
- 5. Execute the "TDA5240-35-25 Explorer_B12.6.xx.x.exe" installer package. In case a previous version of the TDA5240-35-25 Explorer is detected, a warning to remove the old version will be displayed.



6. The setup wizard appears. Press the *"Next"* button to proceed with the installation.



7. If custom installation path is desired, enter it now. Press the "*Next*" button to proceed with the installation.





8. Read the license agreement carefully and accept it to proceed with the installation. Select the check box button *"I accept..."* and press the *"Next"* button to proceed the installation.



9. Confirm the Installation by pressing the *"Install"* button





10. A progress bar indicates the setup progress now. **Notice**: If a "*User Account Control*" dialog appear, press the "Yes" button to continue installation.



11. After the installation procedure has finished, press the *"Close"* button to terminate the setup application.





Installing SIB 2.0 Server

The SIB 2.0 Server offers communication services and protocol handling for compatible interface boards (SIB2, UWlink). The Explorer software can be used without SIB 2.0 Server for creating configurations only. With the SIB 2.0 Server and an interface board you are able to download the configuration to the chip. To verify it, status registers and FIFO can be read on the Explore page.

NOTE: SIB 2.0 Server setup is automatically done during installation of the Explorer software. Anyhow, the manual installation procedure is described below.

1. Start installed Explorer software from the start menu (*Start -> Programs -> Infineon Technologies -> TDA5240-35-25 Explorer 6.xx.x*).



- 2. Choose SIB 2.0 Server Setup
- 3. Click the "Start" button



The setup wizard appears. Press the "Next" button to proceed with the installation.
 Notice: If a "User Account Control" dialog appear, press the "Yes" button to continue installation.



 You need to install all Software components shown here except of "SP3x/PMA5110 Extension". After choosing the required software components (A) please click on the "Next" button.





6. Click on the "Install" button to install the software on your computer



7. A progress bar indicates the setup progress now.





8. Setup will be completed by clicking the *"Finish"* button





2 User Interface and Getting Started

To start configuration utility choose the application loader executable (*NextGenLoader.exe*) from the start menu (*Start -> Programs -> Infineon Technologies -> TDA5240-35-25 Explorer 6.xx.x*).

The loader pad offers a runtime environment for installed applications.

In the following description the TDA5240/35/25 B12 Explorer is described. Please note that the TDA5235 Explorer contains just subset functionalities of the TDA5240 Explorer. TDA5235 supports only 2 sets of configuration and only 1 RF channel per configuration, while TDA5240 supports 4 sets of configuration and 3 RF channels per configuration. Therefore the TDA5240 is mainly reflected in the following figures. TDA5225 provides no digital baseband processing (no Signal Recognition feature, no CDR, no Framer, no Message-ID, only limited Self-Polling features). Differences to the TDA5225 and the TDA5235 are highlighted in the description of the configuration pages.



2.1 Infineon Evaluation Software Startup Screen

- 1. Close-Button
- 2. Minimize-button
- 3. SIB 2.0 Server Setup
- 4. TDA5240 B12 Explorer / TDA5235 B12 Explorer / TDA5225 B12 Explorer
- 5. Start-Button

2.2 Starting TDA5240/35/25 Explorer

- Choose "TDA5240 B12 Explorer", the "TDA5225 B12 Explorer", or the "TDA5235 B12 Explorer" on the NEXTGENLOADER pad (4)
- 2. Click the Start-button (5)
- 3. A splash-screen is displayed during application loading



3 TDA5240/35/25- B12 Explorer



Figure 2: Wizard Startpage

- 1. TDA5240/35/25 tab
- Logging tab
- 3. Wizard tab
- 4. Registers tab (see chapter 3.4)
- 5. Explore tab (see chapter 3.3)
- 6. About tab



There are 2 major areas in this software which can be easily accessed by their corresponding tabs:

- TDA5240/35/25 tab (1) for:
 - o Configuring the device by using the wizard (3) (Chapter 3.2)
 - Viewing the register content in the Register tab (Chapter 3.4)
 - Communicating with the device in the Explore tab (Chapter 3.3)
- Logging tab (2) for viewing the log-file (Chapter 4)

Getting additional information about available functions

Explo SIB2	rer Register	
54 Mi	zard Registers Explore About	
A5:	Subgroup Selection 1 Master Control Unit	A _ Configuration Selection
Logging TD	Chip control: Operating Mode © Sleep Mode C Run Mode Slave C Self Polling Mode Hold in register config. state: Multi C B Configuration C C D C A+B+C A+B+C C A+B+C+D C A+B+C+D Init PLL after coming from HOLD Lock Data FIFO Init of FIFO at at EDM C Init of FIFO at Cycle Start Frame Start Config. A Modulation Run Mode Slave Self Polling Mode Wake In B Run Mode	Port Pin Port Pin 0 Output Signal Selection Port Pin Image: Port Pin 2 Selection: inv. high p. Port Pin 2 Selection: inv. high p. NINT Port Pin 3 Selection: inv. high p. RX_RUN Image: Pin 2 Selection: Inv. high p. RX_RUN Image: Pin 2 Selection: Inv. high p. RX_RUN
	r ASK ASK ASK	(r.f. A)
	C FSK FSK FSK	
	C ASK FSK ASK C FSK ASK FSK	A ROW Computation: Enable Interrupt at signal NIN I: For Active Level on PP0 for Conf. A For A Wake Up A Wake Up
	External Data Processing: C Chip Data (RX Mode: TMCDS) C Data (MF) (RX Mode: TMMF, TMRDS)	Image: Control Contro Control Control Control Control Control Control Control Control C
		Next ->
Chip SIE Re Cry	a Control 32::LNZS0379:;GRZ00002 fresh Open Close rstal Oscillator [MHz]: 21.948717 Choose slightly different Choose slightly different Crystal frequency	Vite Registers

Figure 3: Valuable Functions - Tooltips

Many input and output fields will give additional tooltip information, a while after moving the cursor over this field. This function is available on the Wizard-Tab, on the Register-Tab and on the Explore-Tab.



3.1 General Control

Expl	orer	
SIB2	Register	
9 W	lizard Registers Explore About	
452	< > Subgroup Selection 1 Master Control Unit	A Configuration Selection
Ê	Chip control:	Port Pin Output Signal:
Logging	Operating Mode Image: State sta	Port Pin 0 Selection: inv. high p. LOW Port Pin 1 Selection: inv. high p. DATA Port Pin 2 Selection: inv. high p. NINT Port Pin 3 Selection: inv. high p. RX_RUN
	□ Lock Data FIFO □ Init of FIFO at at EOM □ Cycle Start □ Init of FIFO at Frame Start	Enable SDO High Power Pad
	Config. A	
	Modulation Run Mode Slave Self Polling Mode Wake Up RunMode	
	, ASK ASK ASK	
	O FSK FSK FSK	Config. A
	C ASK FSK ASK	RX RUN Configuration: Enable Interrupt at signal NINT:
	C FSK ASK FSK	Active Level on PPO for Conf. A A A A Wake Up A
	External Data	Image: Construction of the construction Image: Construction Image: Construction Image: Construction Image: Construction Image: Construction Image: Construction <td< th=""></td<>
		Next ->
	IP Control IB2::LNZ50379::GRZ00002 eftestn open Close Tystal Oscil ator [MHz]: 2 Choose slightly different C) stal frequency Read Registers	Status Register download ==> OK (27 registers written) Register download ==> OK (27 registers written) Verting burst mode register download Service SIB2::LNZS0379::GRZ00002/TDA5240 initialized Verticen.Internal.TDA5240RegisterController
1	4 Figure 4: 0	General Control

- 1. SIB & Evaluation board selection
- 2. Virtual status indication LED
- 3. Register control buttons
- 4. Crystal oscillator adjustment

Note:

- Functions from the Chip control selection (1) can be chosen from "SIB2 menu bar".
- Functions from the Register control buttons (3) can be chosen from "Register menu bar".
- The address format of the evaluation hardware is defined as follows: SIB2::<master board ID>::<sub board ID> If the master-board should be addressed directly the sub-board ID has to be replaced by the key "BOARD".



3.1.1 Chip Control

Choose your sub-board from the chip control-Selection combo-box (1). If a SIB board is connected when the Explorer runs already you have to press the Refresh button to update the combo-box.

Most calculations of the Explorer have the crystal frequency as an input variable. For some special cases it is possible to adjust this input within a small range (4). If the entered value is not in the valid range of +/-10 kHz around the recommended crystal frequency of 21.948717 MHz the input field turns to red and the default frequency is used then. When choosing a different frequency also the second IF at 274 kHz will be detuned. This can be compensated by adjusting the RF channel frequency. When changing the crystal frequency other than the default value, all wizard pages need to be checked again.

3.1.2 SIB (System Interface Board) Status

Press the "Open"-Button. If the virtual LED (2) turns from red to green, your board will be ready to use. Communication with the chip is only possible when opening a sub-board device (sub board ID must not be "BOARD"). A sub board can be identified by the sub-board serial key.

The SIB connection procedure performs following operations:

- Establishing a connection to the SIB server. If the SIB server process is not started, it will be started now. If the SIB server start takes longer than the Explorer start or a SIB board has been connected after starting the Explorer you may have to refresh the device list by pressing the "Refresh" button
- The SIB hardware is verified. If a wrong sub-board is connected or an outdated SIB server plug-in for the target device is installed, the connection fails. If you are sure about using the correct firmware, please try to plug the sub-board off and on to force a firmware update and press the "Refresh" button followed by the "Open" button again.
- After the connection to the SIB hardware has been established successfully, the message "Device SIB2::MASTERBD::SUBBOARD/TDA52xx initialized" will be displayed. The chip variant is being verified and compared to the running Explorer variant. If the chip variant does not match the running Explorer variant, a correct operation is not guaranteed and a warning will be displayed in the SIB status box.
- A message box appears and you will be asked whether you want to reload the actual Explorer configuration to the chip. Choose "Yes" to download the settings of the actual configuration. This will bring the chip to a state where its settings represent exactly the settings of the Explorer software. If you choose "No" the chip will be reset, but no configuration is transferred to it. The configuration of the Explorer will be set to the default register settings. Any former setting gets lost unless you saved it to a SPI configuration file.
- When downloading the register settings the first time, a set of registers is written additionally to these which were affected by the settings you made. These registers are listed in the appendix (see 5.1 Register patch list) and they are written to equalize the default state of hardware and software. All write operations done by the Explorer are mapped to the SPI configuration file, therefore all settings you produce while experimenting using the Explorer are available in the output file regardless how often you change and download a setting to the chip.

3.1.3 Updating Registers

Changes in the configuration can be transferred to the chip by pressing the "Write Registers" button. If there is any difference in the actual configuration between the user interface and the hardware, the LED "Updated" indicated this by a red color. After a successful update of the registers the color of the LED changes to green. If the color of the LED is dark grey, a connection



to the evaluation hardware is not yet established.

The default download mode for writing registers uses the SPI burst command. All differences of registers between the user interface and the chip are grouped block wise and a SPI burst command is executed for each block separately. If an initial switch to the sleep/hold mode is necessary a separate standard SPI write command is used.

You can force the usage of standard SPI write commands for all registers by un-checking the "Use Burst Mode" checkbox.

The content of read-only registers can be updated by pressing the "Read Registers" button. All controls in the configuration user interface that represents the content of a read-only register will be updated automatically and the register list in the "Registers" tab will be set to the new values.

Important:

• Only read-only registers are affected, you cannot perform read operations on writeable register!

To perform FIFO readout on trial, the "Read FIFO" button can be used. The actual FIFO content is read and will be displayed in the SIB status box. For a more detailed evaluation it is recommended to use the "Run" section of the Explore page.



3.2 Wizard

Gaining efficiency by using the wizard

If you are running this software for the first time it is recommended to use the Wizard to generate your first configurations. Please apply the wizard pages in sequential order as input values of following wizard pages can depend on values from previous pages. The Wizard offers you easy access to the registers of the TDA5240/35/25 and makes your first steps more comfortable.

<u> </u>	<u> </u>	5 🔨	
Explorer			
SIB2 Register			
Q Wizad Registers Explore About			X
Subgroup Selection 1 Master	r Control Unit		A - Configuration Selection
Chip control:		Port Pin Output Signal:	
Operating Mode C Sleep Mode C Run Hold in register Configuration configuration Selection: Int PLL Look Data FIFO Config. A Config. B Config. Modulation ©	Mode Slave © Self Polling Mode C A C B C C C B C C C C C A+B C A+B+C C A+B+C+D after coming from HOLD Init of FIFO at Self Polling Mode Wake Up RunMode ASK ASK ASK Self Polling Mode	Port Pin 0 Selection: inv. high p. LOW ▼ □ □ Port Pin 1 Selection: inv. high p. DATA ▼ □ □ Port Pin 2 Selection: inv. high p. NINT ▼ □ □ Port Pin 3 Selection: inv. high p. RX_RUN ▼ □ □ Enable SDO High Power Pad	
C C External Data C No dea Processing: C Chip Data (M	FSK FSK FSK ASK ASK FSK tivation of functional blocks ta (RX Mode: TMCDS) 5) (RX Mode: TMMF, TMRDS)	Cornig. A [Cornig. C] RX RUN Configuration: Image: Configuration Image: Configuration Image: Configuration Image: Configuration	Enable Interrupt at signal NINT:
Chip Control SIB2::LNZS0379::GRZ00002 Refresh Open Close Crystal Oscillator [MHz]: 21,948717	Read FIFD Read FIFD Choose slightly different Crystal frequency	Use Burst Mode Updated Write Registers	Next ->
	Figure 5: 0	General Control	3 —

Figure 5: General Control

- 1. Navigation buttons
- 2. Subgroup selection
- 3. Next button
- 4. Configuration selection
- 5. Active configuration

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Navigating thru the wizard can be done by 3 different ways.

- 1. Direct access by selecting the subgroup in the drop-down menu (2)
- 2. Browsing forward and backward by pressing the navigation buttons (1)
- **3.** Pressing the "*Next*" button (3), this option is recommended when creating a configuration for the first time, as input values of following wizard pages can depend on values from previous pages.

The TDA5240/35/25 has a multi-configuration capability. Some register settings describe the same functions, but they take effect only if the configuration they belong to becomes active. In the Wizard pages all configuration-dependent settings are framed by a configuration selection tab. The tab header changes in dependency of the active configurations. Whenever you change the active page of the tab (4) the content of the tab page is updated to the settings of the new configuration selection. Switching to another Wizard page retains the active configuration (5). Calculations which forces recalculations on other wizard pages than the active one are performed for the actual configuration only.

Some wizard pages offer interactive configuration support, which will be described in detail for each page of the wizard. These are features like automatic enabling/disabling of controls in dependency of different operating mode, appliance of limits, calculations and dependency updates over multiple wizard pages. In the following subsections for each Wizard page the available calculations and dependencies are explained in the associated paragraphs.

The data management of the Explorer configuration software is concentrated at the register grid on the Registers tab. Individual Wizard pages communicate with the register grid to exchange register content. Whenever the content of the register grid changes, the affected controls will be automatically updated (passive dependencies).

Note: It is not recommended to apply manual changes on the Register Tab, as these changes are not subject of input validation. Otherwise inconsistent settings might be generated.

Beside this data exchange the necessity of reacting to the change of input variables of calculations is given. These changes have impact on registers and the result of a calculation can have impact to registers on other Wizard pages. Whenever an input variable of a calculation targets a register setting of another Wizard page, a calculation will be initiated automatically (active dependency). Figure 6 shows the relationships between the pages.



Figure 6: Active Dependencies of Wizard Pages

To restore a configuration, loading the register values of the TDA5240/35/25 is not enough. Due to the fact that several calculation inputs have impact on a set of registers to summarize the complexity of the registers, these inputs cannot be reproduced from the register values directly. To guarantee exact restoring of the saved configuration such input variables are stored separately in the configuration file (5.2) as persistent variables (for each configuration by appending A/B/C/D to the variable name). Beside numeric values (e.g. data-rate) also textual values will be stored (e.g. TSI pattern name) in the configuration file. Existing persistent variables are described in the chapter of the corresponding Wizard page.



3.2.1 Master Control Unit

Fxplo	vrer	
SIB2	Register	
Q Wi	zard Registers Explore About	
22	> Subgroup Selection 1 Master Control Unit	Configuration Selection
₽ -	Chip control:	Port Pin Output Signal:
Logging	Operating Mode Image: State config. state: Multi Image: State config. state: Image: State config. State configuration Image: State configuration	Port Pin 0 Selection: inv. high p. LOW Image: Constraint of the processing of the procesing of the processing of the procesing of the
	Wake Up RunMode	Config. A
	C ASK FSK ASK C FSK ASK FSK	RX RUN Configuration: Enable Interrupt at signal NINT:
	External Data O No deactivation of functional blocks Processing: O Chip Data (RX Mode: TMCDS) O Data (MF) (RX Mode: TMMF, TMRDS)	✓ Active Level on PP2 for Conf. A ✓ O A Message ID Found ✓ Active Level on PP3 for Conf. A ✓ O A Message ID Found Check for active high, uncheck for active low ✓ O A End of Message
		Next ->
Chip SIE Re Cry	p Control B2::LNZS0379::GRZ00002	Status Uge Burst Mode Updated Write Registers Vertice SIB2:::LNZS0379::GR20002/TDA5240 initialized NextGen.internal.TDA5240RegisterController

Figure 7: Wizard Page 1 - Master Control Unit

This Wizard-tab allows you to configure:

- Operating mode
- Modulation type selection
- Port Pin output signals
- Interrupt masks

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

Dependencies

The Wizard Page 5 - Digital Receiving Unit depends on the Wizard Page 1 - Master Control Unit.

A change of the modulation type selection or a change of the external data processing selection has an impact on the calculation of the register values for the data-rate. At least one of the port pins must be set to output "DATA" to make the setting for the raw data slicer available on wizard



page 5. The buttons "Force EOM" and "Force TOTIM" on the Explore page are operational only if external data processing is set to "Chip Data" or "MF Data".

This page allows you to set the available configurations. This has an impact on all pages that contain a configuration selection tab.

Interactivity

The available configurations and modulation types depend on the selected operating mode. Only the currently possible configurations and modulation types are visible and enabled. If the option "Lock Data FIFO at EOM" is checked, the option "Init of FIFO at Cycle Start" gets inactive and vice versa.

Differences for the TDA5225

The selection for external data processing and FIFO related control bits not available. The content of the port pin output signals is limited to the signals supported by the TDA5225. It is only possible to select the interrupt mask for a wake-up.

When using the DATA output signal (like in a TDA5225), this DATA output signal can be optimized for minimal jitter. In this case a data rate oversampling factor can be set on wizard page 5.

🐴 E	plorer	
SI	2 Register	
ç	Wizard Registers Explore About	
22	< > Subgroup Selection 1 Master Control Unit	Configuration Selection
ĮŽ.	Chip control:	Port Pin Output Signal:
Logging	Operating Mode	Port Pin 0 Selection: inv. high p. LOW Image: First state sta
	Modulation Run Mode Slave Self Polling Mode Wake Up RunMode ASK ASK ASK FSK FSK FSK ASK FSK ASK FSK ASK FSK ASK External Data Processing: Chip Data (RX Mode: TMCDS)	Config. A Enable Interrupt at signal NINT: IV Active Level on PP0 for Conf. A IV IV Active Level on PP1 for Conf. A IV IV Active Level on PP2 for Conf. A IV IV Active Level on PP2 for Conf. A IV IV Active Level on PP2 for Conf. A IV IV Active Level on PP2 for Conf. A IV
	Optimal for highest sensitivity at ideal sampling point Optimization: Optimal for minimal jitter at DATA output signal	Active Level on PP3 for Conf. A A Message ID Found Check for active high, uncheck for active low
	Chip Control SIB2::LN2S0268::GRZ20030	Status S
	Refresh Open Close Read Registers Crystal Oscillator [MHz]: 21,948717 Choose slightly different Crystal frequency Read Registers	Updated >>Device SiB2::LNZS0268::GRZ20030/TDA5240 initialized >>Could not initialize SIB SIB2::LNZS0268::BOARD

Figure 8: Wizard Page 1 - Master Control Unit (minimal jitter at DATA output signal)



Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B).



3.2.2 RF PLL

🐴 Đ	kplorer								
SIB	32 Reg	gister							
各	Wizard	Registers Explore	About						
452	< >	Subgroup Selection	2 RF PLL					A - Configuration Selection	on
Ê	Conf	ig. A Config. B Co	onfig.C)Conf	ig. D					
ogging						_	Possible EMI Source #1 [MHz]	Possible EMI Source #2 [I	MHz]
1				Band Selection:	315MHz 💌	Out of Oand	21	5	
	Nr -	of Channels: Channel 1		Receive Frequency Channel 1 [MHz]:	317.979987				
	c	Channel 1 + 2		Receive Frequency Channel 2 [MHz]:	314,989986	si	Spur mixed with 1x LO cannot be eliminated by changing the injection ide, thus the crystal frequency must be shifted by 9,332 kHz	Spur mixed with 1xLO can eliminated by changing thei side, thus the crystal frequenc shifted by 2,222 kHz	not be njection sy must be
	¢	Channel 1 + 2 + 3		Receive Frequency Channel 3 [MHz]:	319,999997			Spur mixed with 1xLO can eliminated by changing thei side, thus the crystal frequenc shifted by 2,344 kHz	not be njection ;y must be
				Double Conver (10.7 MHz/274 I	sion 🖵— Single Co (Hz) 🚺— (274 kHz)	nversion			
				R	XRF Receive Side Band Select: = RF LO = RF - IF1 + IF1		For a proper function of J LO injection side or to us	AFC it is recommended to chan se a smaller AFC limit value.	ge the
								Nex	d>
Г	Chip Con	ntrol			1		Status		
	SIB2::LN Refresh Crystal (NZS0379::GRZ00002	Close	hoose slightly different rystal frequency	Read FIFO	Use Burst Mode Updated Write Registers	>>SFR_NPWR 0x00BC== 0x00 >>SFR_SPWR 0x00BC== 0x00 >>SFR_SPWR 0x00BC== 0x00 >>SFR_RSSIPMF 0x00BC== 0x00 >>SFR_RSSIRX 0x00BAC== 0x00		• •

Figure 9: Wizard Page 2 - RF PLL

This Wizard-tab allows you to configure:

- RF PLL channels
- Conversion Mode and LO injection side

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

Dependencies

This page does not have direct dependencies from other pages - excepting the visibility of channels (the operating mode selection has impact on the number of active channels).

The calculation of the polling period on Wizard Page 9 - Polling Timer Unit is depending on number of active channels and is also depending on the selected self polling mode.



Calculations

This page allows you to configure the SD-PLL just by entering the desired frequency in one of the textboxes for up-to three channels. The results are displayed on the "Registers" tab at the corresponding registers. Consider that all active channels must be set to a frequency within the same frequency band. If this is not the case, the application will indicate it with the "*Out of band*" LED.

Switching the sideband or conversion selection also initiates a recalculation of the RF settings.

The input frequency is compared to the selected sideband and a warning message will be displayed next to the frequency input textbox if the optimal sideband is not chosen.

Certain EMI frequencies can have negative influence to sensitivity. So there are additional input fields for entering known frequencies of your system to check their influence. A warning message gets displayed in such a case. Calculation formulas for this case are given in the "Register Value Calculation" Addendum to the Data sheet.

The warning message "For a proper function of AFC it is recommended to change the LO injection side or to use a smaller AFC limit value." appears in case the AFC would possibly need to change the Integer value of the LO multiplication factor. Therefore the warning gives possible solutions for this case.

Interactivity

Some input fields for the frequency are hidden if they are not needed in the actual configuration. If you enter an input frequency, the band selection is set automatically, but only when all active channels are set to a valid frequency within the same frequency band. If you change the actual frequency band selection and the active channels are not located within the new band, the frequency of all channels is set to the default value of the new frequency band.

Differences for the TDA5225

There are no differences to the TDA5240 Explorer.

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B). A channel selection is not shown because there is only one receive channel available.



3.2.3 Crystal Oscillator

Explorer				• X
SIB2 R	egister			
Q Wizar	d Registers Explore About			
> 22	> Subgroup Selection 3 Crystal Oscillator and System Clock	A - C	onfiguration Selection	n
Ê				
BL	XTAL Calibration:			
ggi	Calibration [pF]: Calibration:			
Ľ	16 ÷ 62.5 fF			
	125 fF			
	J0001F			
	Lable High Precision Mode during SLEEP Mode			
Г	External Clock Generation Unit			
	I Finable external clock generation unit			
	Crystal Oscillator Frequency [MHz]: 21,948717			
	Clock Divider: 11			
	· Constant suction finites factor 2			
	+ Constant System division factor: 2			
	Resulting CLKOUT-Frequency [kHz]: 997,669			
	,			
			Next	->
	and the second se			
SIB2::	LNZS0379::GRZ00002			<u>^</u>
Refre	sh Open Close >>SFR_NPWR 0x00BD<== 0x00 sh Open Close >>SFR_SPWR 0x00BD<== 0x00			
Crysta	al Oscillator [MHz]: 21 948717 Choose slightly different Read Registers Write Registers >>SFR_RSSIPMF 0x00BB<== 0x00	0		
	Crystal frequency			•
	Figure 10: Wizard Page 3 - Crystal Oscillator			

This Wizard-tab allows you to configure:

- XTAL Calibration / Trimming for fine trimming the crystal frequency
- External Clock Generation

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

Dependencies

This page does not have dependencies from other pages.

Calculations

The CLKOUT-frequency is calculated from the crystal oscillator frequency and the given clock divider factor. The resulting frequency is displayed for informational purposes only. The crystal oscillator frequency can be altered slightly in the chip control section (1).



By activating the check-box 'Choose slightly different Crystal frequency' the crystal oscillator input field turns to writable. You are allowed to enter values within a range of +/- 10 kHz compared to the default crystal oscillator frequency.

Persistent variables

Beside the content of the registers affected by this page, this input will be stored additionally in the configuration file:

• XTAL: The crystal oscillator frequency (default is 21948717 Hz).

Differences for the TDA5225

There are no differences to the TDA5240 Explorer.

Differences for the TDA5235

There are no differences to the TDA5240 Explorer.



3.2.4 RF IF Frontend

1	xplorer 🖂 🗖 🖉
S	B2 Register
4	Wizard Registers Explore About
A52	< > Subgroup Selection 4 RF IF Frontend Configuration Selection
ging TD	RF-FE & IF-Attenuation Config. A Config. C Config. D Switch off RF-path IF-Attenuation: 5.6 dB
Log	RSSI Filter Control C
	Next ->
	Chip Control Status
	SIB2::LNZS0379:GRZ00002 Image: Constraint of the second
	Crystal Oscillator [MHz]: 21,948717 Choose slightly different Crystal frequency Crys

Figure 11: Wizard Page 4 - RF IF Frontend

This Wizard-tab allows you to configure:

- RF/IF Front End
- RSSI

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

Dependencies

This page does not have dependencies from other pages - excepting the single/double conversion selection of Wizard Page 2 - RF PLL that changes the available options for the IF attenuation setting. If you change the conversion type you may have to adjust the IF attenuation manually afterwards.



Interactivity

The IF buffer can be set independently from the number of desired IF filters. The tool gives a proposal for enabling or disabling the IF filter, when selecting the number of IF filters.

Differences for the TDA5225

There are no differences to the TDA5240 Explorer.

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B).



3.2.5 Digital Receiving Unit

SIB2 Register Wizard Registers Explore About Image: Subgroup Selection 5 Digital Receiving Unit Image: Config. A Image: Config. A
Wizard Registers Explore About < > Subgroup Selection 5 Digital Receiving Unit Config. A Config. A
Image: Subgroup Selection 5 Digital Receiving Unit Image: Configuration Selection Image: Configuration Selection
Config. A
Delog: Delog: <th< th=""></th<>
AFC Start Config. OFF RSSI Slope Compensation: AFC Start Config. OFF Decay (Down) Time Ibit. 127
Auto Configure Filters Raw DATA Slicer.
Band Pass Filter Bandwidth (analog BW): Predemodulation Bandwidth (digital BW/): Settling Time [bits]: 15 ▲ BW selection: 1/32 ▼ BW selection: 1/32 ♥ BW se
Jub KHZ Z82 KHZ Image: Constraint of the second of th
Signal and Noise Detector Settings (Signal Recognition)
Please also refer to appropriate Application Note
Signal detection (=Squelch) only
C Noise detection only
C Signal and noise detection simultaneously SIGDETLO Level: SIGDETLO range sel. fac.: Peak Detector Slew Rate:
C Signal and noise detection simultaneously + SIGDETLO
Source of SPWR Readout Register: SIGDET 0/1
Chip Control
Bitezh Chara
Crystal Oscillator [MHz]: 21,948717 Covetal frequency:

Figure 12: Wizard Page 5 - Digital Receiving Unit

This Wizard-tab allows you to configure:

- Datarate
- Resulting FSK/ASK Settings
- Filter Settings
- RSSI Slope and Offset Compensation
- Peak Memory Filter (PMF)
- RAW Data Slicer (DATA output)
- Digital Receiver functions
- Signal Recognition Thresholds (Signal Detector, FSK Noise Detector)

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.



Dependencies

The Wizard Page 10 - AGC AFC depends on the Wizard Page 5 - Digital Receiving Unit.

Most calculations on this page and enabling/disabling of some controls depend on the selected modulation type on page Wizard Page 1 - Master Control Unit.

Calculations

By entering a value in the data-rate field the recalculation of all related registers is initiated. A new value becomes valid when you enter the data-rate and press the return key afterwards, when you change the data-rate by pressing the up or down button, or if you entered the data-rate and the input field looses the focus. The calculation is not done during entering number in the data-rate field.

Input variables for the data-rate calculation are:

- The data-rate input field
- The chips-per-bit switch
- The modulation type setting
- Analog and digital filter settings
- External processing selection (DATA (matched filter) output mode)

Changing one of the input variables for the data-rate calculation will also force a recalculation.

The automatic calculation of the best fitting digital filter bandwidth is done by default. If you want to select the digital filter bandwidth manually you have to uncheck the "Auto Configure Filters" checkbox.

The settings of the RSSI slope and RSSI offset compensation are translated to the corresponding register values.

Calculating the peak memory filter is supported in two directions. You can either enter the desired attack and decay time in dimensions of bit or you can select the attack and decay factor. When auto configuring is enabled, entering a time will configure the proper factor in respect of the actual data-rate. The best factor will be chosen although the entered time may not fit the calculated factor ideally. Only the value for the attack and decay factor is saved and not the value of the attack and decay time. Therefore whenever this wizard page is opened again, the values for the attack and decay time will be back calculated. This may cause slightly different time values than you have entered before.

Interactivity

The input fields for the configuration of the signal and noise detector will be enabled or disabled in dependency of the selected signal and noise detector mode. Settings not needed for configuring the selected mode will be disabled and are not accessible.

The raw data slicer group-box is displayed only if at least one of the port pins is set to the output signal "DATA".

The anti-aliasing-filter can be configured only if automatic filter configuration is disabled and the anti-aliasing filter is not bypassed for the RSSI pin.



If the actual filter and data-rate setting does not follow the Carson bandwidth rule, an alert message box pops up.

Persistent variables

Beside the content of the registers affected by this page, these inputs will be stored additionally in the configuration file:

- CHIPSPERBIT: Chips per bit selection below the data-rate input field (default is 2 chip/bit)
- AUTOCONF: Activation of auto-filter-configuration (default is activated)
- FDEV: Expected max. FSK deviation (default is +/- 64 kHz)
- FDEVMIN: Expected min. FSK deviation (default is +/- 10 kHz)
- DATARATE: Data-rate input (default is 2000 bit/s)
- Wizard_4_Digital_Receiving_UnitAUTOCONF: Automatic configuration of filters in the analog and digital frontend (default is enabled)
- Wizard_5_RF_IF_FrontendAUTOCONF: Automatic configuration of peak memory filter attack and decay time (default is enabled)
- AUTOCONF_SLICER: Automatic configuration of the RAW data slicer (default is enabled)
- STIME: Settling time of RAW data slicer (default is 15 bit)

Differences for the TDA5225

For the TDA5225 Explorer the signal and noise detector settings are not available. The AFC start configuration cannot be set to 'Start on signal recognition event'. No decoder can be configured for the TDA5225. The digital receiver calculations differ from the calculations used by the TDA5240 Explorer.

On selecting minimal jitter option for DATA output on wizard page 1, an oversampling of the datarate can be activated for the internal data processing (virtually higher datarate). Please use the information given in the tooltip for this input field.



🐴 Ex	👎 Explorer					
SIB	SIB2 Register					
ស្ត	Wizard Registers Explore About					
452	< > Subgroup Selection 5 Digital Receiving Unit	▼ ○		A _ Configuration Selection		
Ê	Config. A					
Logging	Enter Datarate [Bits/s]: 2000 1 Chip/Bit Oversampling Factor: Band Pass Filter Bandwidth (analog BW): 300 kHz AFC Start Config: Predemodulation Bandwidth (digital BW): 282 kHz Anti Aliasing Filter: 40 kHz W Bypass AAF for RSSI pin	DELOG-RSSI (config-inde RSSI Offset Compensation: RSSI Slope Compensation: I RSSI Slope Compensation: Auto Configure Settling Time (bits): I5	BW selection: 1/32 T BW selection: 1/32 T BW sel. scaling: 1/4 T	Peak Memory Filter: Image: Attack Configure Filter Attack (Up) Time [bit]: Attack Factor: 2.5 Decay (Down) Time [bit]: 3.7 • Decay (Down) Time [bit]: 3.7 • Decay (Down) Time [bit]: 1.7 • Decay Factor: 2.4 Imit PMF at EOM		
	Chip Control		Status			
SIB2::LNZS0268::GRZ20245 Generation Consester State Crystal Oscillator [MHz]: 21:948717 Choose slightly different Crystal frequency Crystal Oscillator [MHz]: Choose slightly different Crystal frequency Crystal Oscillator [MHz]: Choose slightly different Crystal frequency Crystal frequency						

Figure 13: Wizard Page 5 - Digital Receiving Unit (TDA5225 – Oversampling for minimal jitter at DATA output signal)

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B).



3.2.6 Clock Data Recovery

Exp	olorer					×
SIB2	Register					
>	Wizard Registers Explore	1			_	_
5 [< > Subaroup Selection 6.0	lock Data Recovery			A - Configuration Selection	
5 L		-1				
-	Config. A Config B Config	. C Config. D			F	- 1
Ĩ					Easy (=default) C Advanced	
ñ	Select predefined CDR setting: -	P Loop Configuration:	I Loop Configuration:	Zero Tube/Slicer Settings:		
1	 Fast (=default) 	4/16 bit	2/16 bit	Peak-Detector slew rate:		
	C Normal	Value:	Value:	up = 1/32; down = 1/256		
	C Slow	1/2 -	1/64 💌			
		PDF inner tolerance range:	Loon Filter Saturation:	Slicer Configuration:		
		Disabled Enabled	2/16 bit 👻	Chip Mode EOM-CV (=defa ▼		
		PDE outer tolerance range:	Correlator output value:			
		Disabled				
	CDR Runin & Dutycycle:			1		
	RUNIN Length:	~				
	6 chips 💌					
	Chip Border Low Level:	Chip Border High Level:	Enable Data Rate Acceptance			
	4	1	Data Rate Acceptance Threshold:			
	Bit Border Low Level:	Bit Border High Level:	Positive: Negative:			
	6	3	30 35			
	Maximum length of code violati	on				
	within datapacket <1bit - 11bit>	1				
	Timing Violation Window Length	1:0x 28				
				1		
					Next>	
_						
	hip Control			Status		
	SIBZ::LNZS03/9::GRZ00002		Read FIFO Use Burst Mode	>>23 registers read >>SFR_NPWR 0x00BD<== 0x00		
	Refresh Open C	ose	Updated	>>SFR_SPWR 0x00BC<== 0x00 >>SFR_RSSIPMF 0x00BB<== 0x00		
1	Prystal Oscillator [MHz]: 21 949717	Choose slightly different	while negisters	>>SFR_RSSIRX 0x00BA<== 0x00		

Figure 14: Wizard Page 6 - Clock Data Recovery

This Wizard-tab allows you to configure:

- P Loop configuration
- I Loop Configuration
- CDR Runin & Dutycycle / Data rate acceptance
- Maximum number of code violations
- Zero Tube / Slicer

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.



Dependencies

This page does not have dependencies from other pages - excepting the TSI settings of Wizard Page 7 - Frame Synchronization Unit that influences the result of the timing violation window length register.

Calculations

The time violation window length register value will be calculated according to the formula in the official datasheet. Inputs of the calculation are the TSI mode (existence of a gap), the user input for the maximum length of a code violation within a data-packet and the number of equal bits (code violations) at the end of the TSI pattern.

Interactivity

For this page predefined 'easy' settings exist that cover most of all common protocol scenarios, so the complexity of the CDR configuration is broken down to three possible settings (2). This 'easy' mode is the recommended default mode for this unit. If you want to configure the CDR manually the page mode can be changed from easy to advanced (1).

The two extremes are:

- Fast: For high data-rate and duty-cycle variations; long gaps within the protocol
- Slow: For high accuracy in data-rate and duty-cycle; at least 6 bit run-in required

Whenever you change to this page, the actual settings are compared to the presets and if one of the presets matches the option box (2) is set to this preset. This means, if you change a CDR setting manually in the registers tab or in a SPI configuration file, the corresponding preset will be detected automatically. If no preset fits the actual setting the page mode changes from easy to advanced.

Persistent variables

Beside the content of the registers affected by this page, these inputs will be stored additionally in the configuration file:

• CV: Maximum length of code violation within data-packet (default is 1 bit)

Differences for the TDA5225

This page is not available in the TDA5225 Explorer.

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B).



3.2.7 Frame Synchronization Unit

🐴 Exp	plorer					
SIB2	2 Register					
6	Q Wizard Registers Explore About					
A52	< > Subgroup Selection 7 Frame Synchronization Unit	A - Configuration Selection				
Ê	Config. A Config. B Config. C Config. D					
Bu	Name of the protocol					
ggi						
2	16 bit 1 SI Mode 8 Bit Parallel TSI Mode 8 Bit Extended TSI Mode 8 Bit TSI Gap Mode	End Of Message Control:				
		EOM by Code Violation				
	TSI Length <1 to 32 chips>: 32	EOM by Sync Loss				
		EOM by Data Length				
	Wildcards for correlator A at					
	the end of TSIA (chips units): 10000					
	Enter TSI biohase					
	encoded data pattern: U000000000000000000000000000000000000					
	Data Length Limit <1 to 256 hits>: 256					
		Code Phase Readjustment in				
		Disabled Enabled				
		(=delauit) 🗸				
		TSI Gap Resync Mode:				
	Disabled (=default)					
	RSSI Detector Start-up Delay: Ju					
		Next>				
=	Chin Control					
	SIB2::LNZS0379::GRZ00002 SIB2::LNZS0379::GRZ000002 SIB2::LNZS0379::GRZ00002 SIB2::LNZS0379::GRZ000002 SIB2::LNZS0379::GRZ000002 SIB2::LNZS0379::GRZ00002 SIB2::LNZS0379::GRZ00002 SIB2::LNZS0379::GRZ00002 SIB2::LNZS0379::LNZS0379::LNZS0379::LNZS0379700002 SIB2::LNZS037970000000000000000000000000000000000	*				
	Refresh Open Close Ope					
	Crystal Oscillator [MHz]: 21.948717 Choose slightly different Crystal Oscillator [MHz]: 21.948717 Costal frequency					

Figure 15: Wizard Page 7 - Frame Synchronization Unit

This Wizard-tab allows you to configure the TSI modes:

- 16 Bit TSI Mode
- 8 Bit Parallel TSI Mode
- 8 Bit Extended TSI Mode
- 8 Bit TSI Gap Mode

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

Dependencies

This page does not have dependencies from other pages.



Calculations

For the 8 Bit TSI Gap Mode the value of the gap-time register will be calculated from the entered time in units of bit. The register can be configured manually by checking the override manually checkbox.

Interactivity

The active TSI mode can be selected by switching to a tab page. The selected tab page defines the active TSI mode. The patterns for the different TSI modes are stored separately during runtime. Only data of the active TSI mode is saved in the configuration file (see Registers tab). That means that you can configure a TSI mode and then change pattern of another TSI mode without touching the configuration of the previous TSI mode, even if the same register has been modified. The configuration of a TSI mode page will be reloaded when you switch to the page. If actually no configuration was done for the TSI mode page you selected (so the page was never selected before), the default register values will be used to fill the input controls. The output field Pattern (A/B) summarizes the entered TSI configuration and displays the expected TSI pattern.

Persistent variables

Beside the content of the registers affected by this page, these inputs will be stored additionally in the configuration file:

- PROTOCOL_NAME: Name of the protocol input field (default is empty)
- PATTERN16: 16 bit TSI mode pattern
- PATTERNA1: 8 bit parallel TSI mode pattern A
- PATTERNB1: 8 bit parallel TSI mode pattern B
- PATTERNA2: 8 bit TSI gap mode pattern A
- PATTERNB2: 8 bit TSI gap mode pattern B
- PATTERNA3: 8 bit extended TSI mode pattern A
- PATTERNB3: 8 bit extended TSI mode pattern B
- GAPTIME: Transmitted gap time input field for TSI gap mode (default is zero)
- TSIGAPOVERRIDE: Override checkbox to enabled TSI gap register values manually (default is unchecked)
- TSILENA: TSI length for TSIA
- TSILENB: TSI length for TSIA
- WCA: Wildcards at the end of TSIA
- DLLIMIT: Payload Data Length Limit for TSIA
- DLLIMITB: Payload Data Length Limit for TSIB

The TSI patterns are stored as persistent variables to allow comfortable entering of different TSI modes for testing purpose during run-time of the software. Patterns are stored independently of the entered TSI length. It is allowed to enter different patterns for different TSI modes, but only the pattern information for the active TSI mode will be store to a configuration file. The TSI pattern for the active TSI mode is reflected in the register settings. On a change of the TSI mode the affected registers are set to the new values. If no pattern information was found in the loaded



configuration file, the default value for the TSI pattern will be set using the TSI pattern register content.

Differences for the TDA5225

This page is not available in the TDA5225 Explorer.

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B).



3.2.8 Message ID

Explorer	👔 Explorer				
SIB2 Register					
Wizard Registers Explore	Q Wizard Registers Explore About				
Subgroup Selection	on 8 Message ID 🗨 🔵	A - Configuration Selection			
Config. A Config. B	Config. C Config. D				
2					
Enable Message ID S	creening ID Scan Start Position: 0				
2-Byte Organized Me	ssage ID 4-Byte Organized Message ID				
Message ID Number	Message 1 (0+1) 0x 0				
 I Byte to scan 	Message 2 (2+3) OX 0				
C 2 Bytes to scan	Message 3 (4+5) OX 0				
	Message 4 (6+7) 0x 0				
	Message 5 (8+9) Ox 0				
	Message 6 (10+11) Ox 0				
	Message 7 (12+13) Ox 0				
	Message 8 (14+15) Ox 0				
	Message 9 (16+17) Ox 0				
	Message 10 (18+19) Ox 0				
		Next ->			
Chip Control		Status			
SIB2::LNZS0379::GRZ00002	Read FIFO	>>23 registers read			
Crystal Oscillator [MHz]: 21,	948717 Choose slightly different Read Registers Write Registers Write Registers	>>>Fr_SFIPME to:0002C== 0x00			

Figure 16: Wizard Page 8 - Message ID

This Wizard-tab allows you to configure:

• Message IDs with different Byte Organization modes

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

Dependencies

This page does not have dependencies from other pages.

Differences for the TDA5225

This page is not available in the TDA5225 Explorer.

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B).



3.2.9 Polling Timer Unit

Ex	plorer					
SIB	SIB2 Register					
4	Wizard Registers Explore About					
A52	< > Subgroup Selection 9 Polling Timer Unit	A Configuration Selection				
Logging TD.	Self Polling Mode Selection Constant On/Off C Fast Fall Back to Sleep C Mixed Mode C Permanent WU Search Active/Idle Lidle Periods:					
	Wake Up Detection - Config. A Config. B Config. C Config. D	Timing (config. specific)				
	Wake Up Criterion: Wake Up Count: Pattern Mode Wake Up Pattern: Pattern Detection (Data Criterion Image: Channel Image: Channel 2 Channel 3 Image: Chann	Sync. search timeout [Bits]: Timeout SYNC [ms]: [7,7500 [7] [7] [380,6983 Timeout TSI [ms]: [7] [6] Channel 1 / Channel 1 [7] [7] [8] [7] [7] [7] [8] [7] [7] [7] [7] [7] [8] [7] [7] [7] [7] [7] [8] [7] [7] [7] [8] [7] [7] [7] [8] [7] [7] [7] [7] [7] [8] [7] [8] [7] [9] [7] [9] [7] [9] [7] [9] [7] [9] [7] [9] [7] [9] [7] [9] [7] [9] [7]				
	Timing Startup Time [ms]: Time Base (TRT=1/#RT) [ms]: On Time (Cfg. A) [ms]: [0.0029 [0.0029 On Time (Cfg. B) [ms]: [0.0029 [0.0029 On Time (Cfg. B) [ms]: [0.0029 Off Time [ms]: On Time (Cfg. C) [ms]: [0.0029 [0.0029 On Time (Cfg. C) [ms]: [0.0029 [0.0029 On Time (Cfg. D) [ms]: [0.0029	Continue with Self Polling Mode after EOM detected in Run Mode Self Polling: Disabled ── ■ Enabled Continue with next Config. in Self Polling Mode after EOM detected in Run Mode Self Polling: Conf. A □ ── Next Conf. A □ ── Next Conf. A □ ── Next				
	L	Next ->				
	Chip Control					
	SIB2::::GRZ10004 Read FIF0 Use Burst Mode	*				
	Open Close Updated Crystal Oscillator [MHz]: 21.948717 Choose slightly different Read Registers Write Registers	Ŧ				

Figure 17: Wizard Page 9 - Polling Timer Unit

This Wizard-tab allows you to configure:

- Self Polling Mode
- Wake up detection
- Timing adjustments for autonomous chip operation mode

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

Dependencies

The number of selected RF channels per configuration has influence to the calculated polling period.

The value for register SYSRCTO is calculated from the selected number of RUNIN chips from Wizard page 6 – Clock Data Recovery.



Calculations

This page integrates calculations for the polling timer unit, the register values for the wake-up level observation time, the Sync Search Time-out and the time-out timers.

The input field of the timing group allows you to configure the on/off-timing, whereas these timer values are multiple of the reference timer. If the reference timer changes, the values for the on-time are set to the next higher time that fits and the value for the off-time is set to the next lower time that fits. The resulting polling period field shows the time $T_{MasterPeriod}$ which is calculated as described in the figures of the Polling Timer Unit chapter of the official datasheet.

Interactivity

This page stays disabled until you select the operating mode Self Polling on Wizard Page 1 - Master Control Unit.

The on-time input fields are displayed in dependency of the active configurations and the selected self polling mode.

The available input field of the wake-up detection group depends on the selection of the wake-up criterion and if a data criterion is selected also on the activation of ultra-fast fallback to sleep.

Differences for the TDA5225

No change of the self polling mode and no selection on different wake-up criteria is possible with the TDA5225 Explorer. Also no Sync Search Time-out and time-out timers are available for the TDA5225 Explorer.

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B). There is only one channel available in the wake-up selection section.



3.2.10 AGC AFC

<u>а</u> Б	xplorer		
SIE	B2 Register		
9	Wizard Registers Explore About		
524	< > Subgroup Selection 10 AGC AFC	▼ ()	A V Configuration Selection
AD			
F	Contig. A		1
ing			
660	AFC (Automatic Frequency Control): AFC Offset Readout:	AGC (Automatic Gain Control): Start Configuration:	AFC/AGC Freeze Delay
Ľ	0 Settling time: Faet	OFF _	Counter Division Ratio:
	Start Configuration:	Freeze Configuration: Enable Restart at Channel	U
	Direct ON	Stay ON	
	Freeze Configuration: Config. Specific Settings:	Digital RSSI Gain Correction: Threshold Offset	
		15.5 dB 🚽 63.9 dB	
	Freq. Offset Saturation Limit:	Gain Control: MIX2 / IF2 Gain Readout:	
	42,87 kHz	Automatic 🚽 0 dB 🚽 0 dB 💌	
		Threshold Hysteresis: Threshold Low:	-
	Enable AFC blocking Enable Restart at Channel	J21.3 0B [0 Threshold Lin:	
	ASK signal Mode	0	-
	LO injection side or to use a smaller AFC limit value.		
		Press the 'Write Register	s' button to download your configuration!
			Mout->
			IN EXC +>
Г	Chip Control	Status	
	SIB2::LNZSU268::GRZ20030 Read	FIFO IM Use Burst Mode >>Register download ==> OK (1 re >>Starting burst mode register dow	gisters written)
	Refresh Open Close Read Re	Opdated >>Register download ==> OK (27 r Write Registers) >>Starting burst mode register download ==> OK (27 r	registers written) 🗉
	Crystal Oscillator [MHz]: 21,948717 Choose slightly different Crystal frequency	>>Device SIB2::LNZS0268::GRZ2	20030/TDA5240 initialized

Figure 18: Wizard Page 10 - AGC AFC

This Wizard-tab allows you to configure:

- AFC (Automatic Frequency Control) Settings
- AGC (Automatic Gain Control) Settings

For information beyond the quick help / tooltip (moving the mouse pointer on a selected item) refer to the official datasheet.

This page is the last page of the wizard. If this page is reached the configuration is ready to be written to the chip. This can be done by pressing the "Write Registers" button in the chip control area.

Dependencies

The data-rate setting of Wizard Page 5 - Digital Receiving Unit is used for the calculation of the AFC filter coefficients.



Calculations

If the auto-configuration of the AFC filters is activated you can configure the AFC filter coefficients by choosing one of the predefined settling time values.

The warning message "For a proper function of AFC it is recommended to change the LO injection side or to use a smaller AFC limit value." appears in case the AFC would possibly need to change the Integer value of the LO multiplication factor. Therefore the warning gives possible solutions for this case.

Interactivity

Changes of the AFC/AGC settings can be done only if the AFC/AGC unit is not switched off.

Persistent variables

Beside the content of the registers affected by this page, these inputs will be stored additionally in the configuration file:

- AUTOCONF: Automatic configuration of AFC filter setting enable (default is enabled)
- ST: AFC filter settling time (default is fast)

Differences for the TDA5225

The AFC and AGC start configuration cannot be set to 'Start on signal recognition event'. The AFC and AGC freeze modes 'Freeze on Signal Recognition Event' and 'Freeze on Symbol Synchronization' are not available for the TDA5225.

Differences for the TDA5235

The TDA5235 Explorer supports only 2 configurations (A and B).



3.3 Explore

The Explore tab integrates basic functionality for interactive chip control. In contrast to the Wizard pages a reasonable usage of the Explore page is possible with connected evaluation hardware only.

3.3.1 Status

Explorer	
SIB2 Register	
Q Wizard Registers Explore About	1
Subgroup Selection Status	A Configuration Selection
Power Readout Statistics General Chip Info Direct Register Control External Processing: ACC AFCOFFSET RSSIPMF RSSIPMF SPV/R SPV/R Average: 0 0 0 NPV/R Std Dev.: 0 0 0 Run AccOFFSET Read 500 \checkmark x AGC Run Automatic NINT detection and further payload processing: Received packets (max. 512): Off Off On Image: Control Image: Control Image: Control Image: Control Run Accomatic NINT detection and further payload Control Image: Control Image: Control Image: Control Off On Control Image: Control Image: Control Image: Control Image: Control Received packets Control Image: Contro Image: Control Image:	Readout ADC Result: ADC Input Selection: • RSSI • Temperature • VDDD / 2 • End of Conversion detected Signal Power: 0/1 100 200 0 - 100 200 • End of Conversion detected Signal Power: 0/1 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 200 0 - 100 - 0 - 0 - 0 <
SIB2::LNZ50379::GRZ00002 Read FIFO Use Burst Mode Refresh Open Close Crystal Oscillator [MHz]: 21,948717 Choose slightly different	s service read galaxies written) glater download ==> OK (1 registers written) ting burst mode register download glater download ==> OK (27 registers written) ting burst mode register download ♥

Figure 19: Explore Page - Status

This Wizard-tab shows readout values of:

- ADC Result
- FSK Noise Power
- Signal Power
- Payload Peak Detector
- Peak Detector
- Serial number, SPI checksum, address and data tracer (General Chip Info)



Following functions can be triggered on this page:

- AFC/AGC Manual Freeze
- Force End of Message (EOM) and Time out Timer (TOTIM)

Readout

The controls are updated on each press of the "Read Registers" button in the chip control area. Reading registers is possible with connected and opened evaluation hardware only. You can perform a continuous readout of the registers shown within the Readout group-box by checking the box "Continuous readout". Continuous readout is stopped by uncheck the box or when the interface board connection has been closed.

Power Readout Statistics

This section provides statistical information on different selectable signal sources (e.g. Signal and Noise Power SPWR, NPWR). All registers check marked in the list on the left side will be read.

By pressing the "Read" button the selected count of readings of the selected power readout registers are done and the average and standard deviation of the results are displayed (readout may take some time!). This can be used for evaluation of threshold values. For further information about using those results to configure the signal and noise detector refer official datasheet or refer to the application note for signal and noise detector threshold settings.

Direct Register Control

In this area registers can be directly addressed. You can either read or write a single register, or you can enter a sequence of registers that should be written in one run.

To verify the success of a single register write operation change to the general chip info tab and press the "Read Registers" button in the Chip Control section. The address and data tracer registers will display the recently written address and value.

Sequences for batch write operations consist of one or more lines of a register name followed by the register value and delimited by a colon (<address:value>). The result of a batch write operation is shown in the SIB status box.

A direct register write access does also an update of the register grid in the Registers tab and this in succession initiates an update of all affected controls in the configuration interface.

Note: Manual changes in the register list are allowed in principle, but not subject of input validation, therefore an inconsistent setting might be generated!

Run Section

This group can be used to simulate a simple application case. When starting the interrupt detection, the correct NINT port pin will be configured from the actual configuration. Press the switch to turn the interrupt detection on. Whenever an interrupt is recognized by the interface board, the counter "Received interrupts" increases and a readout of the interrupt status registers is done. If at least one configuration indicates an end of message, the FIFO of the TDA5240/35 is read and the payload peak value in the corresponding textbox is updated. A successful read



FIFO operation is indicated by increasing the "Processed messages" counter. The resulting data of the read FIFO operation is displayed in textbox as HEX string ("0x") and the same data is displayed as binary string ("0b").

It is possible to compare the incoming data with a predefined payload pattern. Just enter the expected payload in the corresponding textbox in hexadecimal format and specify the number of bits of the incoming data. If a data packet has been received, it will be compared automatically and the result of the comparison is visualized by an increment of the "Correctly received payload data" counter on success. Up to 512 incoming packets can be buffered by the Explorer software. The packet history can be reviewed by selecting a packet in the received packets combo-box.

Differences for the TDA5225

Signal and noise-power readout is not possible with the TDA5225. Automatic payload processing is not available in the TDA5225 Explorer.

Differences for the TDA5235

There are no differences to the TDA5240 Explorer.



2

1

3.4 Registers Tab

🐴 Đ	kplorer	r				
SIB	32 R	Register				
9	Wizan	d Registers Explore About			\wedge	
524		Register	Address Valu	e 7 6 5 4 3 2 1 0		Register Map / SPI File Control
A		SFR_A_WUPAT0	0x018 0x00			
E		SFR_A_WUPAT1	0x019 0x00			
Bu		SFR_A_WUBCNT	0x01A 0x00		· · · · · · · · · · · · · · · · · · ·	Save Mode: Save Active
ggi		SFR_A_WURSSITH1	0x01B 0x00			Load Defaults Save Mapping File
Ĩ.		SFR_A_WURSSIBL1	0x01C 0xFF			
—		SFR_A_WURSSIBH1	0x01D 0x00			<pre><please a="" description="" enter="" setting=""></please></pre>
		SFR_A_WURSSITH2	0x01E 0x00			
		SFR_A_WURSSIBL2	0x01F 0xFF	$\mathbf{\overline{\mathbf{A}}} \mathbf{\overline{\mathbf{A}}} \mathbf{\overline{\mathbf{A}}$		-
		SFR_A_WURSSIBH2	0x020 0x00			Note: Manual changes in the register list
		SFR_A_WURSSITH3	0x021 0x00			are allowed in principle, but not subject of
		SFR_A_WURSSIBL3	0x022 0xFF	V V V V V V V		Therefore an inconsistent setting might be
		SFR_A_WURSSIBH3	0x023 0x00			generated !!!
		SFR_A_SIGDETSAT	0x024 0x42			
		SFR_A_WULOT	0x025 0x00			
		SFR_A_SYSRCTO	0x026 0x7C			
		SFR_A_TOTIM_SYNC	0x027 0xFF	V V V V V V		
		SFR_A_TOTIM_TSI	0x028 0x00			
		SFR_A_TOTIM_EOM	0x029 0x00			
		SFR_A_AFCLIMIT	0x02A 0x02			
		SFR_A_AFCAGCD	0x02B 0x00			
		SFR_A_AFCSFCFG	0x02C 0x01			
		SFR_A_AFCK1CFG0	0x02D 0x50			
		SFR_A_AFCK1CFG1	0x02E 0x00			Find register
	•	SFR_A_AFCK2CFG0	0x02F 0x50			
		SFR_A_AFCK2CFG1	0x030 0x00			lenter register name
		SER & PMELIDSE	0x031 0x42			
	Chip C	Control			Status	
	SIB2::	:LNZS0379::GRZ00002		Read FIFO Use Burst Mode	>>23 registers read	
	Refre	esh Open Close		O Updated	>>SFR_SPWR 0x00BC<== 0x00	
	Crysta	al Oscillator [MHz]: 21 948717	Choose slightly diffe	rent Read Registers Write Registers	>>SFR_RSSIRX 0x00BA<== 0x00	
			Crystal frequency		1	•

Figure 20: Registers Tab

- 1. Register view/(selection) area
- 2. Scroll bar
- 3. File Control
- 4. Find register area

3.4.1 Register Selection Area (Register Grid)

This area gives you full access to all available registers. Each marker (checkbox for a bit) can be set or deleted by clicking on it. All changes you make in the wizard will also be made in the register tab and vice versa.

Note: Manual changes in the register list are allowed in principle, but not subject of input validation, therefore an inconsistent setting might be generated!



The register grid offers you several possibilities to perform settings and access registers.

- Grid sort: Click the header of a column to sort the registers by name or address
- Leave the mouse pointer above a column of the grid to popup a tooltip containing the full name of the register
- Double-click the content of the "Value" column to enter the edit mode of the value of a register. Enter a valid hexadecimal number (in c-style format, with a leading 0x) to set the register to a new value.
- Click into the columns 0 to 7 to change a single bit of a register. The hexadecimal value field will be updated automatically.
- Whenever a register value is changed on one of the wizard pages the pointer in the register list is set to the corresponding register address. You can check the setting by switching from the wizard page to the register page after entering a value on a wizard page. If an input forces a calculation and/or more than a single register is affected, then the pointer marks the last register that was affected by the operation.

3.4.2 Scroll Bar

The register set is very large, scroll up and down in normal Microsoft Windows behavior.

3.4.3 File Control

Saving and loading of register sets can be done here. You have several options by selecting the drop down menu:

Save Active	All differences between the active configurations (A, B, C, D) of the setting and the reset values of the chip are saved. Only patched registers of the active configurations will be saved. When reloading a configuration that has been save using this mode the patched registers for the inactive configurations are merged with the loaded registers.
	Note: When using the operating mode run-mode slave only the actual active configuration will be saved. If more than one configuration is used, it is recommended to use the save modes "Save Difference" or "Save All" to preserve all settings.
Save Difference	All differences between the actual setting and the reset values of the chip are saved. It will not be considered whether a configuration is active or not active in this setting. This method includes all patched registers as listed in the appendix.
Save All	All registers displayed in the register list are saved.
Save configuration page (_A_, _B_, _C_, _D_)	All registers of a specific configuration are saved, even if they are not touched by the actual setting. This mode can't be used to retrieve an operational SPI configuration.



Regardless of the save mode selection the chip mode control register is written as first (sleep mode) and as last write command of the output file.

A short description for the configuration can be entered in the textbox below the file selection box.

To open a configuration from a file press the left button, to save a configuration to a file press the right button. In the appearing open or save file dialog box the path and name of the target file can be selected.

Choose the desired type of file using the "Files of type" or the "Save as type" dropdown box. Enter a filename or select a file in the pane above to open or save a configuration.

It is allowed to open configuration files created for other product versions. The TDA5240 Explorer is capable of loading TDA5235 and TDA5225 configurations. The TDA5225 and TDA5235 Explorer variants can load other configuration files, but if a register is set in a configuration that is not available in another Explorer variant, this register will be ignored and a warning message informs about this. It is recommended to review the settings when loading a configuration build for a different product.

These types of configuration files are supported:

- _spi.def Standard TDA5240/35/25 configuration file format: This is the default output of the TDA5240/35/25. The register settings are saved using an address-independent format. A sample SPI configuration file can be found in the appendix. The output does not generate page switches explicitly - a page switch is implicitly coded by using register names. The Explorer software generates page switches automatically when downloading. If the SPI configuration is used in custom software you have to ensure the correct insertion of page switches.
- .txt Configuration Address Data: Write commands and addresses are converted to the corresponding hexadecimal values. Whenever a page switch is necessary the write command including the new page value for the switch are inserted.
- C-Header File:

Generates a two-dimensional constant field, containing pairs of register-names and values. Using an appropriate SFR header file is necessary to define the register addresses. The Explorer can generate this header file automatically (press the "*Save Mapping File*" button on the Registers page). The generated file contains meta-information needed by the Explorer to read back the settings.





Figure 21: Types of Configuration Files



3.4.4 Find Register Area



Figure 22: Find Register Area

If a name of a register is filled in the textbox (6) a marker will be set at the position of the register (5). The marker position is always updated when registers are modified. So it is easy to find the register that belongs to a setting on the Wizard pages by change the setting and switch to the Registers tab afterwards. When the last operation was a calculation the marker points to the last register that was modified by this calculation.



4 Logging

E	Texplorer						
SI	SIB2 Register						
육	😝 🗑 🕞 📬 🗙 Clear Messages 📳 Pause Scrolling 🍙 Stop						
52	E- 🎲 NextGen Repository - ALL	Time	Logger	Message	A		
ð		09:48:46,8475	Meter_Controller	SFR_ADCRESH 0x00AE<== 0x00			
F		09:48:46,8631	Meter_Controller	SFR_ADCRESL 0x00AF<== 0x00			
0		09:48:46,8787	Meter_Controller	SFR_VACRES 0x00B0<== 0x00			
<u> </u>		09:48:46,8943	Meter_Controller	SFR_AFCOFFSET 0x00B1<== 0x00			
6		09:48:46,9099	Meter_Controller	SFR_AGCGAINR 0x00B2<== 0x00			
٩ ٩		09:48:46,9255	Meter_Controller	SFR_SPIAT 0x00B3<== 0x4E			
_		09:48:46,9411	Meter_Controller	SFR_SPIDT 0x00B4<== 0x01			
		09:48:46,9567	Meter_Controller	SFR_SPICHKSUM 0x00B5<== 0x00			
		09:48:46,9879	Meter_Controller	SFR_SN0 0x00B6<== 0x63			
		09:48:47,0035	Meter_Controller	SFR_SN1 0x00B7<== 0xA9			
		09:48:47,0191	Meter_Controller	SFR_SN2 0x00B8<== 0x0D	=		
		09:48:47,0347	Meter_Controller	SFR_SN3 0x00B9<== 0x00			
		09:48:47,0503	Meter_Controller	SFR_RSSIRX 0x00BA<== 0x00			
		09:48:47,0659	Meter_Controller	SFR_RSSIPMF 0x00BB<== 0x00			
		09:48:47,0815	Meter_Controller	SFR_SPWR 0x00BC<== 0x00			
		09:48:47,0971	Meter_Controller	SFR_NPWR 0x00BD<== 0x00			
		09:48:47,0971	Meter_Controller	23 registers read	-		
	Message Details						
	Level Time		Logger				
	Thread Eventi						
	Exception	" j					
	Message				× 1		
					-		
	24 Messages received 24 Messages b	uffered			.::		
r	Chip Control			T Status			
	SIB2:1 NZS0379:GBZ00002		Read FIFO	I lee Burst Mode >>23 registers read	A		
			Hodd HI O	>>SFR_NPWR 0x00BD<== 0x00			
	Herresh Upen Close			Upualeu SSFR_SPWR 0x00BC<== 0x00 SSER_SSIPME 0x00BR<== 0x00 SSER_SSIPME 0x00BR<== 0x00 SSER_SSIPME 0x00BR<== 0x00 SSER_SSIPME 0x00BR<== 0x00 SSER_SSIPME 0x00BR<== 0x00 SSER_SSIPME 0x00BR<== 0x0BR<== 0x00BR<== 0x00BR<== 0x0BR<== 0x0BR<== 0x0BR<==			
	Crystal Oscillator [MHz]: 21,948717	Choose slightly of Crystal frequence	lifferent Read Registers	>>SFR_RSSIRX 0x00BA<== 0x00	-		
L				ц×.			

Figure 23: Logging

Logging information and warnings are displayed here. Use the context menu of the NextGen Repository item in the tree view to change the warning-level.

Infineon Technologies wishes you a successful start into the TDA5240/35/25 world of applications!



5 Appendix

5.1 Register Patch List

The Explorer configuration software is build for obtaining optimal settings for a widespread number of applications. To start from a user friendly default state of the chip, some registers are set immediately after the chip reset is done, when opening the SIB2 connection. In the default save mode these patched registers will be saved in the SPI configuration file only if they are required for the saved configuration (e.g. if configuration B is not active in the actual setting, a patched register for a register in configuration B will not be written).

If a patched register is modified during creation of a configuration and the new register value is equal to the default value of the chip, no write command for this register will be generated for the SPI configuration file. When loading a configuration from a SPI configuration file the user interface will be set to the default values of the chip. It is presumed that the SPI configuration file contains already entries for patched registers.

Register Name	Absolute Address	Value
SFR_A_AFCK1CFG0	0x02D	0x50
SFR_A_AFCK2CFG0	0x02F	0x50
SFR_B_AFCK1CFG0	0x12D	0x50
SFR_B_AFCK2CFG0	0x12F	0x50
SFR_C_AFCK1CFG0	0x22D	0x50
SFR_C_AFCK2CFG0	0x22F	0x50
SFR_D_AFCK1CFG0	0x32D	0x50
SFR_D_AFCK2CFG0	0x32F	0x50
SFR_A_CDRRI	0x048	0x02
SFR_B_CDRRI	0x148	0x02
SFR_C_CDRRI	0x248	0x02
SFR_D_CDRRI	0x348	0x02
SFR_PPCFG0	0x081	0x53
SFR_A_TSILENA	0x04E	0x01
SFR_B_TSILENA	0x14E	0x01
SFR_C_TSILENA	0x24E	0x01
SFR_D_TSILENA	0x34E	0x01
SFR_A_SYSRCTO	0x026	0x7C
SFR_B_SYSRCTO	0x126	0x7C
SFR_C_SYSRCTO	0x226	0x7C
SFR_D_SYSRCTO	0x326	0x7C



5.2 SPI Configuration File Format

The standard file format for saving and loading TDA5240/35/25 configurations has an easy-toparse format for direct usage in target applications and is formatted as plain ASCII text. The output consists of a header section and a SPI write command section. Changes of the header are not allowed if you indent to reuse the file with the Explorer software. It is allowed to add comments to the SPI write command section, but for changes of the register values it has to be considered that they are not subject of input validation and therefore an inconsistent setting might be generated.

The header section starts with the parser version information, the login name of the current user and a timestamp that shows when the configuration file has been created. The next line gives information about the software that was used to create this file and the target product this configuration file is valid for. The three placeholders (LastChangedDate/Rev/Author) are inserted for inserting information automatically when utilizing versioning tools. The text between the SPI_CONFIGURATION_METAINFO tag and the SPI_CONFIGURATION_SETTINGS tag is the setting description that has been entered when saving the SPI configuration file in the Explorer software.

All lines after the SPI_CONFIGURATION_SETTINGS tag and before the END tag are considered as persistent variables. They are composed of the Wizard page name, followed by the variable name and the configuration (A/B/C/D) the variable belongs to. After the colon as delimiter the ASCII representation of the variable value is suffixed.



//File build with nextGen V2.37, File Parser V1.0.1							
//File generated by: "username"							
//Date: 28.02.2011 18:27:02							
//Output generated by B12 Explorer (build B12.6.51) for product TDA5240							
// \$LastChangedDate\$							
// \$Rev\$	// \$Rev\$						
// \$Author\$	// \$Author\$						
// SPI_CONFIGURATION_METAINFO							
// <please a="" enter="" setting<="" th=""><th colspan="7">//<please a="" description="" enter="" setting=""></please></th></please>	// <please a="" description="" enter="" setting=""></please>						
// SPI_CONFIGURATION_SETT	INGS						
//Wizard_4_Digital_Receiv	ing_UnitC	VSPLA:1					
//Wizard_4_Digital_Receiv	ing_UnitD	ATARATEA:2000					
//Wizard_4_Digital_Receiv	ing_UnitF	DEVA:64					
//Wizard_4_Digital_Receiv	ing_UnitF	DEVMINA:10					
//Wizard_4_Digital_Receiv	ing_UnitC	HIPSPERBITA:1					
//Wizard_5_RF_IF_Frontend	AUTOCONFA	.:1					
//Wizard_4_Digital_Receiv	ing_UnitA	UTOCONFA:1					
//Wizard_4_Digital_Receiv	ing_UnitA	UTOCONF_SLICERA:1					
//Wizard_4_Digital_Receiv	ing_UnitS	TIMEA:15					
//Wizard_10_AGC_AFCFOFFSE	TMAX:10						
//Wizard_10_AGC_AFCAUTOCO	NFA:1						
//Wizard_10_AGC_AFCSTA:1							
//Wizard_10_AGC_AFCRATIOA	:10						
//Wizard_6_Clock_Data_Rec	overyCVA:	1					
//XTAL:21948717	//XTAL:21948717						
//Wizard_7_Frame_Synchron	ization_U	InitPROTOCOL_NAMEA:''					
//Wizard_7_Frame_Synchron	ization_U	nitTSILENA6A:1					
//Wizard_7_Frame_Synchron	ization_U	nitDLLIMIT1A:256					
//Wizard_7_Frame_Synchron	ization_U	nitPATTERN16A:'0'					
//SAVEMODE:'Save Active[A]'						
//END							
Write SFR_CMC0	0x00						
Write SFR_A_SIGDETSAT	0x42	//Signal Detector Saturation Threshold Register					
Write SFR_A_SYSRCTO	0x7C	//Synchronization Search Time-Out Register					
Write SFR_A_AFCSFCFG	0x01	//AFC Start/Freeze Configuration Register					
Write SFR_A_AFCK1CFG0	0x50	//AFC Integrator 1 Gain Register 0					
Write SFR_A_AFCK2CFG0	0x08	//AFC Integrator 2 Gain Register 0					
Write SFR_A_PDECF	0x10	//Pre Decimation Factor Register					
Write SFR_A_PDECSCFSK	Write SFR_A_PDECSCFSK 0x2A //Pre Decimation Scaling Register FSK Mode						
Write SFR_A_PDECSCASK	Write SFR_A_PDECSCASK 0x28 //Pre Decimation Scaling Register ASK Mode						
Write SFR_A_SRC	Write SFR_A_SRC 0x02 //Sampe Rate Converter NCO Tune						
Write SFR_A_EXTSLC	0x0B	//Externel Data Slicer Configuration					
Write SFR_A_CDRRI	0x02	//Clock and Data Recovery RUNIN Configuration Register					
Write SFR_A_TSILENA	0x01	//TSI Length Register A					
Write SFR_PPCFG0	0x53	//PP0 and PP1 Configuration Register					
Write SFR_CMC0	0x12						

Figure 24: SPI Configuration File Example