

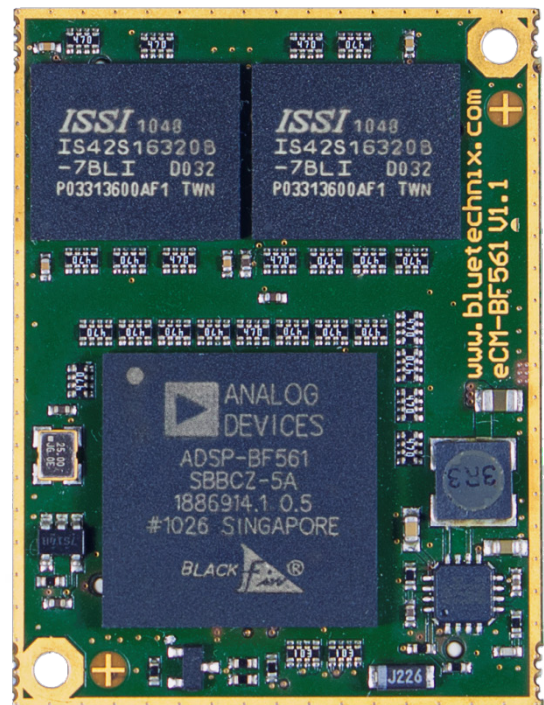
# BLUETECHNIX

## Embedding Ideas

# eCM-BF561

Hardware User Manual

Version 1.4





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#### Information

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#### Warning

Due to technical requirements components may contain dangerous substances.

## 1 Introduction

The Core Module eCM-BF561 is optimized for performance and parallel data processing. The module integrates processor, RAM, flash and power supply at a size of 44x33mm! It is based on the high performance ADSP-BF561 from Analog Devices. The eCM-BF561 is designed for industrial and commercial applications. It addresses 128MByte SDRAM via its 32bit wide SDRAM bus and has an onboard NOR-flash of 32MByte.

### 1.1 Overview

Figure 1-1 shows the main components of Core Module eCM-BF561.

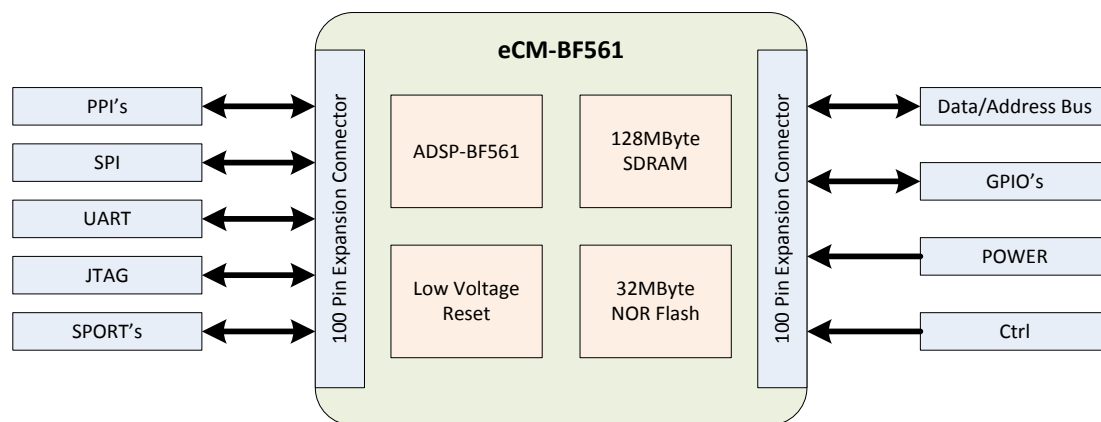


Figure 1-1: Main components of the eCM-BF561 module

- **Analog Devices Blackfin Processor BF561**
  - Industrial version (see chapter **Error! Reference source not found.**)
    - ADSP-BF561SBBCZ-5A (Rev 0.5; -40° - 85°C)
  - Commercial version (see chapter **Error! Reference source not found.**)
    - ADSP-BF561SKBCZ-6A (Rev 0.5; 0° - 70°C)
- **128 MB SDRAM**
  - Industrial version (see chapter **Error! Reference source not found.**)
    - IS42S16320B-7BL
    - SDRAM Clock up to 133MHz
    - 2x (32Mx16, 512Mbit at 3.3V)
  - Commercial version (see chapter **Error! Reference source not found.**)
    - IS42S16320B-7BL
    - SDRAM Clock up to 133MHz
    - 2x (32Mx16, 512Mbit at 3.3V)
- **32 MB of Flash**
  - PF48F4000P0ZBQE (16Mx16, 128Mbit at 3.3V; all 32MByte addressable)
  - Additional flash memory can be connected through the expansion board as parallel Flash using asynchronous chip select lines or as a SPI flash.
- **Core Voltage Regulator**



- 1.35V
- **Low Voltage Reset Circuit**
  - Module resets if power supply goes below 2.93V for at least 140ms
- **Connectors**
  - SPORT 0
  - SPORT 1
  - UART
  - SPI
  - PPI-0 (Parallel Port Interface 0)
  - PPI-1 (Parallel Port Interface 1)
  - GPIO's
  - Data Bus
  - Address Bus, Control Signals
  - nRESET
  - Boot-Mode
  - JTAG
  - Power Supply

## 1.2 Applications

- Parallel digital signal processing
- Imaging and consumer multimedia
- Set top boxes
- Automotive vision systems
- Portable media players
- Digital video camera systems
- Video conference applications

## 2 General Description

### 2.1 Functional Description

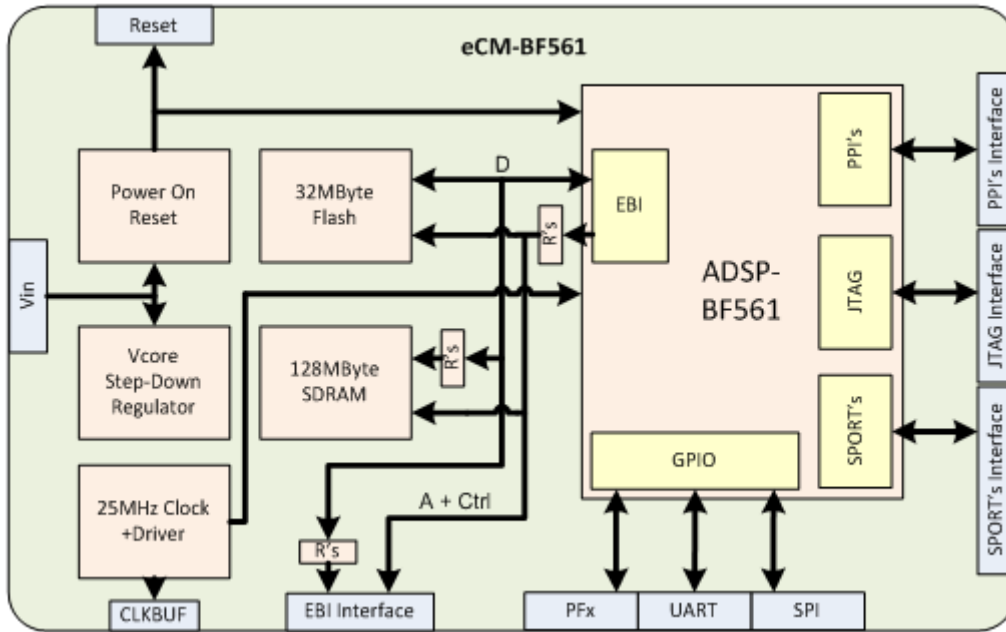


Figure 2-1: Functional Overview

### 2.2 Boot Mode

By default the Boot Mode is set to 00 (BMODE0 pin = LOW, BMODE1 pin = LOW). The boot mode pins are available on the connectors.

BMODE1-0	Description
00	Execute from 16-bit external memory (Bypass Boot ROM) (uBoot, uClinux)
01	01 Boot from 8-bit/16-bit flash (BLACKSheep® OS)
10	Boot from SPI host slave mode
11	Boot from SPI serial EEPROM (16-, 24-bit address range)

Table 2-1 Boot Mode

### 2.3 Memory Map

#### 2.3.1 Core Module Memory

Memory Type	Start Address	End Address	Size	Comment
FLASH *)	0x20000000	0x21FFFFFF	32MB	Intel PF48F4000P0ZBQE
SDRAM	0x00000000	0x07FFFFFF	128MB	32Bit Bus, 2x ISSI IS42S16320-7BL

Table 2-2: Memory Map

\*) Please be aware that you have to unlock the flash before starting an erase process!





### 2.3.2 Externally Addressable Memory (on connector)

The Blackfins External Bus Interface (EBI) allows connecting devices via an asynchronous memory interface.

AMS Line	Start Address	End Address	Max. Size
nAMS1	0x24000000	0x27FFFFFF	128MB
nAMS2	0x28000000	0x2BFFFFFF	128MB
nAMS3	0x2C000000	0x2FFFFFFF	128MB

Table 2-3: External Addressable Memory



### 3 Specifications

#### 3.1 Electrical Specifications

##### 3.1.1 Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IN}$	Input supply voltage	3.0	3.3	3.6	V
$I_{3V3 @ 25^{\circ}C}$	3.3V current	-	700	-	mA
$V_{OH}$	High level output voltage	2.4	-	-	V
$V_{OL}$	Low level output voltage	-	-	0.4	V
$I_{IH}$	IO input current	-	-	10	$\mu A$
$I_{OZ}$	Three state leakage current	-	-	10	$\mu A$
$f_{CCLK}$	Core clock frequency	100	-	600	MHz

Table 3-1: Electrical characteristics

##### 3.1.2 Maximum Ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions greater than those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input supply voltage	-0.3	4.1	V
$V_{IO}$	Input or output voltage	-0.5	3.6	V
$I_{OH} / I_{OL}$	Current per pin	0	10	mA
$T_{AMB}$	Ambient temperature	-40	85	$^{\circ}C$
$T_{STO}$	Storage temperature	-55	150	$^{\circ}C$
$\phi_{MB}$	Relative ambient humidity	-	90	%

Table 3-2: Absolute Maximum Ratings

##### 3.1.3 ESD Sensitivity



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## 4 Connector Description

### 4.1 Connector X1

Please mind the mounted pull up, pull down and serial resistors on the Core Module (see column “Type”).

Pin No.	Signal Name	Type	Function
1	PPI0D0	I/O	PPI Data
2	PPI0D1	I/O	PPI Data
3	PPI0D2	I/O	PPI Data
4	PPI0D3	I/O	PPI Data
5	PPI0D4	I/O	PPI Data
6	PPI0D5	I/O	PPI Data
7	PPI0D6	I/O	PPI Data
8	PPI0D7	I/O	PPI Data
9	PPI0SYNC3	I/O	PPI Sync
10	PPI0SYNC2/TMR9	I/O	PPI Sync
11	PPI0SYNC1/TMR8	I/O	PPI Sync
12	PPI0CLK	I	PPI Clock
13	GND	Power	
14	PPI1D0	I/O	PPI Data
15	PPI1D1	I/O	PPI Data
16	PPI1D2	I/O	PPI Data
17	PPI1D3	I/O	PPI Data
18	PPI1D4	I/O	PPI Data
19	PPI1D5	I/O	PPI Data
20	PPI1D6	I/O	PPI Data
21	PPI1D7	I/O	PPI Data
22	PPI1D8/PF32	I/O	PPI Data
23	PPI1D9/PF33	I/O	PPI Data
24	PPI1D10/PF34	I/O	PPI Data
25	PPI1D11/PF35	I/O	PPI Data
26	PPI1D12/PF36	I/O	PPI Data
27	PPI1D13/PF37	I/O	PPI Data
28	PPI1D14/PF38	I/O	PPI Data
29	PPI1D15/PF39	I/O	PPI Data
30	PPI1SYNC3	I/O	PPI Sync
31	PPI1SYNC2/TMR11	I/O	PPI Sync
32	PPI1SYNC1/TMR10	I/O	PPI Sync
33	PPI1CLK	I	PPI Clock
34	3V3	Power	
35	3V3	Power	
36	3V3	Power	
37	GND	Power	
38	GND	Power	
39	GND	Power	
40	NMI0	I – 10k pull down	Nonmaskable Interrupt Core A
41	NMI1	I – 10k pull down	Nonmaskable Interrupt Core A
42	RX/PF27	I/O	UART Receive/GPIO
43	TX/PF26	I/O	UART Transmit/GPIO
44	GND	Power	



Pin No.	Signal Name	Type	Function
45	TCK	I – 10k pull up	JTAG Clock
46	TDO	O	JTAG Data Out
47	TDI	I – 10k pull up	JTAG Data In
48	TMS	I – 10k pull up	JTAG Mode Select
49	NTRST	I – 4k7 pull down	JTAG Reset
50	NEMU	O	Emulation Out
51	PF10	I/O	GPIO
52	PF11	I/O	GPIO
53	PF12	I/O	GPIO
54	PF13	I/O	GPIO
55	PF14	I/O	GPIO
56	DT0SEC/PF17	I/O	Sport0 Transmit Data Secondary
57	DT0PRI/PF18	I/O	Sport0 Transmit Data Primary
58	TFS0/PF16	I/O	Sport0 Transmit Frame Sync
59	TSCLK0/PF29	I/O	Sport0 Transmit Serial Clock
60	DR0SEC/PF20	I/O	Sport0 Receive Data Secondary
61	DR0PRI	I	Sport0 Receive Data Primary
62	RFS0/PF19	I/O	Sport0 Receive Frame Sync
63	RSCLK0/PF28	I/O	Sport0 Receive Serial Clock
64	GND	Power	
65	CLKBUF	O – 47R serial	Clock Out (25Mhz permanent)
66	GND	Power	
67	SCK	I/O	SPI Clock
68	MISO	I/O	Master In Slave Out
69	MOSI	I/O	Master Out Slave In
70	nc	-	
71	nc	-	
72	DT1SEC/PF22	I/O	Sport1 Transmit Data Secondary
73	DT1PRI/PF23	I/O	Sport1 Transmit Data Primary
74	TFS1/PF21	I/O	Sport1 Transmit Frame Sync
75	TSCLK1/PF31	I/O	Sport1 Transmit Serial Clock
76	DR1SEC/PF25	I/O	Sport1 Receive Data Secondary
77	DR1PRI	I	Sport1 Receive Data Primary
78	RFS1/PF24	I/O	Sport1 Receive Frame Sync
79	RSCLK1/PF30	I/O	Sport1 Receive Serial Clock
80	GND	Power	
81	PF8	I/O	GPIO
82	PF9	I/O	GPIO
83	nc	-	
84	nc	-	
85	nc	-	
86	nc	-	
87	nc	-	
88	nc	-	
89	nc	-	
90	nc	-	
91	nc	-	
92	nc	-	
93	PPI0D15/PF47	I/O	PPI Data
94	PPI0D14/PF46	I/O	PPI Data
95	PPI0D13/PF45	I/O	PPI Data



Pin No.	Signal Name	Type	Function
96	PPIOD12/PF44	I/O	PPI Data
97	PPIOD11/PF43	I/O	PPI Data
98	PPIOD10/PF42	I/O	PPI Data
99	PPIOD9/PF41	I/O	PPI Data
100	PPIOD8/PF40	I/O	PPI Data
201	GND	Shield	
202	GND	Shield	
203	GND	Shield	
204	GND	Shield	
205	GND	Shield	
206	GND	Shield	
207	GND	Shield	
208	GND	Shield	
209	GND	Shield	
210	GND	Shield	

Table 4-1 - Connector Description X1

## 4.2 Connector X2

Please mind the mounted pull up, pull down and serial resistors on the Core Module (see column “Type”).

Pin No.	Signal Name	Type	Function
101	NABE0	O – 47R serial	Byte Enable
102	NABE1	O – 47R serial	Byte Enable
103	NABE2	O – 47R serial	Byte Enable
104	NABE3	O – 47R serial	Byte Enable
105	A2	O – 47R serial	Address Bus
106	A3	O – 47R serial	Address Bus
107	A4	O – 47R serial	Address Bus
108	A5	O – 47R serial	Address Bus
109	A6	O – 47R serial	Address Bus
110	A7	O – 47R serial	Address Bus
111	A8	O – 47R serial	Address Bus
112	A9	O – 47R serial	Address Bus
113	A10	O – 47R serial	Address Bus
114	A11	O – 47R serial	Address Bus
115	GND	Power	
116	3V3	Power	
117	3V3	Power	
118	3V3	Power	
119	GND	Power	
120	GND	Power	
121	GND	Power	
122	D0	I/O – 47R serial	Data Bus
123	D1	I/O – 47R serial	Data Bus
124	D2	I/O – 47R serial	Data Bus
125	D3	I/O – 47R serial	Data Bus
126	D4	I/O – 47R serial	Data Bus
127	D5	I/O – 47R serial	Data Bus
128	D6	I/O – 47R serial	Data Bus
129	D7	I/O – 47R serial	Data Bus
130	D8	I/O – 47R serial	Data Bus
131	D9	I/O – 47R serial	Data Bus



Pin No.	Signal Name	Type	Function
132	D10	I/O – 47R serial	Data Bus
133	D11	I/O – 47R serial	Data Bus
134	D12	I/O – 47R serial	Data Bus
135	D13	I/O – 47R serial	Data Bus
136	D14	I/O – 47R serial	Data Bus
137	D15	I/O – 47R serial	Data Bus
138	nc	-	
139	NRESET	I – 470R pull up	Reset
140	nc	-	
141	NAMS1	O – 47R serial	Bank Select
142	NAMS2	O – 47R serial	Bank Select
143	NAMS3	O – 47R serial	Bank Select
144	NAOE	O – 47R serial	Output Enable
145	NARE	O – 47R serial	Read Enable
146	NAWE	O – 47R serial	Write Enable
147	ARDY	I – 10k pull up	Hardware Ready Control
148	GND	Power	
149	SCLK	O – 47R serial	Clock Output
150	GND	Power	
151	nc	-	
152	nc	-	
153	nc	-	
154	BMODE1	I – 10k pull down	Bode Mode
155	BMODE0	I – 10k pull down	Bode Mode
156	NFLASH_WP	I – 10k pull up	Flash Write Protect
157	NBGH	O – 47R serial	Bus Grant Hang
158	NBR	I – 10k pull up	Bus Request
159	NBG	O – 47R serial	Bus Grant
160	GND	PWR	
161	PF15/EXT CLK	I/O	GPIO/ External Timer Clock Input
162	PF0/SPISS/TMR0	I/O	GPIO/Slave SPI Select/Timer
163	PF1/SPISEL1/TMR1	I/O	GPIO/SPI Select/Timer
164	PF2/SPISEL2/TMR2	I/O	GPIO/SPI Select/Timer
165	PF3/SPISEL3/TMR3	I/O	GPIO/SPI Select/Timer
166	PF4/SPISEL4/TMR4	I/O	GPIO/SPI Select/Timer
167	PF5/SPISEL5/TMR5	I/O	GPIO/SPI Select/Timer
168	PF6/SPISEL6/TMR6	I/O	GPIO/SPI Select/Timer
169	PF7/SPISEL7/TMR7	I/O	GPIO/SPI Select/Timer
170	D31	I/O – 47R serial	Data Bus
171	D30	I/O – 47R serial	Data Bus
172	D29	I/O – 47R serial	Data Bus
173	D28	I/O – 47R serial	Data Bus
174	D27	I/O – 47R serial	Data Bus
175	D26	I/O – 47R serial	Data Bus
176	D25	I/O – 47R serial	Data Bus
177	D24	I/O – 47R serial	Data Bus
178	D23	I/O – 47R serial	Data Bus
179	D22	I/O – 47R serial	Data Bus
180	D21	I/O – 47R serial	Data Bus
181	D20	I/O – 47R serial	Data Bus
182	D19	I/O – 47R serial	Data Bus
183	D18	I/O – 47R serial	Data Bus
184	D17	I/O – 47R serial	Data Bus



Pin No.	Signal Name	Type	Function
185	D16	I/O – 47R serial	Data Bus
186	nc	-	
187	A25	O – 47R serial	Address Bus
188	A24	O – 47R serial	Address Bus
189	A23	O – 47R serial	Address Bus
190	A22	O – 47R serial	Address Bus
191	A21	O – 47R serial	Address Bus
192	A20	O – 47R serial	Address Bus
193	A19	O – 47R serial	Address Bus
194	A18	O – 47R serial	Address Bus
195	A17	O – 47R serial	Address Bus
196	A16	O – 47R serial	Address Bus
197	A15	O – 47R serial	Address Bus
198	A14	O – 47R serial	Address Bus
199	A13	O – 47R serial	Address Bus
200	A12	O – 47R serial	Address Bus
211	GND	Shield	
212	GND	Shield	
213	GND	Shield	
214	GND	Shield	
215	GND	Shield	
216	GND	Shield	
217	GND	Shield	
218	GND	Shield	
219	GND	Shield	
220	GND	Shield	

Table 4-2 - Connector Description X2

## 5 Application Information

### 5.1 Supply Voltage Decoupling

For better stability we recommend to add a 100nF capacitor to each power supply pin and an additional 47µF tantalum capacitor to the  $V_{IN}$  voltage rail next to the module.

### 5.2 Reset circuit

The integrated Reset circuit monitors the 3.3V power rail. If this voltage drops below 2.93V, the  $\overline{\text{RESET}}$  signal will be asserted. If the 3.3V voltage domain rises above this threshold,  $\overline{\text{RESET}}$  will be kept low for 140 to 280ms and will be released afterwards.

The  $\overline{\text{RESET}}$  signal is an open collector output with an internal pull-up resistor of 470Ω. This signal can be used as external manual reset by connecting an external push-button that ties the signal to ground.

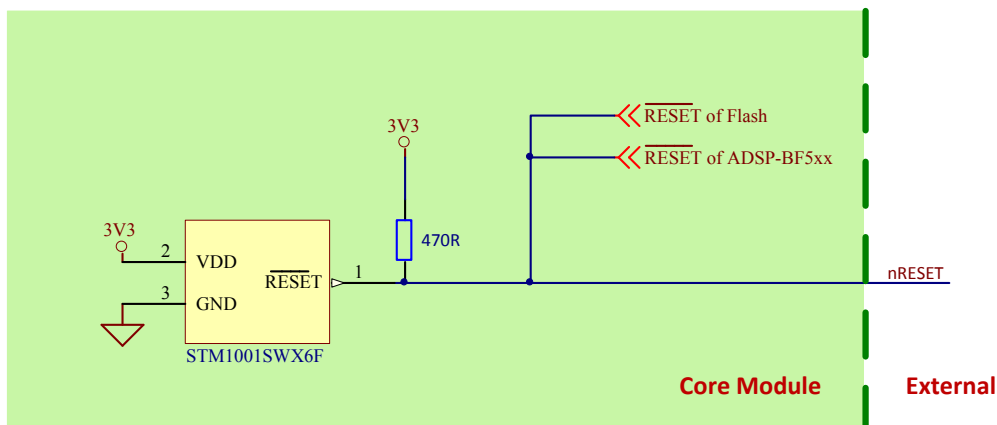


Figure 5-1: Reset circuit

### 5.3 Application Example Schematics

Have a look at our eDEV-BF5xx schematics, which can be found at <http://www.bluetechnix.com/goto/edev-bf5xx> to get application examples.



## 6 Mechanical Outline

### 6.1 Top View

Figure 6-1 shows the top view of the mechanical outline of the eCM-BF561 Core Module. All dimensions are given in millimeters! Outline dimensions +/- 0,5mm.

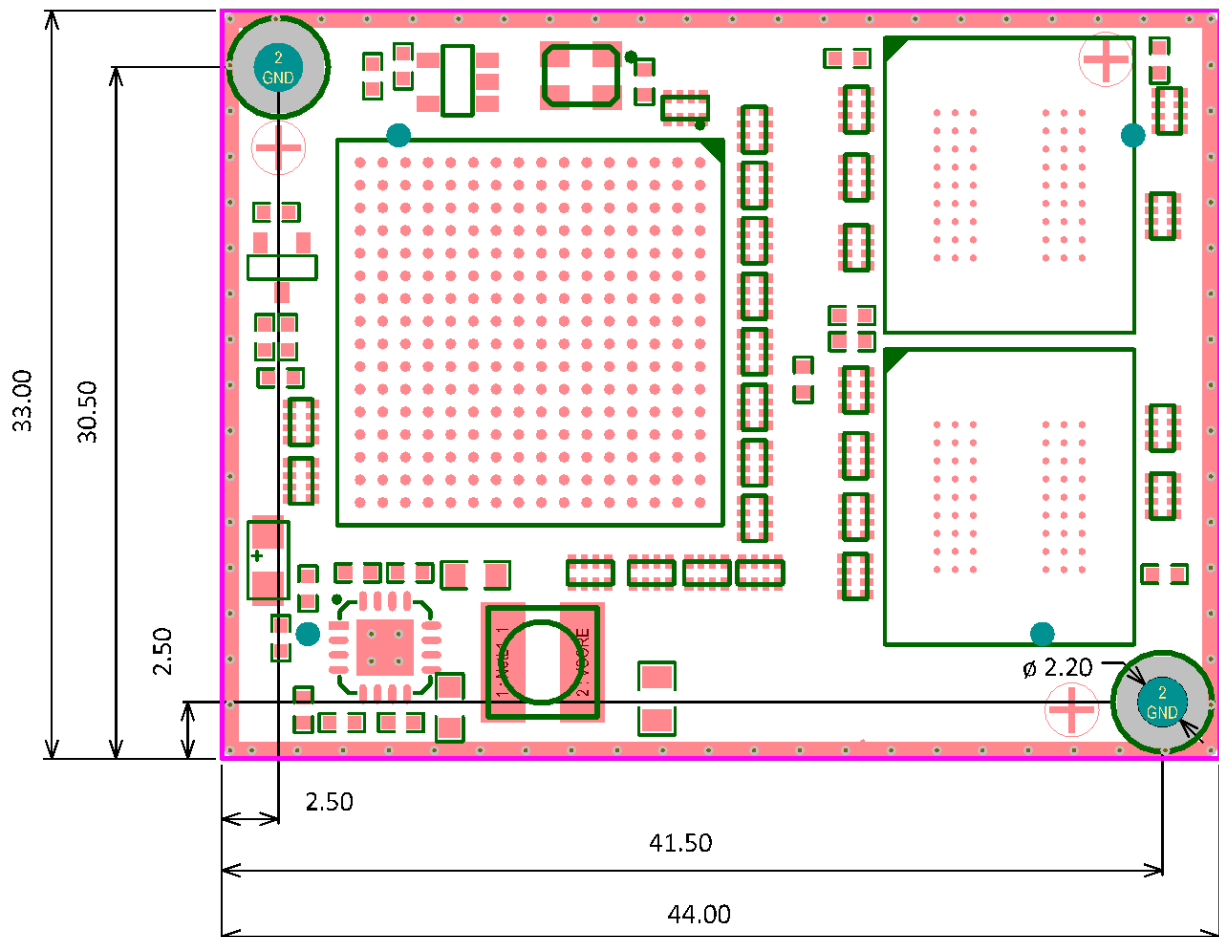


Figure 6-1: Mechanical outline (top view)

### 6.2 Bottom View

Figure 6-2 shows the bottom of the mechanical outline of the eCM-BF561 Core Module. All dimensions are given in millimeters!

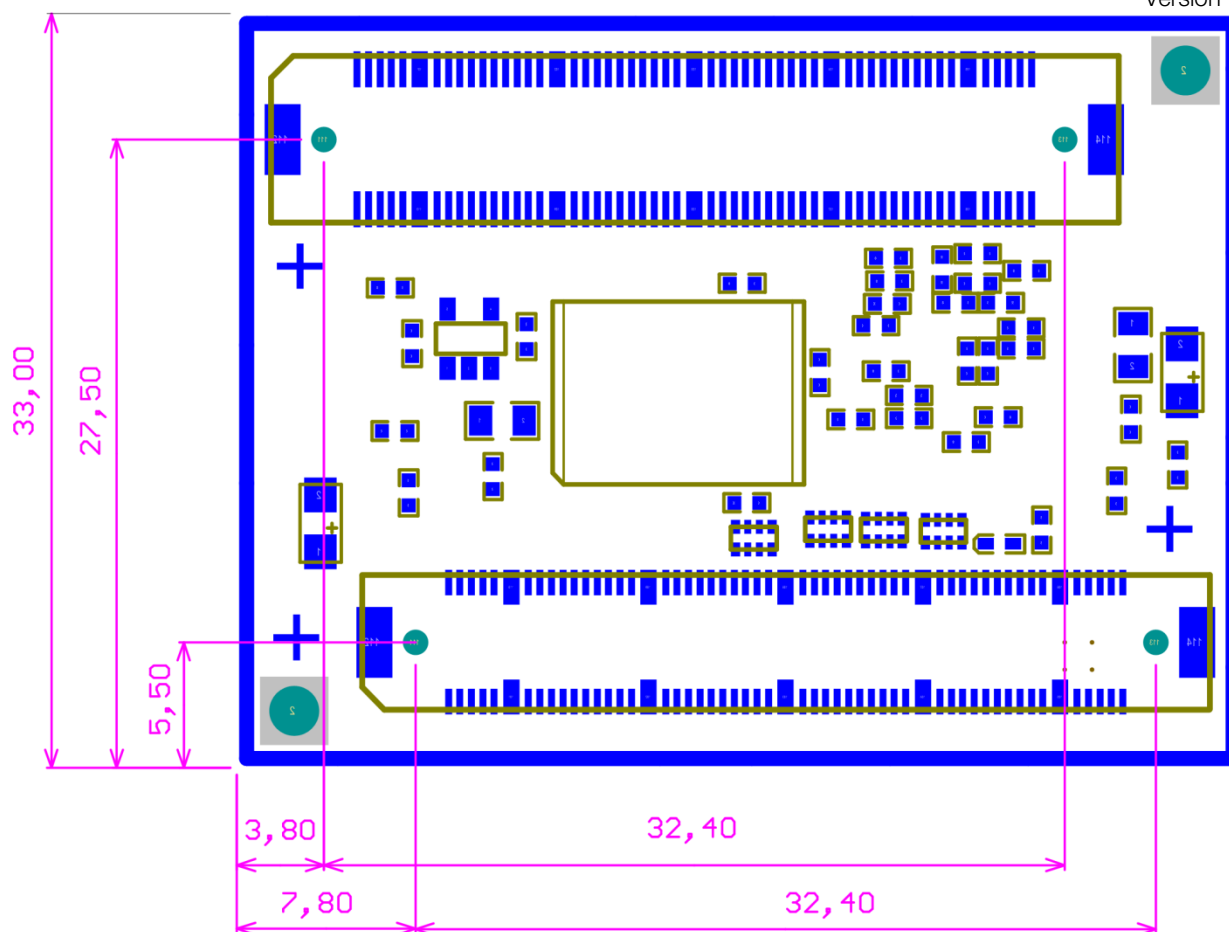


Figure 6-2: Mechanical outline and Bottom Connectors (bottom view)

### 6.3 Side View

Figure 6-3 shows the mechanical outline from side of the eCM-BF561 Core Module. All dimensions are given in millimeters!

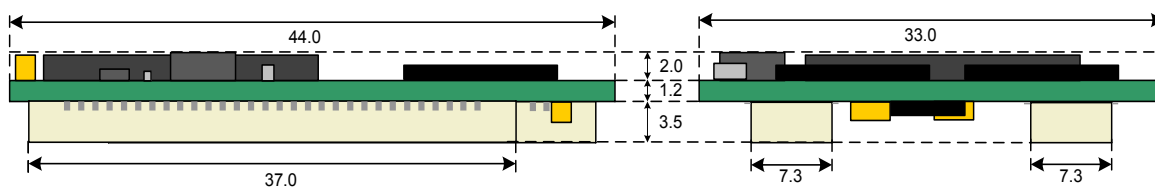


Figure 6-3: Mechanical outline (side view)

## 6.4 Footprint

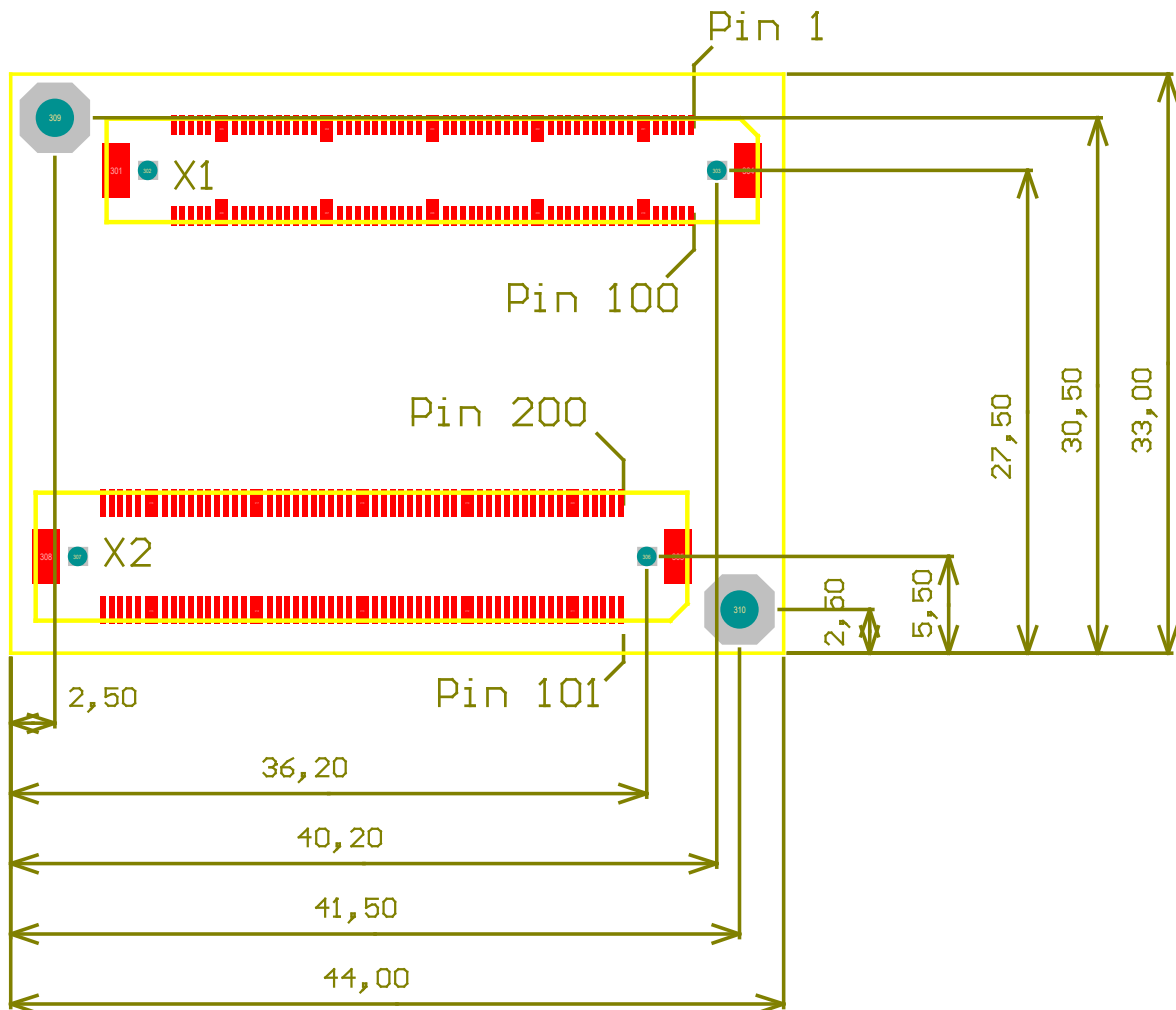


Figure 6-4: Footprint (top view)

The footprint for Altium Designer is available on request. The used connectors can be found in Table 6-1. For detailed dimensions of the connectors please see the datasheet from the manufacturer's homepage.

## 6.5 Connectors

Connector Core Module	Matching Connector	Manufacturer	Manufacturer Part No.
X1	X2	Hirose	FX-10A-100S/10SV
X2	X1	Hirose	FX-10A-100P/10SV

Table 6-1: Core Module connector types

The Core Module features 2 connectors, one male and one female. The base board uses the same connectors but oriented in the opposite way.



## 7 Support

### 7.1 General Support

General support for products can be found at Bluetechnix' support site <https://support.bluetechnix.at/wiki>

### 7.2 Board Support Packages

Board support packages and software downloads are for registered customers only  
<https://support.bluetechnix.at/software/>

### 7.3 Blackfin® Software Support

#### 7.3.1 BLACKSheep® OS

BLACKSheep® OS stands for a powerfully and multithreaded real-time operating system (RTOS) originally designed for digital signal processing application development on Analog Devices Blackfin® embedded processors. This high-performance OS is based on the reliable and stable real-time VDK kernel from Analog Devices that comes with VDSP++ IDE. Of course BLACKSheep® OS is fully supported by all Bluetechnix Core-Modules and development hardware.

#### 7.3.2 LabVIEW

You can get LabVIEW embedded support for Bluetechnix Core Modules by Schmid-Engineering AG  
<http://www.schmid-engineering.ch>.

#### 7.3.3 uClinux

You can get uClinux support (boot loader and uClinux) for Bluetechnix Core Modules at  
<http://blackfin.uClinux.org>.

### 7.4 Blackfin® Design Services

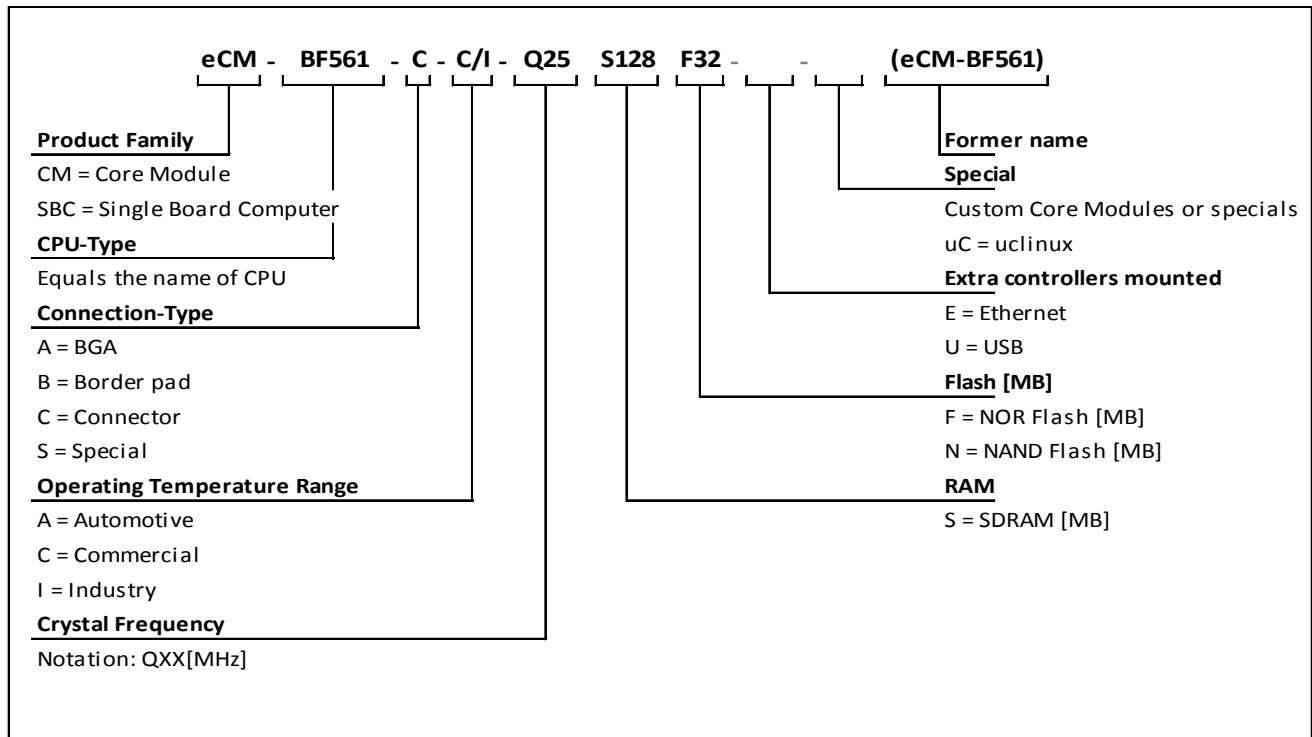
Based on more than seven years of experience with Blackfin, Bluetechnix offers development assistance as well as custom design services and software development.

#### 7.4.1 Upcoming Products and Software Releases

Keep up to date with all product changes, releases and software updates of Bluetechnix at  
<http://www.bluetechnix.com>.



## 8 Ordering Information



### 8.1 Predefined mounting options for CORE MODULE NICKNAME

Article Number	Name	Temperature Range
100-1214-1	eCM-BF561-C-C-Q25S128F32 (eCM-BF561)	Commercial
100-1214-1-TR	eCM-BF561-C-C-Q25S128F32 (eCM-BF561) Tape Reel (50 pcs per reel)	Commercial
100-1215-1	eCM-BF561-C-I-Q25S128F32	Industrial
100-1215-1-TR	eCM-BF561-C-I-Q25S128F32	Industrial

Table 8-1 - Mounting options

Development boards for the eCM-BF561 are listed in the following table.

Article Number	Name	Description
100-2342-2	eDEV-BF5xx	Blackfin Evaluation Board
100-2350-1	CDEV-BF5xx	Camera Development Board
100-3106	CDK – Camera Development Kit	CDK Camera Development Kit with eCM-BF561 and ISM-MT9M024
100-3400	Blackfin Evaluation Starter Package	eDEV-BF5xx and eCM-BF561

Table 8-2 - Development boards for eCM-BF561

**NOTE:** Custom Core Modules are available on request! Please contact Bluetechnix ([office@bluetechnix.com](mailto:office@bluetechnix.com)) if you are interested in custom Core Modules.



## 9 Dependability

### 9.1 MTBF

Please keep in mind that a part stress analysis would be the only way to obtain significant failure rate results, because MTBF numbers just represent a statistical approximation of how long a set of devices should last before failure. Nevertheless, we can calculate an MTBF of the Core Module using the bill of material. We take all the components into account. The PCB and solder connections are excluded from this estimation. For test conditions we assume an ambient temperature of 30°C of all Core Module components except the Blackfin® processor (80°C) and the memories (70°C). We use the MTBF Calculator from ALD (<http://www.aldservice.com/>) and use the reliability prediction MIL-217F2 Part Stress standard. Please get in touch with Bluetechnix ([office@bluetechnix.com](mailto:office@bluetechnix.com)) if you are interested in the MTBF result.



## 10 Product History

### 10.1 Version Information

#### 10.1.1 eCM-BF561-C-C-Q25S128F32 (eCM-BF561)

Version	Component	Type
1.1.1	Processor	ADSP-BF561SKBCZ-6A (Rev 0.5)
	RAM	IS42S16320B-7BL
	Flash	PF48F4000P0ZBQE (32MB)

Table 10-1: Overview eCM-BF561-C-C-Q25S128F32 product changes

#### 10.1.2 eCM-BF561-C-I-Q25S128F32

Version	Component	Type
1.1.1	Processor	ADSP-BF561SBBCZ-5A (Rev 0.5)
	RAM	IS42S16320B-7BLI
	Flash	PF48F4000P0ZBQE (32MB)

Table 10-2: Overview eCM-BF561-C-I-Q25S128F32 product changes

### 10.2 Anomalies

Version	Date	Description
V1.0	2011 02 11	No anomalies reported yet.
V1.1	2011 07 18	No anomalies reported yet.

Table 10-3: Overview product anomalies



## 11 Document Revision History

Version	Date	Document Revision
1	2009 12 03	First release V1.0 of the Document
2	2011 07 18	Updated document with industrial version.
3	2011 10 18	Typical $I_{3V3}$ set to 700mA
4	2013 06 17	ARDY pin set to input, FLASH_WP renamed to nFLASH_WP (active low) Update to new CI

Table 11-1: Revision history





## 12 List of Abbreviations

Abbreviation	Description
<b>ADI</b>	Analog Devices Inc.
<b>AI</b>	Analog Input
<b>AMS</b>	Asynchronous Memory Select
<b>AO</b>	Analog Output
<b>CM</b>	Core Module
<b>DC</b>	Direct Current
<b>DSP</b>	Digital Signal Processor
<b>eCM</b>	Enhanced Core Module
<b>EBI</b>	External Bus Interface
<b>ESD</b>	Electrostatic Discharge
<b>GPIO</b>	General Purpose Input Output
<b>I</b>	Input
<b>I<sup>2</sup>C</b>	Inter-Integrated Circuit
<b>I/O</b>	Input/Output
<b>ISM</b>	Image Sensor Module
<b>LDO</b>	Low Drop-Out regulator
<b>MTBF</b>	Mean Time Between Failure
<b>NC</b>	Not Connected
<b>NFC</b>	NAND Flash Controller
<b>O</b>	Output
<b>OS</b>	Operating System
<b>PPI</b>	Parallel Peripheral Interface
<b>PWR</b>	Power
<b>RTOS</b>	Real-Time Operating System
<b>SADA</b>	Stand Alone Debug Agent
<b>SD</b>	Secure Digital
<b>SoC</b>	System on Chip
<b>SPI</b>	Serial Peripheral Interface
<b>SPM</b>	Speech Processing Module
<b>SPORT</b>	Serial Port
<b>TFT</b>	Thin-Film Transistor
<b>TISM</b>	Tiny Image Sensor Module
<b>TSC</b>	Touch Screen Controller
<b>UART</b>	Universal Asynchronous Receiver Transmitter
<b>USB</b>	Universal Serial Bus
<b>USBOTG</b>	USB On The Go
<b>ZIF</b>	Zero Insertion Force

Table 12-1: List of abbreviations



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