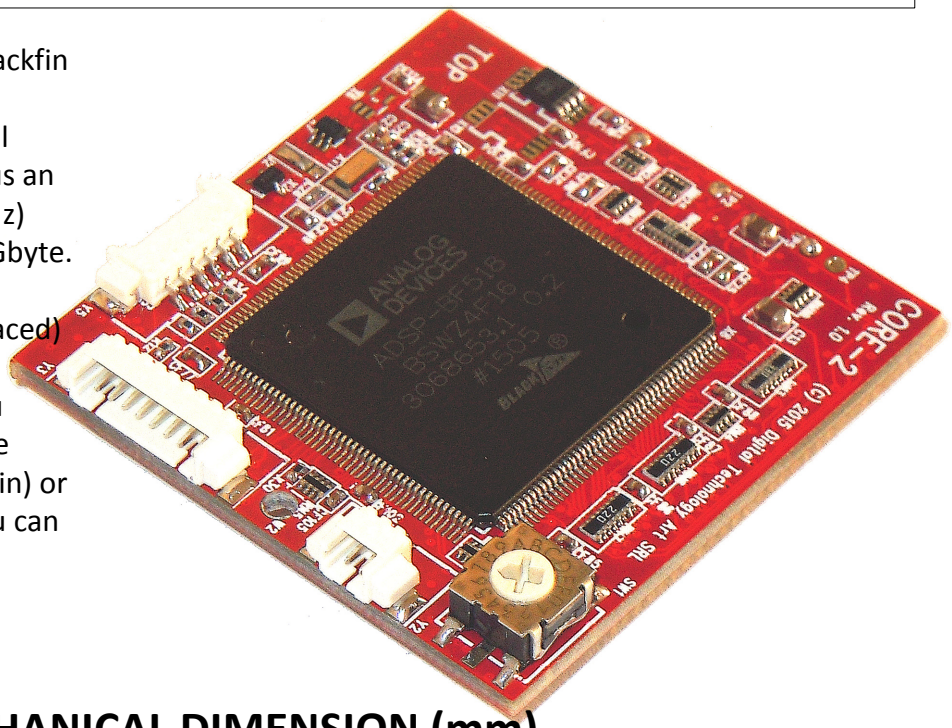
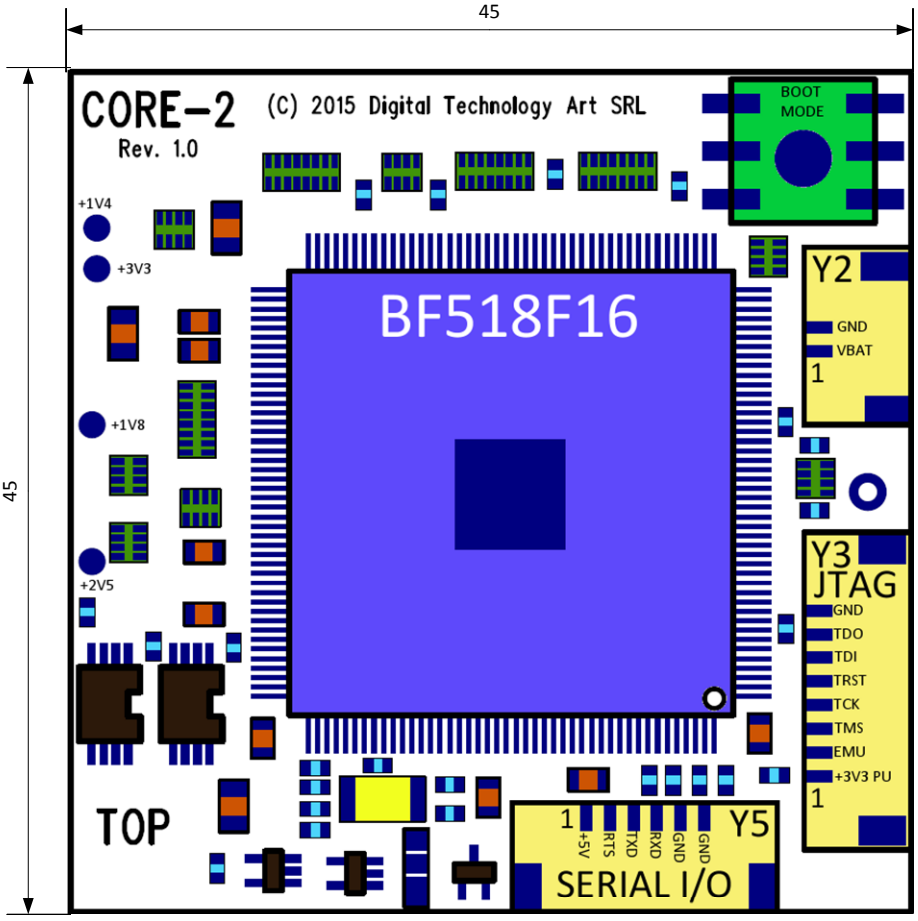
User Manual

CORE-2



CORE-2 is mini module based on Blackfin BF518F16 by Analog Device Inc.
In a minimum space are available all voltages supply required by DSP plus an external SDRAM (64 Mbyte 133 MHz) and an optional NAND FLASH by 8 Gbyte.
All DSP bus signals and its ports are accessible trough two (1.27 mm spaced) male connectors.
Is a system ready to use, simply you must supply a +5V and with our free development system (GNU Toolchain) or with Analog Device CROSSCORE you can start the development.

MECHANICAL DIMENSION (mm)



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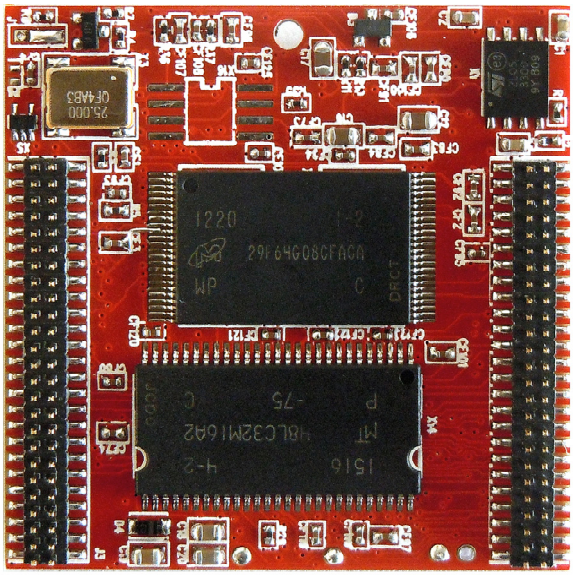
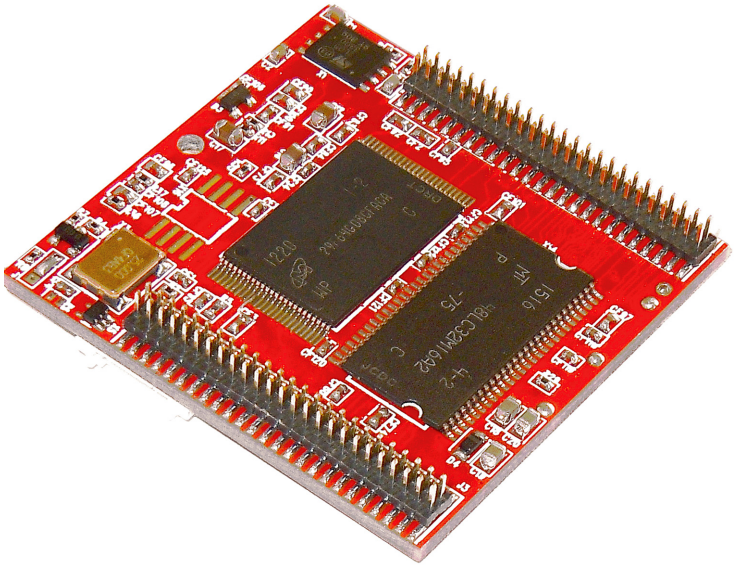
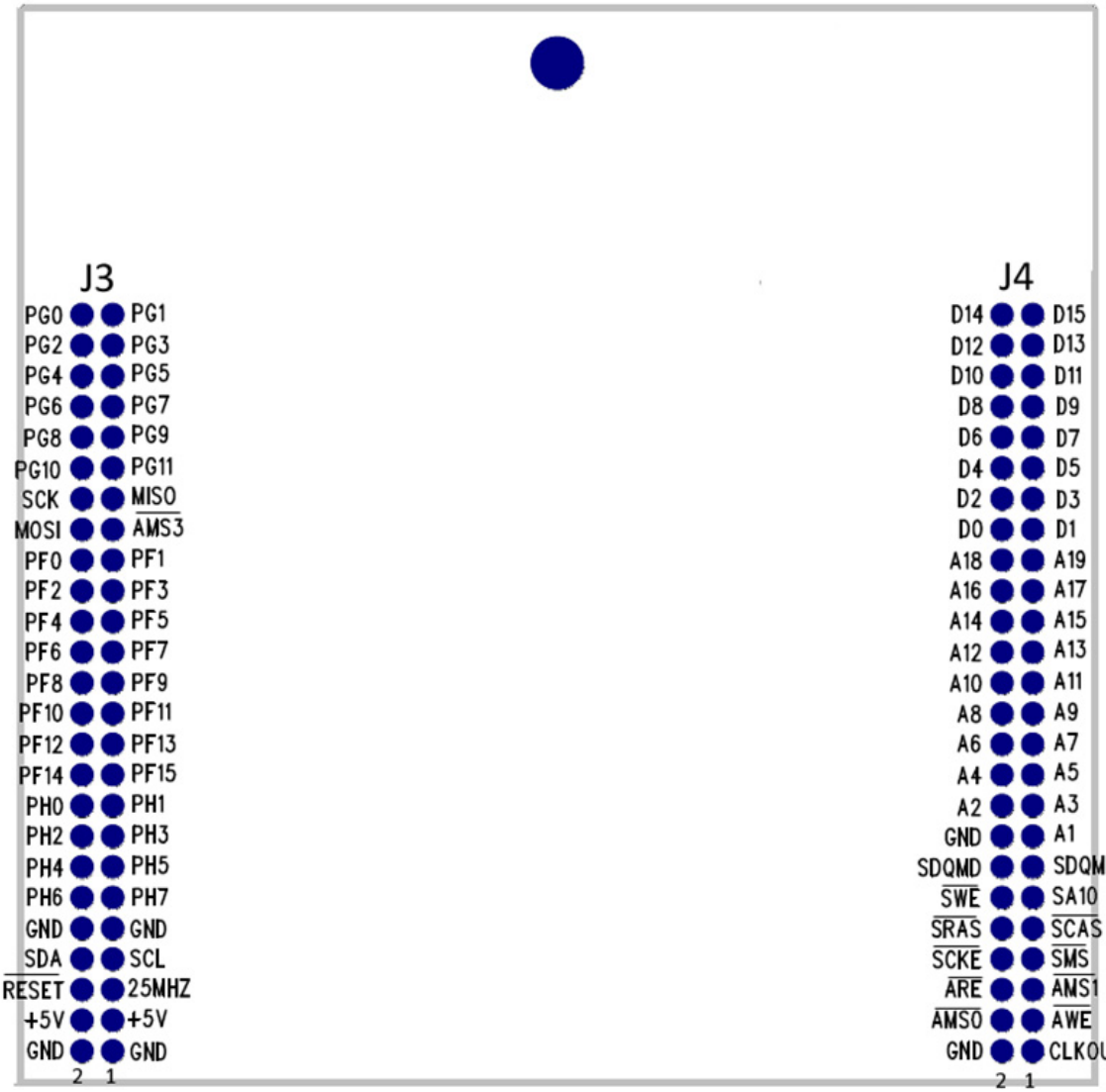
CORE-2

BOTTOM VIEW





BOTTOM VIEW SIGNALS



J3-I/O CONNECTOR

PIN	SIGNAL	DESCRIPTION
1	GND	Power supply return
2	GND	Power supply return
3	+5V	Power supply +5V ±5% max 70mA @ 400MHz
4	+5V	Power supply +5V ±5% max 70mA @ 400MHz
5	25MHz	Oscillator output
6	/RESET	Active low RESET output signal
7	SCL	TWI Serial Clock
8	SDA	TWI Serial Data
9	GND	Power supply return
10	GND	Power supply return
11	PH7	GPIO/SPORT0 Transmit Data Primary/SPI1 Slave Select Enable 6 GPIO/SPORT1 Secondary Rx Data/UART1 Receive/Timer 7/Timer2 Alternate Clock Input
12	PH6	GPIO/SPORT1 Secondary Tx Data/UART1 Transmit/SPI1 Slave Select 1 /Counter Zero Marker
13	PH5	GPIO/SPORT1 Tx Clock/Asynchronous Memory Hardware Ready Control/ External Clock for PTP TSYNC/Counter Down Gate
14	PH4	GPIO/SPORT1 Tx Frame Sync/Asynchronous Memory Output Enable/SPI0 Slave Select 3/Counter Up Direction
15	PH3	GPIO/SPORT1 Primary Tx Data/SPI1 Master Out Slave In/RSI Data 7
16	PH2	GPIO/SPORT1 Rx Clock/SPI1 Clock/RSI Data 6
17	PH1	GPIO/SPORT1 Rx Frame Sync/SPI1 Master In Slave Out/RSI Data 5
18	PH0	GPIO/SPORT1 Primary Rx Data/SPI1 Device Select/RSI Data 4
19	PF15	GPIO/SPI1 Master Out Slave In/PPI Data 1 GPIO/Ethernet MII PHY Interrupt/PPI Data 15/Alternate PWM Sync
20	PF14	GPIO/Ethernet MII Transmit Enable/PPI Data 14/PWM BL Out
21	PF13	GPIO/Ethernet MII or RMII Receive D1/PPI Data 13/PWM BH Output
22	PF12	GPIO/Ethernet MII Transmit D1/PPI Data 12/PWM AL Output
23	PF11	GPIO/Ethernet MII Receive D0/PPI Data 11/PWM AH output /Timer3 Alternate Capture Input
24	PF10	GPIO/Ethernet MII or RMII Transmit D0/PPI Data 10/Timer 3
25	PF9	GPIO/Ethernet Management Channel Serial Data/PPI Data 9/Timer 2
26	PF8	GPIO/Ethernet Management Channel Clock/PPI Data 8/SPI1 Slave Select 4
27	PF7	GPIO/SPI0 Slave Select 1/PPI Data 7/PWM Sync
28	PF6	GPIO/Ethernet MII Collision/PPI Data 6/PWM CL Out/Timer1 Alternate Capture Input C
29	PF5	GPIO/Ethernet MII Receive Data Valid/PPI Data 5/PWM CH Out /Timer0 Alternate Capture Input
30	PF4	GPIO/Ethernet MII Receive Clock/PPI Data 4/PWM BL Out/Timer1 Alternate CLK
31	PF3	GPIO/Ethernet MII Data Receive D3/PPI Data 3/PWM BH Output/Timer0 Alternate Clock
32	PF2	GPIO/Ethernet Transmit D3/PPI Data 2/PWM AL Output
33	PF1	GPIO/Ethernet MII Receive D2/PPI Data 1/PWM AH Output/Timer7 Alternate Clock
34	PF0	GPIO/Ethernet MII Transmit D2/PPI Data 0/SPI1 Slave Select 2/Timer6 Alternate Clock
35	/AMS3	GPIO/SPI0 Slave Select 2/PPI Frame Sync3/Asynchronous Memory Bank Select 3
36	MOSI	GPIO/SPI0 Master Out Slave In/Timer 1/PPI Frame Sync2/PWM Trip/PTP Auxiliary Snapshot Trigger Input
37	MISO	GPIO/SPI0 Master In Slave Out/Timer0/PPI Frame Sync1/PTP Clock Out
38	SCK	GPIO/SPI0 Clock/PPI Clock/External Timer Reference/PTP Pulse Per Second Out
39	PG11	GPIO/SPI0 Slave Device Select/Asynchronous Memory Bank Select 2/SPI1 Slave Select 5/Timer2 Alternate CLK
40	PG10	GPIO/SPORT0 Secondary Rx Data/UART0 Receive/Timer4 Alternate Capture Input
41	PG9	GPIO/SPORT0 Secondary Tx Data/UART0 Transmit/Timer 4
42	PG8	GPIO/SPORT0 Tx Clock/RSI Clock/Timer 6/Timer6 Alternate Capture Input
43	PG7	GPIO/SPORT0 Tx Primary Data/RSI Command/Timer 1/PPI Frame Sync2
44	PG6	GPIO/SPORT0 Tx Frame Sync/RSI Data 3/Timer0/PPI Frame Sync1
45	PG5	GPIO/SPORT0 Rx Frame Sync/RSI Data 2/PPI Clock/External Timer Reference
46	PG4	GPIO/SPORT0 Rx Clock/RSI Data 1/Timer 5/Timer5 Alternate Capture Input
47	PG3	GPIO/SPORT0 Primary Rx Data/RSI Data 0/SPI0 Slave Select 5/Timer3 Alternate CLK
48	PG2	GPIO/Ethernet MII or RMII Reference Clock/DMA Req 0/PWM CL Out
49	PG1	GPIO/Ethernet MII or RMII Receive Error/DMA Req 1/PWM CH Out
50	PG0	GPIO/Ethernet MII or RMII Carrier Sense or RMII Data Valid/HWAIT/SPI1 Slave Select3

J4-BUS CONNECTOR

PIN	SIGNAL	DESCRIPTION
1	CLKOUT	SDRAM Clock Output
2	GND	Power supply return
3	/AWE	Asynchronous Memory Write Enable
4	/AMS0	Asynchronous Memory Bank Selects
5	/AMS1	Asynchronous Memory Bank Selects
6	/ARE	Asynchronous Memory Read Enable
7	/SMS	SDRAM Bank Select
8	/SCKE	SDRAM Clock Enable
9	/SCAS	SDRAM Column Address Strobe
10	/SRAS	SDRAM Row Address Strobe
11	SA10	SDRAM A10 Signal
12	/SWE	SDRAM Write Enable
13	SDQM1	Byte Enable or Data Mask
14	SDQMD	Byte Enable or Data Mask 2
15	A1	Address Bus
16	GND	Power supply return
17	A3	Address Bus
18	A2	Address Bus
19	A5	Address Bus
20	A4	Address Bus
21	A7	Address Bus
22	A6	Address Bus
23	A9	Address Bus
24	A8	Address Bus
25	A11	Address Bus
26	A10	Address Bus
27	A13	Address Bus
28	A12	Address Bus
29	A15	Address Bus
30	A14	Address Bus
31	A17	Address Bus
32	A16	Address Bus
33	A19	Address Bus
34	A18	Address Bus
35	D1	Data Bus
36	D0	Data Bus
37	D3	Data Bus
38	D2	Data Bus
39	D5	Data Bus
40	D4	Data Bus
41	D7	Data Bus
42	D6	Data Bus
43	D9	Data Bus
44	D8	Data Bus
45	D11	Data Bus
46	D10	Data Bus
47	D13	Data Bus
48	D12	Data Bus
49	D15	Data Bus
50	D14	Data Bus

BOOT MODE

SW1	BOOT MODE
0	Idle/No Boot
1	Boot from 8- or 16-bit external flash memory
2	Boot from internal SPI memory
3	Boot from external SPI memory (EEPROM or flash)
4	Boot from SPI0 host
5	Boot from OTP memory
6	Boot from SDRAM
7	Boot from UART0 Host

Y3-JTAG X ICE-100

PIN	SIGNAL	DESCRIPTION
1	+3.3V 330uA	Pull Up 10K to +3.3V
2	/EMU	Emulation Output
3	TMS	JTAG Mode Select
4	TCK	JTAG CLK
5	/TRST	JTAGReset
6	TDI	JTAG Serial Data In
7	TDO	JTAG Serial Data Out
8	GND	Power supply return

Y5-SERIAL I/O

PIN	SIGNAL	DESCRIPTION
1	+5V	Power supply
2	RTS	Request To Send
3	TXD	Transmit Serial Data
4	RXD	Receive Serial Data
5	GND	Power supply return
6	GND	Power supply return

Y2-RTC BATTERY

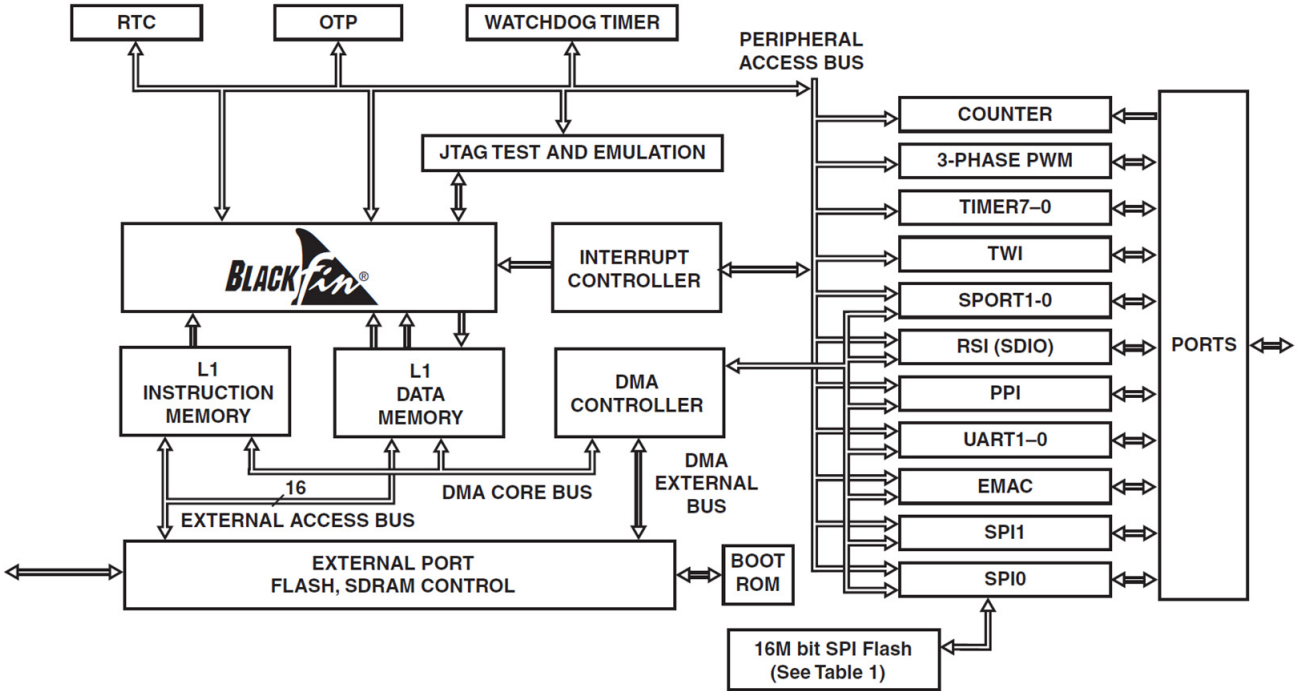
PIN	SIGNAL	DESCRIPTION
1	VBAT	+3V RTC supply
2	GND	Power supply return

USB2 CONNECTION

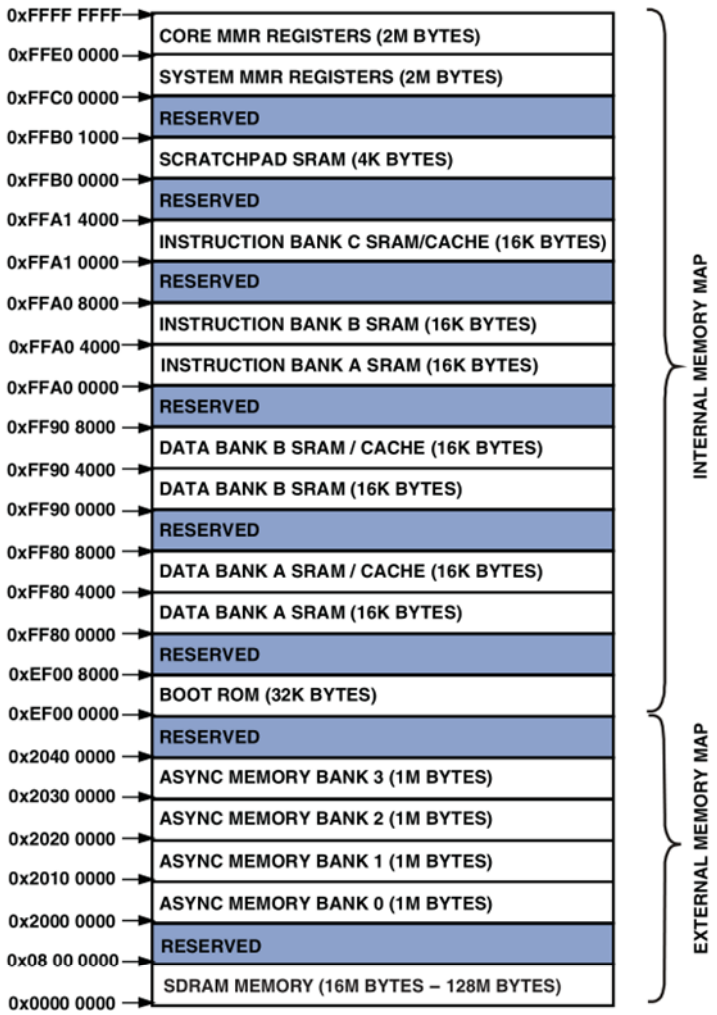
With a **TTL-232RG-VSW5V-WE** by FTDI is possible to connect and supply CORE-2 with a personal computer by USB 2 interface.
With this link you can download and debug the program with our GNU toolchain available in MDI program.

Y5	SIGNAL	TTL-232RG-VSW5V-WE
1	+5V	RED wire
2	RTS	No connection
3	TXD	YELLOW wire
4	RXD	ORANGE wire
5	GND	No connection
6	GND	BLACK wire

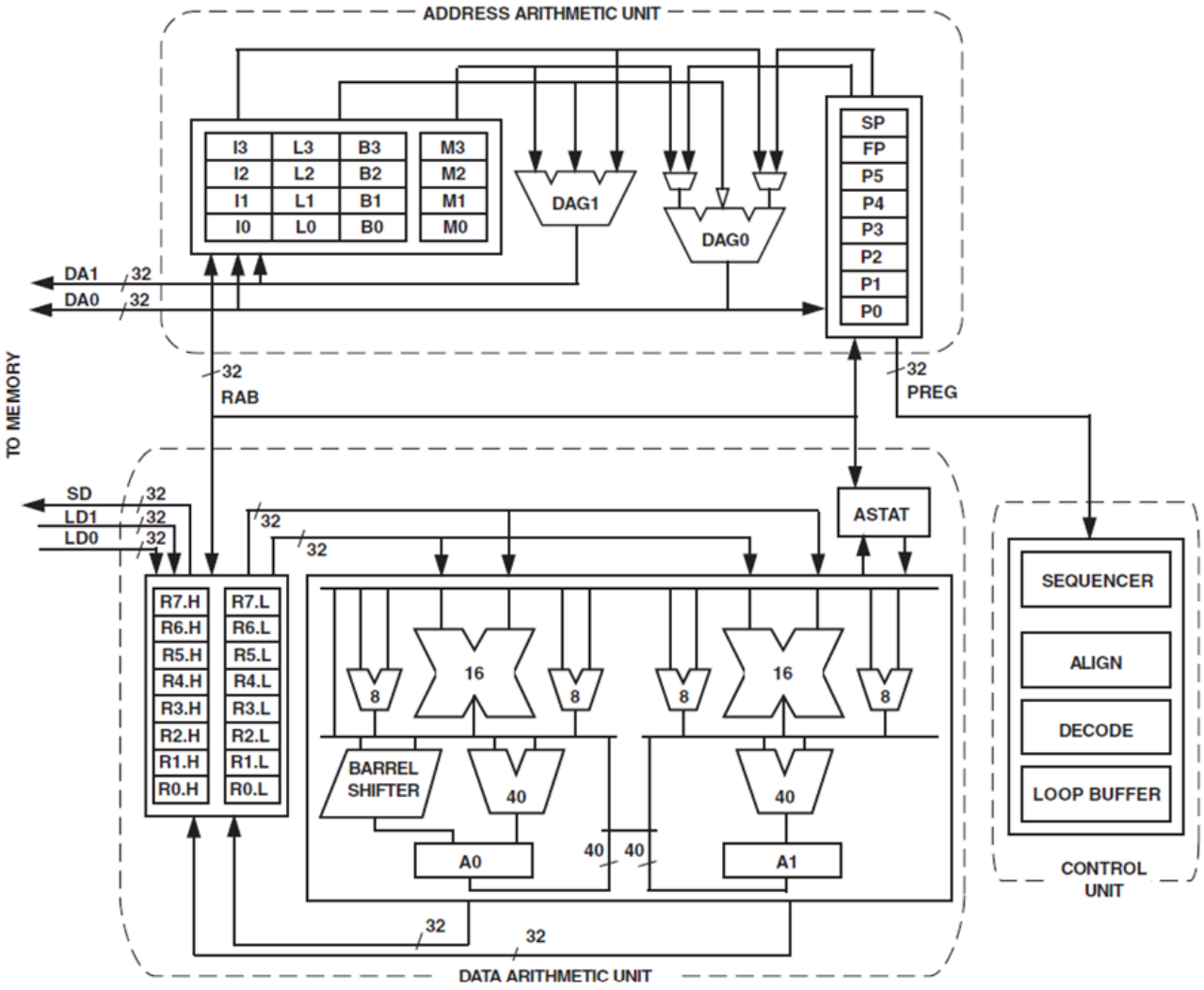
BF518 FUNCTIONAL BLOCK DIAGRAM



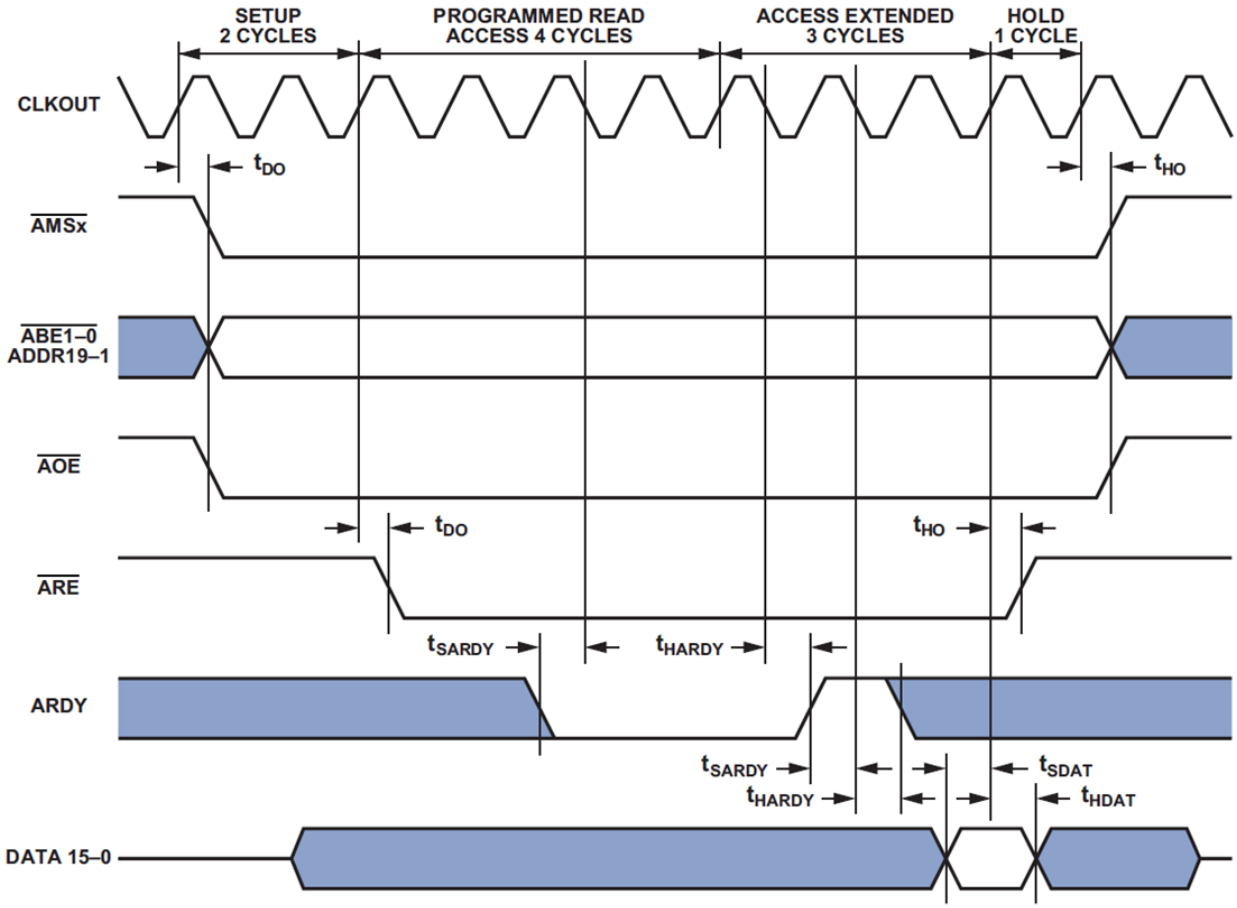
BF518 MEMORY MAP



BLACKFIN PROCESSORE CORE

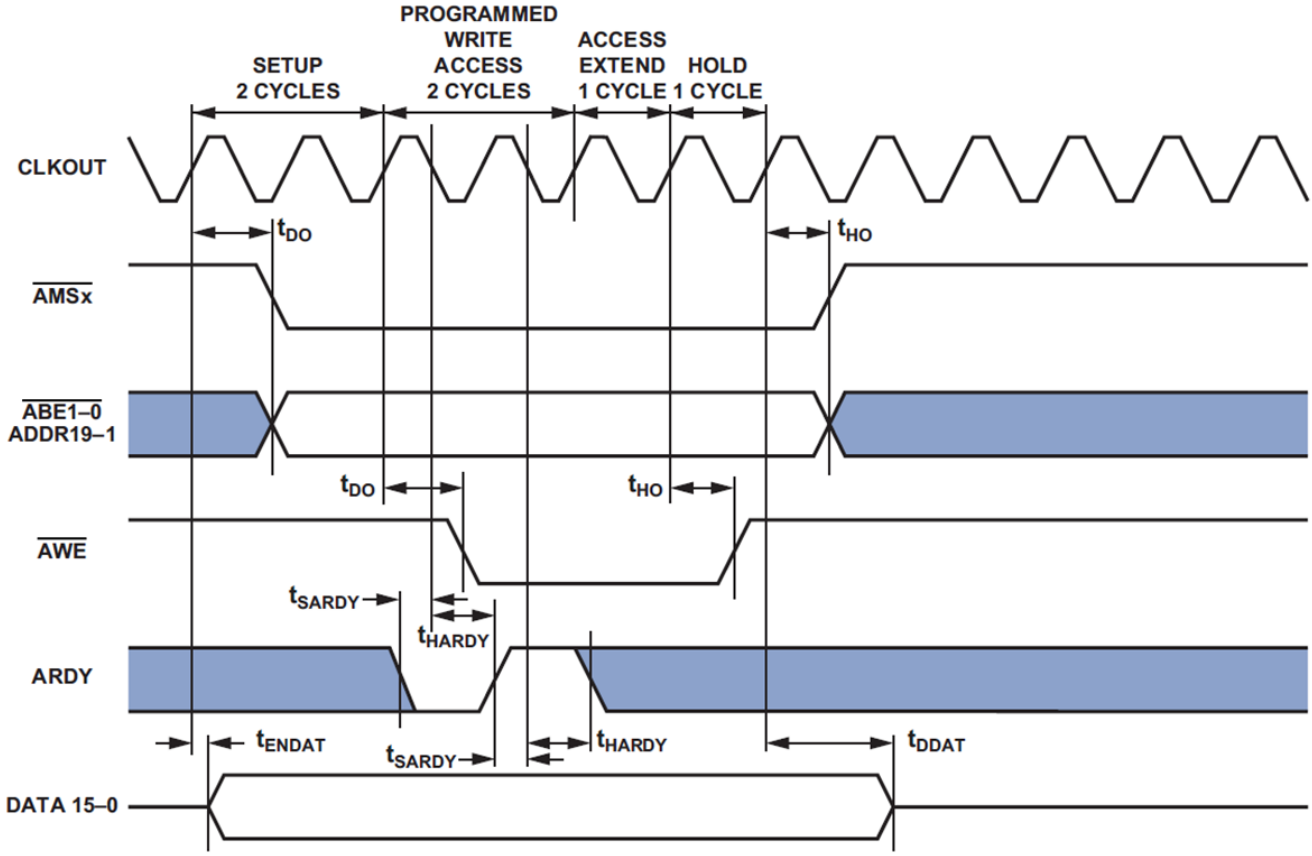


READ CYCLE TIMING ON BUS



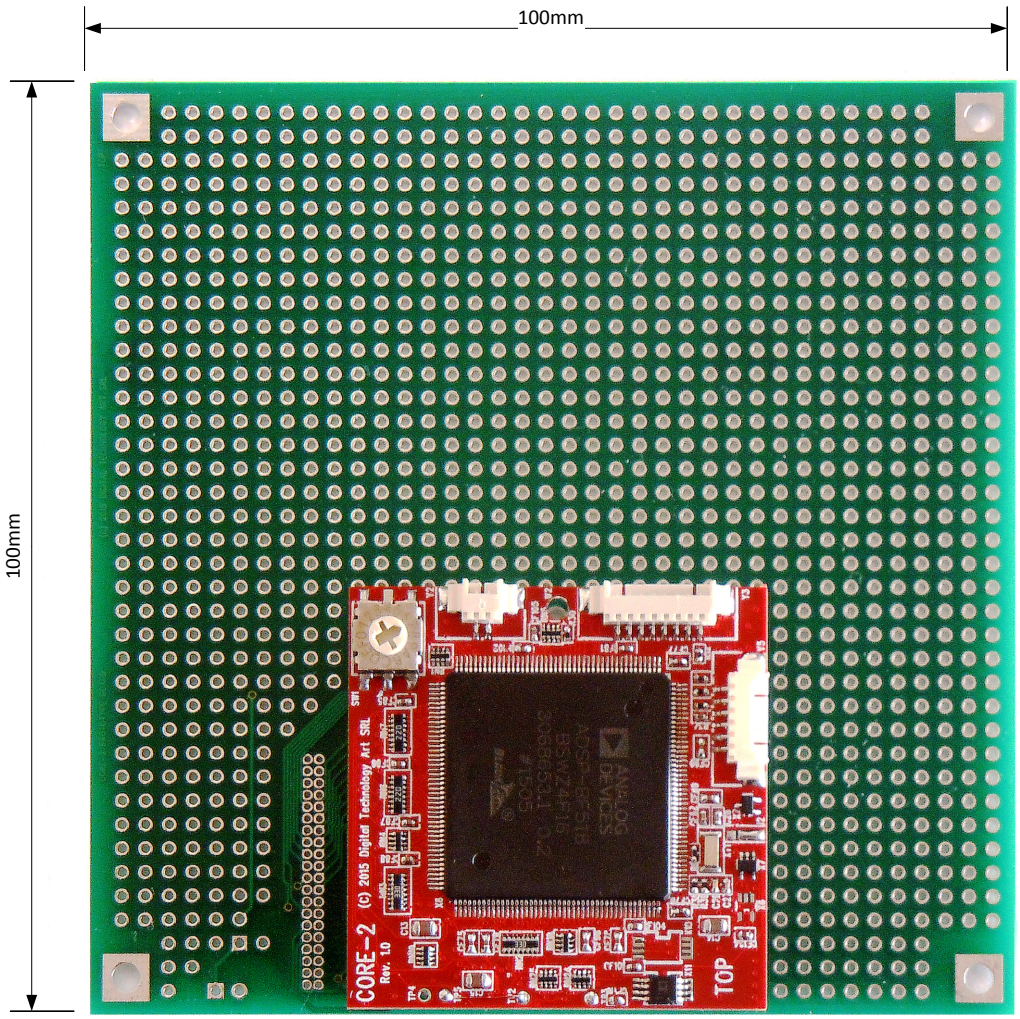
Parameter		V_{DDMEM} 3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.2		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

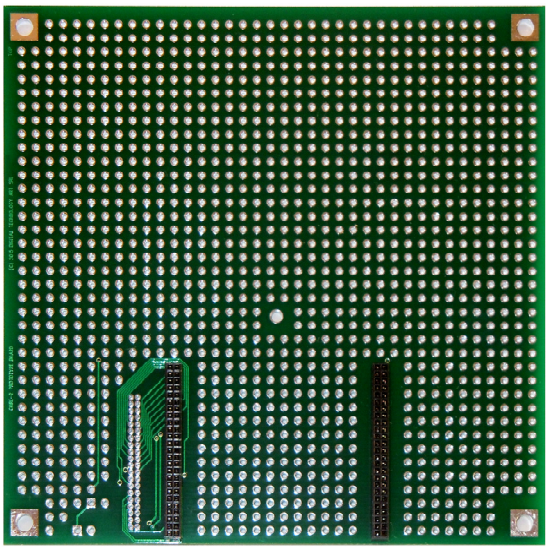
WRITE CYCLE TIMING ON BUS



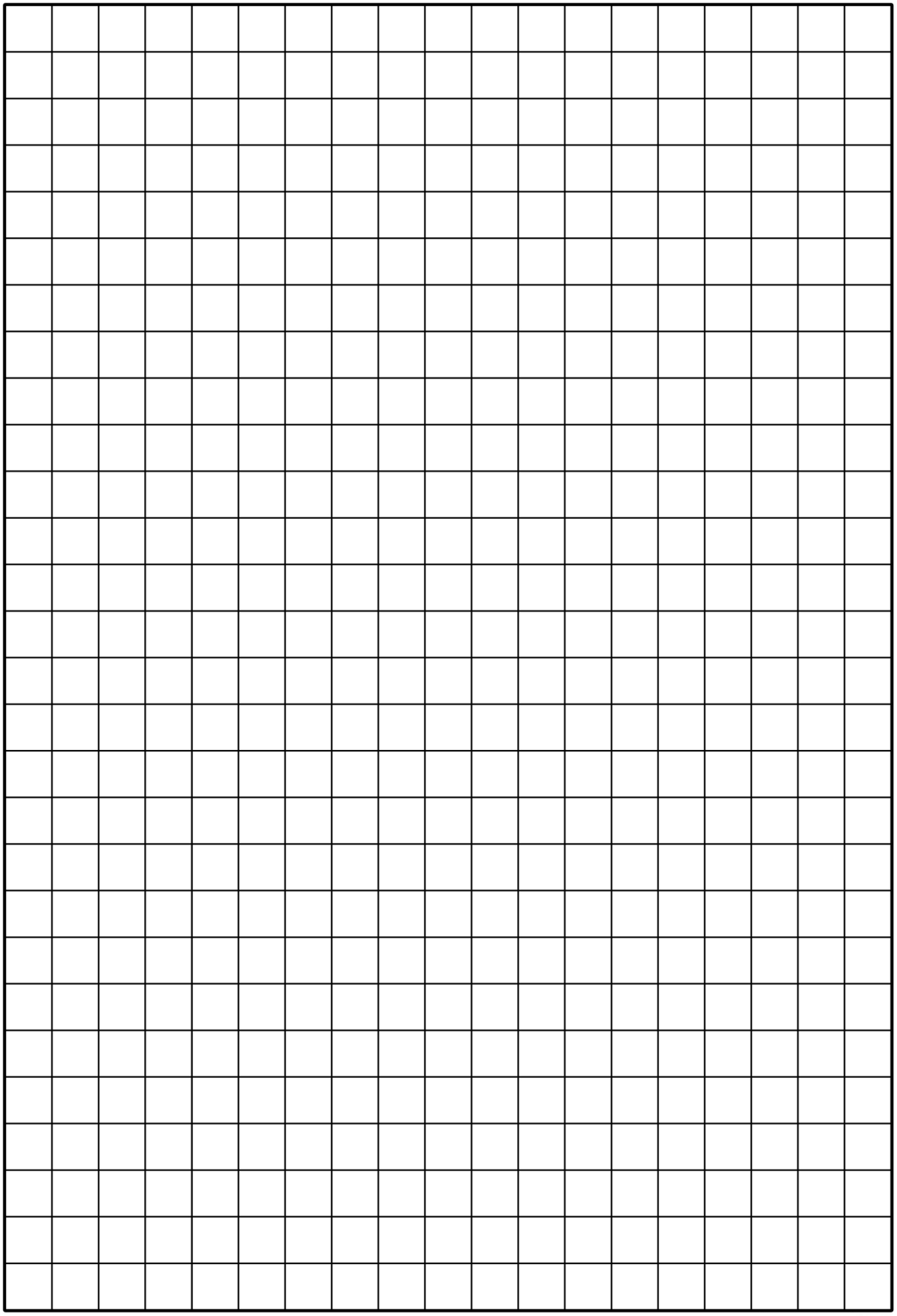
Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.2		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	0		ns
t_{DO}	Output Delay After CLKOUT[1]		6	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

ACCESSORIES - PROTOTYPE BOARD





CORE-2



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