IOS-330
16-Bit High-Density Analog Input Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The I/O Server Module (IOS) Series IOS-330 module is a precision 16-bit, high density, single size IOS, with the capability to monitor 16 differential or 32 single-ended analog input channels. The IOS-330 utilizes state of the art Surface Mounted Technology (SMT) to achieve its high channel density. Four units may be mounted on a carrier board to provide up to 64 differential or 128 single-ended analog input channels per 6U-VMEbus system slot or ISA bus (PC/AT) system slot. The IOS-330 offers a variety of features which make it an ideal choice for many industrial and scientific applications as described below.

Important Note: The following IOS model are accessories to the IOS Server Models: IOS-7200, IOS-7200-WIN, IOS-7400, and IOS-7400-WIN; which are cULus Listed. This equipment is suitable for use in Class I, Division 2, Groups A, B, C, and D or non-hazardous locations only.

Model	Operating Temperature Range
IOS-330	-40 to 85°C

KEY IOS-330 FEATURES

- **A/D 16-Bit Resolution** - 16-bit capacitor-based successive approximation Analog to Digital Converter (ADC) with integral sample and hold and reference.
- **5 μsec Conversion Time** - A maximum conversion rate of 200 kHz is supported. Maximum recommended conversion rate for specified accuracies is 67 kHz.
- **High Density** - Monitors up to 16 differential or 32 single-ended analog inputs (acquisition mode and channels are selected via programmable control registers).
- **Individual Channel Mailbox -** Two storage buffer registers are available for each of the 16 differential channels. If configured for 32 single-ended channels, one storage buffer register is available for each of the 32 channels.
- **Interrupt Upon Conversion Complete Mode** - May be programmed to interrupt upon completion of conversion for each individual channel or upon completion of conversion of the group of all scanned channels.
- **Programmable Control of Channel Scanning** - Scan all channels or a subset of the channels to allow an overall higher sample rate. The channels digitized include all sequential channels beginning with a specified start-channel value and ending with a specified end-channel value.
- **User Programmable Interval Timer** - Controls the delay between each channel converted when Uniform-Continuous or Single Scan modes are selected. If Burst-Continuous is selected, the Interval Timer controls the delay after a group of channels are converted before conversion is initiated on the group again. Supports a minimum interval of 5 μsec and a maximum interval of 2.09 seconds.

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- **Uniform Continuous Scanning Mode** - All channels selected for scanning are continually digitized in a round robin fashion with the interval between conversions controlled by the programmed interval timer. The results of each conversion are stored in the channel's corresponding Mailbox buffer. Scanning is initiated by a software or external trigger. Scanning is stopped by software control.
- **Burst Continuous Scanning Mode** - All selected input scan channels are sequentially digitized at a 67 kHz conversion rate (15 μsec conversion times). At the end of a programmed interval time a new conversion of all channels is re-initiated. The conversion results are stored in each channel's Mailbox buffer. This mode can be used as a pseudo-simultaneous sampling mode for low to medium speed applications requiring simultaneous channel acquisition. For example, if four channels are selected then they could be pseudo-simultaneously converted every 60 μsec (each of the channels actually takes 15 μsec). This is repeated in bursts determined by the programmed interval time. The scan is initiated by a software or external trigger. Scanning is stopped by software control.
- **Uniform Single Cycle Scan Mode** - All channels selected for scanning are digitized once with the idle time between each channel conversion controlled by the programmed interval timer. The scan is initiated by a software or external trigger.
- **Burst Single Cycle Scan Mode** - All channels selected for scanning are digitized once at a 66.7 kHz conversion rate (15 μsec/Channel). The scan is initiated by a software or external trigger.
- **External Trigger Scan Mode** - A single channel is digitized with each external trigger. Successive channels are digitized in sequential order with each new external trigger. This mode allows synchronization of conversions with external events that are often asynchronous.
- **External Trigger Output** - The external trigger is assigned to a field I/O line. This external trigger may be configured as an output signal to provide a means to synchronize other IOS-330's or devices to a single IOS-330's on board timer reference.
- **User Programmable Gain Amplifier** - Provides independently software controlled gains (1, 2, 4, and 8 V/V) for each of the 16 differential or 32 single-ended channels.
- **Precision On Board Calibration Voltages** - Calibration autozero and autospan precision voltages are available to permit host computer correction of conversion errors. Trimmed calibration voltages include: 0 V (local analog ground), 0.6125 V, 1.225 V, 2.45 V, and 4.9 V.
- **Hardware DIP Switch For Selection of A/D Ranges** - Both bipolar (±5 V, ±10 V) and unipolar (0 to 5 V and 0 to 10 V) ranges are available. Selected range applies to all channels and can not be individually selected on a per channel basis.
- **New Data Register** - This register can be polled, to indicate when new digitized data is available in the Mailbox. A set bit indicates a new digitized data value is available in the bit's corresponding Mailbox register. Register bits are cleared upon read of their corresponding Mailbox register or start of a new scan cycle.
- **Missed Data Register** - A set bit in the Missed Data Register indicates that the last digitized value was not read by the host computer quickly enough and has been overwritten by a new conversion. The Missed Data Register has a bit corresponding to each of the 16 differential or 32 single-ended channels. Each Missed Data Register bit is cleared by a read of its corresponding Mailbox data value or start of a new scan cycle.
- **User Programmable Data Output Format** - Software control provides selection of straight binary or binary two's complement data output format.
- **Hardware Jumpers For Selection of Internal or External Supply** - Hardware jumper provide a means to select internal ±12 volts or external ±15 volt supplies. External supplies are required when using inputs exceeding ±8.5 volts.
- **Fault Protected Input Channels** - Analog input overvoltage protection from -35 V to +55 V is provided in the event of power loss or power off.
- **Conduction Cooled Module** - I/O modules employ advanced thermal technologies. A thermal pad and module cover wicks heat away from the module and transfers the energy to a heat spreading friction plate. Heat moves to the enclosure walls where it is dissipated by the external cooling fins.

I/O SERVER MODULE SOFTWARE LIBRARY

IOS MODULE Win32 DRIVER SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows Embedded Standard applications interfacing with I/O Server Modules installed on Acromag Industrial I/O Server systems. This software (Model IOSSW-DEV-WIN) consists of a low-level driver and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic.NET, Borland C++ Builder and others. The DLL functions provide a high-level interface to the IOS carrier and modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IOS MODULE LINUX SOFTWARE

Acromag provides a software product (sold separately) consisting of Linux® software. This software (Model IOSSW-API-LNX) is composed of Linux libraries designed to support applications accessing I/O Server Modules installed on Acromag Industrial I/O Server systems. The software is implemented as a library of "C" functions which link with existing user code.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

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This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. All possible DIP switch and jumper settings will be discussed in the following sections. The DIP switch and jumper locations are shown in the *Drawings* Section.

Remove power from the board when configuring hardware jumpers, installing IOS modules, cables, termination panels, and field wiring. Refer to IOS-330 Jumper Location in the *Drawing* section and the following paragraphs for configuration and assembly instructions.

Default Hardware Jumper Configuration

When the board is shipped from the factory, it is configured as follows:

- Analog input range is configured for a bipolar input with a 10 volt span (i.e. an ADC input range of -5 to +5 Volts).
- Internal +12 and -12 Volt power supplies are used (sourced from P1 connector).
- The default programmable software control register bits at power-up are described in section 3. The control registers must be programmed to the desired gain, mode, and channel configuration before starting ADC analog input acquisition.

Analog Input Range Hardware Jumper Configuration

Power should be removed from the board when installing IOS modules, cables, termination panels, and field wiring. Refer to the *Drawings* Section of this manual and the following discussion for configuration and assembly instructions.

Table 2.1:Analog Input Range Selections/DIP Switch Settings

Desired ADC Input Range* (VDC)	Required Input Span (Volts)	Required Input Type	Switch Settings ON	Switch Settings OFF
-5 to +5	10	Bipolar	1,3,4,9	2,5,6,7,8
-10 to +10**	20	Bipolar	2,5,6,9	1,3,4,7,8
0 to +5	5	Unipolar	1,3,5,8	2,4,6,7,9
0 to +10**	10	Unipolar	1,3,4,7	2,5,6,8,9

* Assuming a gain of 1.
** These ranges can only be achieved with ±15V external power supplies. The input ranges will be clipped if ±12V supplies are used, typically to ±9.8 V maximum inputs.

Power Supply Hardware Jumper Configuration

The selection of internal or external analog power supplies is accomplished via hardware jumpers J1 and J2. J1 (J2) controls the selection of either the internal +12 (-12) Volt supply sourced from P1 connector, or the external +15 (-15) Volt supply sourced from the P2 connector. The configuration of the jumpers for the different supplies is shown in Table 2.2. "IN" means that the pins are shorted together with a shorting clip. "OUT" means that the clip has been removed. The jumper locations are shown in IOS-330 Jumper Location in the *Drawing* Section.

Table 2.2: Power Supply Selections (Pins of J1 and J2)

Power Supply Selection*	J1 (1&2)	J1 (2&3)	J2 (1&2)	J2 (2&3)
±12 Volt (Internal, P1)	OUT	IN	OUT	IN
±15 Volt (External, P2)	IN	OUT	IN	OUT

* Internal and external supplies should not be mixed (e.g. do not use +12 Volts with -15 Volts).

Software Configuration

Software configurable control registers are provided for control of external trigger mode, data output format, acquisition mode, timer control, interrupt mode, convert channel(s) selection, and channel gain selection. No hardware jumpers are required for control of these functions. These control registers must also be configured as desired before starting ADC analog input acquisition. Refer to section 3 for programming details.

CONNECTORS

IOS Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IOS modules to the carrier board. P2 is a 50-pin female receptacle header which mates to the male connector of the carrier board. This provides excellent connection integrity and utilizes gold-plating in the mating area. The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IOS model (see Table 2.3) and correspond to the pin numbers of the field I/O interface connector on the IOS carrier board. When reading Table 2.3, note that channel designators are abbreviated to save space. For example, single ended channel 0 is abbreviated as “S00”; the +input for differential channel 0 is abbreviated as “D00+”. Both of these labels are attached to pin 1, but only one is active for a particular installation (i.e. if your inputs are applied differentially, which is recommended for the lowest noise and best accuracy, follow the differential channel labeling for each channel’s + and - input leads).

> IMPORTANT: All unused analog input pins should be tied to analog ground. Floating unused inputs can drift outside the input range causing temporary saturation of the input analog circuits. Recovery from saturation is slow and affects the reading of the desired channels.

Table 2.3: IOS-330 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
S00,D00+	1	S24,D08-	26
S16,D00-	2	COMMON	27
COMMON	3	S09,D09+	28
S01,D01+	4	S25,D09-	29
S17,D01-	5	COMMON	30
COMMON	6	S10,D10+	31
S02,D02+	7	S26,D10-	32
S18,D02-	8	COMMON	33
COMMON	9	S11,D11+	34
S03,D03+	10	S27,D11-	35
S19,D03-	11	COMMON	36
COMMON	12	S12,D12+	37
S04,D04+	13	S28,D12-	38
S20,D04-	14	COMMON	39
COMMON	15	S13,D13+	40
S05,D05+	16	S29,D13-	41
S21,D05-	17	SENSE	42
COMMON	18	S14,D14+	43
S06,D06+	19	S30,D14-	44
S22,D06-	20	+15 VOLTS	45
COMMON	21	S15,D15+	46
S07,D07+	22	S31,D15-	47
S23,D07-	23	-15 VOLTS	48
COMMON	24	EXT TRIGGER*	49
S08,D08+	25	SHIELD	50

***** Indicates that the signal is active low.
Sense is the common ground for all single ended inputs.

Analog Inputs: Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating. It must be referenced to analog common on the IOS module and be within the normal input voltage range.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references and when minimizing noise and maximizing accuracy are key concerns. See Analog Input Connection in the *Drawing* Section for analog input connections for differential and single-ended inputs. Shielded cable of the shortest length possible is also strongly recommended.

Single-ended inputs only require a single lead (+) per channel, with a shared "sense" (reference) lead for all channels, and can be used when a large number of input channels come from the same location (e.g. printed circuit board). The channel density doubles when using single-ended inputs, and this a powerful incentive for their use. However, caution must be exercised since the single "sense" lead references all channels to the same common which will induce noise and offset to the degree they are different.

The IOS-330 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed. Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IOS-330 input module.

External Trigger Input/Output

The external trigger signal on pin 49 of the P2 connector can be programmed to input a TTL compatible external trigger signal, or output IOS-330 hardware generated triggers to allow synchronization of multiple IOS-330s.

As an input, the external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The external trigger signal is an active low edge sensitive signal. That is, the external trigger signal will trigger the IOS-330 hardware on the falling edge. Once the external trigger signal has been driven low, it should remain low for a minimum of 500n seconds.

As an output an active-low TTL signal can be driven to additional IOS-330s, thus providing a means to synchronize the conversions of multiple IOS-330s. The additional IOS-330s must program their external trigger for signal input and convert on external trigger only mode. See section 3.0 for programming details to make use of this signal.

3.0 PROGRAMMING INFORMATION

IOS IDENTIFICATION PROM - (Read Only, 32 Even-Byte Addresses)

Each IOS module contains identification (ID) information that resides in the ID space.. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IOS" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IOS-330 ID information does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the even addresses in a 64 byte block. The IOS-330 ID space contents are shown in Table 3.1. Note that the base-address for the IOS module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID space. Execution of an ID space read requires 1 wait state.

Table 3.1: IOS-330 ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	Numeric Value (Hex)	Field Description
00	49	
02	50	
04	41	
06	43	
08	A3	Acromag ID Code
0A	11	IOS Model Code[1]
0C	00	Not Used (Revision)
0E	00	Reserved
10	00	Not Used
12	00	Not Used
14	0C	Total Number of ID PROM Bytes
16	5A	CRC
18 to 3E	00	Not Used

Notes (Table 3.1):

1. The IOS model number is represented by a two-digit code within the ID space (the IOS-330 model is represented by 11 Hex).

I/O SPACE ADDRESS MAP

This board is addressable in the I/O Server Module space to control the acquisition of analog inputs from the field. As such, three types of information are stored in the I/O space: control, status, and data.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1 to A6, but the IOS-330 uses only a portion of this space. The I/O space address map for the IOS-330 is shown in Table 3.2. Note that the base address for the IOS module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. Both 16 and 8-bit accesses to the registers in the I/O space are permitted.

Table 3.2: IOS-330 I/O Space Address (Hex) Memory Map[2]

Base Addr+	MSB D15 D08	LSB D07 D00	Base Addr+
01	Control Register		00
03	Timer Prescaler	Interrupt Vector	02
05	Conversion Timer		04
07	End Channel Value	Start Channel Value	06
09	New Data Register Channels 0 to 15		08
0B	New Data Register Channels 16 to 31		0A
0D	Missed Data Register Channels 0 to 15		0C
0F	Missed Data Register Channels 16 to 31		0E
11	Not Used Bits15 to Bit 01	Start Convert Bit-0	10
13	Not Used[1]	Trigger Mask Reg[4]	12
	Not Used[1]		
	↓		
1F	Not Used[1]		1E
21	Gain Select Ch 01	Gain Select Ch 00	20
23	Gain Select Ch 03	Gain Select Ch 02	22
25	Gain Select Ch 05	Gain Select Ch 04	24
27	Gain Select Ch 07	Gain Select Ch 06	26
29	Gain Select Ch 09	Gain Select Ch 08	28
2B	Gain Select Ch 11	Gain Select Ch 10	2A
2D	Gain Select Ch 13	Gain Select Ch 12	2C
2F	Gain Select Ch 15	Gain Select Ch 14	2E
31	Gain Select Ch 17	Gain Select Ch 16	30
33	Gain Select Ch 19	Gain Select Ch 18	32
35	Gain Select Ch 21	Gain Select Ch 20	34
37	Gain Select Ch 23	Gain Select Ch 22	36
39	Gain Select Ch 25	Gain Select Ch 24	38
3B	Gain Select Ch 27	Gain Select Ch 26	3A
3D	Gain Select Ch 29	Gain Select Ch 28	3C
3F	Gain Select Ch 31	Gain Select Ch 30	3E
41	Mailbox Ch 00 (SE or Diff. Mode)[3]		40
43	Mailbox Ch 01 (SE or Diff. Mode)		42
45	Mailbox Ch 02 (SE or Diff. Mode)		44
47	Mailbox Ch 03 (SE or Diff. Mode)		46
49	Mailbox Ch 04 (SE or Diff. Mode)		48
4B	Mailbox Ch 05 (SE or Diff. Mode)		4A
4D	Mailbox Ch 06 (SE or Diff. Mode)		4C
4F	Mailbox Ch 07 (SE or Diff. Mode)		4E
51	Mailbox Ch 08 (SE or Diff. Mode)		50
53	Mailbox Ch 09 (SE or Diff. Mode)		52
55	Mailbox Ch 10 (SE or Diff. Mode)		54
57	Mailbox Ch 11 (SE or Diff. Mode)		56
59	Mailbox Ch 12 (SE or Diff. Mode)		58
5B	Mailbox Ch 13 (SE or Diff. Mode)		5A
5D	Mailbox Ch 14 (SE or Diff. Mode)		5C
5F	Mailbox Ch 15 (SE or Diff. Mode)		5E
61	Mailbox Ch 16 SE (Ch 00 Diff. Mode)[3]		60
63	Mailbox Ch 17 SE (Ch 01 Diff. Mode)		62
65	Mailbox Ch 18 SE (Ch 02 Diff. Mode)		64
67	Mailbox Ch 19 SE (Ch 03 Diff. Mode)		66
69	Mailbox Ch 20 SE (Ch 04 Diff. Mode)		68
6B	Mailbox Ch 21 SE (Ch 05 Diff. Mode)		6A
6D	Mailbox Ch 22 SE (Ch 06 Diff. Mode)		6C
6F	Mailbox Ch 23 SE (Ch 07 Diff. Mode)		6E
71	Mailbox Ch 24 SE (Ch 08 Diff. Mode)		70
73	Mailbox Ch 25 SE (Ch 09 Diff. Mode)		72
75	Mailbox Ch 26 SE (Ch 10 Diff. Mode)		74
77	Mailbox Ch 27 SE (Ch 11 Diff. Mode)		76
79	Mailbox Ch 28 SE (Ch 12 Diff. Mode)		78
7B	Mailbox Ch 29 SE (Ch 13 Diff. Mode)		7A
7D	Mailbox Ch 30 SE (Ch 14 Diff. Mode)		7C
7F	Mailbox Ch 31 SE (Ch 15 Diff. Mode)		7E

Notes (Table 3.2):

1. All addresses that are "Not Used" will read as logic low.
2. All Reads and writes are 1 wait state (except a Mailbox read issued simultaneously with an ongoing hardware write of a new convert value. In this case a read cycle will include from 1 to 6 wait states).
3. The Mailbox is one level deep when using single ended channels; it is two levels deep with differential mode.
4. The trigger mask register is only available in Revision B product or later. Contact factory for further details.

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Control Register, (Read/Write) - (Base + 00H)

This read/write register is used to: select the output data format, select the external trigger signal as an input or output, select acquisition input mode, select scan mode, enable/disable the timer, and select the interrupt mode.

The function of each of the control register bits are described in Table 3.3. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or system reset sets all control register bits to 0.

Table 3.3: Control Register

BIT	FUNCTION
0	Not Used[1]
1	Output Data Format 0 = Binary Two's Complement 1 = Straight Binary See Tables 3.4 and 3.5 for a description of these two data formats.
2	External Trigger 0 = Input 1 = Output It is possible to synchronize the data acquisition of multiple IOS-330 modules. A single master IOS-330 module must be selected to output the external trigger signal while all other IOS-330 modules are selected to input the external trigger signal. The external trigger signal (pin 49 of the field I/O connector) must also be wired together.
5,4,3	Acquisition Input Mode 000 = All Channels Differential Input 001 = All Channels Single Ended Input 010 = Not Used 011 = 4.9000v Calibration Voltage Input 100 = 2.4500v Calibration Voltage Input 101 = 1.2250v Calibration Voltage Input 110 = 0.6125v Calibration Voltage Input 111 = Auto Zero Calibration Voltage Input
7,6	Not Used[1]
10,9,8	Scan Mode 000 = Disable 001 = Uniform Continuous 010 = Uniform Single 011 = Burst Continuous 100 = Burst Single 101 = Convert on External Trigger Only 110 = Not Used 111 = Not Used See the Modes of Operation section for a description of each of these scan modes.
11	Timer Enable 0 = Disable 1 = Enable
13,12	Interrupt Control 00 = Disable Interrupts 01 = Interrupt After Convert of Each Channel 10 = Interrupt After Conversion of all selected channels is completed. A group of channels includes all channels from the Start Channel up to and including the End Channel value. 11 = Disable Interrupts
14,15	Not Used[1]

Notes (Table 3.3):

1. All bits labeled "Not Used" will return on a read access the last value written.

Analog Input Ranges and Corresponding Digital Output Code

Selection of an analog input range is implemented via the DIP switch setting given in Table 2.1. The ideal input voltage corresponding to each of the supported input ranges is given in Table 3.4. Then in Table 3.5 the digital output code corresponding to each of the given ideal analog input values is given in both binary two's complement and straight binary formats.

Table 3.4: Supported Full-Scale Ranges and Ideal Analog Input

DESCRIPTION	ANALOG INPUT			
Input Range	±10V	0 to 10V	±5V	0 to 5V
LSB (Least Significant Bit) Weight	305 µV	153 µV	153 µV	76 µV
+ Full Scale Minus One LSB	9.999695 Volts	9.999847 Volts	4.999847 Volts	4.999924 Volts
Midscale	0 V	5 V	0 V	2.5 V
One LSB Below Midscale	-305 µV	4.999847 Volts	-153 µV	2.499924 Volts
- Full Scale	-10 V	0 V	-5 V	0 V

The digital output format is controlled by bit-1 of the Control register. The two formats supported are Binary Two's Complement and Straight Binary. The hex codes corresponding to these two data formats are depicted in Table 3.5.

Table 3.5: Digital Output Codes and Input Voltages

	DIGITAL OUTPUT	
DESCRIPTION	**Binary 2's Comp** (Hex Code)	**Straight Binary** (Hex Code)
+ Full Scale - 1 LSB	7FFF	FFFF
Midscale	0000	8000
1 LSB Below Midscale	FFFF	7FFF
- Full Scale	8000	0000

Interrupt Vector Register (Read/Write, 02H)

The Vector Register can be written with an 8-bit interrupt vector. This vector is provided to the carrier and system bus upon an active INTSEL* cycle. Read or writing to this register is possible via 16-bit or 8-bit data transfers. 16-bit data transfers will implement simultaneous access the Interrupt Vector and Timer Prescaler registers. The register contents are cleared upon reset.

Interrupt Vector Register							
MSB							LSB
07	06	05	04	03	02	01	00

Interrupts are released on an interrupt acknowledge cycle. Read of the interrupt vector during an interrupt acknowledge cycle signals the IOS-330 to remove its interrupt request.

Timer Prescaler Register (Read/Write, 03H)

The Timer Prescaler register can be written with an 8-bit value to control the interval time between conversions.

Timer Prescaler Register							
MSB							LSB
15	14	13	12	11	10	09	08

This 8-bit number divides an 8 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions.

The Timer Prescaler has a minimum allowed value restriction of 28 hex or 40 decimal. A Timer Prescaler value of less then 40 (decimal) will result in an empty Mailbox Register buffer. This minimum value corresponds to a conversion interval of 5 μsec which translates to the maximum conversion rate of 200 KHz. Although the board will operate at the 200 KHz conversion rate, conversion accuracy will be sacrificed.

The formula used to calculate and determine the desired Timer Prescaler value is given in the Conversion Timer section which immediately follows this section.

Read or writing to this register is possible via 16-bit or 8-bit data transfers. A 16-bit data transfer will implement simultaneous access to the Interrupt Vector and Timer Prescaler registers. The Timer Prescaler register contents are cleared upon reset.

Conversion Timer Register (Read/Write, 04H)

The Conversion Timer Register can be written to control the interval time between conversions. Read or writing to this register is possible with either 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

Conversion Timer Register	
MSB	LSB
15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00

This 16-bit number is the second divisor of an 8 MHz. clock signal and is used together with the Timer Prescaler Register to derive the frequency of periodic triggers for precisely timed intervals between conversions.

The interval time between conversion triggers is generated by cascading two counters. The first counter, the Timer Prescaler, is clocked by an 8 MHz. clock signal. The output of this clock is input to the second counter, the Conversion Timer, and the output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$\frac{\text{TimerPrescaler} * \text{ConversionTimer}}{8} = \text{T in } \mu\text{sec}$$

Where: **T** = time period between trigger pulses in microseconds.
Timer Prescaler can be any value between 40 and 255 decimal.
Conversion Timer can be any value between 1 and 65,535 decimal.

The maximum period of time which can be programmed to occur between conversions is (255 ∗ 65,535) ÷ 8 = 2.0889 seconds. The minimum time interval which can be programmed to occur is
(40 ∗ 1) ÷ 8 = 8 μsec. This minimum of 8 μsec is defined by the minimum conversion time of the hardware but does sacrifice conversion accuracy. To achieve specified conversion accuracy a minimum conversion time of 15 μsec is recommended (see the specification chapter for details regarding accuracy).

Start Channel Value Register (Read/Write, 06H)

The Start Channel Value register can be written with a 5-bit value to select the first channel that is to be converted once conversions have been triggered. All channels between the start and end channel values are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The Start Channel Value register can be read or written with 8-bit data transfers. In addition, the Start Channel Value register can be simultaneously accessed with the End Channel Value via a 16-bit data transfer. The unused bits are zero when read. The register contents are cleared upon reset.

Start Channel Value Register					
Unused	Start Channel Value				
07 06 05	04	03	02	01	00

After running data conversions are halted, the internal hardware pointers are reinitialized to the start channel value. Thus when conversions are started again, the first channel converted is defined by the Start Channel Value register.

End Channel Value Register (Read/Write, 07H)

The End Channel Value register can be written with a 5-bit value to indicate the last channel in a sequence to be converted. When scanning, all channels between and including the start and end channels are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The End Channel Value register can be read or written with 8-bit data transfers. In addition, the End Channel Value register can be simultaneously accessed with the Start Channel Value with a 16-bit data transfer. The unused data bits are zero when read. The register contents are cleared upon reset.

End Channel Value Register					
Unused	End Channel Value				
15 14 13	12	11	10	09	08

New Data Registers (Read Only, 08H to 0BH)

The New Data registers can be read to determine which channels of the Mailbox buffer contain new converted data. A set bit in the New Data register indicates that the Mailbox buffer, corresponding to the channel of the set bit, contains new converted data. A set New Data register bit is cleared upon a read of its corresponding Mailbox buffer.

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The New Data bits are also cleared at the start of all new data acquisition cycles initiated with either the Software Start Convert command or an external trigger. This is done to avoid mistaking data from an old scan cycle with that of a new scan cycle.

The New Data registers can be read via 16-bit or 8-bit data transfers. In addition, the register contents are cleared upon reset.

New Data Register (Read Only, 08H)								
Data Bit	07	06	05	04	03	02	01	00
SE or Diff. Ch. l	07	06	05	04	03	02	01	00
New Data Register (Read Only 09H)								
Data Bit	15	14	13	12	11	10	09	08
SE or Diff. Ch.	15	14	13	12	11	10	09	08
New Data Register (Read Only 0AH)								
Data Bit	07	06	05	04	03	02	01	00
SE Channel	23	22	21	20	19	18	17	16
Diff. Channel	07	06	05	04	03	02	01	00
New Data Register (Read Only 0BH)								
Data Bit	15	14	13	12	11	10	09	08
SE Channel	31	30	29	28	27	26	25	24
Diff. Channel	15	14	13	12	11	10	09	08

Missed Data Registers (Read Only, 0CH to 0FH)

The Missed Data registers can be read to determine if a channel's Mailbox buffer has been overwritten with new converted data before the last converted value was read. A set bit in the Missed Data register indicates a converted value corresponding to the channel of the set bit was overwritten before being read. A set Missed Data register bit is cleared upon a read of its corresponding Mailbox buffer.

The Missed Data bits are also cleared at the start of all new data acquisition cycles initiated with either the Software Start Convert command or an external trigger. This is done to avoid mistaking missed data from an old scan cycle with that of a new scan cycle.

The Missed Data registers can be read via 16-bit or 8-bit data transfers. In addition, the register contents are cleared upon reset.

Missed Data Register (Read Only, 0CH)								
Data Bit	07	06	05	04	03	02	01	00
SE or Diff. Ch.	07	06	05	04	03	02	01	00
Missed Data Register (Read Only 0DH)								
Data Bit	15	14	13	12	11	10	09	08
SE or Diff. Ch.	15	14	13	12	11	10	09	08

Missed Data Register (Read Only 0EH)								
Data Bit	07	06	05	04	03	02	01	00
SE Channel	23	22	21	20	19	18	17	16
Diff. Channel	07	06	05	04	03	02	01	00
Missed Data Register (Read Only 0FH)								
Data Bit	15	14	13	12	11	10	09	08
SE Channel	31	30	29	28	27	26	25	24
Diff. Channel	15	14	13	12	11	10	09	08

Start Convert Register (Write Only, 10H)

The Start Convert register is a write-only register and is used to trigger conversions by setting data bit-0 of this register to a logic one. The desired mode of data acquisition must first be configured by setting the following registers to the desired values and modes: Control, Interrupt Vector, Timer Prescaler, Conversion Timer, Start Channel Value, End Channel Value, and Gain Select.

This register can be written with either a 16-bit or 8-bit data value. Data bit-0 must be a logic one to initiate data conversions.

For the External Trigger Only mode the Software Start Convert bit is not used to start data acquisition. However, the Start Convert bit should be set prior to the first external trigger. In this mode the Start Convert bit serves as a means for the hardware to identify the occurrence of the first External Trigger. On the first external trigger (given the Software Start Convert bit is set) converted data from the A/D Converter is not written to the Mailbox buffer since it is old convert data. See the Convert On External Trigger Only-Mode (in the Modes of Operation section) for additional details.

Start Convert Register							
Not Used							Start Convert
07	06	05	04	03	02	01	00

At least 5 μsec of data acquire time should be provided after programming of the Control register, Start Value register, and Gain Selects before a Software Start Convert command is issued. These configuration registers control the IOS-330 on board multiplexers and programmable gain amplifier which, respectively, control the channel and gain selected for the input provided to the converter.

Trigger Mask Register (Read/Write Only, 12H)

The Trigger Mask register can be used to temporarily disable external triggers when they are enable via bit 2 of the Control Register. When bit 0 of this register is set to a logic low (default), then the external triggers are enabled. If bit 0 of this register is set to a logic high, then the external triggers are disabled. This register can be written with either a 16-bit or 8-bit data value.

BIT	FUNCTION
0	External Trigger Mask 0 = ENABLE external triggers (default) 1 = DISABLE external triggers
7-1	Not Used. Will always read logic low.

Gain Select Registers (Read/Write, 20H - 3FH)

The Gain Select registers are readable/writeable and are used to individually select the gain corresponding to each of the 32 channels. See Table 3.2 which lists the Gain Select register addresses corresponding to each of the 32 channels. In differential mode, Gain Select registers corresponding to channels 0 to 15 are utilized.

The four gain settings supported (1, 2, 4, and 8) are listed in Table 3.6 with their correspond binary select code. A gain can be selected by writing the desired binary code to the least significant two bits of a given Gain Select register.

Table 3.6: Gain Select Binary Codes

Gain	Data Bits 7 to 2	Data Bit 1	Data Bit 0
1	Unused	0	0
2	Unused	0	1
4	Unused	1	0
8	Unused	1	1

The Gain Select register contents are set to "00" upon power up or system reset. The Gain Select registers corresponding to all channels selected for conversion must be written with the desired gain select binary codes prior to initializing data conversions. This register can be written with either a 16-bit or 8-bit data value.

Mailbox Buffer (Read Only, 40H - 7EH)

The Mailbox Buffer is read-only, and contains 16-bit digitized input channel values. The Mailbox Buffer has 32 storage locations-one for each of the 32 channels supported by the IOS-330 in the single ended mode of operation. If the IOS-330 is used in the differential mode of operation each of the 16 channels supported are allocated two Mailbox Buffer locations.

See Table 3.2 which gives the Mailbox Buffer address locations corresponding to each of the 32 channels (or 16 channels in differential mode). In differential mode the first digitized data values will be stored in buffer locations 40H to 5FH while the second digitized values are stored in buffer locations 60H to 7EH. The storage of data in the Mailbox, in differential mode, will continue to alternate between these two Mailbox sections.

The New Data register can be read to determine which Mailbox Buffers contain updated digitized data. A set bit in the New Data register indicates an updated digitized data value resides in its corresponding Mailbox Buffer. In addition, the Missed Data register can be read to determine if a Mailbox Buffer has been overwritten with a new digitized value before the previous one had been read. A set bit in the Missed Data register indicates that a digitized data value has been lost or overwritten.

All register accesses to the IOS-330 require one wait state with the exception of a read access to the Mailbox Buffer. A read access to the Mailbox Buffer could take up to six wait states if a read is issued while a hardware write of channel data to the same Mailbox is currently underway. Most of the time, contention with hardware writes is not an issue. In which case, one wait state is required for a read access to the Mailbox.

MODES OF OPERATION

The IOS-330 provides five different modes of analog input acquisition to give the user maximum flexibility for each application. These modes of operation include: uniform continuous, uniform single, burst continuous, burst single, and convert on external trigger only. In all modes a single channel or a sequence of channels may be converted. The following sections describe the features of each and how to best use them.

Uniform Continuous-Mode

In uniform continuous mode of operation, conversions are performed continuously (in sequential order) for all channels between and including the Start and End Channel Values. The interval between conversions is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used, bit-2 of the Control register must be set low to accept the external trigger as an input signal.

Stopping the execution of uniform continuous conversions is possible by writing 000 to the Scan Mode bits (8-10) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register board address location.

When configured for differential input, the Mailbox functions as a dual level data buffer. The first half of the Mailbox is used to store all selected channel data for the initial pass through the channels defined by the Start and End Value registers. The second half of the Mailbox is then used to store the channel data corresponding to the second pass though all selected channels. Storage of channel data continues to alternate between the first and second halves of the Mailbox Buffer. As seen in Table 3.2, the first half of the Mailbox is defined by word addresses 40H to 5EH while the second half is defined by word addresses 60H to 7EH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 8 μsec after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 8 μsec after the interval time of the last selected channel has expired.

If interrupts are selected to go active after conversion of each channel be sure to program a large enough interval between conversions to allow adequate time for execution of an interrupt service routine. It may also be necessary to allow time for your computer to perform other housekeeping operations between servicing interrupts.

Uniform Single-Mode

In uniform single mode of operation, conversions are performed once (in sequential order) for all channels between and including the Start and End Channel Values. The interval between conversions is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used, bit-2 of the Control register must be set low to accept the external trigger as an input signal.

When configured for differential input, the Mailbox functions as a dual level data buffer. However, for Uniform Single Mode, only one pass from the start channel to the end channel is implemented. Thus, only the first half of the Mailbox buffer is utilized. As seen in Table 3.2, the first half of the Mailbox is defined by word addresses 40H to 5EH

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 8 µsec after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 5 µsec after the interval time of the last selected channel has expired.

Burst Continuous-Mode

In burst continuous mode of operation, conversions are continuously performed in sequential order from the channel defined by the Start Channel Value to the channel defined by the End Channel Value. Within a group of channels, the interval between conversions is fixed at 15 µsec. However the interval after conversion of a group of channels can be controlled by the interval timer (Timer Prescaler and Conversion Timer).

Burst modes can be used to provide pseudo-simultaneous sampling for many low to medium speed applications requiring simultaneous channel acquisition. The 15 µsec between conversion of each channel can essentially be considered simultaneous sampling for low to medium frequency applications.

After software selection of the burst continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used, bit-2 of the Control register must be set low to accept the external trigger as an input signal.

Stopping the execution of burst continuous conversions is accomplished by writing 000 to the Scan Mode bits (8-10) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register board address location.

When configured for differential input, the Mailbox functions as a dual level data buffer. The first half of the Mailbox is used to store all selected channel data for the initial pass through the channels defined by the Start and End Value registers. The second half of the Mailbox is then used to store the channel data corresponding to the second pass though all selected channels. Storage of channel data continues to alternate between the first and second halves of the Mailbox Buffer. As seen in Table 3.2, the first half of the Mailbox is defined by word addresses 40H to 5EH while the second half is defined by word addresses 60H to 7EH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued every 15 µsec. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 20 µsec after conversion of the last channel in the group has started.

At this time 15 µsec between interrupts is not sufficient time to perform back to back interrupt acknowledge cycles on the VME and PC platforms. Thus, interrupting after each channel is converted cannot be recommended.

Burst Single-Mode

In burst single mode of operation conversions are performed once for all channels (in sequential order) starting with Start Channel and ending with the End Channel. The interval between conversions of each channel is fixed at 15 µsec. The interval timer has no functionality in this mode of operation.

After software selection of the burst single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used, bit-2 of the Control register must be set low to accept the external trigger as an input signal.

When configured for differential input, the Mailbox functions as a dual level data buffer. However, for Burst Single Mode, only one pass from the start channel to the end channel is implemented. Thus, only the first half of the Mailbox buffer is utilized. As seen in Table 3.2, the first half of the Mailbox is defined by word addresses 40H to 5EH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, an interrupt will be issued every 15 µsec (not recommended). If interrupt upon completion of a group of channels is selected, an interrupt will be issued 20 µsec after conversion of the last channel has started.

Convert On External Trigger Only-Mode

In convert on External Trigger Only Mode of operation each conversion is initiated by an external trigger (falling edge of a logic low pulse) input to the IOS-330 on the EXT TRIGGER* signal of the P2 connector. Conversions are performed for each channel between and including the Start and End Channel Values in sequential order. The interval between conversions is controlled by the period between external triggers. The interval timer has no functionality in this mode of operation and must be disabled by setting bit-11 of the control register to logic low.

The external trigger signal must be configured as an input for this mode of operation. The external trigger can be configured as an input by setting bit-2 of the Control register low.

At least 5 µsec of data acquire time should be provided after programming of the Control register, Start Value register, and Gain Selects before the first external trigger is issued. These configuration registers control the IOS-330 on board multiplexers and programmable gain amplifier which, respectively, control the channel and gain selected for the input provided to the converter.

In the external trigger only mode, it is important to understand the sequence in which converted data is transferred from the ADC to the Mailbox Buffer. Upon an external trigger the selected analog signal is converted but remains at the ADC while the previous digitized value is output from the ADC to the Mailbox Buffer. Thus, with this sequence the Mailbox is consistently updated with the previous cycle’s converted data. In other words, new data in the Mailbox is one cycle behind the ADC. With this sequence, at the end of data conversions, one additional external trigger is required to move the data from the ADC to the Mailbox buffer. At the start of data conversion, with the first external trigger signal (given the Start Convert Bit is set), data is not input to the Mailbox buffer since the data in the ADC buffer is old convert data.

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The IOS-330 requires the setting of the Start Convert bit to logic one prior to receiving the first active external trigger pulse. This will prevent erroneous data from being written into the Mailbox Buffer corresponding to the first channel converted. This is the only mode of operation in which the Start Convert bit does not cause data conversions.

When configured for differential input, the Mailbox functions as a dual level data buffer. The first half of the Mailbox is used to store all selected channel data for the initial pass through the channels defined by the Start and End Value registers. The second half of the Mailbox is then used to store the channel data corresponding to the second pass though all selected channels. Storage of channel data continues to alternate between the first and second halves of the Mailbox Buffer. As seen in Table 3.2, the first half of the Mailbox is defined by word addresses 40H to 5EH while the second half is defined by word addresses 60H to 7EH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, an interrupt will be issued 8 μsec after a valid external trigger pulse is detected. The only exception to this is upon the very first external trigger pulse, no interrupt will be issued since data is not written to the Mailbox buffer. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 8 μsec after detection of the first external trigger following conversion of all channels in the selected group. Again, one extra external trigger is needed to complete update of the Mailbox buffer for the selected group of channels.

External Trigger Only mode of operation can be used to synchronize multiple IOS-330 modules to a single IOS-330 running in uniform continuous, uniform single, burst continuous, or burst single mode. The external trigger, of the IOS-330 running uniform or burst mode, must be programmed as an output. The external trigger signal of that IOS-330 must then be connected to the external trigger signal of all other IOS-330s that are to be synchronized. These other IOS-330s must be programmed for External Trigger Only Mode. Data conversion can then be started by writing high to the Start Convert bit of the IOS-330 configured for Uniform or Burst mode.

PROGRAMMING CONSIDERATIONS FOR ACQUIRING ANALOG INPUTS

The IOS-330 provides different methods of analog input acquisition to give the user maximum flexibility for each application. The following sections describe the features of each and how to best use them.

USE OF CALIBRATION SIGNALS

Reference signals for analog input calibration have been provided to improve the accuracy over the uncalibrated state. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Programmable Gain Amplifier (PGA) and the Analog to Digital Converter (ADC). The untrimmed PGA and ADC have significant offset and gain errors (see specifications in chapter 6) which reveal the need for software calibration.

Calibrated Performance

Very accurate calibration of the IOS-330 can be accomplished by using calibration voltages present on the board. The four voltages and the analog ground reference are used to determine two points of a straight line which defines the analog input characteristic. The calibration voltages are precisely adjusted at the factory to provide optimum performance, as detailed in chapter 6.

The calibration voltages are used with the auto zero signal to find two points that determine the straight line characteristic of the analog front end for a particular range. The recommended calibration voltage selection for each range is summarized in Table 3.7.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages and range constants.

$$\text{Corrected\_Count} = \left[\frac{65536 * \text{m}}{\text{Ideal\_Volt\_Span}}\right] * \left[\text{Count\_Actual} + \frac{(\text{Volt}_{\text{CALLO}} * \text{Gain}) - \text{Ideal\_Zero}}{\text{m}} - \text{Count}_{\text{CALLO}}\right] \quad (1)$$

Where "**m**" represents the actual slope of the transfer characteristic as defined in equation 2:

$$\text{m} = \text{Gain} * \left[\frac{\text{Volt}_{\text{CALHI}} - \text{Volt}_{\text{CALLO}}}{\text{Count}_{\text{CALHI}} - \text{Count}_{\text{CALLO}}}\right] \quad (2)$$

Gain	=	The Programmable Gain Amplifier Setting Used (See Table 3.7)
$\text{Volt}_{\text{CALHI}}$	=	High Calibration Voltage (See Table 3.7)
$\text{Volt}_{\text{CALLO}}$	=	Low Calibration Voltage (See Table 3.7)
$\text{Count}_{\text{CALHI}}$	=	Actual ADC Data Read With High Calibration Voltage Applied
$\text{Count}_{\text{CALLO}}$	=	Actual ADC Data Read With Low Calibration Voltage Applied
Ideal_Volt_Span	=	Ideal ADC Voltage Span (See Table 3.8)
Count_Actual	=	Actual Uncorrected ADC Data For Input Being Measured
Ideal_Zero	=	Ideal ADC Input For “Zero” (See Table 3.8)

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Table 3.7: Recommended Calib. Voltages For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Rec. Low Calib. Voltage "$Volt_{CALLO}$" (Volts)	Rec. High Calib. Voltage "$Volt_{CALHI}$" (Volts)
-5 to +5	1	-5 to +5	0.0000 (Auto Zero)	4.9000 (CAL0)
-2.5 to +2.5	2	-5 to +5	0.0000 (Auto Zero)	2.4500 (CAL1)
-1.25 to +1.25	4	-5 to +5	0.0000 (Auto Zero)	1.2250 (CAL2)
-0.625 to +0.625	8	-5 to +5	0.0000 (Auto Zero)	0.6125 (CAL3)
-10 to +10	1	-10 to +10	0.0000 (Auto Zero)	4.9000 (CAL0)
-5 to +5	2	-10 to +10	0.0000 (Auto Zero)	4.9000 (CAL0)
-2.5 to +2.5	4	-10 to +10	0.0000 (Auto Zero)	2.4500 (CAL1)
-1.25 to +1.25	8	10 to +10	0.0000 (Auto Zero)	1.2250 (CAL2)
0 to +5	1	0 to +5	0.6125 (CAL3)	4.9000 (CAL0)
0 to +2.5	2	0 to +5	0.6125 (CAL3)	2.4500 (CAL1)
0 to +1.25	4	0 to +5	0.6125 (CAL3)	1.2250 (CAL2)
0 to +0.625*	8	0 to +5	0.0000 (Auto Zero)*	0.6125 (CAL3)
0 to +10	1	0 to +10	0.6125 (CAL3)	4.9000 (CAL0)
0 to +5	2	0 to +10	0.6125 (CAL3)	4.9000 (CAL0)
0 to +2.5	4	0 to +10	0.6125 (CAL3)	2.4500 (CAL1)
0 to +1.25	8	0 to +10	0.6125 (CAL3)	1.2250 (CAL2)

*The hardware offset may prevent you from calibrating this range.

Table 3.8: Ideal Voltage Span and Zero For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	"Ideal_Volt _Span" (Volts)	"Ideal_ Zero" (Volts)
-5 to +5	1	-5 to +5	10.0000	-5.0000
-2.5 to +2.5	2	"	"	"
-1.25 to +1.25	4	"	"	"
-0.625 to +0.625	8	"	"	"
-10 to +10	1	-10 to +10	20.0000	-10.0000
-5 to +5	2	"	"	"
-2.5 to +2.5	4	"	"	"
-1.25 to +1.25	8	"	"	"
0 to +5	1	0 to +5	5.0000	0.0000
0 to +2.5	2	"	"	"
0 to +1.25	4	"	"	"
0 to +0.625	8	"	"	"
0 to +10	1	0 to +10	10.0000	0.0000
0 to +5	2	"	"	"
0 to +2.5	4	"	"	"
0 to +1.25	8	"	"	"

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) for each active input range should not be determined immediately after startup but after the module has reached a stable temperature and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 64) of the calibration parameters should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

Calibration Programming Example 1

Assume that the desired input range is -10 to +10 volts (select desired input range via hardware DIP switch). Channels 0 to 3 are connected differentially, and corrected input channel data is desired. From Tables 3.7 & 3.8, several calibration parameters can be determined:

Gain = 1 (From Table 3.7)
$Volt_{CALHI}$ = 4.9000 volts (CAL0; From Table 3.7)
$Volt_{CALLO}$= 0.0000 volts (Auto Zero; From Table 3.7)
Ideal_Volt_Span = 20.0000 volts (From Table 3.8)
Ideal_Zero = -10.0000 volts (From Table 3.8)

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

Determination of the $Count_{CALLO}$ Value

1. Execute Write of 043AH to Control Register at Base Address + 00H.
   a) Select Straight Binary
   b) External Trigger Input
   c) Auto Zero Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

2. Execute Write of 1F00H to End/Start Channel Value Register at Base Address + 06H. This will permit 32 conversions of the Auto Zero value to be stored in the 32 Mailbox Buffers.

3. Execute write of 00H, as byte data transfers only, to Gain Select Channel Registers Base Address + 20H to 3FH. This selects a gain of one for all 32 channels.

4. Execute Write 0001H to the Start Convert Bit at Base Address + 10H. This starts the burst single mode of conversions. Thirty two conversions of the Auto Zero are implemented and stored in the 32 Mailbox Buffers.

5. Execute Read of the 32 Mailbox Buffers at Base Address + 40H to 7EH.

6. Take the average of the 32 ADC values and save this number as $Count_{CALLO}$.

Determination of the $Count_{CALHI}$ Value

7. Execute Write of 041AH to Control Register at Base Address + 00H.
   a) Select Straight Binary
   b) External Trigger Input
   c) Select 4.9000v Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

8. Writing the Start Channel Value, End Channel Value, and the Gain Selects is not necessary if they have not been changed from that programmed in steps 2 and 3 above.

9. Execute Write 0001H to the Start Convert Bit at Base Address + 10H. This starts the burst single mode of conversions. Thirty two conversions of the 4.9 volt calibration voltage are implemented and stored in the 32 Mailbox Buffers.

10. Execute Read of the 32 Mailbox Buffers at Base Address + 40H to 7EH.

11. Take the average of the 32 ADC values and save this number as $Count_{CALHI}$.

Calculate Equation 2

Calculate m = actual_slope from equation 2, since all parameters are known. It is now possible to correct input channel data from any input channel using the same input range (i.e. -10 to +10 volts with a PGA gain = 1). Repeat the above steps periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

Measure Channels 0 to 3 Differentially and Correct

12. Execute Write of 0402H to Control Register at Base Address + 00H.

    a) Select Straight Binary
    b) External Trigger Input
    c) All Channels Differential Input
    d) Burst Single Scan Mode
    e) Timer Disabled
    f) Interrupts Disabled

13. Execute Write of 0300H to End/Start Channel Value Register at Base Address + 06H. This will permit conversions of channels 0 to 3. Writing the Gain Selects is not necessary since they do not need to change from that programmed in step 3 above.

14. Execute Write 0001H to the Start Convert Bit at Base Address + 10H. This starts the burst single mode of conversions. Conversions of channels 0 to 3 are implemented and corresponding results are stored in the first four Mailbox Buffer locations at Base Address + 40H to 46H.

15. Execute Read of the 4 Mailbox Buffers at Base Address + 40H to 46H. The data represents the uncorrected "Count_Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known, calculate the calibrated value "Corrected_Count". This is the desired, corrected value. Repeat this procedure for each of the channels.

16. If channel response time requirements are not high speed it is recommended that a running average (i.e. of the last 8, 16, 32, etc.) of readings be maintained for each channel. This will minimize noise effects and provide the best accuracy.

<u>Calibration Programming Example 2</u>

Assume that the desired input range is 0 to +1.25 volts (selection of the desired input range is implemented via hardware DIP switch). Channels 3 to 13 are connected single ended, and corrected input channel data is desired. The calibration voltages are converted using burst single mode (for quick conversion of the calibration voltages) while the actual data will be converted using uniform single mode. From Tables 3.7 and 3.8, several calibration parameters can be determined:

Preselect 0 to 10v ADC Range via hardware DIP switch.
Gain = 8 (From Table 3.7)
$Volt_{CALHI}$ = 1.2250 volts (CAL2; From Table 3.7)
$Volt_{CALLO}$ = 0.6125 volts (CAL3; From Table 3.7)
Ideal_Volt_Span = 10.0000 volts (From Table 3.8)
Ideal_Zero = 0.0000 volts (From Table 3.8)

The 0 to +5v ADC range could alternatively be used with a gain of 4. This approach may reduce the affect of noise over the ADC range and gain selected in this example.

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

Determination of the $Count_{CALLO}$ Value

1. Execute Write of 0432H to Control Register at Base Address + 00H.
   a) Select Straight Binary
   b) External Trigger Input
   c) Select 0.6125v Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

2. Execute Write of 1F00H to End/Start Channel Value Register at Base Address + 06H. This will permit 32 conversions of the calibration voltage to be stored in the 32 Mailbox Buffers.

3. Execute Write of 03H, as byte data transfers only, to Gain Select Channel Registers Base Address + 20H to 3FH. This selects a gain of eight for all 32 channels.

4. Execute Write 0001H to the Start Convert Bit at Base Address + 10H to start burst single mode conversions. Thirty two conversions of the calibration voltage are implemented and stored in the 32 Mailbox Buffers.

5. Execute Read of the 32 Mailbox Buffers at Base Address + 40H to 7EH.

6. Take the average of the 32 ADC values and save this number as $Count_{CALLO}$.

Determination of the $Count_{CALHI}$ Value

7. Execute Write of 042AH to Control Register at Base Address + 00H.
   a) Select Straight Binary
   b) External Trigger Input
   c) Select 1.2250v Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

8. Writing the Start Channel Value, End Channel Value, and the Gain Selects is not necessary if they have not been changed from that programmed in steps 2 and 3 above.

9. Execute Write 0001H to the Start Convert Bit at Base Address + 10H. This starts a burst single mode of conversions. Thirty two conversions of the 1.2250 calibration voltage are implemented and stored in the 32 Mailbox Buffers.

10. Execute Read of the 32 Mailbox Buffers at Base Address + 40H to 7EH.
11. Take the average of the 32 ADC values and save this number as $Count_{CALHI}$.

Calculate Equation 2

Calculate m = actual_slope from equation 2, since all parameters are known. It is now possible to correct input channel data from any input channel using the same input range (i.e. 0 to +1.25 volts with a PGA gain = 8). Repeat the above steps periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

Measure Channels 3 to 13 Single Ended and Correct Using Uniform Single Mode

12. Execute Write of 0A0AH to Control Register at Base Address + 00H.
    a) Select Straight Binary
    b) External Trigger Input
    c) Select Single Ended Input
    d) Uniform Single Scan Mode
    e) Timer Enabled
    f) Interrupts Disabled

13. Execute Write of 0D03H to End/Start Channel Value Register at Base Address + 06H. This will permit conversions of channels 3 to 13. Writing the Gain Selects is not necessary since they do not need to change from that programmed in step 3 above.

14. Execute Write of 50H, as a byte data transfer, to the Timer Prescaler at Base Address + 02H. This sets the Timer Prescaler to 80 decimal.

15. Execute Write 0008H to the Conversion Timer at Base Address + 04H. This Conversion Timer value in conjunction with the Timer Prescaler sets the interval time between conversions to $(80 * 8) \div 8 = 80\ \mu$sec.

16. Execute Write 0001H to the Start Convert Bit at Base Address + 10H. This starts a uniform single mode of conversions. Conversions of channels 3 to 13 are implemented and stored in their corresponding Mailbox Buffers.

17. Execute Read of the Mailbox Buffers at Base Address + 46H to 5AH. The data represents the uncorrected “Count_Actual” term in equation 1. Since all parameters on the right hand side of equation 1 are known. The calibrated value "Corrected_Count" can be calculated for each of the channels.

18. If channel response time requirements are not high speed it is recommended that a running average (i.e. of the last 8, 16, 32, etc.) of readings be maintained for each channel. This will minimize noise effects and provide the best accuracy.

Error checking should be performed on the "Corrected_Count" value to make sure that calculated values below 0 or above 65,535 are restricted to those end points. Note that the software calibration cannot recover signals near the end points of each range which are clipped off due to the uncalibrated hardware (e.g. PGA and ADC) or power supply limitations.

See the specification chapter for details regarding the maximum corrected (i.e. calibrated) error.

Programming Interrupts

Interrupts can be enabled for generation after conversion of individual channels or after a group of channels have been converted. Interrupts generated by the IOS-330 use interrupt request line INTREQ0* (Interrupt Request 0). The interrupt release mechanism is Release On Acknowledge (ROAK) type. That is, the IOS-330 will release the INTREQ0* signal during an interrupt acknowledge cycle from the carrier.

The IOS-330 Interrupt Vector register can be used as a pointer to an interrupt handling routine. The vector is an 8-bit value and can be used to point to any one of 256 possible locations to access the interrupt handling routine.

Interrupt Programming Example

1. Clear the Interrupt Enable Bits in the Carrier Board Status Register by writing a "0" to bit 2 and bit 3.
2. Enable the IOS-330 for interrupt after each channel or after conversion of a group of channels by setting bits 12 and 13 of the IOS-330 Control Register as required.
3. Write a “1” to bit 2 of the Carrier Status/Control Register Module Interrupt Enable bit to enable IOS module interrupts to the PCI bus.
4. Interrupts can now be generated after start of a scan mode of operation (burst, continuous, or external trigger only).

General Sequence of Events for Processing an Interrupt

1. The IOS-330 asserts the Interrupt Request 0 Line (INTREQ0*) in response to an interrupt condition.
2. A generated interrupt is recognized by the carrier board and is recorded in the carrier board's Interrupt Pending Register and passed to the PCI bus by driving interrupt request signal INTA# active.
3. The host processor uses the PCI interrupt to locate an interrupt service routine to process interrupts from the carrier board.
4. The carrier board interrupt service routine examines the carrier board's Interrupt Pending Register and invokes IOS module interrupt service routines to service individual IOS modules.
5. The IOS-330 interrupt is serviced by reading converted data resident in the Mailbox Buffer of the IOS-330. Use the New Data Available Register to identify valid Mailbox Buffer data.
6. The carrier board interrupt service routine accesses the interrupt space of the IOS module selected to be serviced. Note that the interrupt space accessed must correspond to the interrupt request signal driven by the IOS module.
7. The carrier board will assert the INTSEL* signal to the appropriate IOS module together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to INTREQ0*; A1 high corresponds to INTREQ1*).
8. The IOS module receives an active INTSEL* signal from the carrier and supplies its interrupt vector to the host processor during this interrupt acknowledge cycle. An IOS module designed to release its interrupt request on acknowledge will release its interrupt request upon receiving an active INTSEL* signal from the carrier. If the IOS module is designed to release it's interrupt request on register access the interrupt service routine must also access the required register to clear the interrupt request.
9. If the IOS module interrupt stimulus has been removed and no other IOS modules have interrupts pending, the interrupt cycle is completed (i.e. the carrier board negates its interrupt request INTA#).

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the IOS-330. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the IOS-330 Block Diagram drawing at the end of this manual as you review this material.

FIELD ANALOG INPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.3). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to the IOS Analog Input Connection Drawing located in the *Drawings* Section for example wiring and grounding connections.

Analog inputs and calibration voltages are selected via analog multiplexers. IOS-330 control logic automatically programs the multiplexers for selection of the required analog input channel. The multiplexer control is based upon selection of single ended or differential analog input and the Start and End channel register values.

Single ended and differential channels cannot be mixed (i.e. they must all be single ended or differentially wired). Up to 32 single ended inputs can be monitored, where each channel's + input is individually selected along with a single sense lead for all channels. Up to 16 differential inputs can be monitored, where each channel's + and - inputs are individually selected.

A Programmable Gain (Instrumentation) Amplifier (PGA) takes as input the selected channel's + and - inputs (or + and sense) and outputs a single ended voltage proportional to it. The gain can be 1, 2, 4, or 8 and is selected through the Gain Control registers.

The output of the PGA feeds the A/D (Analog to Digital) Converter. The A/D Converter is a state of the art, 16-bit, successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the A/D has accurately digitized the input. Then it returns to sample mode to acquire the next channel. Once a conversion has been started, control logic on the IOS-330 automatically updates the multiplexer and PGA for the next channel to be converted as required. This allows the input to settle for the next channel while the previous channel is converting. This pipelined mode of operation facilitates a maximum system throughput.

A miniature DIP switch on the board controls the range selection for the A/D Converter (-5 to +5, -10 to +10, 0 to 5, and 0 to 10 Volts) as detailed in section 2. DIP switch selection should be made prior to powering the unit. Thus, all channels will use the same A/D Converter range. However, the analog input range can vary on an individual channel basis depending on the programmable gain selection.

The logic interface provides +/- 12 Volt supplies to the analog circuitry. The -10 to +10 and 0 to +10 Volt A/D Converter ranges will be clipped if these supplies are used, typically to +/-8.5 Volt maximum inputs. The user has the option of providing +/- 15 Volt external supplies to fully utilize input ranges to +/- 10 Volts. These supplies are selected via hardware jumpers J1 and J2 as detailed in section 2. Jumper selection should be made prior to powering the unit. Internal and external supplies should not be mixed (e.g. do not use +12 Volts with -15 Volts). When selecting supplies, low noise linear supplies are preferred. All supplies should switch ON or OFF at the same time.

The board contains four precision voltage references and a ground (autozero) reference for use in calibration. These provide considerable flexibility in obtaining accurate calibration for the desired A/D Converter range and gain combination, when compared to fixed hardware potentiometers for offset and gain calibration of the A/D Converter and PGA.

IOS INTERFACE LOGIC

IOS interface logic of the IOS-330 is imbedded within the FPGA. This logic includes: address decoding, I/O and ID read/write control circuitry, and ID PROM implementation.

The carrier to IOS module interface implements access to both ID and I/O space via 16 or 8-bit data transfers. Read only access to ID space provides the identification for the individual module (as given in Table 3.1). Read and write accesses to the I/O space provide a means to control the IOS-330 and retrieve newly converted data from the Mailbox buffer.

Access to both ID and I/O spaces are implemented with one wait state read or write data transfers. There is one exception, on a rare occasions read and write operations to the Mailbox buffer may contend. Since the Mailbox buffer is not implemented as a dual port memory, simultaneous read and write access to RAM is not possible. If a read access to the RAM is initiated simultaneously with an internal RAM write (for update of the Mailbox buffer with ADC data), the read access will be held until after the write operation has completed. Thus, the read operation from RAM (Mailbox) may require up to six waits to avoid contention with an internal write cycle.

IOS-330 CONTROL LOGIC

All logic to control data acquisition is imbedded in the IOS's FPGA. The control logic of the IOS-330 is responsible for controlling the operation of a user specified sequence of data acquisitions. Once the IOS-330 has been configured, the control logic performs the following:

- Controls the channel multiplexers based upon start and end channel values, and single ended or differential analog input mode.
- Selects channel gain at the programmable gain amplifier corresponding to the current channel.
- Controls data conversion at the A/D Converter based on one of five different scan modes of operation.
- Controls data transfer from the A/D Converter to the FPGA's 16-bit serial shift register.
- Controls and updates the Mailbox buffer, New Data register, and Missed Data register.
- Stops data acquisition for Single Cycle Scan modes.
- Provides external or internal trigger control.
- Controls the interval between data conversions.
- Issues interrupt requests to the carrier.

INTERNAL CHANNEL POINTERS

Internal counters in the FPGA are used as pointers to: control the multiplexers for selection of the current channel's analog signal; select and set the current channel's Gain; and control update of the Mailbox RAM buffer. The start channel register controls the value at which these counters start, and the end value register controls the maximum channel number which is reached.

In the continuous modes of operation these counters continuously cycle, in sequential order, from the defined start value to the defined end value. When the continuous mode of operation is halted by disabling the scan mode via the control register, the internal hardware counter remains at the count value reached when halted. Upon start of a new scan mode, via the software start convert bit or external trigger, the internal pointers are reinitialized. Thus, the first channel converted, upon restart of data conversions, will correspond to that set in the start value register.

A 16-bit serial shift register is implemented in the IOS's FPGA. This serial shift register interfaces to the A/D Converter. A clock signal provided by the converter is used to serially shift the new data from the converter to the FPGA's 16-bit serial shift register. Use of the converter's clock signal (instead of an external clock) minimizes the danger of digital noise feeding through and corrupting the results of a conversion in process.

The converted data serially shifted, from the A/D Converter to the FPGA, represents the analog signal digitized in the previous convert cycle. That is, the A/D Converter transfers digitized analog input data to the FPGA one convert cycle after it has been digitized. Serially shifting of the 16-bits of digitized data to the FPGA and then writing to the Mailbox buffer is completed 8 μsec after start of the convert cycle.

Upon initiation of an A/D convert cycle, the analog input data is digitized and stored into an internal A/D Converter buffer. Also during this cycle, the last converted data value is moved from the A/D Converter buffer to the FPGA's Mailbox Buffer. At this time the New Data Available bit corresponding to the previous converted channel is set in the FPGA register.

Understanding this sequence of events is important when using the External Trigger Only scan mode. The first digitized value received from the A/D Converter in External Trigger Only mode will not be written to the Mailbox buffer if the Start Convert bit is set prior to issuance of the first external trigger signal. This first value received from the A/D Converter is digitized data that has remained in the A/D Converter's buffer from a previous data acquisition session. Likewise, to update the Mailbox with the last desired digitized data value one additional convert cycle is required.

For all other scan modes the FPGA control logic will automatically discard the first digitized data value received from the A/D Converter. It is not written to the Mailbox buffer. In addition, the FPGA logic also automatically generates the required "flush" convert signals to obtain the last converted data value from the A/D Converter.

EXTERNAL TRIGGER

The external trigger connection is made via pin 49 of the P2 Field I/O Connector. For the Burst and Continuous scan modes the falling edge of the external trigger will start data acquisition which will then be controlled by the FPGA. For External Trigger Only mode, each falling edge of the external trigger causes a conversion at the A/D Converter. Once the external trigger signal has been driven low, it should remain low for minimum of 500n seconds.

TIMED PERIODIC TRIGGER CIRCUIT

Timed Periodic Triggering is provided by two programmable counters (an 8-bit Timer Prescaler and a 16-bit Conversion Timer). The Timer Prescaler is clocked by the 8MHz. board clock. The output of the Timer Prescaler counter is then used to clock the second counter (Conversion Timer). In this way, the two counters are cascaded to provide variable time periods anywhere from 8 μsec to 2.0889 seconds. The output of the second counter is used to trigger the start of new A/D conversions for the Uniform Scan modes of operation. For the Burst Continuous mode, the interval between conversions of each channel is fixed at 15 μsec. However, the interval between the group (burst) of channels can be controlled by the Interval Timer.

INTERRUPT CONTROL LOGIC

The IOS-330 can be configured to generate an interrupt after completion of conversion of a single channel or after conversion of a group of channels is completed. IOS interrupt signal INTREQ0* is issued to the carrier to request an interrupt. The interrupt release mechanism employed is ROAK (Release On Acknowledge). The IOS-330 will release the INTREQ0* signal during an interrupt acknowledge cycle from the carrier.

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5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at an elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board. Use the unmodified example we provide.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature................-40 to +85°C
Relative Humidity.........................5-95% non-condensing.
Storage Temperature...................-55°C to +150°C.

Physical Configuration.................Single I/O Server Module
Length.................................. 4.030 in. (102.36 mm).
Width....................................1.930 in. (49.02 mm)
Board Thickness...................0.062 in. (1.59 mm)
Height…………………….......0.500 in. (12.7 mm)

Power Requirements:
+5 Volts (±5%)......................65 mA, Typical
200 mA, Maximum.
+12V/+15V (±5%) ....14 mA, Typical
20 mA, Maximum.
-12V/-15V (±5%) ....11 mA, Typical
15 mA, Maximum.

Note:
2. The +/-12 volt power supplies are normally supplied through P1 (logic interface connector). Optionally (jumper selectable on the IOS), the user may connect external +/-15 volt supplies through the field I/O interface connector, P2.

Non-Isolated...............................Logic and field commons have a direct electrical connection.

ANALOG INPUTS

Input Channels (Field Access).....32 Single-ended or 16 Differential
Input Signal Type........................Voltage (Non-isolated).
Input Ranges (DIP switch selectable):
Bipolar -5 to +5 Volts[3]
Bipolar -10 to +10 Volts[3,4]
Unipolar 0 to +5 Volts[3]
Unipolar 0 to +10 Volts[3,4]

Notes:
3. Range assumes the programmable gain is equal to one. Additional ranges are created with other gains. Divide the listed range by the programmable gain to determine the actual input range. Input signal ranges may actually fall short of reaching the specified endpoints due to hardware limitations. For example, if an input may reach zero volts or less, a bipolar input range should be selected.
4. These ranges can only be achieved with ±15 Volt external power supplies. The input ranges will be clipped if ±12 Volt supplies are used, typically to ±9.8 Volt maximum inputs.

Programmable Gains.....................x1, x2, x4, and x8.
Input Overvoltage Protection..........VSS - 20 V to VDD + 40 V with Power ON.
-35 V to +55 Volts Power OFF
Input Resistance............................1000 MΩ, Typical.
Input Bias Current..........................1 nA., Typical.
Common Mode
Rejection Ratio (60 Hz)[8]................96 dB., Typical.
Channel to Channel
Rejection Ratio (60 Hz)[8]................96 dB., Typical.

Radiated Field Immunity3 (RFI).......Designed to comply with IEC61000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN61000-6-1 with error less than ±0.5% of FSR.
Electromagnetic Interference Immunity3 (EMI)..............................Error is less than ±0.25% of FSR under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Surge Immunity.............................. Not required for signal I/O per European Norm EN61000-6-1.
Electric Fast Transient Immunity3(EFT)..............................Complies with IEC61000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN61000-6-1.
Radiated Emissions........................Meets or exceeds European Norm EN61000-6-3 for class B equipment.

(ADC) ADS8509 or equivalent @25°C:
ADC...TI ADS8509
A/D Resolution...........................16-bits.
Data Format Binary 2's Complement and Straight Binary
No Missing Codes[8].....................No Missing Codes 15-bits ADC
A/D Integral Linearity Error[8].......±1 LSB Typical, ±2 LSB Maximum ADC
Unipolar Zero Error[5].................±5 mV Maximum, for 0-10 V Range, ±3 mV Maximum for 0-5 V Range.
Bipolar Offset Error[5].................±5 mV Maximum, for ±10 V Range, ±5 mV Maximum for ±5 V Range.
Full Scale Error[5]........................±0.5% Maximum.

(PGA) AD8251 or equivalent @25°C:
PGA..ADI AD8251
PGA Linearity Error.................±0.005% Maximum (3.27 LSB)
Offset Error RTI[5].......................±1.0 mV Typical, ±2.5 mV Maximum.
Gain Error (all gains)[5]..............0. 01% Typical, 0. 1% Maximum.
Note:
5. Software calibration eliminates these error components.

Programmable Calibration Voltages

Calibration Signal	Ideal Value (Volts)	Maximum Tolerance[8] @25°C (Volts)	Maximum Temperature Drift[6] (ppm/°C)
Auto Zero	0.0000	±0.000150	0
CAL0	4.9000	±0.000228	±10
CAL1	2.4500	±0.000228	±15
CAL2	1.2250	±0.000228	±15
CAL3	0.6125	±0.000228	±15

Note:
6. Worst case temperature drift is the sum of the ±10 ppm/°C * drift of the cal voltage reference (± 15 ppm/°C for "E" Version) plus the ±5 ppm/°C drift of the resistors in the voltage divider.

Maximum Overall Calibrated Error @ 25°C

The maximum corrected (i.e. calibrated) error is the worst case accuracy possible. It is the sum of error components due to ADC quantization of the low and high calibration signals, PGA and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25°C.

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max. Err[7,8,10] ±LSB (% Span)	Typ. Err[7,8,10] ±LSB (% Span)
-5 to +5	1	-5 to +5	8.6 LSB (0.013%)	2 LSB (0.003%)

Note:
7. A total of 256 input samples, autozero values, and calibration voltages were averaged with a throughput Rate of 67 kHz conversions/second. Follow the input connection recommendations of Section 2, because input noise and non-ideal grounds can degrade overall system accuracy. For critical applications multiple input samples should be averaged to improve performance. Accuracy versus temperature depends on the temperature coefficient of the calibration voltage.

Settling Time (20V step)[8]...............3.5 µS to 0.01%, Typical (PGA).
A/D Conversion Time.....................5 µS Maximum
Conversion Rate............................200 kHz Maximum
Recommended Conversion Rate[8]..67 kHz.
A/D Triggers.................................External and Software.
Input Noise[8,9]................................2 LSB rms, Typical.
Temperature Coefficient................See spec of calibration voltages.
Interrupt...Vectored Interrupt on end channel conversion or end of group of channel conversions.
Note:
8. Reference Test Conditions: Differential inputs, ±5V input range, PGA Gain = 1, Temperature 25°C, ±12V internal power supplies, 67K conversions/second, using Acromag's APC8621A PCI carrier with a 6 inch shielded cable length connection to the field analog input signals.
9. A total of 2048 input samples were taken statistically, assuming a normal distribution, to determine the RMS value.
10. Accuracy may be further improved by increasing the time between conversions (e.g. from 15 µsec to 30 µsec).

External Trigger Input/Output

As An Input:..........................Must be an active low 5 volt logic TTL compatible, debounced signal referenced to analog common. Conversions are triggered on the falling edge of this trigger signal. Minimum pulse width 500n seconds
As An Output:.......................Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for a maximum of 500n seconds.

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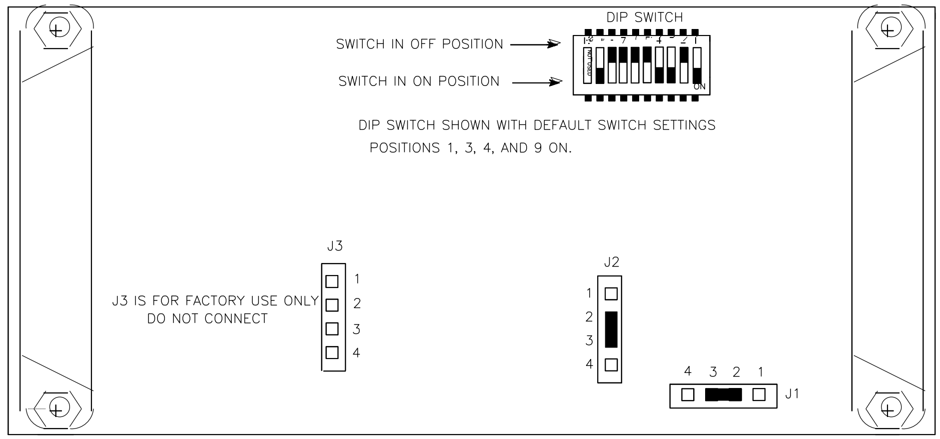


COMPONENT SIDE VIEW

ANALOG INPUT RANGE SELECTION (DIP Switch Settings)

DESIRED ADC INPUT RANGE * (VDC)	REQUIRED INPUT SPAN (VOLTS)	REQUIRED INPUT TYPE	SWITCH SETTINGS ON	SWITCH SETTINGS OFF
−5 TO +5**	10	Bipolar	1,3,4,9	2,5,6,7,8
−10 TO +10***	20	Bipolar	2,5,6,9	1,3,4,7,8
0 TO +5	5	Unipolar	1,3,5,8	2,4,6,7,9
0 TO +10***	10	Unipolar	1,3,4,7	2,5,6,8,9

* ASSUMING A GAIN OF 1

** THE BOARD IS SHIPPED WITH THE DEFAULT DIP SWITCH SETTING FOR THE −5 TO +5 VOLT ADC INPUT RANGE AS SHOWN IN THE ABOVE DIAGRAM.

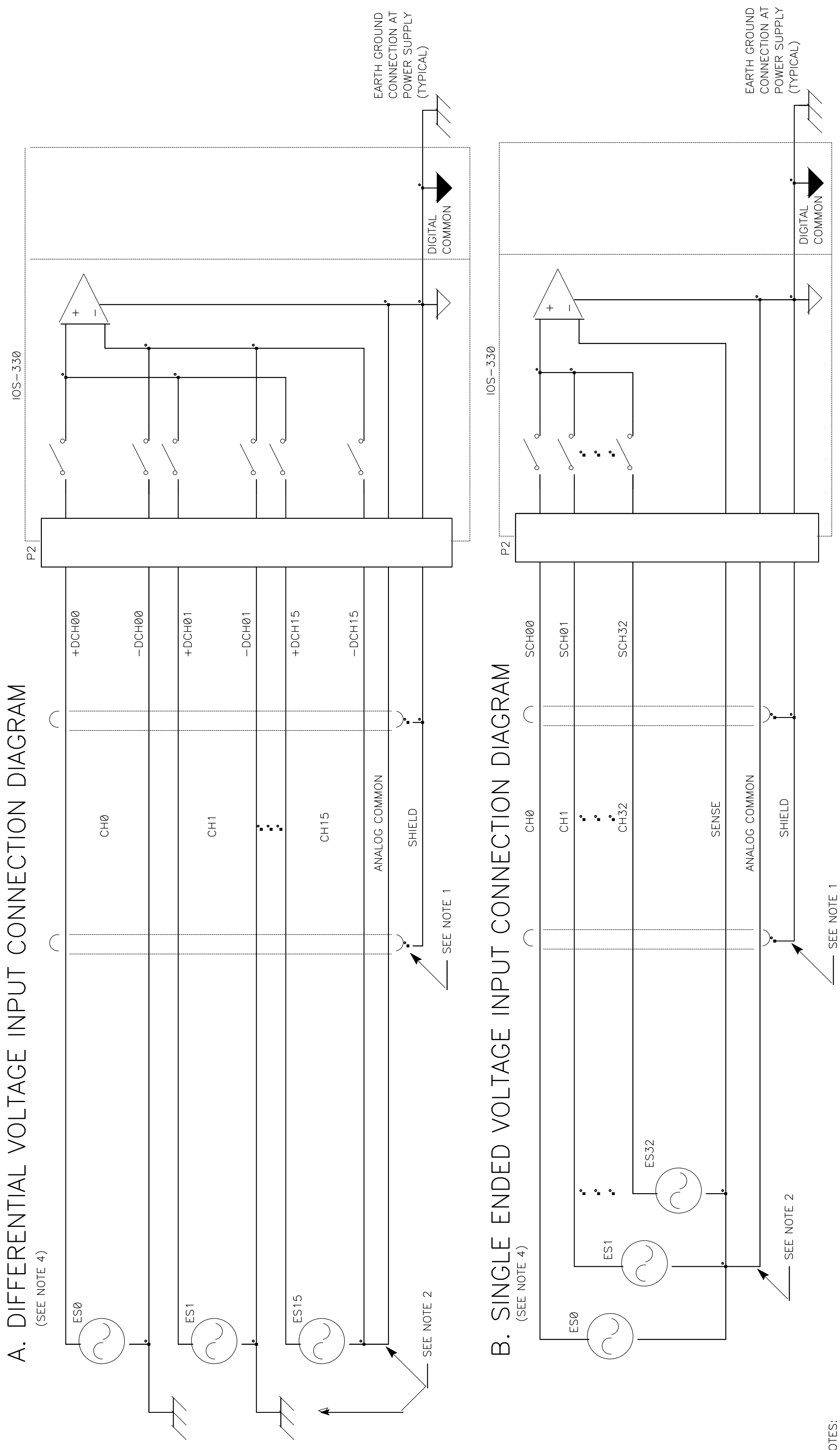
*** THESE RANGES CAN ONLY BE ACHIEVED WITH +/−15 VOLT EXTERNAL POWER SUPPLIES. THE INPUT RANGES WILL BE CLIPPED IF +/−12 VOLT SUPPLIES ARE USED, TYPICALLY TO +/−8.5 VOLT MAXIMUM INPUTS.

POWER SUPPLY SELECTIONS (PINS OF J1 AND J2)

POWER SUPPLY SELECTION *	J1 (1 & 2)	J1 (2 & 3)	J2 (1 & 2)	J2 (2 & 3)
+/−12 VOLT (INTERNAL)**	OUT	IN	OUT	IN
+/−15 VOLT (EXTERNAL)	IN	OUT	IN	OUT

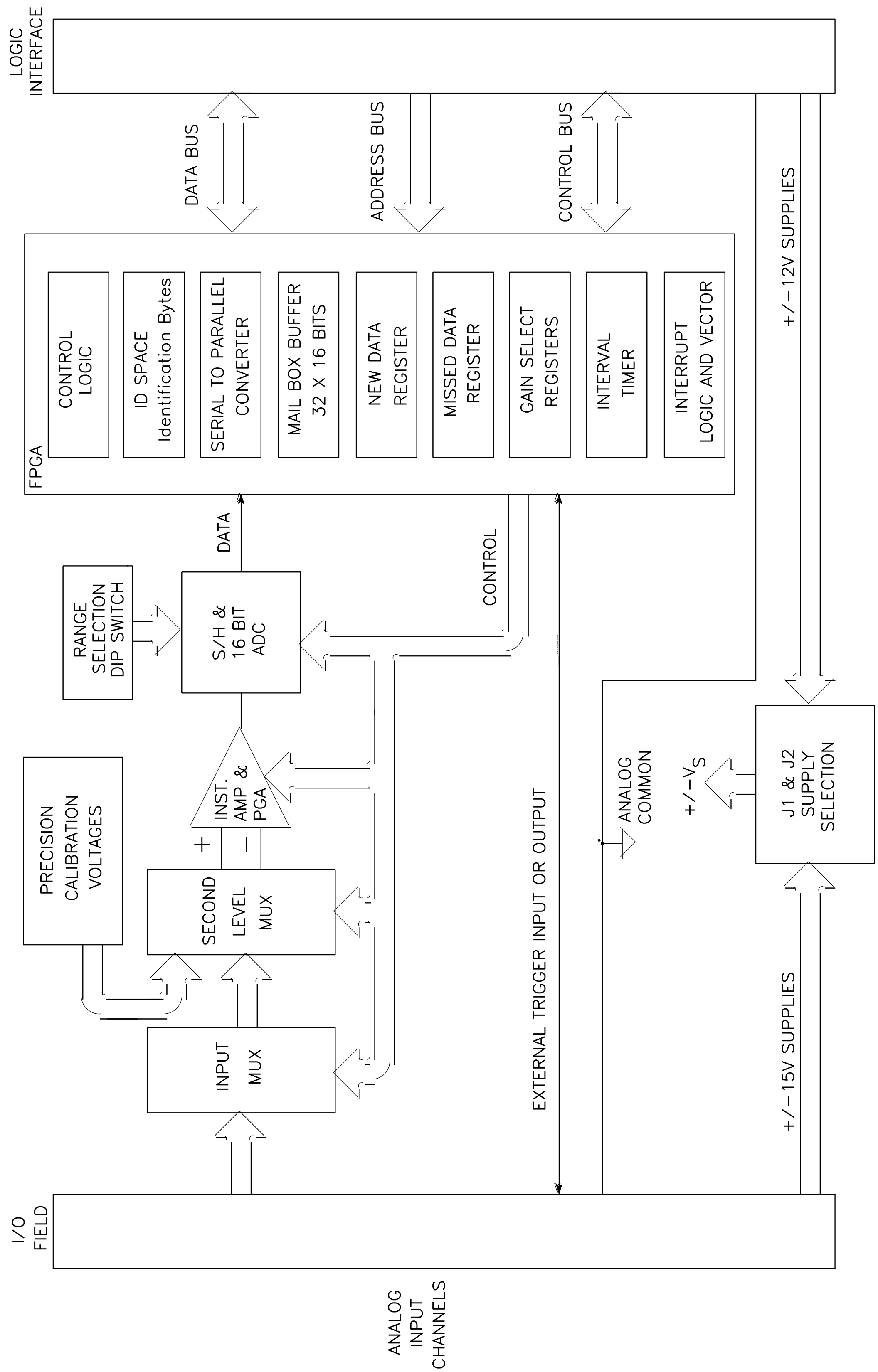
* INTERNAL AND EXTERNAL SUPPLIES SHOULD NOT BE MIXED (E.G. DO NOT USE +12 VOLTS WITH −15 VOLTS).
** THE BOARD IS SHIPPED WITH THE DEFAULT JUMPER SETTING FOR +/− 12 VOLT SUPPLIES AS SHOWN IN THE DIAGRAM ABOVE.

IOS−330 JUMPER LOCATIONS



NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON, IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.
3. EXTERNAL SUPPLIES CAN BE USED BY JUMPERING, IT IS RECOMMENDED THAT THE SUPPLY COMMONS BE CONNECTED TO ANALOG COMMON.
4. DIFFERENTIAL VOLTAGE INPUT CONNECTIONS ARE RECOMMENDED OVER SINGLE ENDED TO ACHIEVE THE GREATEST ACCURACY AND LOWEST NOISE.



IOS-330 BLOCK DIAGRAM