# NOTICE

**The drivers and utilities for Octagon products, previously provided on a CD, are now in a self-extracting zip file located at the Octagon Systems web site on the product-specific page. Download this file to a separate directory on your hard drive, then double click on it to extract the files. All references in this manual to files and directories on the CD now refer to files in the Utilities zip file.**

# 5720 User's Manual

**Doc. #03363 Rev 0494**

**OCTAGON SYSTEMS CORPORATION®**

6510 W. 91st Ave. Westminster, CO 80030
**Tech. Support**: 303–426–4521

## COPYRIGHT



## TRADEMARKS



## NOTICE TO USER

The information contained in this manual is believed to be correct. However, Octagon assumes no responsibility for any of the circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement. Octagon makes no representation or warranty that such applications will be suitable for the use specified without further testing or modification.

Octagon Systems Corporation general policy does not recommend the use of its products in life support applications where the failure or malfunction of a component may directly threaten life or injury. It is a Condition of Sale that the user of Octagon products in life support applications assumes all the risk of such use and indemnifies Octagon against all damage.

# IMPORTANT!

**Please read before installing your product.**

Octagon's products are designed to be high in performance while consuming very little power. In order to maintain this advantage, CMOS circuitry is used.

CMOS chips have specific needs and some special requirements that the user must be aware of. Read the following to help avoid damage to your card from the use of CMOS chips.

# Using CMOS Circuitry in Industrial Control

Industrial computers originally used LSTTL circuits. Because many PC components are used in laptop computers, IC manufacturers are exclusively using CMOS technology. Both TTL and CMOS have failure mechanisms, but they are different. This section describes some of the common failures which are common to all manufacturers of CMOS equipment. However, much of the information has been put in the context of the Micro PC.

Octagon has developed a reliable database of customer-induced, field failures. The average MTBF of Micro PC cards exceeds 11 years, yet there are failures. Most failures have been identified as customer-induced, but there is a small percentage that cannot be identified. As expected, virtually all the failures occur when bringing up the first system. On subsequent systems, the failure rate drops dramatically.

- Approximately 20% of the returned cards are problem-free. These cards, typically, have the wrong jumper settings or the customer has problems with the software. This causes frustration for the customer and incurs a testing charge from Octagon.

- Of the remaining 80% of the cards, 90% of these cards fail due to customer misuse and accident. Customers often cannot pinpoint the cause of the misuse.

- Therefore, 72% of the returned cards are damaged through some type of misuse. Of the remaining 8%, Octagon is unable to determine the cause of the failure and repairs these cards at no charge if they are under warranty.

The most common failures on CPU cards are over voltage of the power supply, static discharge, and damage to the serial and parallel ports. On expansion cards, the most common failures are static discharge, over voltage of inputs, over current of outputs, and misuse of the CMOS circuitry with regards to power supply sequencing. In the case of the video cards, the most common failure is to miswire the card to the flat panel display. Miswiring can damage both the card and an expensive display.

- **Multiple component failures** - The chance of a random component failure is very rare since the average MTBF of an Octagon card is greater than 11 years. In a 7 year study,

Octagon has never found a single case where multiple IC failures were not caused by misuse or accident. It is very probable that multiple component failures indicate that they were user-induced.

- **Testing "dead" cards** - For a card that is "completely nonfunctional", there is a simple test to determine accidental over voltage, reverse voltage or other "forced" current situations. Unplug the card from the bus and remove all cables. Using an ordinary digital ohmmeter on the 2,000 ohm scale, measure the resistance between power and ground. Record this number. Reverse the ohmmeter leads and measure the resistance again. If the ratio of the resistances is 2:1 or greater, fault conditions most likely have occurred. A common cause is miswiring the power supply.

- **Improper power causes catastrophic failure** - If a card has had reverse polarity or high voltage applied, replacing a failed component is not an adequate fix. Other components probably have been partially damaged or a failure mechanism has been induced. Therefore, a failure will probably occur in the future. For such cards, Octagon highly recommends that these cards be replaced.

- **Other over-voltage symptoms** - In over-voltage situations, the programmable logic devices, EPROMs and CPU chips, usually fail in this order. The failed device may be hot to the touch. It is usually the case that only one IC will be overheated at a time.

- **Power sequencing** - The major failure of I/O chips is caused by the external application of input voltage while the Micro PC power is off. If you apply 5V to the input of a TTL chip with the power off, nothing will happen. Applying a 5V input to a CMOS card will cause the current to flow through the input and out the 5V power pin. This current attempts to power up the card. Most inputs are rated at 25 mA maximum. When this is exceeded, the chip may be damaged.

- **Failure on power-up** - Even when there is not enough current to destroy an input described above, the chip may be destroyed when the power to the card is applied. This is due to the fact that the input current biases the IC so that it acts as a forward biased diode on power-up. This type of failure is typical on serial interface chips.

- **Serial and parallel** - Customers sometimes connect the serial and printer devices to the Micro PC while the power is off. This can cause the failure mentioned in the above section, *Failure upon power-up*. Even if they are connected with the Micro PC on, there can be another failure mechanism. Some serial and printer devices do not share the same power (AC) grounding. The leakage can cause the serial or parallel signals to be 20-40V above the Micro PC ground, thus, damaging the ports as they are plugged in. This would not be a problem if the ground pin is connected first, but there is no guarantee of this. Damage to the printer port chip will cause the serial ports to fail as they share the same chip.

- **Hot insertion** - Plugging cards into the card cage with the power on will usually not cause a problem. (**Octagon urges that you do not do this!**) However, the card may be damaged if the right sequence of pins contacts as the card is pushed into the socket. This usually damages bus driver chips and they may become hot when the power is applied. This is one of the most common failures of expansion cards.

- **Using desktop PC power supplies** - Occasionally, a customer will use a regular desktop PC power supply when bringing up a system. Most of these are rated at 5V at 20A or more. Switching supplies usually require a 20% load to operate properly. This means 4A or more. Since a typical Micro PC system takes less than 2A, the supply does not regulate properly. Customers have reported that the output can drift up to 7V and/or with 7-8V voltage spikes. Unless a scope is connected, you may not see these transients.

- **Terminated backplanes** - Some customers try to use Micro PC cards in backplanes that have resistor/capacitor termination networks. CMOS cards cannot be used with termination networks. Generally, the cards will function erratically or the bus drivers may fail due to excessive output currents.

- **Excessive signal lead lengths** - Another source of failure that was identified years ago at Octagon was excessive lead lengths on digital inputs. Long leads act as an antenna to pick up noise. They can also act as unterminated transmission lines. When 5V is switch onto a line, it creates a transient waveform. Octagon has seen submicrosecond pulses of 8V or more. The solution is to place a capacitor, for example 0.1 µF, across the switch contact. This will also eliminate radio frequency and other high frequency pickup.

# TABLE OF CONTENTS

# PREFACE

This manual is a guide to the proper configuration, installation, and operation of your 5720 Analog Input Card. Installation instructions, card mapping information, jumpering options and technical specifications are described in the main section of the manual. Additional programming examples and technical information are included in the appendices.

The 5720 Analog Input Card is part of the Octagon Micro PC system. It is designed to be used with any of the Micro PC Control Cards. You can use your 5720 card in conjunction with other Micro PC expansion cards, tailoring your system for a wide variety of applications. The 5720 card can also be used in an IBM compatible PC. Micro PC cards are too tall to fit in an XT, but will fit in AT industrial sized and other AT–size cases.

All Micro PC products are modular, so creating a system is as easy as selecting and plugging in the products you need.

## CONVENTIONS USED IN THIS MANUAL

1. Information which appears on your screen (output from your system, commands or data that you key in) is shown in a different type face.

   ```
   Octagon 5016 BIOS vers x.xx
   Copyright (c) 1991, Octagon Systems, Corp.
   All Rights Reserved.
   ```

2. Italicized refers to information that is specific to your particular system or program, e.g.,

   Enter *filename*

   means enter the name of your file.

3. Warnings always appear in this format:

   **WARNING:** The warning message appears here.

4. Paired angle brackets are used to indicate a specific key on your keyboard, e.g., <ESC> means the escape key; <CTRL> means the control key; <F1> means the F1 function key.

5. All addresses are given in hexadecimal.

## SYMBOLS AND TERMINOLOGY

Throughout this manual, the following symbols and terminology are used:

| | |
|---|---|
| W[ – ] | Denotes a jumper block and the pins to connect. |
| BIOS drive | The solid–state disk which contains the system BIOS and ROM–DOS. |
| Control Card | Contains the CPU, memory, and operating system and controls the operation of all the extension cards. |
| DRAM | Dynamic Random Access Memory devices. DRAMs provide volatile memory with unlimited read and write cycles. |
| Expansion Card | The expansion cards add I/O functions to the Micro PC system, such as analog input/ output, digital input/output, motion control, display, and so on. |
| Flash EPROM | Electrically erasable EPROM which allows approximately 10,000 writes. |
| Memory device | The type of static RAM, DRAM, flash EPROM or EPROM specified for either volatile or nonvolatile memory. |
| PC SmartLINK | A serial communications software package designed by Octagon for use with the 5720 8–Bit Analog Input Card. Refers to all versions of PC SmartLINK. |

| | |
|---|---|
| ROM | Read Only Memory devices. ROMs provide nonvolatile memory, have a limited number of write cycles, and include EPROMs, EEPROMs, and flash EPROMs. |
| ROM–DOS | DOS operating system included in Micro PC ROM. |
| Solid–State Disk (SSD) | A simulated disk using a high speed solid–state memory device, for example flash EPROM, EEPROM, or static RAM. |
| Static RAM | Static Random Access Memory device. Static RAMs provide volatile memory with unlimited read and write cycles. They may be used with a battery back–up module. |
| TTL Compatible | Transistor transistor logic compatible; 0–5V logic levels. |
| H | The suffix “H” denotes a hexadecimal number. A decimal number has no prefix or suffix. For example, 1000H and 4096 are equivalent. |

## TECHNICAL SUPPORT

If you have a question about the 5720 Analog Input Card and cannot find the answer in this manual, call Technical Support. They will be ready to give you the assistance you need.

When you call, please have the following at hand:

Your *5720 User's Manual*

A description of your problem.

The direct line to Technical Support is 303–426–4521.

This page intentionally left blank.

# CHAPTER 1 OVERVIEW

## DESCRIPTION

The 5720 8–Bit Analog Input Card is designed for low cost applications requiring analog input and digital control. It has an 8–channel analog to digital converter with 8–bit resolution. The 8–single ended channels are multiplexed under software control. The 5720 has a conversion time of 8.5 uS and a throughput of 100,000 samples per second.

The input range of the 5720 is 0–5V. Inputs are protected from overload up to +/–16V even when the power is off. A precision 5V reference is provided and never needs calibration.

The 5720 also has 24 digital I/O lines. These lines may be programmed as either inputs or outputs in groups of four and eight for direct connection to an opto rack for interface with high current AC and DC voltages.

The 5720 A/D Card measures 4.5 in. x 4.9 in. and uses one slot of the Micro PC card cage.

## MAJOR FEATURES

**High Performance A/D Converter**

- 8–bit resolution
- 8 single–ended inputs
- 0–5V input range
- +/–16V over voltage protection
- 100,000 samples per second

**24 Digital I/O Lines**

- Configured and controlled by software
- 24 lines that may be independently configured as inputs or outputs in groups of four and eight
- All I/O lines may directly interface with optical relays

**Access Indicator**

- Front mounted, high visibility LED
- Flashes briefly when the card is accessed

**Easy I/O Address Selection**

- Jumper selectable I/O addresses
- Up to 8 cards may be used in a system

# CHAPTER 2 INSTALLATION

## DESCRIPTION

This chapter includes information on setting the base address, selecting the interrupt source and interrupt request line and installing the 5720 8–Bit Analog Input Card in the card cage. This card is designed to be used with Octagon's Micro PC system. It uses one card slot and plugs directly into the Micro PC backplane (motherboard).

## EQUIPMENT

You will need the following equipment (or equivalent) to use your 5720:

- 5720 8–Bit Analog Input Card
- Micro PC Control Card
- Micro PC Card Cage
- Power Module
- PC SmartLINK

You may also want to use:

- AIN–5B Signal Conditioning Board
- STB–26 Terminal Board
- MUX–16 Analog Multiplexer Board
- ITB–8/16 or ITB–16/8 Level Conversion Board
- Opto Rack

Before installing the 5720 A/D Card, refer to figure 2–1 for the location of various connectors and jumpers

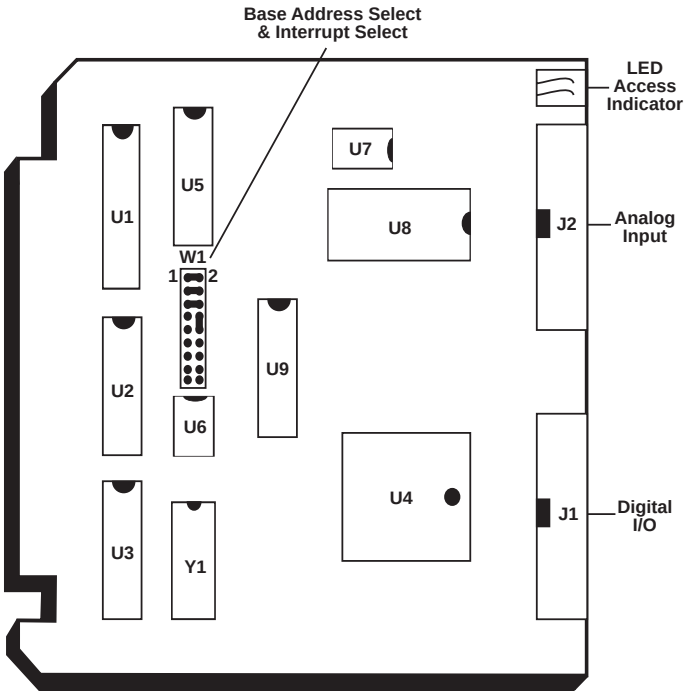



Figure 2–1—5720 Component Diagram

## JUMPER SETTINGS

The 5720 is shipped with default jumper connections in place. If you are setting up the 5720 for the first time, we recommend you not change the jumpers until you have completed the installation procedures and the DEMO program.

### Base Addresses

The base address of the 5720 is configurable via jumpers and is set to 100H at the factory. If there is another card in your system with a base address of 100H, you must use a different base address

(or change the address of the other card). To change the base address, change the configuration of jumper block W1. The table below lists the jumper configurations and corresponding base addresses:

| **Base Address Select: W1** | |
|---|---|
| **Pins Jumpered** | **Base Address** |
| [1-2] [3-4] [5-6]* | 100H |
| [1-2] [3-4] | 110H |
| [1-2] [5-6] | 120H |
| [1-2] | 130H |
| [3-4] [5-6] | 140H |
| [3-4] | 150H |
| [5-6] | 160H |
| Not jumpered | 170H |

* = default

## 5720 QUICK START

The following instructions are a quick overview of installing and using the 5720 card with factory default settings. For more information on the specific features of the card, please refer to the appropriate chapter.

**WARNING:** The 5720 card contains static sensitive CMOS components. The greatest danger occurs when the card is plugged into a card cage. The 5720 card becomes charged by the user and the static discharges to the backplane from the pin closest to the card connector. If that pin happens to be

an input pin, even TTL inputs may be damaged. To avoid damaging your card and its components:

1. Ground yourself before handling the 5720 card.

2. Disconnect power before removing or inserting the 5720 card.

Take care to correctly position the 5720 in the card cage. The Vcc and ground signals must match those on the backplane. Figure 2–2 shows the relative positions of the 5720 and the backplane.

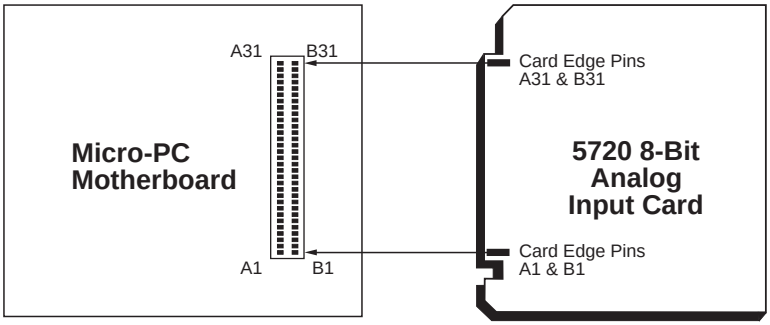



Figure 2–2 — Edge Connector Orientation

1. Install the 5720 in the Micro PC card cage.

2. Position the cage so that the backplane is away from you, the power module is to the right, and the open side of the cage is closest to you. The lettering on the backplane should be right side up ( for example, you should be able to read “A31” on the backplane), with the words OCTAGON SYSTEMS CORP. running vertically along the left side of the backplane. This position is “feet down” for a table mount cage and “feet back” for a rear mount.

3. Slide the 5720 into the card cage. You may use any slot. The components on the card should face to the left.

4. Turn on the card cage power.

5. Execute the following example program:

```
10  OUT 256,255
20  PRINT INP(256)
```

**Explanation**
Line 10 Start CH0. Base address is 256.
Line 20 Read CH0

This routine represents the simplest way a single analog sample may be taken. The BASIC commands are generic and should be compatable with any BASIC supporting standard syntax.

The following is a functional diagram of the 5720 and depicts how the analog input and digital I/O features are inter-related:

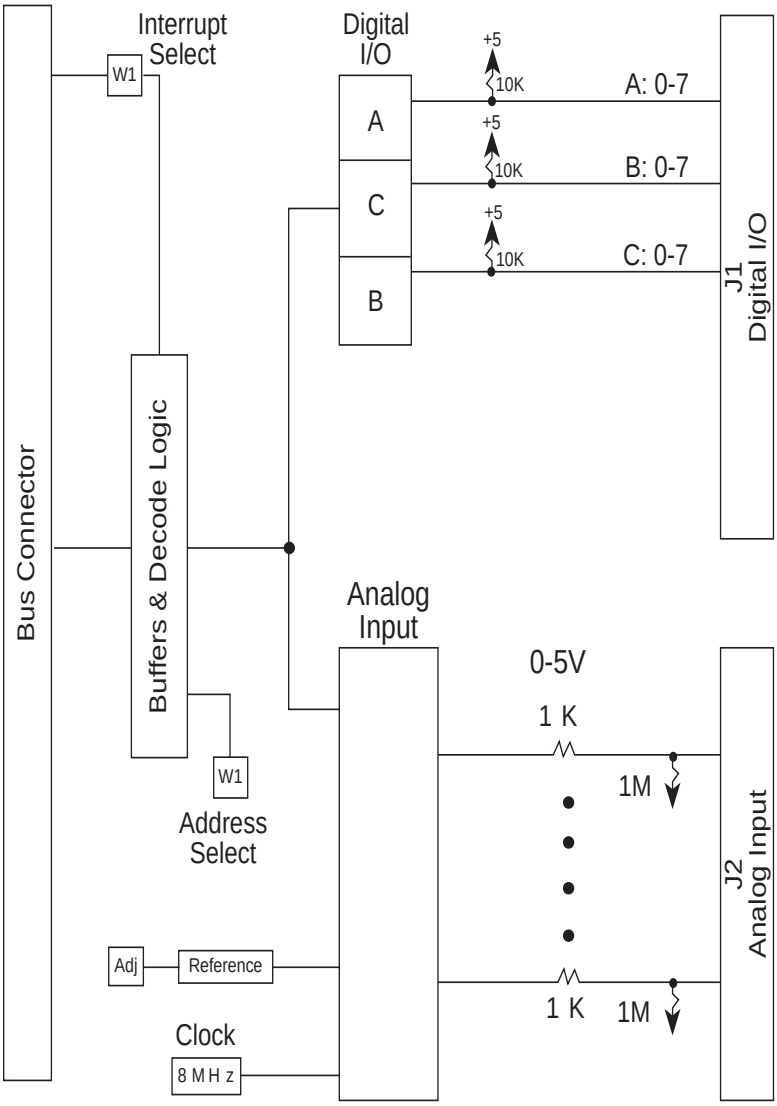



Figure 2–3—5720 Functional Diagram

## TROUBLESHOOTING

If you have trouble getting your system to work properly, remove all cards except the control Card and the 5720 from your system. Check the power module to make sure the system is receiving power. The 5720 requires 5V +/– .25V at 60 mA when measured at the connector pins. The power module ripple should be less than 50 mV. Also, verify all the jumpers are configured properly. If you changed the jumpers and the system is not working properly, return the system to the default jumper settings and verify that the card works properly. If you still encounter difficulties, please contact Technical Support at 303–426–4521.

This page intentionally left blank.

## DESCRIPTION

On the 5720 the analog inputs are multiplexed. The 8 single–ended inputs are selectively coupled, one at a time, to a single analog–to–digital converter. For example, to start a conversion on CH6, output FFH to Base Address+6 (OUT Base Address+6). When the conversion is complete, the A/D converter issues an End of Conversion (EOC) signal and the data may be read. This End of Conversion may be read as bit 0 at Base Address+12 or optionally jumpered to cause an interrupt.

The 5720 supports the STB–20 Terminal Board for connection to field wiring. The STB–20 brings the lines from the 5720 out to screw terminals. You can then use 12 to 22 gauge solid or stranded wire to connect field equipment. The STB–20 is connected to the 5720 (J2) via a CMA–20 cable.

| **Analog Connector: J2** | | | |
|---|---|---|---|
| **Single-Ended** | **Pin #** | **Single-Ended** | **Pin #** |
| IN 0 | 1 | IN 5 | 11 |
| GND | 2 | GND | 12 |
| IN 1 | 3 | IN 6 | 13 |
| GND | 4 | GND | 14 |
| IN 2 | 5 | IN 7 | 15 |
| GND | 6 | GND | 16 |
| IN 3 | 7 | Reserved | 17 |
| GND | 8 | Reserved | 18 |
| IN 4 | 9 | Reserved | 19 |
| GND | 10 | Reserved | 20 |

## VOLTAGE RANGE

The input voltage range is fixed for unipolar operation of 0–5V. The 8–bit resolution of the A/D converter allows this range to be read as a digital value from 0 to 255 in 19.53 mV steps. The 5720 is designed for an over voltage range from +/–16V.

**WARNING:** The input range should not exceed +/–16V or you will damage the card.

The following tables show the transition values at endpoints and at midpoint:

| **Data Transition Values** | | |
|---|---|---|
| **Transition** | **Represents** | **Equals** |
| FE to FF | Full scale | +5V - 3/2 LSB |
| 00 to 01 | Zero | 0 - 1/2 LSB |

| **Analog Input Data Representation** | | |
|---|---|---|
| **Range** | **Full Scale Reading** | **Least Significant Bit** |
| 0-5V | $2^8 = 256$ | 5V/256 = 19.53 mV |

## CALIBRATION

The 5720 is calibrated at the factory to 0–5V full scale. The card must be recalibrated only if the input voltage range changes (e.g. the potentiometer (R4) is inadvertently turned or if you need to detect overrange). You may recalibrate the 5720 for overrange at a maximum of 20 mV per count for 5.12V full scale. The input range should not be adjusted for less than 5V.

To recalibrate:

- Using a precision voltmeter, measure pin 12 of U8 for 5.000V while adjusting the potentiometer (R4)

or

- If overrange detection is needed, adjust R4 until the the value of 5.12V is measured

**WARNING:** A reference that is set over or under these values values can corrupt data. They also draw more current. Do not exceed recommended values.

## CHANNEL SELECTION & A/D CONVERSION

Channel 0 of the 5720 is set at the base address. When you select a specific channel to read, this automatically starts the A/D conversion for that channel. The following tables list address bits used to select an analog channel:

| **Channel Selection** | |
|---|---|
| **Base Address +** | **Channel** |
| 0 | 0 |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| 5 | 5 |
| 6 | 6 |
| 7 | 7 |

When the conversion is complete, the A/D converter provides an End of Conversion (EOC) signal. When the conversion is complete, that data may be read.

The EOC status bit is contained in data bit 0 at location Base Address+12. When this bit equals 1, the data is ready to be read. This bit will be reset to 1 when access is made to read the data. The following is a summary of the steps required to perform an A/D conversion:

| **Analog Input Data** | | |
|---|---|---|
| **Address** | **DB7** | **D0** |
| Base + 0 | MSB | LSB |

1. Select channel and start A/D conversion.
   `OUT BASE ADDRESS+CHANNEL, 255`

2. Wait 8.5 uS or check EOC bit =1

3. Read results:
   `INP BASE ADDRESS + CHANNEL`

**NOTE:** When reading the result of a conversion, input from the Base Address for this location can be used for all channels.

If you are using BASIC programs ( e.g., GW BASIC, QuickBASIC, etc.), the commands will take longer to execute than the time it takes to do a conversion, so it is unlikely you will ever get a "busy signal" from the converter. Maximum conversion time is 8.5 uS for the 5720.

## Polling and Interrupts

The completion of a conversion is detected in one of three ways — by detecting an interrupt, by polling a status bit or by waiting 8.5 uS or longer after issuing starting the conversion.

### Polling

Polling is the simpler of the two procedures and is adequate for most applications. The following program example converts all 8 channels and displays them on the screen. It demonstrates polling the End of Conversion signal. Base Address is set to 100H.

**BASIC Example**

```
10  REM 5720 DEMO PROGRAM V.1A
20  FOR C=0 TO 15
30  OUT BASEADDRESS+C  : REM START CONVERSION
40  IF INP(BASEADDRESS+13) AND 1<>1 THEN GOTO 40
50  PRINT "CH";C;"=";INP(256)
60  NEXT
70  FOR I=0 TO 1000
80  NEXT
90  GOTO 20
```

**Interrupts**

Configure jumper block W1 for the desired interrupt request line to the Control Card. For example, W1[7–8] selects IRQ2. Make sure that the interrupt you select does not conflict with other interrupts on the bus.

| **Interrupt Request Lines: W1** | |
|---|---|
| **Pins Jumpered** | **Interrupt Request Line** |
| [7-8] | IRQ 2 |
| [9-10] | IRQ 3 |
| [11-12] | IRQ 4 |
| [13-14] | IRQ 5 |
| [15-16] | IRQ 6 |
| [17-18] | IRQ 7 |
| [8-10]* | No interrupt |

* = default

This page intentionally left blank.

# CHAPTER 4 DIGITAL I/O

## DESCRIPTION

The 5720 has 24 digital I/O lines that will interface with 0–5V switch and sensor inputs and provide logic level outputs. These lines have a 10K pull–up resistor and are terminated with a 26–pin IDC connector at J1. The three sets of 8 lines may be programmed as either inputs or outputs in groups of four or eight. The individual ports are designated A, B, and C. Port A has the lowest address; each half of port C is controllable (upper and lower C). The following table shows the connector pinouts for each port:

| Digital I/O: J1 | |
|---|---|
| **Pin #** | **Function** |
| 19 | Port A, line 0 |
| 21 | Port A, line 1 |
| 23 | Port A, line 2 |
| 25 | Port A, line 3 |
| 24 | Port A, line 4 |
| 22 | Port A, line 5 |
| 20 | Port A, line 6 |
| 18 | Port A, line 7 |
| 10 | Port B, line 0 |
| 8 | Port B, line 1 |
| 4 | Port B, line 2 |
| 6 | Port B, line 3 |
| 1 | Port B, line 4 |
| 3 | Port B, line 5 |
| 5 | Port B, line 6 |
| 7 | Port B, line 7 |
| 13 | Port C, line 0 |
| 16 | Port C, line 1 |
| 15 | Port C, line 2 |
| 17 | Port C, line 3 |
| 14 | Port C, line 4 |
| 11 | Port C, line 5 |
| 12 | Port C, line 6 |
| 9 | Port C, line 7 |
| 2 | +5V |
| 26 | Gnd |

The HEX addresses of the 82C55 ports for J1 are listed below:

| 82C55 Port Addresses: J1 | |
|---|---|
| **Port** | **Address** |
| A | Base + 08H |
| B | Base + 09H |
| C | Base + 0AH |
| Control Register | Base + 0BH |

On power–up or reset, all three ports are in the input state. You can alter which ports are inputs or outputs by writing a control command to the control register in the 82C55. The examples below assume the base address is 100H. The 82C55 Control Register table on the following page lists the control commands for the different input/output possibilities.

### Programming Example

If you want all three ports to be outputs, use:

```
OUT BASE ADDRESS+0BH, 80H
```

Port A will now output all “1”s after

```
OUT BASE ADDRESS+08H, FFH
```

or all “0”s after

```
OUT BASE ADDRESS+08H, 0
```

| 82C55 Control Register Commands | | | | | |
|---|---|---|---|---|---|
| **HEX** | **DEC** | **Port A*** | **Port B*** | **Port UC*** | **Port LC*** |
| 80H | 128 | OUT | OUT | OUT | OUT |
| 81H | 129 | OUT | OUT | OUT | IN |
| 82H | 130 | OUT | IN | OUT | OUT |
| 83H | 131 | OUT | IN | OUT | IN |
| 88H | 136 | OUT | OUT | IN | OUT |
| 89H | 137 | OUT | OUT | IN | IN |
| 8AH | 138 | OUT | IN | IN | OUT |
| 8BH | 139 | OUT | IN | IN | IN |
| 90H | 144 | IN | OUT | OUT | OUT |
| 91H | 145 | IN | OUT | OUT | IN |
| 92H | 146 | IN | IN | OUT | OUT |
| 93H | 147 | IN | IN | OUT | IN |
| 98H | 152 | IN | OUT | IN | OUT |
| 99H | 153 | IN | OUT | IN | IN |
| 9AH | 154 | IN | IN | IN | OUT |
| 9BH | 155 | IN | IN | IN | IN |

* Ports A and B must be either all inputs of all outputs. Each half of Port C is controllable. Upper C (UC) includes bits 4 through 7 and Lower C (LC) includes bits 0 through 3.

## INTERFACING TO AN OPTO MODULE RACK

When heavy–duty loads and inputs (up to 3A and 260V AC or DC) are required, the 5720 digital I/O lines can interface with the MPB series opto module racks. The opto modules have the advantage of providing 4000V of isolation between the high voltage systems and the 5720. A CMA–26 cable connects the 5720 at J1 to the opto rack. The MPB series opto rack requires +5V and ground to operate. Refer to the MPB Opto Rack documentation for further information.

The following table lists the corresponding opto channel for a particular 82C55 port:

| Opto Channel Selection | |
|---|---|
| **Opto Channel** | **82C55 Port** |
| 0-3 | Lower Port C |
| 4-7 | Upper Port C |
| 8-15 | Port A |
| 21-23 | Port B |

## INTERFACING TO SWITCHES OR OTHER DEVICES

The STB–26 terminal board provides a convenient way to interface switches or other devices to the 5720. A CMA–26 cable connects the STB–26 to J1. Digital I/O devices are then connected to the screw terminals on the STB–26. Refer to the STB–26 Terminal Board documentation for further information.

For applications requiring medium voltage inputs or outputs, the ITB–8/16 or ITB–16/8 Level Conversion Board provides a medium voltage, high current interface. Medium voltage logic, up to 28V, is used to convert these voltage levels to TTL levels used by the 5720. You can connect lamps, small solenoids and relays. A CMA–26 cable connects the ITB board to J1 on the 5720. Refer to the ITB–8/16, –16/8 Level Conversion Board for further information.

This page intentionally left blank.

## TECHNICAL SPECIFICATIONS

**Digital I/O**
Type: 82C55
Logic low input: 0–.8V
Logic high input: 2.0–5.0V
Pull–up resistor: 10K
Logic low output: 0–5V
Logic high output: 2.4–5.0V
Output current: 2.5 mA
Opto rack interface: Drives 12 mA modules

**Analog Inputs**
Type: ADC0809 compatible
Channels: 8 single–ended
Input range: 0–5.000V
Overload protection: +/–16V without damage
Input impedance: 1 Mohm minimum
Conversion time: 8.5 uS
Throughput: 100,000 per second

**Power Specifications**
5V +/–5%, 60 mA

**Environmental Specifications**
–20° to 70° C operating, standard
–40° to 85° C operating, extended
–50° to 90° C nonoperating
RH 5% to 95%, noncondensing

## JUMPER CONFIGURATIONS

| **Base Address Select: W1** | |
|---|---|
| **Pins Jumpered** | **Base Address** |
| [1-2] [3-4] [5-6]* | 100H |
| [1-2] [3-4] | 110H |
| [1-2] [5-6] | 120H |
| [1-2] | 130H |
| [3-4] [5-6] | 140H |
| [3-4] | 150H |
| [5-6] | 160H |
| Not jumpered | 170H |

* = default

## CONNECTOR PINOUTS

| Digital I/O: J1 | |
|---|---|
| **Pin #** | **Function** |
| 19 | Port A, line 0 |
| 21 | Port A, line 1 |
| 23 | Port A, line 2 |
| 25 | Port A, line 3 |
| 24 | Port A, line 4 |
| 22 | Port A, line 5 |
| 20 | Port A, line 6 |
| 18 | Port A, line 7 |
| 10 | Port B, line 0 |
| 8 | Port B, line 1 |
| 4 | Port B, line 2 |
| 6 | Port B, line 3 |
| 1 | Port B, line 4 |
| 3 | Port B, line 5 |
| 5 | Port B, line 6 |
| 7 | Port B, line 7 |
| 13 | Port C, line 0 |
| 16 | Port C, line 1 |
| 15 | Port C, line 2 |
| 17 | Port C, line 3 |
| 14 | Port C, line 4 |
| 11 | Port C, line 5 |
| 12 | Port C, line 6 |
| 9 | Port C, line 7 |
| 2 | +5V |
| 26 | Gnd |

| Analog Connector: J2 | | | |
|---|---|---|---|
| **Single-Ended** | **Pin #** | **Single-Ended** | **Pin #** |
| IN 0 | 1 | IN 5 | 11 |
| GND | 2 | GND | 12 |
| IN 1 | 3 | IN 6 | 13 |
| GND | 4 | GND | 14 |
| IN 2 | 5 | IN 7 | 15 |
| GND | 6 | GND | 16 |
| IN 3 | 7 | Reserved | 17 |
| GND | 8 | Reserved | 18 |
| IN 4 | 9 | Reserved | 19 |
| GND | 10 | Reserved | 20 |

## PC BUS PINOUTS

| Micro PC "A" | | | | | |
|---|---|---|---|---|---|
| **Pin #** | **Description** | **Signal** | **Pin #** | **Description** | **Signal** |
| A1 | I/O CH CK* | O | A17 | A14 | I |
| A2 | D7 | I/O | A18 | A13 | I |
| A3 | D6 | I/O | A19 | A12 | I |
| A4 | D5 | I/O | A20 | A11 | I |
| A5 | D4 | I/O | A21 | A10 | I |
| A6 | D3 | I/O | A22 | A9 | I |
| A7 | D2 | I/O | A23 | A8 | I |
| A8 | D1 | I/O | A24 | A7 | I |
| A9 | D0 | I/O | A25 | A6 | I |
| A10 | I/O CH RDY | O | A26 | A5 | I |
| A11 | AEN | I | A27 | A4 | I |
| A12 | A19 | I | A28 | A3 | I |
| A13 | A18 | I | A29 | A2 | I |
| A14 | A17 | I | A30 | A1 | I |
| A15 | A16 | I | A31 | A0 | I |
| A16 | A15 | I | | | |

* = active low

| Micro PC "B" | | | | | |
|---|---|---|---|---|---|
| **Pin #** | **Description** | **Signal** | **Pin #** | **Description** | **Signal** |
| B1 | GND | I | B17 | DACKI* | I |
| B2 | RESET | I | B18 | DRQ1 | O |
| B3 | +5V | O | B19 | DACK0* | I |
| B4 | IRQ2 | O | B20 | CLOCK | I |
| B5 | -5V | Not used | B21 | IRQ7 | O |
| B6 | DRQ2 | O | B22 | IRQ6 | O |
| B7 | -12V | O | B23 | IRQ5 | O |
| B8 | Reserved | Not used | B24 | IRQ4 | O |
| B9 | +12V | O | B25 | IRQ3 | O |
| B10 | Analog Gnd | O | B26 | DACK2* | O |
| B11 | MEMW* | I | B27 | T/C | O |
| B12 | MEMR* | I | B28 | ALE | I |
| B13 | IOW* | I | B29 | Aux +5V | O |
| B14 | IOR* | I | B30 | OSC | I |
| B15 | DACK3* | I | B31 | Aux Gnd | O |
| B16 | DRQ3 | O | | | |

* = active low

## INTEL 82C55A DATA SHEET

intel.

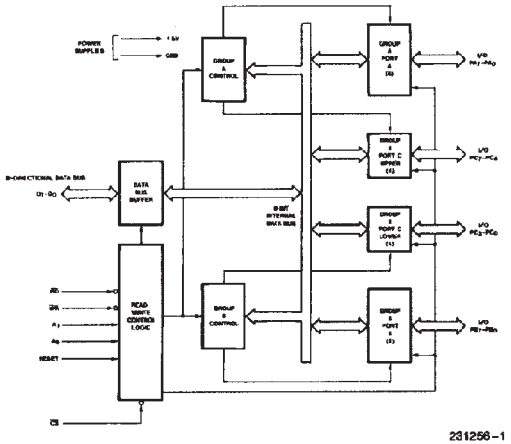
# 82C55A
# CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **Compatible with all Intel and Most Other Microprocessors**
- **High Speed, "Zero Wait State" Operation with 5 MHz 8086/88 and 80186/188**
- **24 Programmable I/O Pins**
- **Low Power CHMOS**
- **Completely TTL Compatible**
- **Control Word Read-Back Capability**
- **Direct Bit Set/Reset Capability**
- **2.5 mA DC Drive Capability on all I/O Port Outputs**
- **Available in 40-Pin DIP and 44-Pin PLCC**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

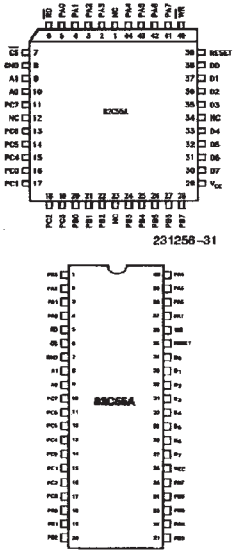
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.




231256-1

**Figure 1. 82C55A Block Diagram**




231256-31

231256-2

**Figure 2. 82C55A Pinout**
Diagrams are for pin reference only. Package sizes are not to scale.


**Order Number: 231256-004**

**Table 1. Pin Description**

| Symbol | Pin Number Dip | Pin Number PLCC | Type | Name and Function |
|---|---|---|---|---|
| $PA_{3-0}$ | 1–4 | 2–5 | I/O | **PORT A, PINS 0–3:** Lower nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch. |
| $\overline{RD}$ | 5 | 6 | I | **READ CONTROL:** This input is low during CPU read operations. |
| $\overline{CS}$ | 6 | 7 | I | **CHIP SELECT:** A low on this input enables the 82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise. |
| GND | 7 | 8 | | **System Ground** |
| $A_{1-0}$ | 8–9 | 9–10 | I | **ADDRESS:** These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers. |

| $A_1$ | $A_0$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | Input Operation (Read) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | Port A - Data Bus |
| 0 | 1 | 0 | 1 | 0 | Port B - Data Bus |
| 1 | 0 | 0 | 1 | 0 | Port C - Data Bus |
| 1 | 1 | 0 | 1 | 0 | Control Word - Data Bus |
| | | | | | **Output Operation (Write)** |
| 0 | 0 | 1 | 0 | 0 | Data Bus - Port A |
| 0 | 1 | 1 | 0 | 0 | Data Bus - Port B |
| 1 | 0 | 1 | 0 | 0 | Data Bus - Port C |
| 1 | 1 | 1 | 0 | 0 | Data Bus - Control |
| | | | | | **Disable Function** |
| X | X | X | X | 1 | Data Bus - 3 - State |
| X | X | 1 | 1 | 0 | Data Bus - 3 - State |

| | | | | |
|---|---|---|---|---|
| $PC_{7-4}$ | 10–13 | 11,13–15 | I/O | **PORT C, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. |
| $PC_{0-3}$ | 14–17 | 16–19 | I/O | **PORT C, PINS 0–3:** Lower nibble of Port C. |
| $PB_{0-7}$ | 18–25 | 20–22, 24–28 | I/O | **PORT B, PINS 0–7:** An 8-bit data output latch/buffer and an 8-bit data input buffer. |
| $V_{CC}$ | 26 | 29 | | **SYSTEM POWER:** + 5V Power Supply. |
| $D_{7-0}$ | 27–34 | 30–33, 35–38 | I/O | **DATA BUS:** Bi-directional, tri-state data bus lines, connected to system data bus. |
| RESET | 35 | 39 | I | **RESET:** A high on this input clears the control register and all ports are set to the input mode. |
| $\overline{WR}$ | 36 | 40 | I | **WRITE CONTROL:** This input is low during CPU write operations. |
| $PA_{7-4}$ | 37–40 | 41–44 | I/O | **PORT A, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch. |
| NC | | 1, 12, 23, 34 | | No Connect |

## 82C55A FUNCTIONAL DESCRIPTION

### General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

### Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

### Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

### Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7–C4)
Control Group B - Port B and Port C lower (C3–C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

### Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

**Port A.** One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

**Port B.** One 8-bit data input/output latch/buffer. Only "pull-up" bus hold devices are present on Port B.

**Port C.** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.

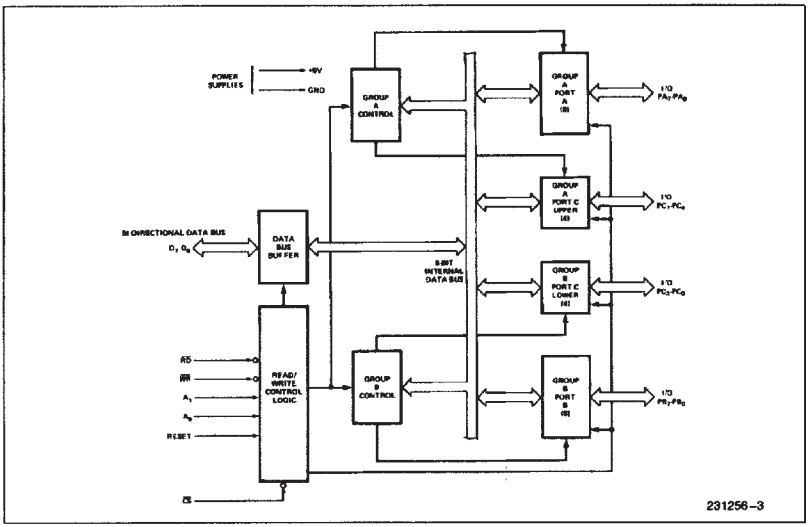
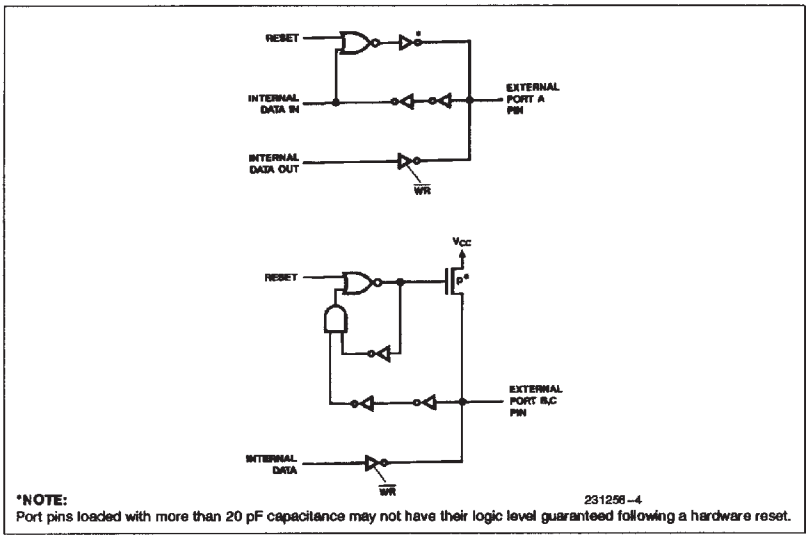



**Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions**




*NOTE:
Port pins loaded with more than 20 pF capacitance may not have their logic level guaranteed following a hardware reset.

**Figure 4. Port A, B, C, Bus-hold Configuration**

## 82C55A OPERATIONAL DESCRIPTION

### Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic input/output
Mode 1 — Strobed Input/output
Mode 2 — Bi-directional Bus

When the reset input goes "high" all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus hold devices (see Figure 4 Note). After the reset is removed the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

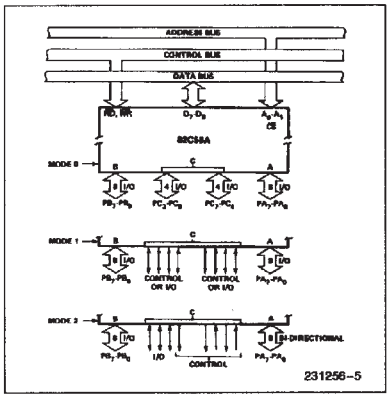



**Figure 5. Basic Mode Definitions and Bus Interface**

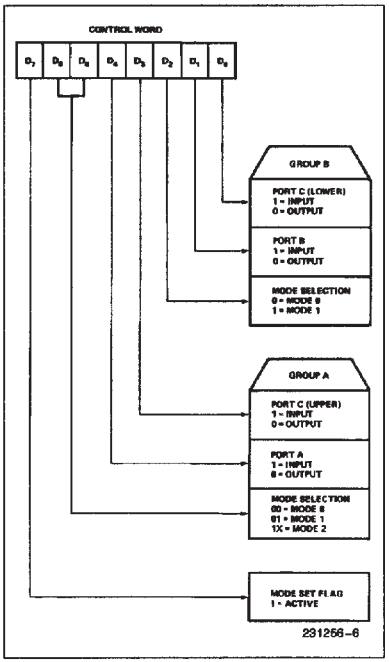



**Figure 6. Mode Definition Format**

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

### Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

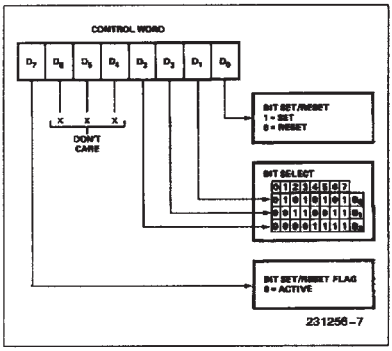



**Figure 7. Bit Set/Reset Format**

**Interrupt Control Functions**

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is SET—Interrupt enable
(BIT-RESET)—INTE is RESET—Interrupt disable

**Note:**
All Mask flip-flops are automatically reset during mode selection and device Reset.

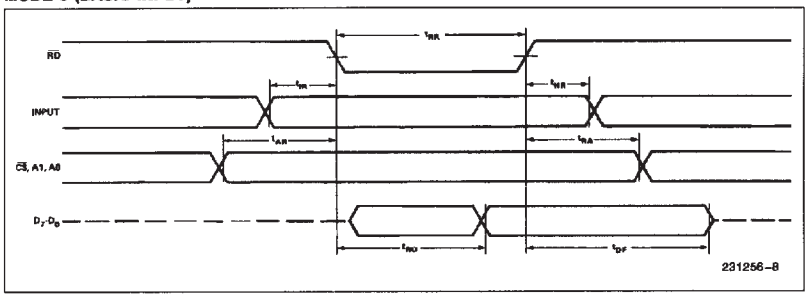
**Operating Modes**

**Mode 0 (Basic Input/Output).** This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

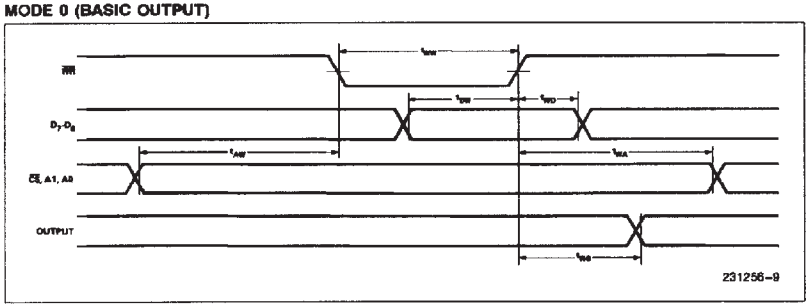
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

**MODE 0 (BASIC INPUT)**



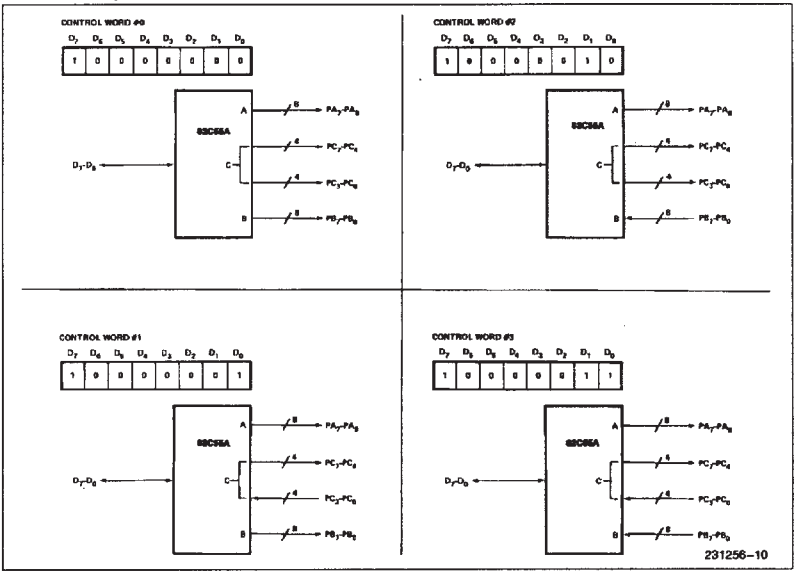

**MODE 0 (BASIC OUTPUT)**



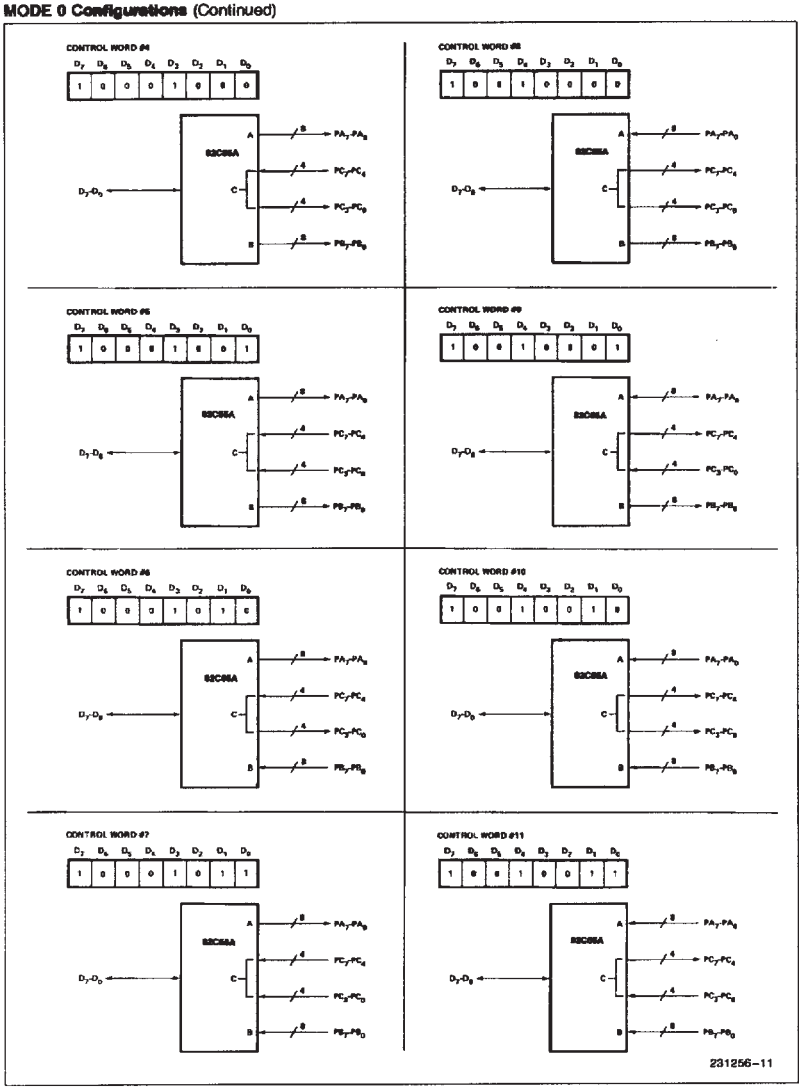
**MODE 0 Port Definition**

| A | | B | | GROUP A | | | GROUP B | |
|---|---|---|---|---|---|---|---|---|
| $D_4$ | $D_3$ | $D_1$ | $D_0$ | PORT A | PORT C (UPPER) | # | PORT B | PORT C (LOWER) |
| 0 | 0 | 0 | 0 | OUTPUT | OUTPUT | 0 | OUTPUT | OUTPUT |
| 0 | 0 | 0 | 1 | OUTPUT | OUTPUT | 1 | OUTPUT | INPUT |
| 0 | 0 | 1 | 0 | OUTPUT | OUTPUT | 2 | INPUT | OUTPUT |
| 0 | 0 | 1 | 1 | OUTPUT | OUTPUT | 3 | INPUT | INPUT |
| 0 | 1 | 0 | 0 | OUTPUT | INPUT | 4 | OUTPUT | OUTPUT |
| 0 | 1 | 0 | 1 | OUTPUT | INPUT | 5 | OUTPUT | INPUT |
| 0 | 1 | 1 | 0 | OUTPUT | INPUT | 6 | INPUT | OUTPUT |
| 0 | 1 | 1 | 1 | OUTPUT | INPUT | 7 | INPUT | INPUT |
| 1 | 0 | 0 | 0 | INPUT | OUTPUT | 8 | OUTPUT | OUTPUT |
| 1 | 0 | 0 | 1 | INPUT | OUTPUT | 9 | OUTPUT | INPUT |
| 1 | 0 | 1 | 0 | INPUT | OUTPUT | 10 | INPUT | OUTPUT |
| 1 | 0 | 1 | 1 | INPUT | OUTPUT | 11 | INPUT | INPUT |
| 1 | 1 | 0 | 0 | INPUT | INPUT | 12 | OUTPUT | OUTPUT |
| 1 | 1 | 0 | 1 | INPUT | INPUT | 13 | OUTPUT | INPUT |
| 1 | 1 | 1 | 0 | INPUT | INPUT | 14 | INPUT | OUTPUT |
| 1 | 1 | 1 | 1 | INPUT | INPUT | 15 | INPUT | INPUT |

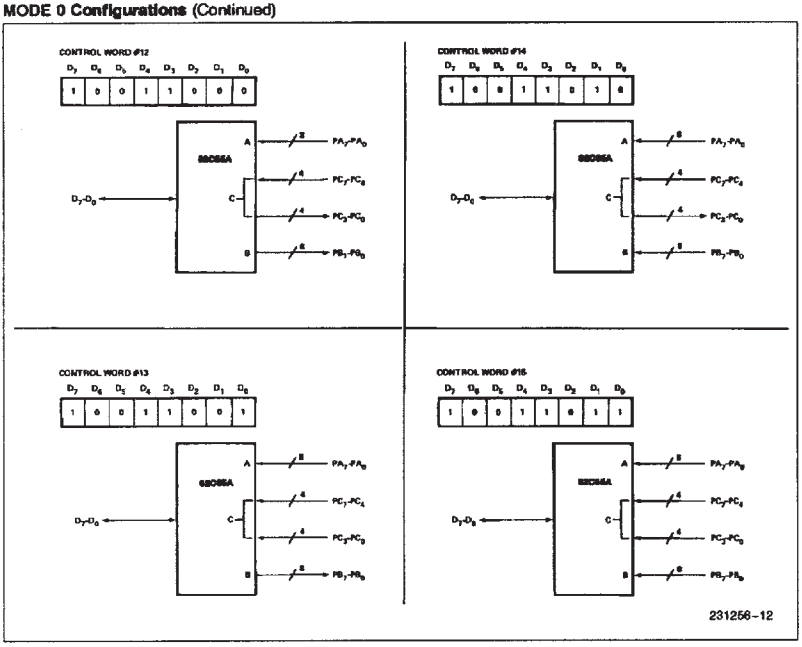
**MODE 0 Configurations**



**MODE 0 Configurations** (Continued)



**MODE 0 Configurations** (Continued)




### Operating Modes

**MODE 1 (Strobed Input/Output).** This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

**Input Control Signal Definition**

**$\overline{STB}$ (Strobe Input).** A "low" on this input loads data into the input latch.

**IBF (Input Buffer Full F/F)**

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

**INTR (Interrupt Request)**

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

**INTE A**

Controlled by bit set/reset of $PC_4$.

**INTE B**

Controlled by bit set/reset of $PC_2$.

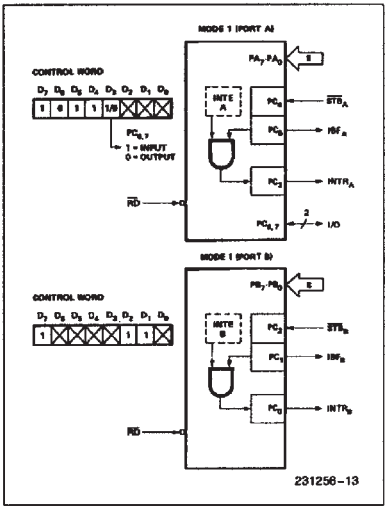



**Figure 8. MODE 1 Input**

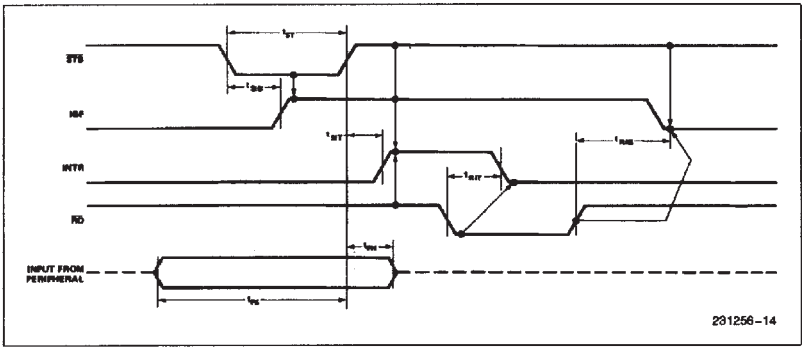



**Figure 9. MODE 1 (Strobed Input)**

**Output Control Signal Definition**

**$\overline{OBF}$ (Output Buffer Full F/F).** The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

**$\overline{ACK}$ (Acknowledge Input).** A "low" on this input informs the 82C55A that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

**INTR (Interrupt Request).** A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

**INTE A**

Controlled by bit set/reset of $PC_6$.

**INTE B**

Controlled by bit set/reset of $PC_2$.

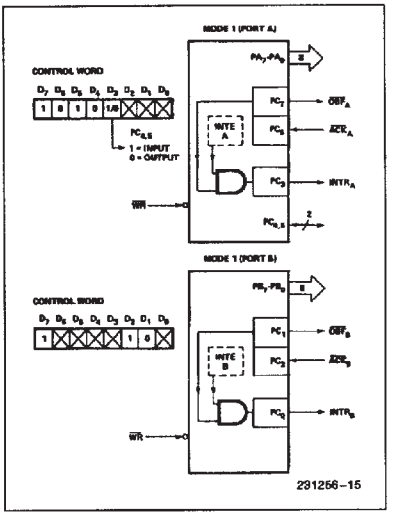



**Figure 10. MODE 1 Output**

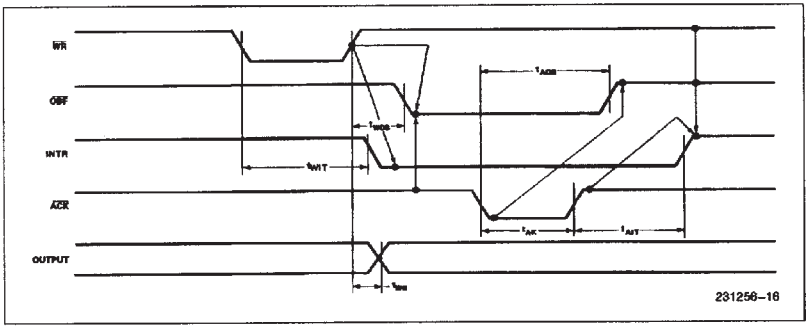



**Figure 11. MODE 1 (Strobed Output)**

**Combinations of MODE 1**

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

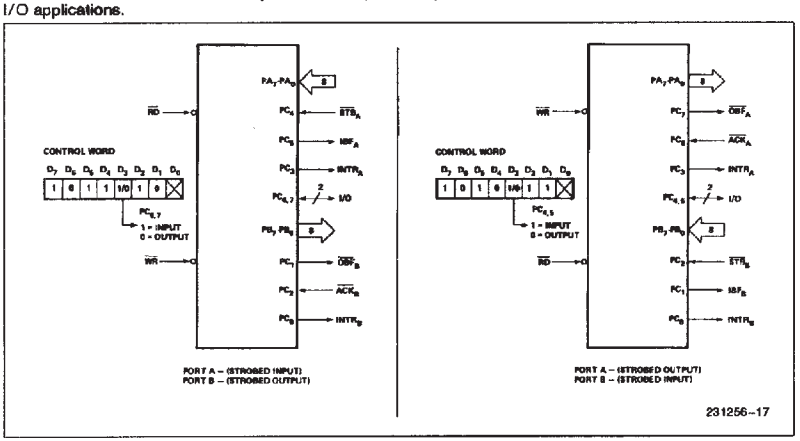



**Figure 12. Combinations of MODE 1**

**Operating Modes**

**MODE 2 (Strobed Bidirectional Bus I/O).** This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A **only.**
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

**Bidirectional Bus I/O Control Signal Definition**

**INTR (Interrupt Request).** A high on this output can be used to interrupt the CPU for input or output operations.

**Output Operations**

**$\overline{OBF}$ (Output Buffer Full).** The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

**$\overline{ACK}$ (Acknowledge).** A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

**INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$).** Controlled by bit set/reset of $PC_6$.

**Input Operations**

**$\overline{STB}$ (Strobe Input).** A "low" on this input loads data into the input latch.

**IBF (Input Buffer Full F/F).** A "high" on this output indicates that data has been loaded into the input latch.

**INTE 2 (The INTE Flip-Flop Associated with IBF).** Controlled by bit set/reset of $PC_4$.

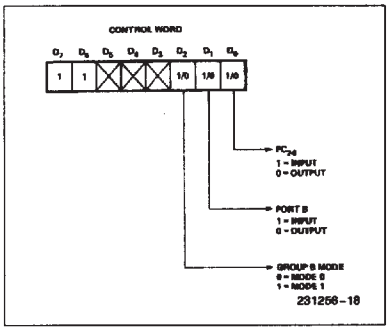



Figure 13. MODE Control Word

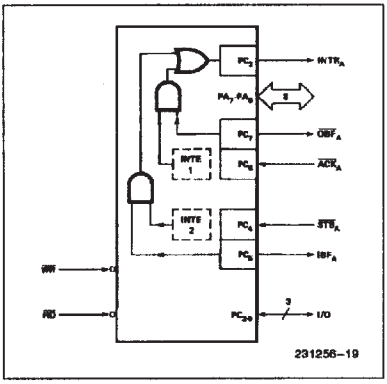



Figure 14. MODE 2

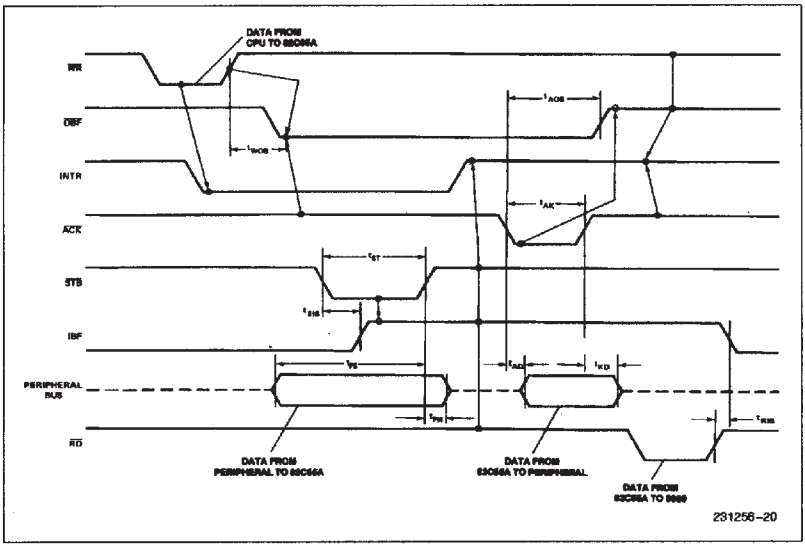



Figure 15. MODE 2 (Bidirectional)

**NOTE:**
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

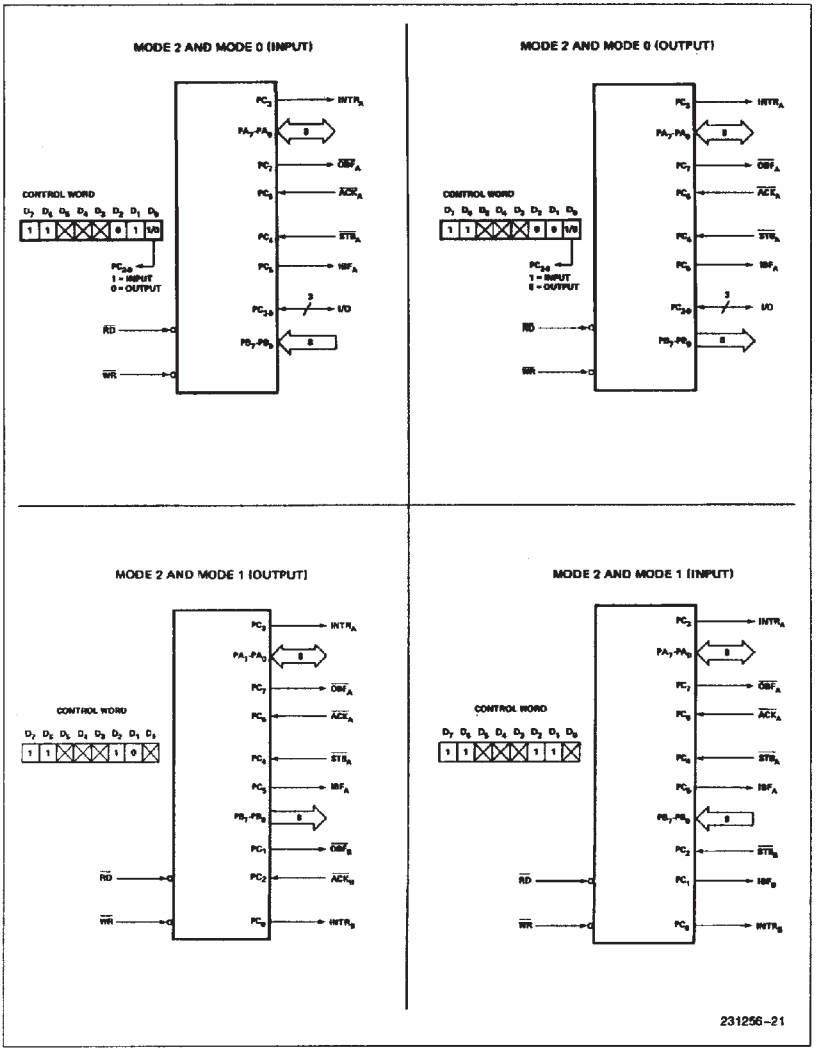



**Figure 16. MODE ¼ Combinations**

**Mode Definition Summary**

| | MODE 0 | | MODE 1 | | MODE 2 |
|---|---|---|---|---|---|
| | IN | OUT | IN | OUT | GROUP A ONLY |
| $PA_0$ | IN | OUT | IN | OUT | ⟷ |
| $PA_1$ | IN | OUT | IN | OUT | ⟷ |
| $PA_2$ | IN | OUT | IN | OUT | ⟷ |
| $PA_3$ | IN | OUT | IN | OUT | ⟷ |
| $PA_4$ | IN | OUT | IN | OUT | ⟷ |
| $PA_5$ | IN | OUT | IN | OUT | ⟷ |
| $PA_6$ | IN | OUT | IN | OUT | ⟷ |
| $PA_7$ | IN | OUT | IN | OUT | ⟷ |
| $PB_0$ | IN | OUT | IN | OUT | — |
| $PB_1$ | IN | OUT | IN | OUT | — |
| $PB_2$ | IN | OUT | IN | OUT | — |
| $PB_3$ | IN | OUT | IN | OUT | — |
| $PB_4$ | IN | OUT | IN | OUT | — |
| $PB_5$ | IN | OUT | IN | OUT | — |
| $PB_6$ | IN | OUT | IN | OUT | — |
| $PB_7$ | IN | OUT | IN | OUT | — |
| $PC_0$ | IN | OUT | $INTR_B$ | $INTR_B$ | I/O |
| $PC_1$ | IN | OUT | $IBF_B$ | $\overline{OBF}_B$ | I/O |
| $PC_2$ | IN | OUT | $\overline{STB}_B$ | $\overline{ACK}_B$ | I/O |
| $PC_3$ | IN | OUT | $INTR_A$ | $INTR_A$ | $INTR_A$ |
| $PC_4$ | IN | OUT | $\overline{STB}_A$ | I/O | $\overline{STB}_A$ |
| $PC_5$ | IN | OUT | $IBF_A$ | I/O | $IBF_A$ |
| $PC_6$ | IN | OUT | I/O | $\overline{ACK}_A$ | $\overline{ACK}_A$ |
| $PC_7$ | IN | OUT | I/O | $\overline{OBF}_A$ | $\overline{OBF}_A$ |

MODE 0 OR MODE 1 ONLY

**Special Mode Combination Considerations**

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 18.

**Current Drive Capability**

Any output on Port A, B or C can sink or source 2.5 mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

### Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

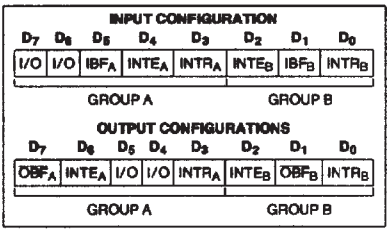



**Figure 17a. MODE 1 Status Word Format**

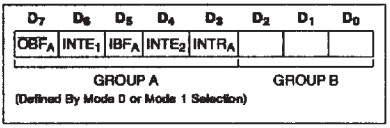



**Figure 17b. MODE 2 Status Word Format**

| Interrupt Enable Flag | Position | Alternate Port C Pin Signal (Mode) |
|---|---|---|
| INTE B | PC2 | $\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1) |
| INTE A2 | PC4 | $\overline{STB}_A$ (Input Mode 1 or Mode 2) |
| INTE A1 | PC6 | $\overline{ACK}_A$ (Output Mode 1 or Mode 2 |

**Figure 18. Interrupt Enable Flags in Modes 1 and 2**

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias....0°C to + 70°C
Storage Temperature .....– 65°C to + 150°C
Supply Voltage .....– 0.5 to + 8.0V
Operating Voltage .....+ 4V to + 7V
Voltage on any Input.....GND – 2V to + 6.5V
Voltage on any Output ..GND – 0.5V to $V_{CC}$ + 0.5V
Power Dissipation .....1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

## D.C. CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±10%, GND = 0V ($T_A$ = –40°C to +85°C for Extended Temperture)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | –0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 2.5 mA |
| $V_{OH}$ | Output High Voltage | 3.0<br>$V_{CC}$ – 0.4 | | V<br>V | $I_{OH}$ = –2.5 mA<br>$I_{OH}$ = –100 µA |
| $I_{IL}$ | Input Leakage Current | | ±1 | µA | $V_{IN}$ = $V_{CC}$ to 0V (Note 1) |
| $I_{OFL}$ | Output Float Leakage Current | | ±10 | µA | $V_{IN}$ = $V_{CC}$ to 0V (Note 2) |
| $I_{DAR}$ | Darlington Drive Current | ±2.5 | (Note 4) | mA | Ports A, B, C<br>$R_{ext}$ = 500Ω<br>$V_{ext}$ = 1.7V |
| $I_{PHL}$ | Port Hold Low Leakage Current | +50 | +300 | µA | $V_{OUT}$ = 1.0V<br>Port A only |
| $I_{PHH}$ | Port Hold High Leakage Current | –50 | –300 | µA | $V_{OUT}$ = 3.0V<br>Ports A, B, C |
| $I_{PHLO}$ | Port Hold Low Overdrive Current | –350 | | µA | $V_{OUT}$ = 0.8V |
| $I_{PHHO}$ | Port Hold High Overdrive Current | +350 | | µA | $V_{OUT}$ = 3.0V |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 10 | mA | (Note 3) |
| $I_{CCSB}$ | $V_{CC}$ Supply Current-Standby | | 10 | µA | $V_{CC}$ = 5.5V<br>$V_{IN}$ = $V_{CC}$ or GND<br>Port Conditions<br>If I/P = Open/High<br>O/P = Open Only<br>With Data Bus =<br>High/Low<br>$\overline{CS}$ = High<br>Reset = Low<br>Pure Inputs =<br>Low/High |

**NOTES:**
1. Pins $A_1$, $A_0$, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset.
2. Data Bus; Ports B, C.
3. Outputs open.
4. Limit output current to 4.0 mA.

## CAPACITANCE

$T_A$ = 25°C, $V_{CC}$ = GND = 0V

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF | Unmeasured pins returned to GND $f_c$ = 1 MHz(5) |
| $C_{I/O}$ | I/O Capacitance | | 20 | pF | |

**NOTE:**
5. Sampled not 100% tested.

## A.C. CHARACTERISTICS

$T_A$ = 0° to 70°C, $V_{CC}$ = +5V ±10%, GND = 0V

$T_A$ = −40°C to +85°C for Extended Temperature

### BUS PARAMETERS

#### READ CYCLE

| Symbol | Parameter | 82C55A-2 | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{AR}$ | Address Stable Before $\overline{RD}\downarrow$ | 0 | | ns | |
| $t_{RA}$ | Address Hold Time After $\overline{RD}\uparrow$ | 0 | | ns | |
| $t_{RR}$ | $\overline{RD}$ Pulse Width | 150 | | ns | |
| $t_{RD}$ | Data Delay from $\overline{RD}\downarrow$ | | 120 | ns | |
| $t_{DF}$ | $\overline{RD}\uparrow$ to Data Floating | 10 | 75 | ns | |
| $t_{RV}$ | Recovery Time between $\overline{RD}/\overline{WR}$ | 200 | | ns | |

#### WRITE CYCLE

| Symbol | Parameter | 82C55A-2 | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{AW}$ | Address Stable Before $\overline{WR}\downarrow$ | 0 | | ns | |
| $t_{WA}$ | Address Hold Time After $\overline{WR}\uparrow$ | 20 | | ns | Ports A & B |
| | | 20 | | ns | Port C |
| $t_{WW}$ | $\overline{WR}$ Pulse Width | 100 | | ns | |
| $t_{DW}$ | Data Setup Time Before $\overline{WR}\uparrow$ | 100 | | ns | |
| $t_{WD}$ | Data Hold Time After $\overline{WR}\uparrow$ | 30 | | ns | Ports A & B |
| | | 30 | | ns | Port C |

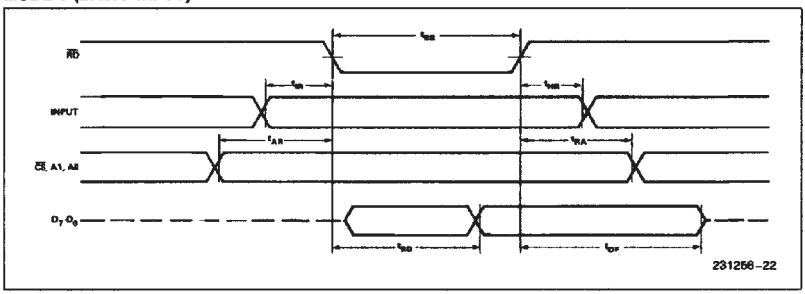
**OTHER TIMINGS**

| Symbol | Parameter | 82C55A-2 | | Units Conditions | Test |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{WB}$ | $\overline{WR}$ = 1 to Output | | 350 | ns | |
| $t_{IR}$ | Peripheral Data Before $\overline{RD}$ | 0 | | ns | |
| $t_{HR}$ | Peripheral Data After $\overline{RD}$ | 0 | | ns | |
| $t_{AK}$ | $\overline{ACK}$ Pulse Width | 200 | | ns | |
| $t_{ST}$ | $\overline{STB}$ Pulse Width | 100 | | ns | |
| $t_{PS}$ | Per. Data Before $\overline{STB}$ High | 20 | | ns | |
| $t_{PH}$ | Per. Data After $\overline{STB}$ High | 50 | | ns | |
| $t_{AD}$ | $\overline{ACK}$ = 0 to Output | | 175 | ns | |
| $t_{KD}$ | $\overline{ACK}$ = 1 to Output Float | 20 | 250 | ns | |
| $t_{WOB}$ | $\overline{WR}$ = 1 to $\overline{OBF}$ = 0 | | 150 | ns | |
| $t_{AOB}$ | $\overline{ACK}$ = 0 to $\overline{OBF}$ = 1 | | 150 | ns | |
| $t_{SIB}$ | $\overline{STB}$ = 0 to IBF = 1 | | 150 | ns | |
| $t_{RIB}$ | $\overline{RD}$ = 1 to IBF = 0 | | 150 | ns | |
| $t_{RIT}$ | $\overline{RD}$ = 0 to INTR = 0 | | 200 | ns | |
| $t_{SIT}$ | $\overline{STB}$ = 1 to INTR = 1 | | 150 | ns | |
| $t_{AIT}$ | $\overline{ACK}$ = 1 to INTR = 1 | | 150 | ns | |
| $t_{WIT}$ | $\overline{WR}$ = 0 to INTR = 0 | | 200 | ns | see note 1 |
| $t_{RES}$ | Reset Pulse Width | 500 | | ns | see note 2 |

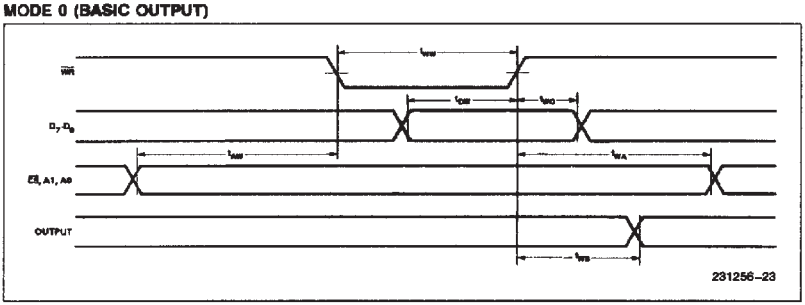
**NOTE:**
1. INTR ↑ may occur as early as $\overline{WR}$ ↓.
2. Pulse width of initial Reset pulse after power on must be at least 50 µSec. Subsequent Reset pulses may be 500 ns minimum.

## WAVEFORMS

### MODE 0 (BASIC INPUT)

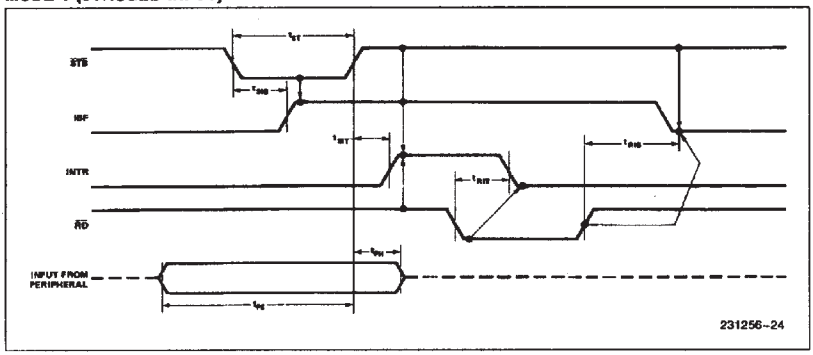



### MODE 0 (BASIC OUTPUT)

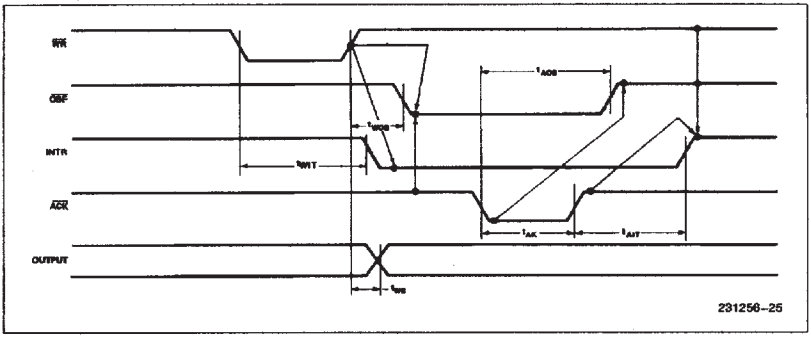


**WAVEFORMS** (Continued)

**MODE 1 (STROBED INPUT)**

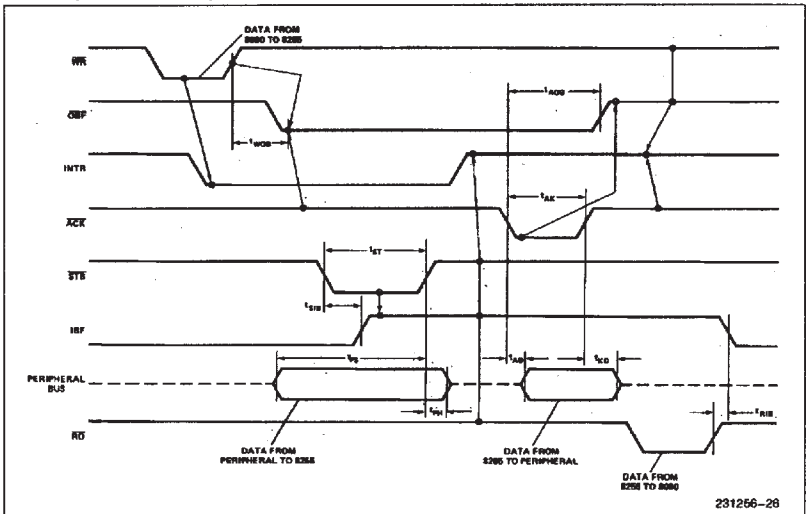



**MODE 1 (STROBED OUTPUT)**



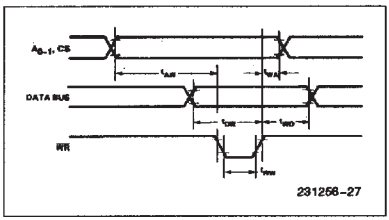
## WAVEFORMS (Continued)

### MODE 2 (BIDIRECTIONAL)

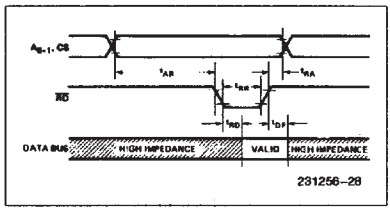



**Note:**
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ AND $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

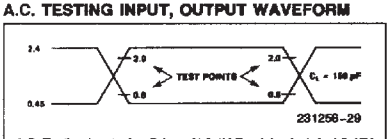
### WRITE TIMING




### READ TIMING

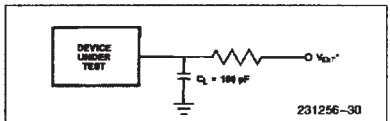



### A.C. TESTING INPUT, OUTPUT WAVEFORM




A.C. Testing Inputs Are Driven At 2.4V For A Logic 1 And 0.45V For A Logic 0 Timing Measurements Are Made At 2.0V For A Logic 1 And 0.8 For A Logic 0.

### A.C. TESTING LOAD CIRCUIT




*$V_{EXT}$ Is Set At Various Voltages During Testing To Guarantee The Specification. $C_L$ Includes Jig Capacitance.

# WARRANTY

Octagon Systems Corporation (Octagon), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the current established warranty period. Octagon's obligation under this warranty shall not arise until Buyer returns the defective product, freight prepaid to Octagon's facility or another specified location. Octagon's only responsibility under this warranty is, at its option, to replace or repair, free of charge, any defective component part of such products.

## LIMITATIONS ON WARRANTY

The warranty set forth above does not extend to and shall not apply to:

1. Products, including software, which have been repaired or altered by other than Octagon personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Octagon.
2. Products which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.
3. The design, capability, capacity, or suitability for use of the Software. Software is licensed on an "AS IS" basis without warranty.

The warranty and remedies set forth above are in lieu of all other warranties expressed or implied, oral or written, either in fact or by operation of law, statutory or otherwise, including warranties of merchantability and fitness for a particular purpose, which Octagon specifically disclaims. Octagon neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Octagon shall have no liability for incidental or consequential damages of any kind arising out of the sale, delay in delivery, installation, or use of its products.

## SERVICE POLICY

1. Octagon's goal is to ship your product within 10 working days of receipt.
2. If a product should fail during the warranty period, it will be repaired free of charge. For out–of–warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.
3. Customers that return products for repairs, within the warranty period, and the product is found to be free of defect, may be liable for the minimum current repair charge.

## RETURNING A PRODUCT FOR REPAIR

Upon determining that repair services are required, the customer must:

1. Obtain an RMA (Return Material Authorization) number from the Customer Service Department, 303-430–1500.
2. If the request is for an out of warranty repair, a purchase order number or other acceptable information must be supplied by the customer.
3. Include a list of problems encountered along with your name, address, telephone, and RMA number.
4. Carefully package the product in an antistatic bag. (Failure to package in antistatic material will VOID all warranties.) Then package in a safe container for shipping.
5. Write RMA number on the outside of the box.
6. For products under warranty, the customer pays for shipping to Octagon. Octagon pays for shipping back to customer.
7. Other conditions and limitations may apply to international shipments.

**NOTE:** PRODUCTS RETURNED TO OCTAGON FREIGHT COLLECT OR WITHOUT AN RMA NUMBER CANNOT BE ACCEPTED AND WILL BE RETURNED FREIGHT COLLECT.

## RETURNS

There will be a 15% restocking charge on returned product that is unopened and unused, if Octagon accepts such a return. Returns will not be accepted 30 days after purchase. Opened and/or used products, non-standard products, software and printed materials are not returnable without prior written agreement.

## GOVERNING LAW

This agreement is made in, governed by and shall be construed in accordance with the laws of the State of Colorado.

The information in this manual is provided for reference only. Octagon does not assume any liability arising out of the application or use of the information or products described in this manual. This manual may contain or reference information and products protected by copyrights or patents. No license is conveyed under the rights of Octagon or others.