PT4

User Manual

Multi-standard Video Decoder IP core with sample rate converter

Revision 0.1
5th November 2015

Revisions

Date	Revisions	Version
05-11-2015	First draft	0.1

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1. Introduction

PT4 is a video decoder accepting all NTSC and PAL encoded composite video inputs, including 960H – 36MHz sampling, and 1280H – 54MHz sampling, and producing an adaptive 2D (line) combed component output with 10 bit BT656 formatted output.

The input to the IP core is 10-bit digital composite video.

PT4 has two synchronization modes:

1. The PT4 provides a PWM output to control an analogue voltage controlled oscillator at a nominal frequency of 27/36/54MHz. All sync separation is performed by the PT4. This is the default mode of operation.
2. The input is fixed 27/36/54MHz clock frequency. The PT4 rate converts this internally using a sample rate converter and digital PLL. This allows the PT4 to accept inputs from video demodulators without re-sampling as well as accepting wide range inputs such as from a VCR or laser disc. All sync separation is also performed internally to the PT4.

The composite video input is passed through a decimating sample rate converter (in sync mode 2 – in sync mode 1 this is bypassed) which interpolates the data down to an average 13.5/18/27MHz output locked to the video line frequency. A numerical controlled oscillator determines the phase of the interpolation. The output from the SRC is the 13.5/18/27MHz interpolated video and a video enable signal which indicates a valid sample.

The decoder is a complementary design. The colour burst from the input composite video is used to phase lock the subcarrier oscillator which then addresses a sine and cosine LUT. These waveforms are used to demodulate the colour component of the composite waveform. The resulting U and V colour components are then low pass filtered and re-modulated using the delayed sine and cosine waveforms. This combined chroma signal is then subtracted from the delayed composite signal to create a notched luminance signal.

The U and V signals are then combed using a 3 line comb filter (for both NTSC and PAL) while the notched luminance is applied to compensating line delays for the comb adaptation. The amplitude difference across the comb filter taps are compared to determine which of the modes has the least error – the notch mode or the combed mode. The comb mode is selected on a pixel by pixel basis.

The difference is then taken between the U/V inputs to the comb and the selected output of the comb filter. If the filter is combing correctly that difference will be the high frequency luma signal. This HF luma is then remodulated using the delayed sine and cosine waveforms and added to the line delayed notched luma to create a full bandwidth luma output, (when in comb mode).

This luma signal and the combed U and V are then amplified and scaled in the processing amplifier before being formatted to a BT656 10-bit output at 27/36/54MHz suitable for driving a DAC or for further video processing.

The notched luma signal is also used to derive the timing signals. The luma is sliced at the mid-point sync pulse amplitude and multiplied by 15 coefficients that are designed such that when the midpoint of the falling edge of the line sync pulse is coincident with the midpoint of the filter coefficients the summed output of the multiplier over that window is zero. This forms our horizontal phase detector for the line locked clock. The error value is then added to a fixed value input to a ratio counter. The lower bits of the ratio counter form a phase word which is used to drive the input sample rate interpolator or converted to a PWM output to drive the control voltage of the external voltage controlled oscillator.

The composite video is also filtered to remove noise and chroma and the horizontal line locked counter is used to extract the vertical sync and determine the odd/even frame

information. This ‘raw’ horizontal and vertical sync information is fed to a sync pulse generator which produces all the synchronising signals required for the decoder.

Control and status registers are written to and read from using a conventional 8 bit wide microprocessor interface.

2. PT4 File Structure

PT4 is supplied as a flat file structure but the design is hierarchical. The top level design file is called PT4.v, a Verilog file; all inputs and outputs to the decoder come from this file. The design is hierarchical with PT4 instantiating two Verilog modules; PT4_Register_control.v and Vdec.v.

Register_control.v provides the control interface to PT4. Vdec.v is the main decoder module and instantiates 18 modules, three of which instantiate a fourth level of modules.

The PT4 module hierarchy is shown in Table 1.

Top Level	Second Level	Third Level	Fourth level
PT4.v	PT4_Register Control.v		
	Vdec.v	Vid_nco.v	time_nco.v
			vid.v
			rnd_sat.v
		HPLL.v	
		SPG.v	
		BLO.v	
		Demod.v	CosSin_ROM.v
		Demod_LPF.v (UDemod_LPF.v, VDemod_LPF.v)	
		Remod.v	
		Line_delays.v	Vdec_rams.v ram_infer_generic.v
		Comb_filter.v	
		HF_remod.v	
		Proc_amp.v	
		D1_format.v	

Table 1 PT4 File Structure

3. Signal Interconnections

The PT4 graphic block symbol is shown in Figure 1.

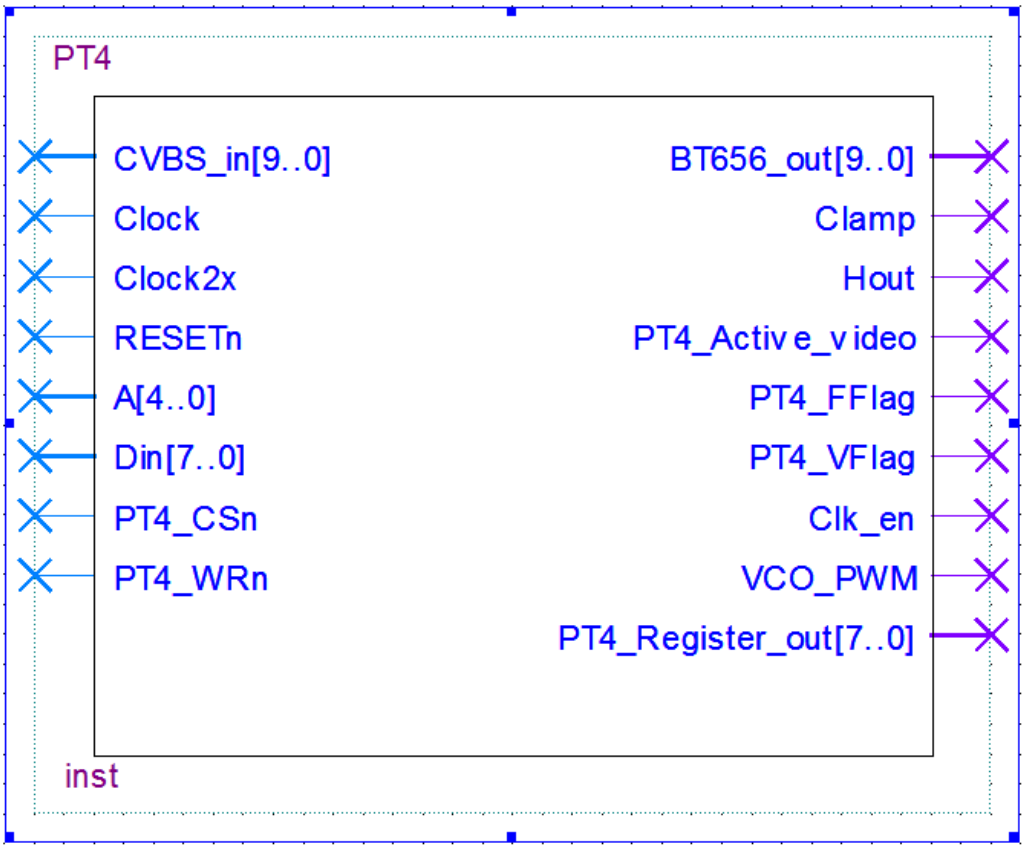

Figure 1 PT4 Block Symbol.

The PT4 signal interconnections are described in Table 2, below.

Inputs	
Signal	**Description**
CVBS_in[9:0]	Digitised composite 10 bit straight binary video input. The data should be valid during the rising edge of the 27/36/54MHz clock.
Clock	This is the free-running 27/36/54MHz to the PT4 (if using the sample rate converter – sync mode 2) or the voltage controlled oscillator input, sync mode 1 (nominal 27/36/54MHz). The rising edge of this clock is used to latch the CVBS_in data. For NTSC/PAL the clock should be 27MHz, for 960H operation the clock should be 36MHz and for 1280H operation the clock should be 54MHz.
Clock2x	Twice input clock input (54/72/108MHz) used to generate the write enables for the line comb memories. The rising edge of this clock should be coincident with the rising edge of Clock.
RESETn	Active low reset signal for all flip flops. Asserting this input sets all the control registers to their default value.

A[4:0]	Control address bus input used to select the control register to be written to/read from.
Din[7:0]	Control data input bus.
PT4_CSn	Control chip select input, active low. Used in combination with the WRn input to control writing to the control registers.
PT4_WRn	Active low write enable input. Used in combination with the PT4_CSn input to control writing to the control registers.
Outputs	
Signal	**Description**
BT656_out[9:0]	Formatted 10 bit BT656 compatible output. Data is valid on the rising edge of Clock.
Clamp	Programmable clamp pulse to analogue input stage. (See Chapter 7).
Hout	Horizontal sync output pulse.
PT4_Active_video	Active video flag (horizontal active video). Conforms to BT656 specification.
PT4_FFlag	Frame flag output (odd/even field identification). Conforms to BT656 specification.
PT4_VFlag	Field flag output (vertical blanking). Conforms to BT656 specification.
Clk_en	Data enable signal for the Y, Cb and Cr outputs (nominal 13.5/18/27MHz). See Chapter 8, 'Synchronising Modes'.
VCO_PWM	Pulse width modulated output used for the control of a voltage controlled oscillator in sync mode 1.
PT4_Register_out[7:0]	Control output data bus. Outputs the control/status register data selected by the A[4:0] bus, independent of PT4_CSn or PT4_WRn.

Table 2 PT4 Signal Interconnections

The Verilog instantiation for PT4 is shown below:

// Instantiate video decoder

```
PT4 PT4_inst
(
.CVBS_in(CVBS_in_sig) ,                          // input [9:0] CVBS_in_sig
.Clock(Clock_sig) ,                              // input  Clock_sig
.Clock2x(Clock2x_sig) ,                          // input  Clock2x_sig
.RESETn(RESETn_sig) ,                            // input  RESETn_sig
.A(A_sig) ,                                      // input [4:0] A_sig
.Din(Din_sig) ,                                  // input [7:0] Din_sig
.PT4_CSn(PT4_CSn_sig) ,                          // input  PT4_CSn_sig
.PT4_WRn(PT4_WRn_sig) ,                          // input  PT4_WRn_sig

.BT656_out(BT656_out_sig) ,                      // output [9:0] BT656_out_sig
.Clamp(Clamp_sig) ,                              // output  Clamp_sig
.Hout(Hout_sig) ,                                // output  Hout_sig
.PT4_Active_video(PT4_Active_video_sig) ,        // output  PT4_Active_video_sig
.PT4_FFlag(PT4_FFlag_sig) ,                      // output  PT4_FFlag_sig
.PT4_VFlag(PT4_VFlag_sig) ,                      // output  PT4_VFlag_sig
.Clk_en(Clk_en_sig) ,                            // output  Clk_en_sig
.VCO_PWM(VCO_PWM_sig) ,                          // output  VCO_PWM_sig
.PT4_Register_out(PT4_Register_out_sig) ,        // output [7:0] PT4_Register_out_sig
);
```

4. Input Signal Levels

The PT4 core requires the composite input levels to be within a certain range to guarantee performance although it can accommodate signals outside of this range. The typical 10-bit input codes for a 100% colour bar input are shown in Figure 2. It is not recommended that an 8 bit input is used because this will only produce a 7 bit luma output with visible contouring.

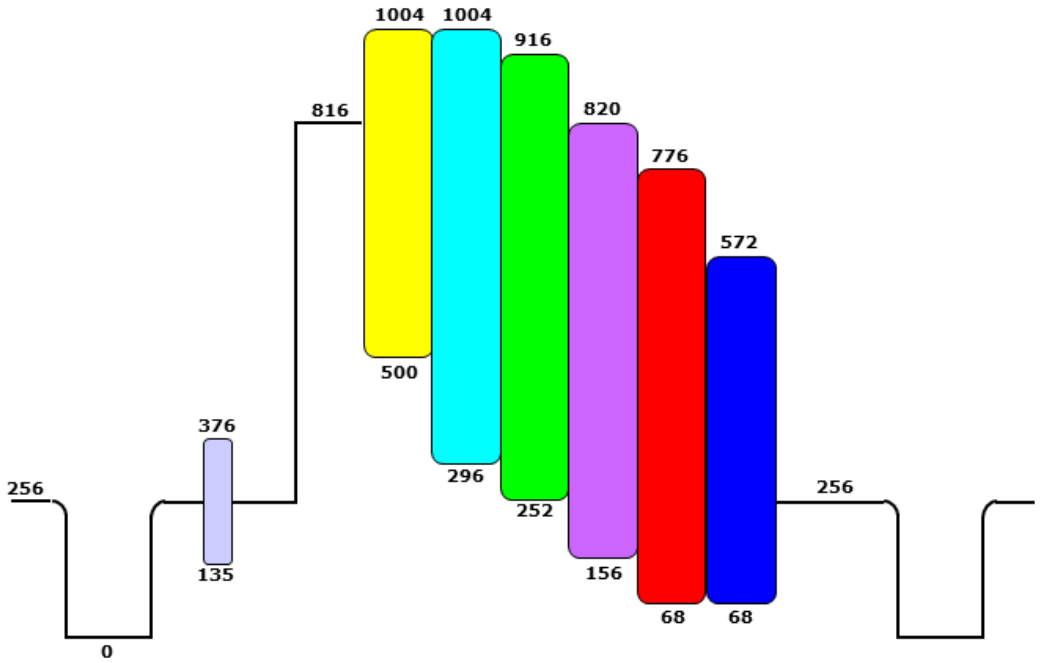

Figure 2 Input CVBS codes.

The analogue video input needs to be clamped before being applied to the ADC because the average DC level (average picture level) varies widely. A sync tip clamp is adequate as the PT4 can restore the black level automatically. A suitable circuit is shown in Chapter 6.

The resulting expected signal levels for the PT4 YCbCr outputs are shown in Table 3, below.

10-bit YCbCr signal Levels 100/0/100/0			
	Y	**Cb**	**Cr**
White	940	512	512
Yellow	840	64	585
Cyan	678	663	64
Green	578	215	137
Magenta	426	809	887
Red	326	361	960
Blue	164	960	439
Black	64	512	512

Table 3 YCbCr Output Signal Levels

5. Technical Overview

A simplified block diagram of the PT4 video decoder front end is shown in Figure 3.

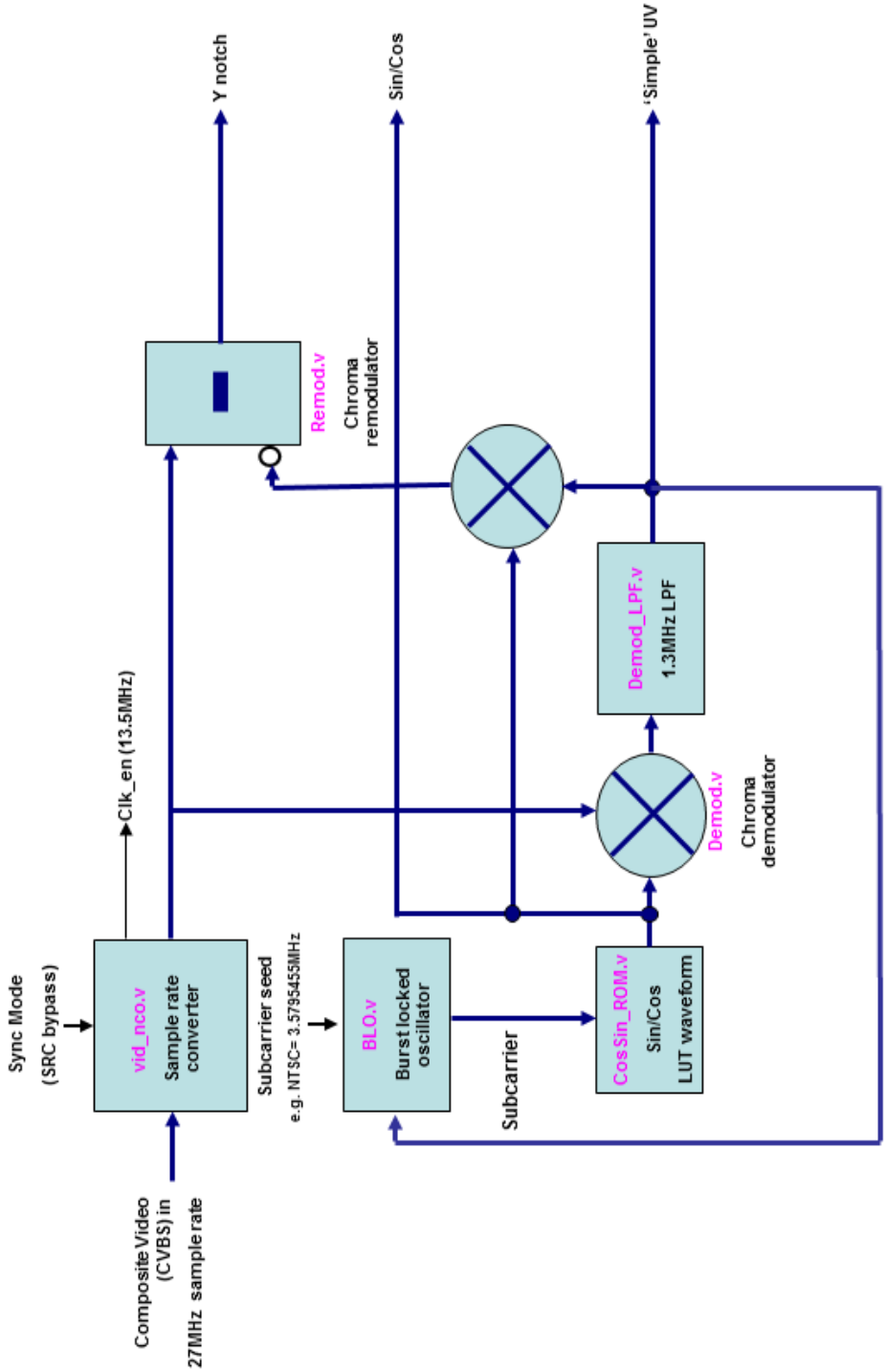

Figure 3 PT4 block diagram (Part 1).

Each of the PT4 Verilog modules is each briefly discussed below.

The input to the PT4 should be 10-bit composite video input sampled at 27MHz (NTSC/PAL), 36MHz (960H) or 54MHz (1280H), with typical input levels as shown in Figure 2. The technical description will assume 27MHz (NTSC/PAL) operation with any differences for 960H or 1280H operation noted.

PT4_Register_control.v

PT4 is controlled via a conventional 8 bit microprocessor control bus. The register interface is discussed in Chapter 10 and the register descriptions can be found in Chapter 11. Writing to a register involves setting up the required register address and strobing both PT4_CSn and PT4_WRn low. Data is written during the PT4_WRn low to high transition.

All of the control registers and the status registers are read asynchronously using the A[4:0] input to select the register. Strobing RESETn low asynchronously loads the default values into the registers.

Vid_nco.v

The role of the sample rate converter depends on the synchronisation mode selected.

In lock mode [1] the sample rate converter is bypassed and it acts only as a decimating filter, allow us to sample drop the 27MHz input to 13.5MHz.

In lock mode [2] the front end is running at a fixed 27MHz clock rate. The sample rate converter clocks a ratio counter at 27MHz and provides a 13.5MHz enable output used to gate the clock of the rest of the PT4. The ratio counter also provide a phase word which is used to interpolate the 'mid-point' of the video samples and map the incoming video onto the new clock domain. The ratio counter is adjusted by adding/subtracting a phase error signal – generated by the horizontal phase detector in the HPLL.v module – to the seed value.
The interpolator uses a Farrow structure; the output from the sample rate converter is an average 13.5MHz enable signal (Clk_en) and the interpolated composite video.

To set the PT4 to sync mode 1 (VCO mode) set register $02, bit to '1' (bypass SRC) and set register $02, bits 1:0 to '00' (set PWM output to control voltage).

To set the PT4 to sync mode 2 (SRC mode) set register $02, bit to '0' (enable SRC) and set register $02, bits 1:0 to '11' (set PWM output to fixed 50% voltage – nominal 27MHz clock. If not using a VCO then do not connect to the VCO_PWM output).

BLO.v

The subcarrier frequency appropriate to the selected colour standard is generated using a 32 bit ratio counter clocked from the 13.5MHz line locked clock.

$$ratio = \frac{\text{phase change per line}}{\text{pixels per line}} = \frac{F_{sc}}{13.5MHz} = \frac{\Delta\theta_{sc}}{360^\circ} = \frac{\text{subcarrier seed}}{2^{32}}$$

The top 11 bits of this ratio counter (the phase word) are used by the demodulator to generate the sine and cosine waveforms.

For the demodulation to correctly operate the generated subcarrier must be frequency and phase locked to the composite video subcarrier which is done by measuring the amplitude of the demodulated and low pass filtered V output during the colour burst. If the frequency and phase of the free-running subcarrier and the colour burst are the same then this error will be zero.

The reference for the BLO is the demodulated and filtered V output from the Demod_LPF. 32 samples of this waveform are taken during the burst pulse; the burst gate pulse from the SPG is used for this purpose. After the 32 samples the accumulated V demod value is stored for one line Two lines are then added for a degree of noise suppression and an error signal is then formed using fractions of the proportional signal and also a recursively filtered (integral) version. The sign of the demodulated V burst is also used by the sync pulse generator to lock up the PAL switch in the case of PAL standards.

The seed word is thus modified using the phase error signal until the input colour burst and the ratio counter are phase locked.

The subcarrier seed is selected automatically with the colour standard selected.

Demod.v

The NTSC chroma signal is originally generated as follows:

$$chroma = U\sin(\omega t) + V\cos(\omega t)$$

When the burst lock loop (BLO) is in lock, the frequency and phase will be the same as when the signal was being modulated. Thus, multiplying the composite video by the sine and cosine of the same frequency and phase gives the following:

$$U' = [U\sin(\omega t) + V\cos(\omega t)] \times \sin(\omega t)$$

$$U' = U\sin^2(\omega t) + V\sin(\omega t)\cos(\omega t)$$

$$U' = U\left[\frac{1-\cos(2\times\omega t)}{2}\right] + \frac{V}{2}\times 2\sin(\omega t)\cos(\omega t)$$

$$U' = \frac{U}{2} - \frac{U\cos(2\times\omega t)}{2} + \frac{V\sin(2\times\omega t)}{2}$$

…and for the V component:

$$V' = [U\sin(\omega t) + V\cos(\omega t)] \times \cos(\omega t)$$

$$V' = U\sin(\omega t)\cos(\omega t) + V\cos^2(\omega t)$$

$$V' = \frac{U}{2} \times 2\sin(\omega t)\cos(\omega t) + V\left[\frac{1+\cos(2\times\omega t)}{2}\right]$$

$$V' = \frac{U\sin(2\times\omega t)}{2} + \frac{V}{2} + \frac{V\cos(2\times\omega t)}{2}$$

The lower 9 bits of the 11-bit phase output from the BLO, (burst locked oscillator), are used to address sine and cosine lookup tables. These 9 bits comprise the phase angle, at subcarrier frequency, within a single quadrant and the top two bits are the quadrant – this method saves memory by only requiring a single quadrant to be stored in the LUT. The output of the CosSin_ROM.v LUT is a 24 bit word; 12 bits cosine and 12 bits sine. The quadrant signs are used to manipulate the sine and cosine data such as to construct a full waveform. The signs are also modified by the PAL switch signal from the SPG in the case of PAL colour standards.

The reconstructed sine and cosine waveforms are then multiplied by the 13.5MHz line-locked composite video from the sample rate converter. The output of the sine channel is the demodulated U signal and the cosine channel output is the demodulated V output. Two over-range bits are catered for at the output to allow for twice subcarrier frequency components (removed by the subsequent low pass filter) and for cross-colour components (removed by the comb filter).

Demod_LPF.v

The output of the demodulator comprises twice frequency components and cross colour as well as the required base-band demodulated chroma. The output is therefore low pass filtered using a 23 tap FIR filter with a nominal -3dB bandwidth of 1.3MHz. The filter provides better than -70dB rejection of all out of band component signals. The output of the filter is the clean ‘simple’ demodulated U and V. The low pass filter response is shown below.

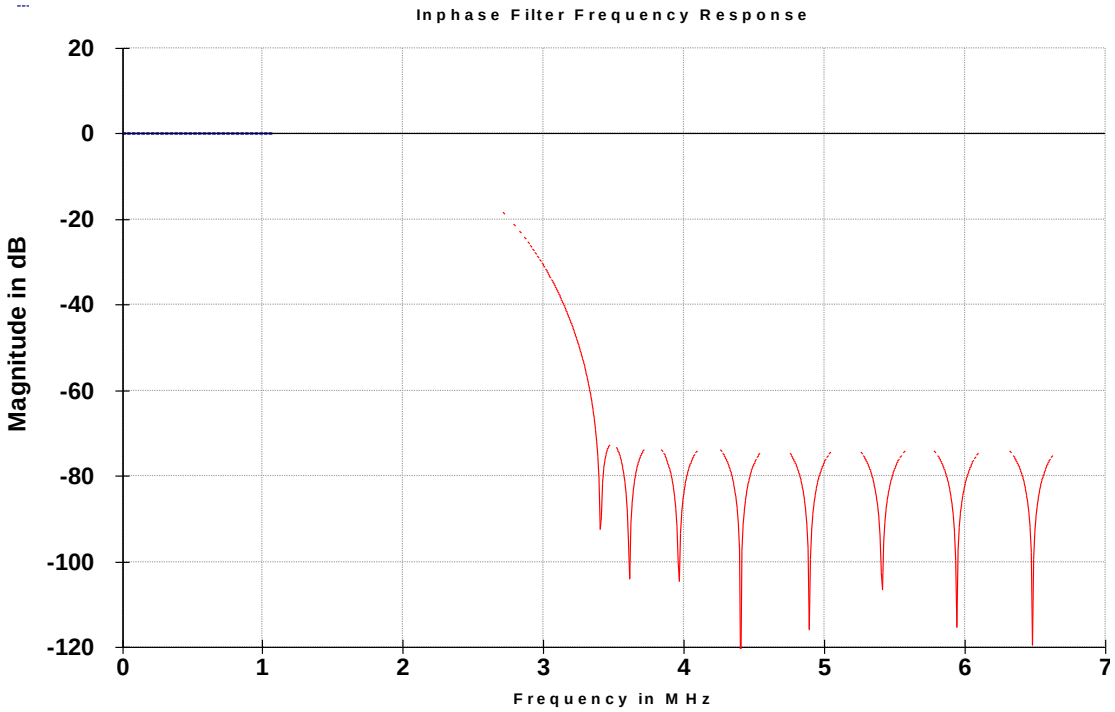

Figure 4 Demodulation low pass filter frequency response 0-6.75MHz.

Remod.v

The demodulated and low pass filtered chroma signal is then frequency shifted back to the subcarrier frequency and subtracted from the composite video to form a notched luma signal. The complementary nature of this architecture ensures there is no missing information through to the comb filter.

The sine and cosine waveforms from the demodulator are delayed to compensate for the demodulator low pass filter delay; the waveforms are then multiplied by the 'simple' U and V outputs of the low pass filter and then added together to reconstruct a chrominance signal centred on the CVBS referenced subcarrier waveform. This chrominance signal is then subtracted from the delayed composite video which provides a clean, notched luma signal with a notch bandwidth equal to the demodulator low pass filter bandwidth of 1.3MHz. This notched luma and the 'simple' demodulated U and V chroma are then applied to the comb filter.

SPG.v

The SPG (sync pulse generator) module provides all of the control signals for the PT4.

The horizontal and frame outputs of the HPLL are used to synchronise two counters, one vertical and one horizontal. From these counters various outputs are decoded; some of the outputs are programmable from the control registers. Outputs include:

Burstgate: A 32 pixel wide pulse used to accumulate demodulated V_demod outputs during the colour burst for the burst locked loop.

Active_video: A moveable position/ fixed width (1440 clock periods) horizontal output pulse used for the BT656 formatting.

PT4_VFlag: Vertical field pulse used for the BT656 formatting.

PT4_FFlag: Vertical frame pulse used for the BT656 formatting.

Clamp: A programmable output pulse intended for black level or sync tip clamping for the analogue front end.

A simplified block diagram of the PT4 video decoder back end is shown in Figure 5.

Line_delays.v

The notched luma and the U and V demodulated outputs are applied to the comb delay memory.

The line delays are formed by separate instantiations of the Vdec_ram.v block which in turn call the generic single port RAM module, ram_infer_generic.v. This avoids the memory being device or vendor specific.

The RAM is addressed a 10 bit line locked counter address and a read before write operation is performed on the RAM using a delayed version of the horizontal counter LSB signal as the control line. The 54MHz clock is used to create the write enable signals to avoid using both edges of the 27MHz.

Comb_filter.v

The demodulated 'simple' U and V outputs also contain high frequency luma information, (cross colour). This can removed as the chroma information has a known line based phase relationship whereas the HF luma and cross colour does not. The comb filter provides this filtering operation.

The comb filter is a chrominance comb in that it reinforced the chroma signals whilst cancelling the cross colour components.

The line comb filter for NTSC is (1/4*0H + 1/2*1H + 1/4*2H) (1 line spacing) and for PAL (1/4*0H + 1/2*1H + 1/4*2H) + [(0H – 2H) * PALswitch] (crosstalk cancellation). **The use of the crosstalk cancellation in PAL permits a 3 line comb (rather than the usual 5 line comb) with a much closer aperture giving more effective combing.**

The notch filter mode reduces the bandwidth of the chroma output, thereby reducing cross-colour amplitude. A simple ¼, ½. ¼ filter is used with a spacing of 4 (NTSC) at 13.5MHz.

For the comb filters to operate correctly the phase relationship of the colour component must be maintained; if not the HF luma will not be cancelled and can even be reinforced. It is therefore necessary to detect when the comb filters fail and switch to a better mode. Normally this failure mode is detected using luminance differences across the comb taps but there are instances where the same luminance value can occur but there are different chroma values which still cause the comb to fail; PT4 measure both luma and chroma comb failure instances.

The failure value for the line comb and notch mode is compared and the lowest error mode selected on a pixel by pixel basis.

The chosen U and V outputs from the filter are input to the processing amplifier. If the U and V outputs of the comb filter is subtracted from the delayed 'simple' U and V inputs to the comb (delayed by the comb filter delay) the output will be the recovered high frequency luma. This high frequency luminance signal is then sent to the HF luma module to be added to the notched luma.

The chosen comb mode may also be displayed on the output by enabling the view comb fail bit in register $03.

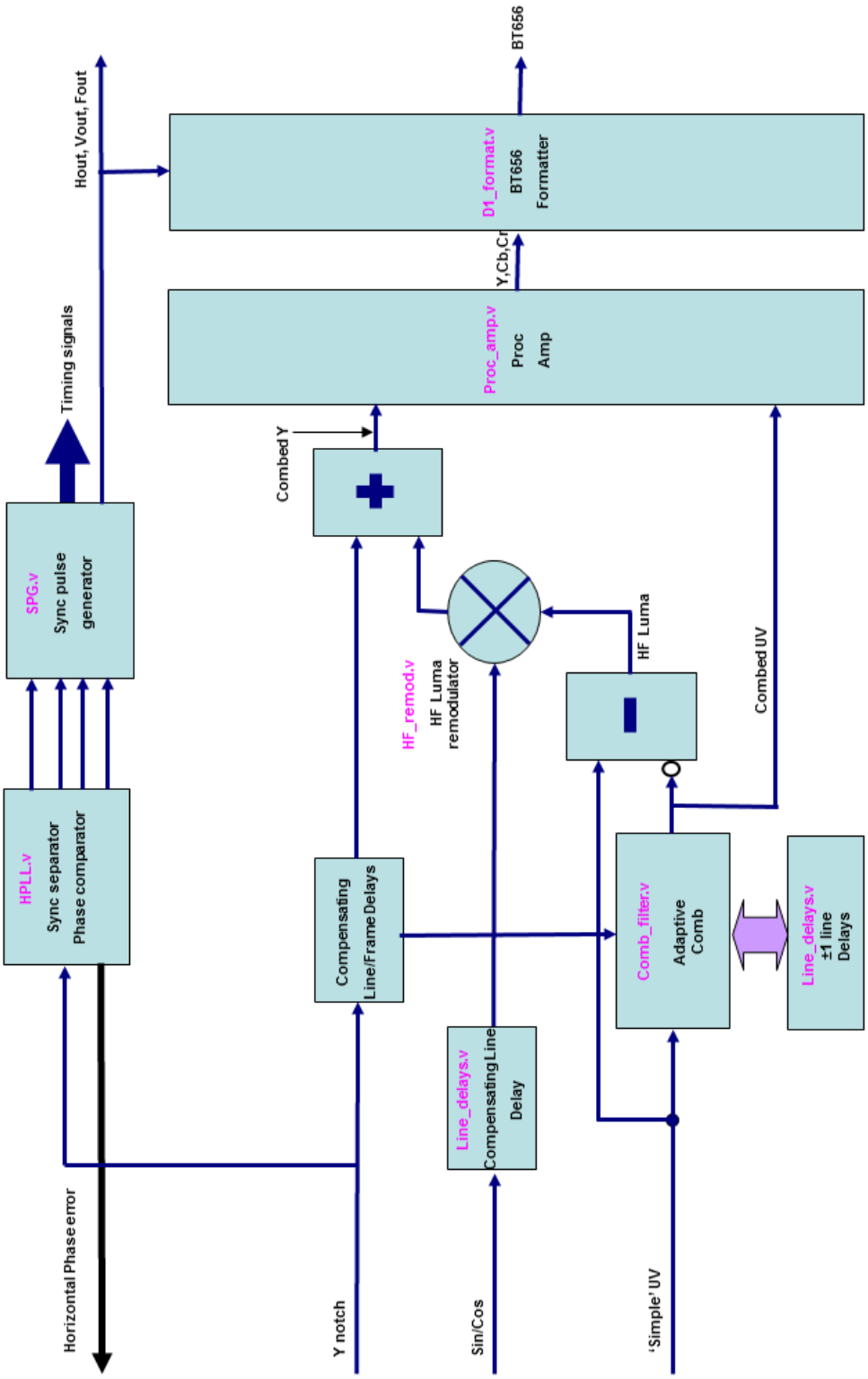

Figure 5 PT4 block diagram (Part 2).

HF_remod.v

The comb filter separates the non-coherent high frequency luma from the coherent chroma signal. The high frequency luma may then be remodulated onto the delayed sine and cosine waveforms and added to the delayed notched luma to form the full bandwidth luma signal. When the comb filter is in ‘simple’ mode the bandwidth of the chroma is reduced so some luma bandwidth is still recovered.

The HF remodulator works in exactly the same way as the Remod.v module except that it uses the one line delayed sine, cosine and notched luma as these are the centre point of the comb filter. The sine and cosine are multiplied by the high frequency U’ and V’ respectively, added together and then added to the notched luma. Because the decoder is a completely complementary design, in comb mode, the full bandwidth luma signal is then recovered. This luma signal is then input to the processing amplifier.

Proc_amp.v

The U and V outputs of the comb filter and the luminance output of the HF_remod module are then co-timed in the processing amplifier, Proc-amp.v. The luma signal then has the black level restored by having the sync offset removed (black level, back porch value).

The U and V signals are also amplified and blanking signals are also applied. The proc-amp output is 4:4:4 Y,Cb,Cr video, each at 10 bits.

D1_format.v

The Y, Cb and Cr outputs from the proc-amp, together with the Active video, Vertical and Frame flags are combined to form a BT656 compatible output. This output is valid on the rising edge of the Clock input. For 960H and 1280H operation the BT656 output has corresponding active video times of 960 pixels and 1280 pixels and the output operates at 36MHz (960H) or 54MHz (1280H).

6. Analogue interface

Figures 6 and 7 illustrate an example analogue front end interface for the PT4 (as used on the SB9 evaluation board).

The composite video input is terminated in 75Ω and then AC coupled into a single supply amplifier, U8, which is biased using a mid-rail reference voltage from U10. D2 prevents over and under-voltage excursions of the video affecting the amplifier input stage.

U20 forms an anti-aliasing filter. To simplify the design of the filter, for NTSC/PAL operation, the ADC is over-sampled at 54MHz (instead of 27MHz) and immediately decimated to 27MHz in the PT4. The anti-aliasing filter is flat to 12MHz (for 1280H operation) and rejects >15dB at 18MHz (for 960H operation). The anti-aliasing filter also has gain to match the input to the ADC. If the PT4 is to be used for NTSC/PAL only the filter values can be altered to match and the ADC sampled at 27MHz.

Because the input is AC coupled and video has a widely varying average DC level, it needs to be DC restored before the ADC. U9 forms a sync-tip clamp, clamping the most negative part of the video waveform to the VCLAMP voltage (the negative reference of the ADC). This ensures that the PT4 will separate the syncs correctly. The black level value of the input is determined by the PT4 and corrected internally ensuring stable blacks in the output luma.

To facilitate other front end architectures a clamp pulse output from the PT4 is provided; it is programmable in position and width. It may be used to provide a sync tip clamp or a black level clamp to a fixed value, which should be approximately 10 bit digital value 256_{10}.

The ADC (U12) is an ADI AD9237. For 1280H operation the 65MHz version should be used – for NTSC/PAL and 960H operation, the 40MHz version is adequate. The output of the ADC is 12 bit straight binary composite video at 27/36/54MHz (but only the top 10 bits are used by the PT4) which may be applied directly to the PT4 video decoder.

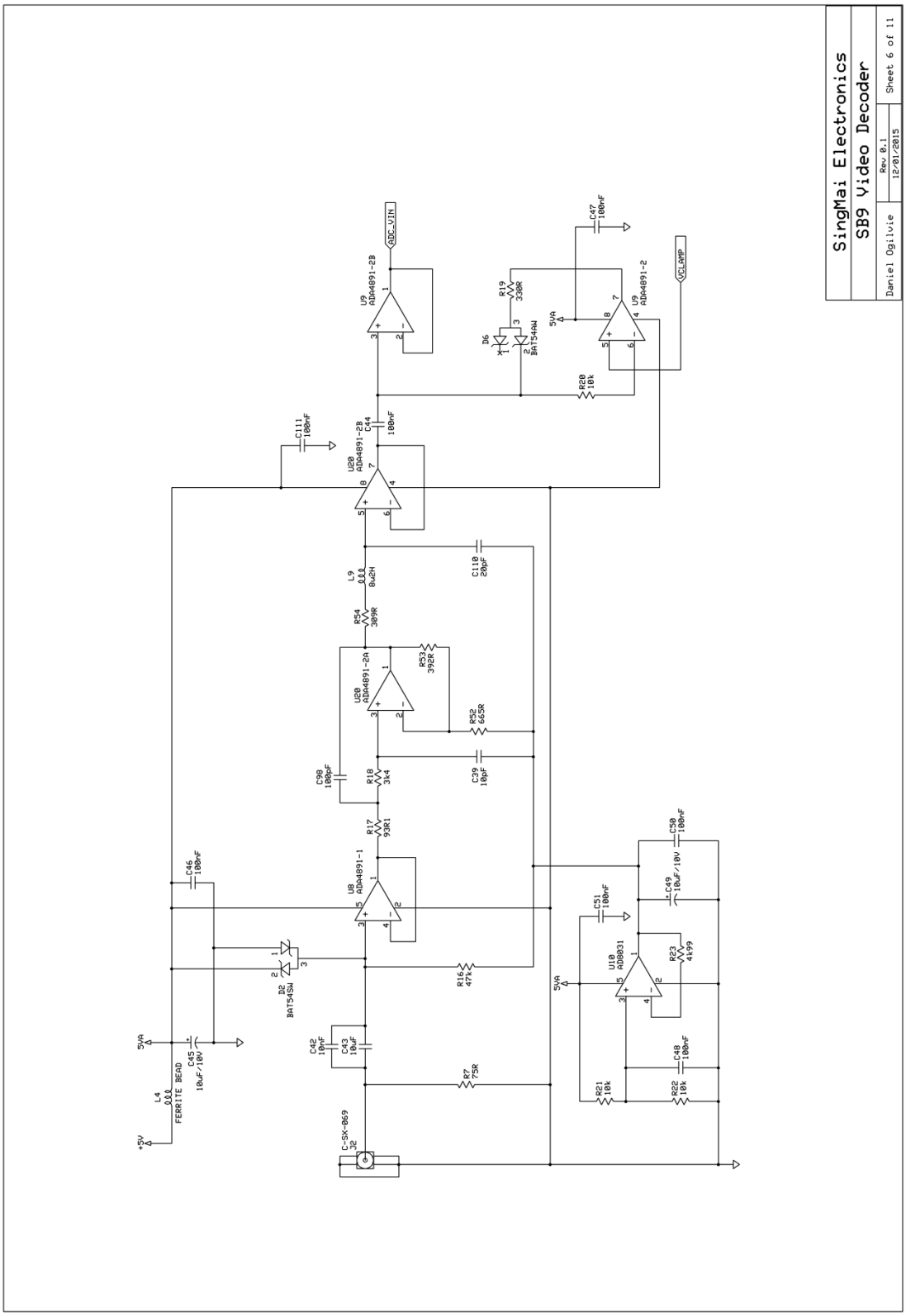

Figure 6 PT4 Analogue input stage schematic.

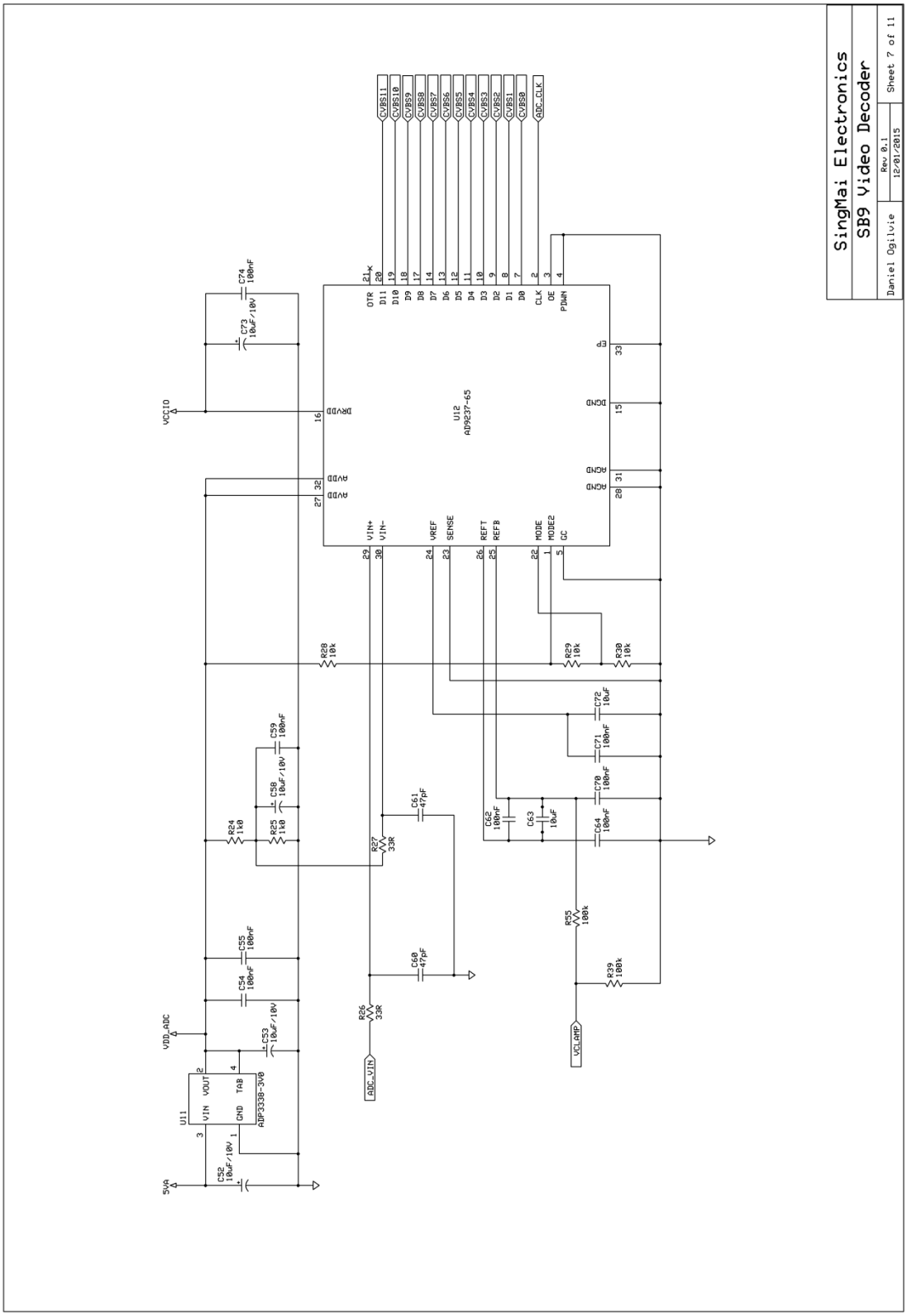

Figure 7 PT4 ADC schematic.

For multiple instantiations of the PT4 it is necessary to completely copy the design as they work on separate clock domains. For multiple instantiations of the PT4 using a fixed clock input (sync mode 1) can produce savings in the analogue front end. For example, for a 4-channel input a single ADC may be used, preceded by a 4:1 analogue switch. The switch and ADC operate at 4 x Clock frequency (e.g. 108MHz for NTSC/PAL) and the ADC data is then de-multiplexed to each PT4 decoder.

7. Synchronising modes

There are two synchronizing modes for the PT4.

In both modes [1] and [2] the sync separation and the horizontal phase locked loop (HPLL) are internal to the PT4; they differ only in the control of the output frequency.

In the first method the PT4 controls the frequency of an external voltage controlled oscillator (VCO); see Figure 8.

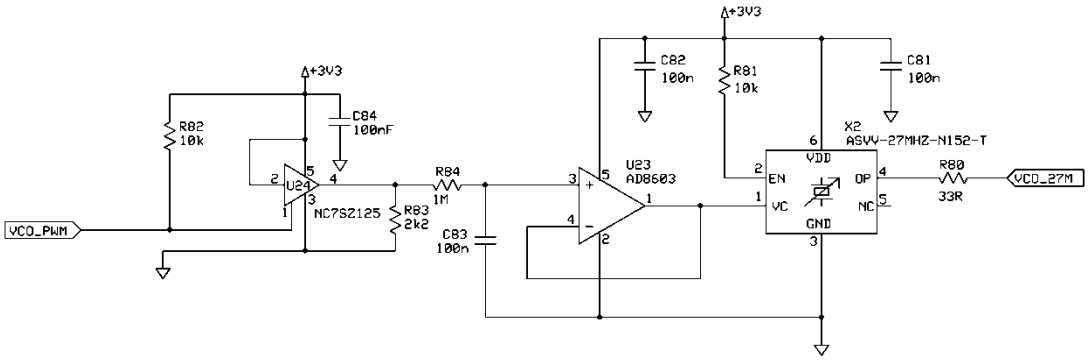

Figure 8 PT4 External VCO Schematic

The PT4 generates a free-running horizontal sync pulse at the correct frequency for the standard selected. It compares the phase of the falling edge of this pulse with the falling edge of the horizontal sync pulse generates a correlation error ‘voltage’ which is used to adjust the 27MHz clock input such that the pulses are coincident.

The error output from the PT4 is available as a pulse width modulated signal at the VCO_PWM port. In Figure 19 this output is buffered to avoid logic level variations affecting the loop and then filtered and buffered before driving the analogue input of a crystal VCO. The output from the VCO is then the 27MHz input (Clk27) of the PT4.

When using the VCO the Clk_en output is at a fixed rate of 13.5MHz, see Figure 9.

It is possible to force the VCO to maximum, minimum, and 50% values using control register 3. When using the VCO the sample rate converter must be bypassed, (control register 3, bit 2).

It is necessary to use a crystal VCO to ensure the jitter is low enough for the line comb filter to work correctly. However some inputs, such as from a VCR tape source or a mechanically scanned laserdisc, can have a horizontal frequency too far out of range or are too unstable in the short term for the VCO to be able to lock. Under these circumstances another synchronization mode is available.

This mode uses a sample rate converter (SRC). The VCO_PWM (if used) should be set to its fixed 50% value or if the VCO is not used a fixed crystal 27MHz clock may be used. The HPLL phase error is fed directly to the sample rate converter which modulates the Clk_en output such there are the correct number of samples in the line and so that the recovered horizontal sync and the internally generated horizontal sync are aligned. Fine adjustment of the phase is performed by interpolating the video to a sub-pixel accuracy using the phase word value and a Farrow filter as the interpolator.

To be updated.

8. Register interface

Figure 10 shows the timing diagram for the register interface; it is a conventional microprocessor interface. Each register is selected via an 5 bit address bus. Writes to unused register locations are ignored.

To write to the selected register the PT4_CSn (chip select) input must be asserted low, the A[4:0] assigned the required register address and the data for this register set up. The PT4_WRn input must then be driven low and high again: On the rising edge of this pulse the data is latched into the address selected. The PT4_CSn should then be returned high.

For the write to occur reliably the address (A[4:0]) and data (Din[7:0]) must be stable and valid during the low to high transition of the PT4_WRn pulse.

The address input also selects the register data that is presented on the PT4_Register_out[7:0] bus. This output is independent of the PT4_CSn or PT4_WRn inputs.

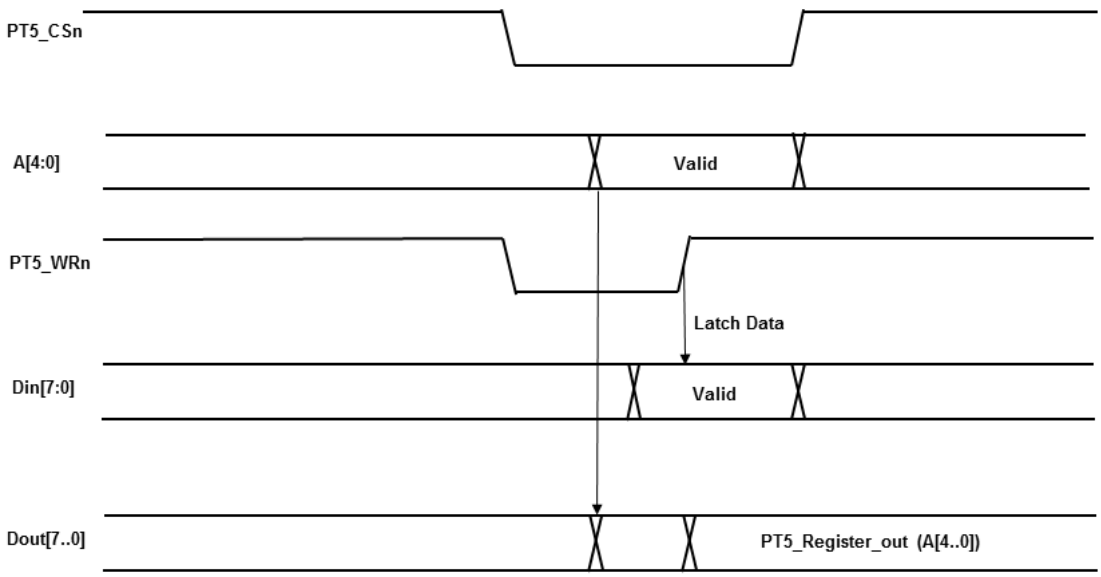

Figure 9 PT4 Register timing.

9. Register descriptions

The following table lists all of the control and status registers. All of the registers are 8 bit wide although some are concatenated together to create longer words. Asserting the RESETn input sets all the registers to their default values. Unused bits read back as '0's.

Note that if the Auto_register_select bit is set to '1' (Control register 1, bit 7), most of the timing and gain registers will not function as the default values will be used instead. However the registers will still be loaded with new values if written to and the reading will reflect the programmed values and not the default values.

Register Offset	Register Name	R/W	Bit Value	Default Value	Description		
Control							
$00	**Control 1**	R/W					
	Auto register select		7	1	If set to '1' the timing and gain values for each colour standard (in auto or manual mode) are automatically programmed to their default values. If set to '0' the timing and gain registers may be programmed by the user (for example for standards such as PAL60 or NTSC443).		
	Auto Colour Standard		6	0	If '1' selects the colour standard based on the detected line standard (525 or 625 line) and the control register 1 bits [4:1] status. If '0' the colour standard is manually set using control register 1 bits [4:0].		
					Line standard	Bit [4:1]	Auto standard
					525	00x0	NTSC-M
					525	00x1	PAL-M
					625	00x0	PAL
					625	00x1	PAL-N
					525	01x0	960H (NTSC)
					625	01x0	960H (PAL)
					525	10x0	1280H (NTSC)
					625	10x0	1280H (PAL)
			5	0	Not used		
	Colour standard		4-0	000	Bits [4:0]	Colour standard	
					00000	NTSC-M	
					00001	NTSC-J	
					00010	PAL-M	
					00100	PAL	
					00110	PAL-N	
					01000	960H (NTSC)	
					01100	960H (PAL)	
					10000	1280H (NTSC)	
					10100	1280H (PAL)	
$01	**Control 2**	R/W					
	View comb fail		7	0	Allows the selected comb mode to be displayed if set to '1'.		
					Comb mode	Displayed colour	
					Simple (notch)	Red	
					Line comb	Blue	
					Frame comb	Green	
			6-3	0	Not used		
	Comb mode		2-0	100	Bits [2:0]	Comb mode	
					000	Forces notch only mode	
					001	Forces line comb only mode	
					011	Not used	
					1xx	Automatically selects the comb mode.	
$02	**Control 3**	R/W					

Register Offset	Register Name	R/W	Bit Value	Default Value	Description	
			7-6	00	Not used	
	ABL		5	1	Enables the automatic black level if set to '1'. The back porch value is measured and subtracted from the composite video (effectively removing the sync pulses from the luma output). If enabled the luma offset control (Registers $15 and $16) is added to the measured black level offset. (See Figure 11).	
	Demod_VBI		4	0	If set to a '1' the vertical blanking interval signals are demodulated. If set to '0' the VBI signals are passed 'flat'.[1]	
	Bypass_demod		3	0	If = '1' the chroma demodulator is bypassed (Cb/Cr outputs set to blanking levels and the luma is passed flat i.e. composite video). Allows the unprocessed ADC data to pass through to the Y channel for test purposes.	
	Bypass_SRC		2	1	Bypasses the sample rate converter if set to '1' (VCO mode). Else uses the SRC for horizontal lock.	
	PWM_control		1-0	00	Bits [1:0]	VCO_PWM output
					00	Error output (VCO lock mode – sync mode 1)
					01	Force VCO_PWM output to '0'. (Test mode – do not use)
					10	Force VCO_PWM output to '1'. (Test mode – do not use).
					11	Force VCO_PWM output to 50%. (SRC lock mode value – sync mode 2)
SPG						
$10	**Active_video_start_value_1**	R/W	7-0	0	Start position of the active video. The width of the active video is preset according to the video standard. Start position is relative to 0H (falling edge of horizontal sync) and is in increments of 1/13.5MHz = 74ns.	
$11	**Active_video_start_value_2**	R/W	1-0	0		
$12	**Burst Start value**	R/W	7-0	82	Start position of the burst gate pulse (used to sample the demodulated U and V burst signals for the BLO loop). Start position is relative to 0H (falling edge of horizontal sync) and is in increments of 1/13.5MHz = 74ns.	
$13	**Clamp start value**	R/W	7-0	0	Start position of the clamp output pulse (used to provide sync tip or black level clamping of the analogue composite video prior to the ADC). Start position is relative to 0H (falling edge of horizontal sync) and is in increments of 1/13.5MHz = 74ns.	
$14	**Clamp end value**	R/W	7-0	0	End position of the clamp output .Start position is relative to 0H (falling edge of horizontal sync) and is in increments of 1/13.5MHz = 74ns. Note if the end value is smaller than the start value the output pulse will be inverted.	
Proc Amp						
$15	**Sub Luma Value_ABL_1**	R/W	7-0	38	Value added to the measured black level offset setup (if the ABL - Register $02 bit 5 - is enabled). As such for PAL it will normally be set to '0' and for NTSC it will be set to 38_{10} (remove NTSC setup pedestal) 10 bit value = (SublumaABL2[1..0],SubLumaABL1[7..0]). (See Figure 17).	
$16	**Sub Luma Value_ABL_2**	R/W	1-0	0		
$17	**Sub Luma Value_1**	R/W	7-0	38	Value subtracted from the processed CVBS output to remove sync and set the black level to 0. (ABL - Register $02 bit 5 - is disabled). 10 bit value = (Subluma2[1..0],SubLuma1[7..0]).	
$18	**Sub Luma Value_2**	R/W	1-0	0		

Register Offset	Register Name	R/W	Bit Value	Default Value	Description
					(See Figure 17).
$19	**Luma Gain 1**	R/W	7-0	42	Gain value for the luma (Y) output. Scaling between processed Y output and BT656 Y output. 10 bit value = (LumaGain2[1..0],LumaGain1[7..0]).
$1A	**Luma Gain 2**	R/W	1-0	2	
$1B	**U Gain 1**	R/W	7-0	95	Scaling between processed U output and Cb output. 10 bit value = (UGain2[1..0],UGain1[7..0]).
$1C	**U Gain 2**	R/W	1-0	1	
$1D	**V Gain 1**	R/W	7-0	246	Scaling between processed V output and Cr output. 10 bit value = (VGain2[1..0],VGain1[7..0]).
$1E	**V Gain 2**	R/W	1-0	0	

Table 4 PT4 Register description.

[1] During the vertical blanking interval (VBI), various test signals or information may be present. It is necessary that the PT4 pass these signals 'unprocessed'. Gains and offsets are automatically adjusted to 'flat' mode during the VBI (i.e. Y gain = 0dB, no black adjustment, comb filter off). Register $02, bit 4 selects whether the VBI data is decoded or passed flat (default mode – CVBS passed unprocessed to output).

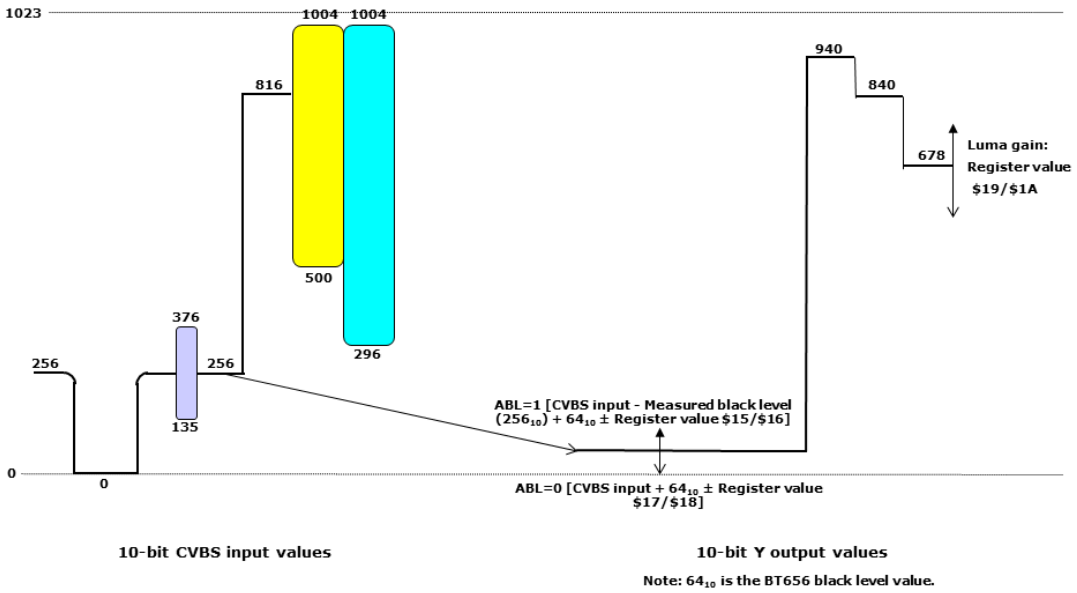

Figure 10 PT4 ABL and Black level control.

10. Specification

The PT4 decoder was measured using a SingMai SB9 platform with an Altera EP4CE15 FPGA which was programmed with the PT4 video decoder IP core (BT656 output from the PT4 is converted to SDI in a Gennum GS9002 serialiser IC).

The source was the composite output of a Tektronix TG2000 video test generator which was fed through an AD9237 12 bit ADC (top 10 bits used – see Chapter 6).

The SDI outputs were measured using a Tektronix WFM700M wavefrom monitor.

Parameter	Specification	Notes
Component Levels	Y - 100IRE ± 1%	SMPTE 75% colour bars
	Cb - 75IRE ± 1%	SMPTE 75% colour bars
	Cr - 75IRE ± 1%	SMPTE 75% colour bars
Component Noise	Y - < -55dB	50% flat field unified weighting
	Cb - < -65dB	50% flat field unweighted
	Cr - > -65dB	50% flat field unweighted
Luminance K-factor	<0.7%	NTC7 Composite
Luminance Frequency response	0-5MHz ± 0.2dB	60IRE Multiburst
Luminance linearity		5 step luminance
Y <> Cb/Cr delay	<±15ns	75% colour bars

Table 5 PT4 Specification

Figure 11 75% colour bar waveform (PAL).

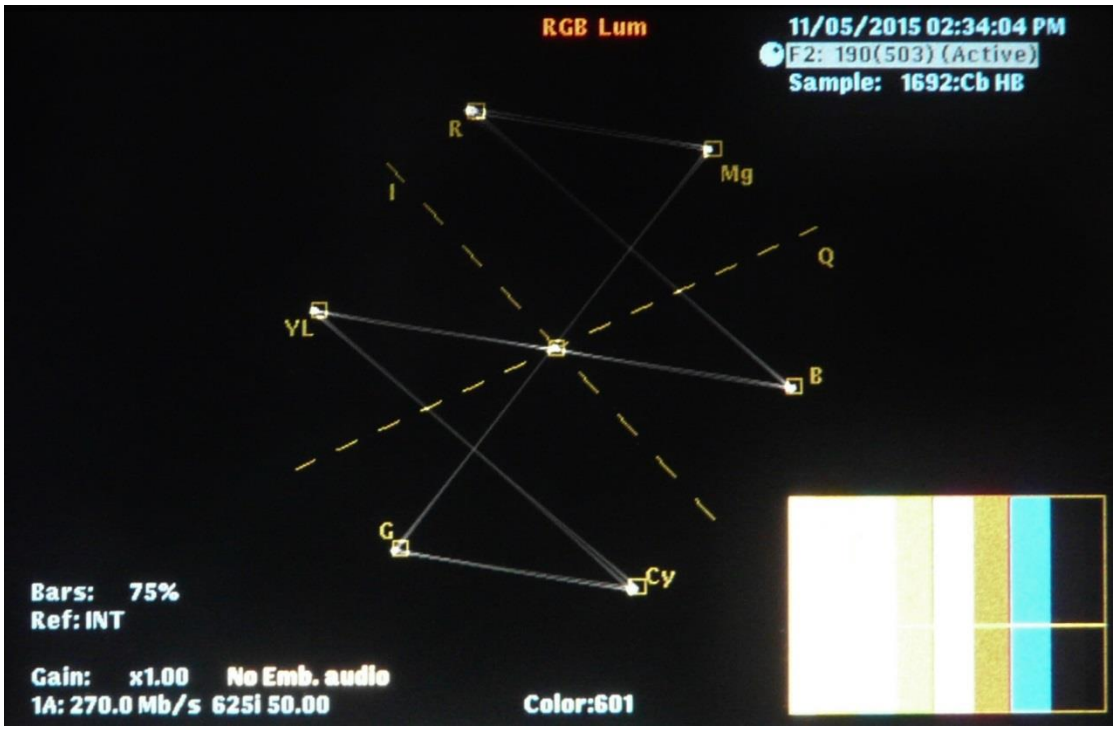

Figure 12 75% colour bars – vectors (PAL).

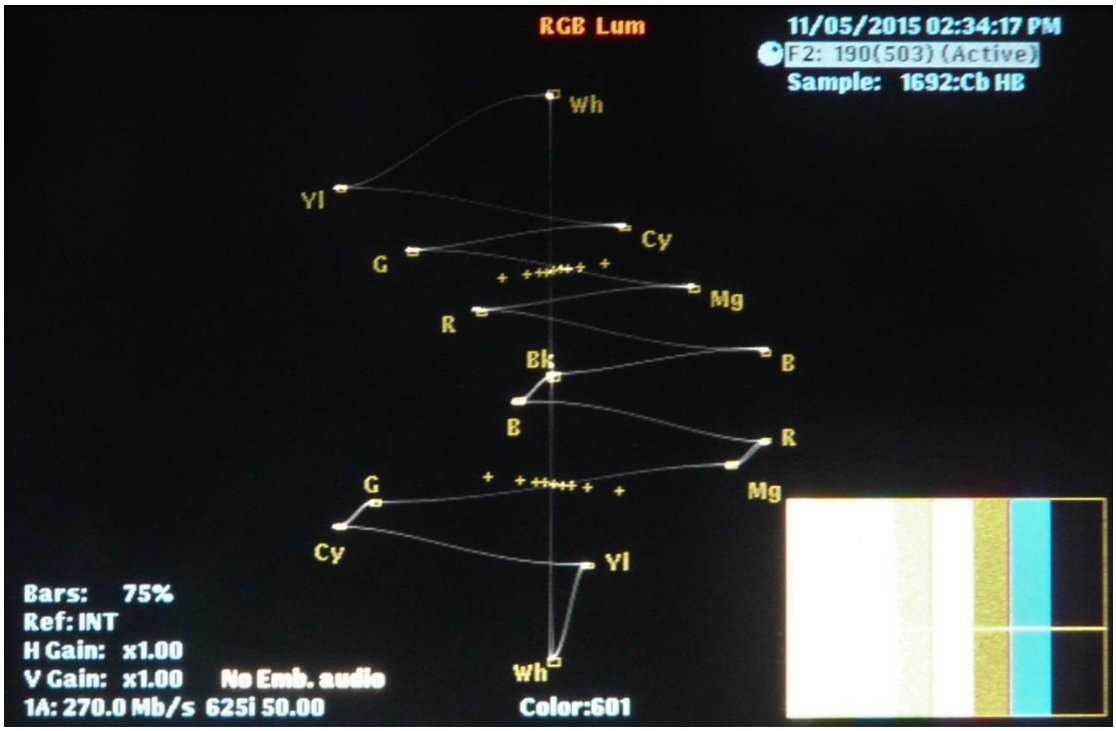

Figure 13 75% colour bars - Lightning display (PAL).

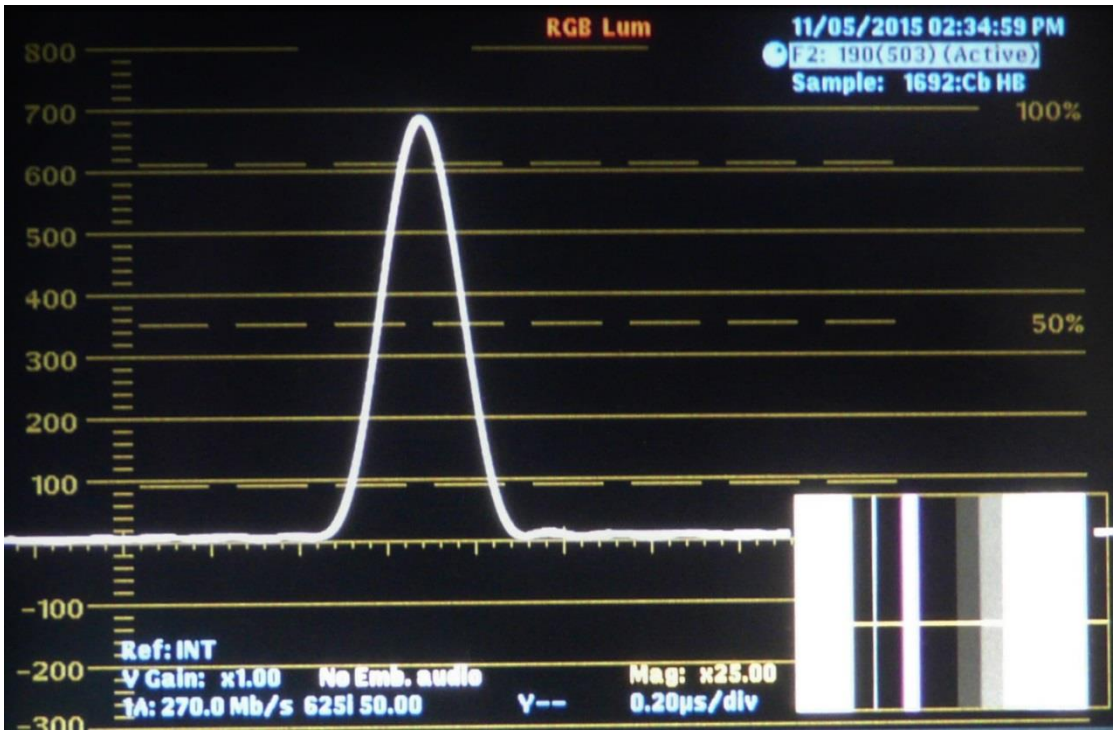

Figure 14 CCIR17 2T pulse. (PAL).

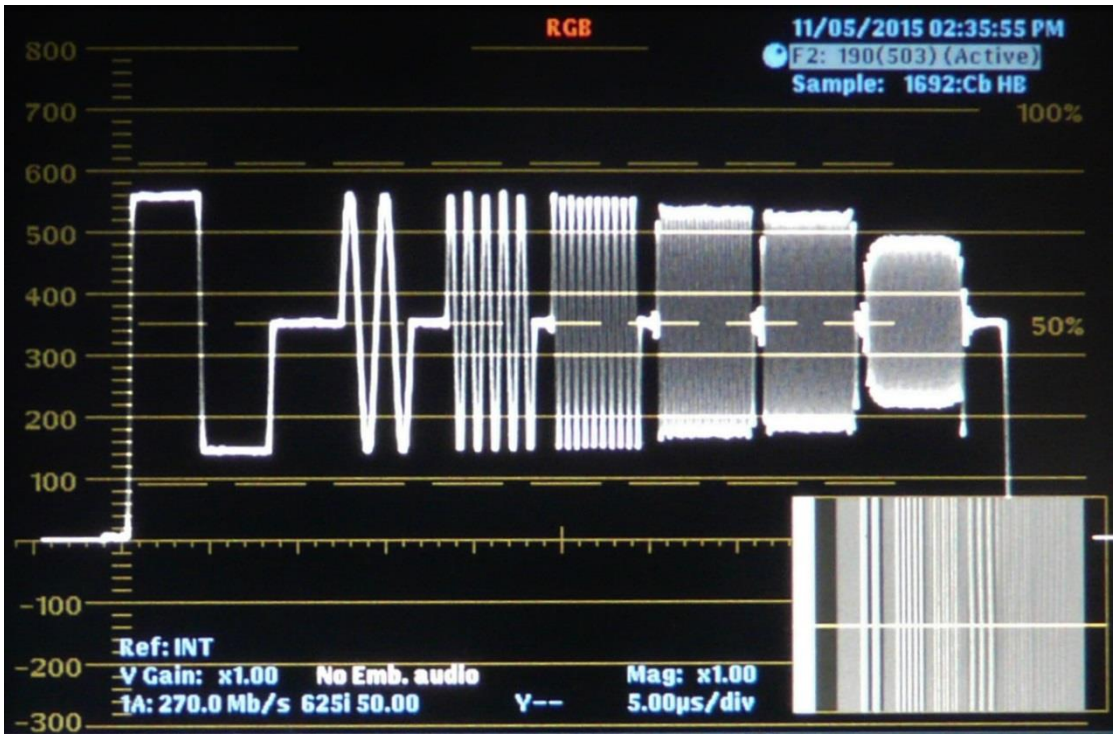

Figure 15 CCIR18 Multi-burst (PAL).

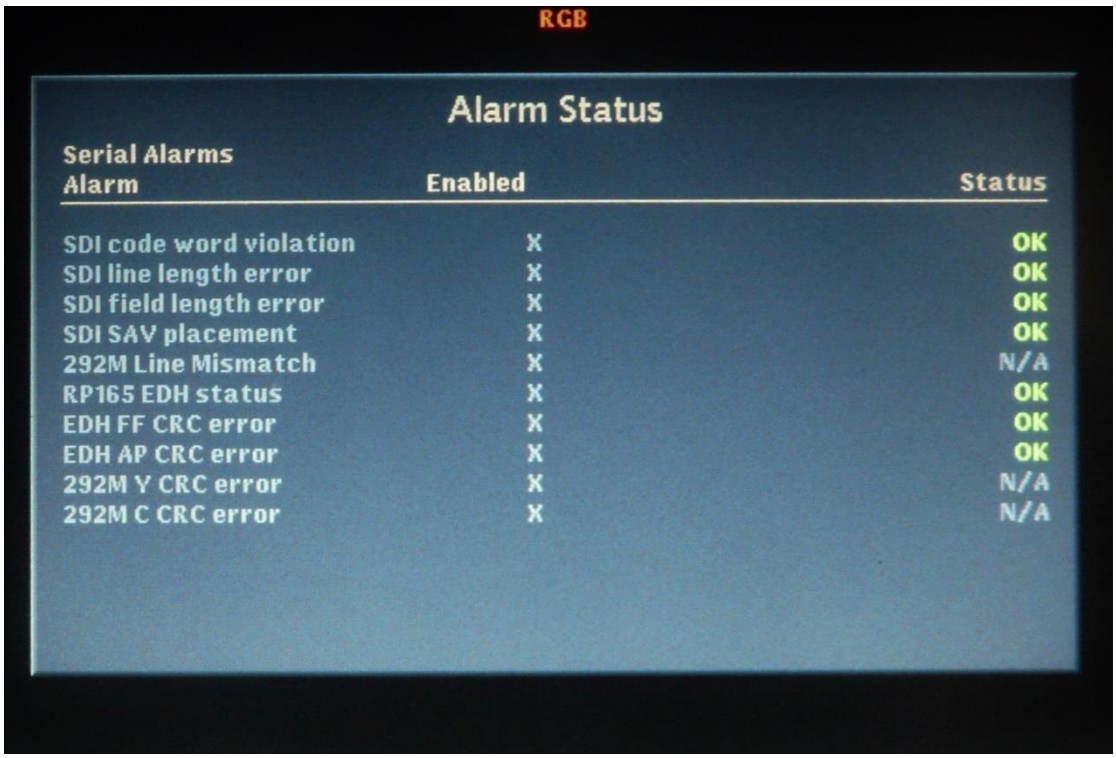

Figure 16 SDI Status display (625i - PAL).