DIRECT CURRENT AUTOMATED BENCH SOLUTION FOR A DUAL OPERATIONAL AMPLIFIER IN CHIP SCALE PACKAGE

by

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An ideal is only reached when it is kept in mind every day until its completion. God's grace, smiles making life enjoyable, slaps on the back expressing support, incentive words, technical ideas and corrections, trust and love fed this daily work. It would not have been possible to complete this project without all those elements together. I want to thank all you who participate in giving me all of that. I will try to learn from you by imitating the example you taught to me.

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ABSTRACT

The development of a direct current (DC) automated bench solution for a dual operational amplifier in Chip Scale Package (CSP) is the purpose of this thesis. Packaging and electrical properties of the device under test (DUT) are described. The design and implementation of the test hardware is covered. A detail explanation of the test program developed in LabVIEW is also included. Finally a statistical analysis is used to verify the system is repeatable and accurate in relationship with an automated test equipment (ATE).

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CHAPTER 1
INTRODUCTION

1.1 Definition of the problem

A new packaging technology called Chip Scale Package (CSP) will be utilized on the dual operational amplifier OPA2347 in Texas Instruments. Reduction of footprint, price and test time is the cause for implementing this technology. This CSP is developed with a wafer level packaging technology, which means that the device is already packaged after sawing the individual die from the wafer; therefore the cost of packaging is saved.

Normally, a device is tested twice before being sent to the costumer, first at probe and then at final test. Final test must be eliminated for this product because there is no automated handler to support production of the device since this is the first CSP product in the company. The problem is to have another way to test the device for correlation with the automated test equipment (ATE).

1.2 Solution of the problem

An automated bench solution must be developed to support results from the existing ATE. Selecting adequate instruments and socket for the device, designing test boards, adapter boards and test software are all part of this solution. The final system has to be much cheaper than ATE and easily hardware and software configurable.

1.3 Previous work

There is an automated bench solution in Texas Instruments for a dual op amp in other than a CSP package without the implementation of all the DC parameters tested at the ATE. The input bias current (I_B) and output swing (SW_{OUT}) tests are not included in this solution. Neither the hardware nor the software of this existing system are documented.

1.4 Chapters summary

Chapter 2 covers the background of the thesis. This is defining the purpose of having an automated bench solution, an introduction to chip scale packaging, an explanation of the op amp, the packaging and electrical characteristics of the device under test (DUT), and the circuitry used to test every DC parameter of the DUT.

Chapter 3 explains the hardware utilized as well as the way to interconnect all. The hardware consists of a modular, computer-based instrumentation platform called PCI eXtensions for instrumentation (PXI) and the design of 2 Adapter Boards and a Device Interface Board (DIB). A Chassis is the core of the system, where different modules are inserted: Digital Multimeter, Analog Output, Multiplexer, Relay Switch, GPIB (General purpose interface bus) and MXI-3. Another MXI-3 card plugged in the PCI slot of a computer is required to interface the software and hardware. The first adapter board has 8 pins in a dual in line package (DIP) format to make the conversion from CSP to DIP. The second one contains gold fingers to make contact with a female edge connector socket. Test circuitry implemented on the DIB is software configurable. The Summing Junction configuration is used test all DC parameters except for Quiescent Current (I_Q) and Bias Current (I_B). The bench board has three socketing options: CSP, PDIP and edge connector.

Chapter 4 examines the test software. The program developed in LabVIEW (Laboratory Virtual Instrument Engineering Workbench) is in charge of controlling the test by applying inputs and measure outputs with the PXI system. A verification routine is first executed and then the DC test.

Chapter 5 performs an statistical analysis to support the conclusion that the automated bench solution is repeatable and accurate in relationship with an automated test equipment (ATE) system.

Chapter 6 gives the conclusion of the thesis by providing the difficulties found and their solutions, the ways to improve the test hardware and software, the limitations of the system and how extra features, like test at temperature and multiple test by multiplexing , can be added.

CHAPTER 2
BACKGROUND

2.1 What is a dc automated bench solution?

A dc automated bench solution is actually a low cost set of automated test equipment controlled by software that is easily hardware configurable and transportable. Transportability plays an important role because test at temperature requires the equipment to be moved to the dedicated ovens. A list of the basic elements needed to build a dc automated bench system is given below.

- Software
- Controller (computer)
- Hardware-software interconnection
- Chassis
- Relay board
- Power supply
- Digital multimeter
- Device interface board

Designing any automated bench system is a fascinating challenge for a test engineer. It involves creativity, knowledge, research, programming skills and patience to deal with all problems involved.

First, the engineer must analyze the expected measurements to know the required resolution, power characteristics and other capabilities of test instruments. Then, the device interface board (DIB) must be developed in accordance with socket specifications and design rules for preventing parasitic resistance, inductance and capacitance that could cause incorrect readings. Finally, after verifying all instruments are properly calibrated the real task starts with putting all the pieces together and making it test with accuracy, repeatability and reproducibility.

A detailed explanation of how the dc automated bench solution for the OPA2347 works is explained in Chapter 3 and Chapter 4. Chapter 3 explains the hardware of the system and Chapter 4 the software.

2.2 Packaging

When the first transistor was developed by Bell Laboratories in 1947, another problem emerged immediately. The device had to be protected from the outside environment to be commercially viable. Packaging the device was needed to provide physical protection and electrical contact. The problem was not solved until 1954, when the manufacturing processes were perfected [1].

Since then, there have been many types of packages. Some of them have leads to make electrical contact while others have solder bumps or plated flat lands. These interconnects are located in different ways depending on customer needs. Some modern integrated circuit (IC) packages are shown in Figure 2.1 [2].

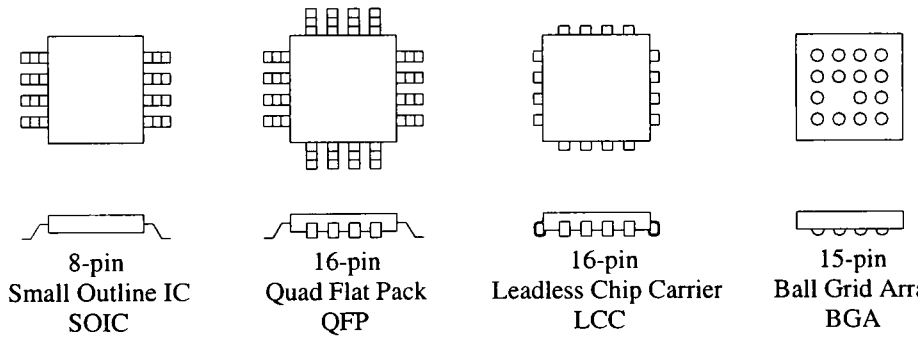

Figure 2.1 Modern integrated circuit (IC) packages

Having an existing product in a Chip Scale Package (CSP) was the starting point of this thesis. According to IPC (Association Connecting Electronics Industries), the package area of a CSP is less than 1.2 times its die area. When the package-to-die size ratio is more than 1.2 and only solder balls are the board-level interconnect, the device is called a BGA (Ball Grid Array) instead of a CSP. This is not always true because pitch

can also be used to classify a product as CSP. For example, Fujitsu's MicroBGA is a CSP because of its fine pitch of 0.8mm even though its package-to-chip size ratio is more than 1.2. Hitachi Cable's Micro Stud Array Package (MSA) does not fit the CSP definition, but it is also considered CSP because of its fine pitch stud array of 0.5mm. Therefore for a device to be classified as CSP most have either one or both of the characteristics listed below [3].

- Package-to-chip size ratio less than 1.2
- Pitch of less than 1mm

CSPs are then classified into four groups as follows [3].

- Customized-lead-frame-based-CSP or Lead On Chip (LOC)
- CSP with flexible substrate or Chip On Flex (COF)
- CSP with rigid substrate
- Wafer-level redistribution CSP

LOC's purpose is to increase the die-to-package size ratio for lead-frame-based packages. CSP with a flexible or rigid substrate utilizes an interposer to redistribute the original die level pitch to a standard CSP pitch (0.5, 0.65, 0.75, 0.8 or 1 mm) singularly (after dicing the wafer). Wafer-level redistribution CSP uses a metal layer instead of a substrate for pitch redistribution on the wafer [3].

CSPs have different characteristics from each other. Some of them can be seen in Table 2.1. The highlighted terms in Table 2.1 indicate particular characteristics of the Device Under Test (DUT) OPA2347 in CSP. The suffix YED is added to OPA2347 to specify that the product is in CSP. A more complete description of the physical and electrical characteristics of the DUT is explained later.

Table 2.1 Some CSP characteristics

Package-to-chip size ratio	<1.2mm	>1.2mm only if pitch ≤1mm			
Pitch (mm)	0.5	0.65	0.75	0.8	1
CSP group	LOC	Flexible Substrate	Rigid substrate	Wafer-level redistribution	
1st-level interconnect	Wire bonds	Metallization (Sputtering/Electroplating)	Inner Lead Bonding (ILB)	Solder bumps	
	C4 solder joints	Stud bumps	Ribbonlike flexible leads	Thin film deposition	
Board-level interconnect	C-lead	Plated flat lands	Solder bumps	Solder studs	Solid core metal spheres
	Plated bumps	Solder pads	Solder balls	Cu bumps	
Terminals location	Top	Bottom	Sides		
Terminals distribution	Array	Frame	Mirror		
Chip orientation	Face up	Face down			
Packaging level	Wafer	Singulated			

2.3 Development of the operational amplifier

The main purpose of an Operational Amplifier (Op Amp) is to achieve mathematical functions. The Op Amp can be used to add, subtract, take the derivative and integrate depending on the configuration of elements connected to it. Its design is based on a three terminal active semiconductor device called a transistor. Bell Laboratories invented the transistor in 1947. This invention replaced the use of vacuum tubes, which was the only technology, at that time, capable of amplifying and detecting electric signals since 1907. In the early days of electronics the electrical system used to do mathematical operations was called an analog computer. Today's fabrication is based on silicon, which is the most popular material used in the production of integrated circuits (IC). An integrated circuit is defined as a combination of circuit elements interconnected on a semiconductor material [1].

Texas Instruments (TI) was one of the first companies to manufacture transistors. TI developed a small radio in 1954. Around 100,000 radios were sold during 1955 for $49.99 each. It was the first radio based on transistors in the market [1].

2.4 Definition of the operational amplifier

The operational amplifier is a high gain active element that can be configured with other elements to perform a specific function. Op amps have two differential inputs, one output and two power supply inputs. Since the op amp can amplify AC signals; the op amp is characterized as an active element. Passive elements, such as resistors, capacitors and inductors, only absorb energy. An active element can provide AC energy by converting the DC energy of its power supplies. Figure 2.2 shows the symbol for the Op Amp.

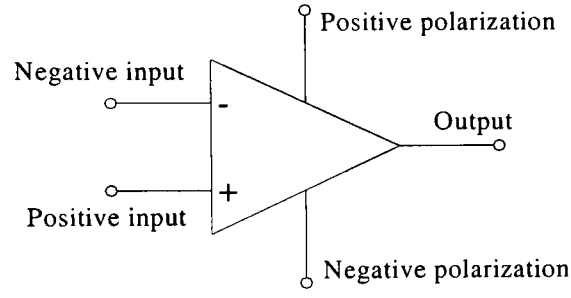

Figure 2.2 Symbol of the operational amplifier.

2.4.1 Real operational amplifier

To understand the real behavior of the Op Amp it is necessary to know some properties of its terminals.

The output voltage (V_{out}) of the Op Amp cannot be more than its polarization voltages (V_+ and V_-). Another important relationship for V_{out} is established in Equation 2.1.

$$Vout = -A(V_1-V_2)$$

Equation 2.1

The high gain, A, has a typical value of 10^6. V_1 is the negative input and V_2 is the positive input. V_1 and V_2 have a high impedance input of $10^{13}\Omega$. The potential difference between the two inputs (V_1-V_2 = V_e) is in the range of 10^{-6} to 10^{-3} volts.

Current flowing into the input terminals has a magnitude of 10^{-12} amperes. It is called bias current (I_B).

These characteristics have values that are either too small or too large in relationship to the other parameters in the circuit. This makes it possible to model the Op Amp as an ideal operational amplifier. As a consequence, circuit analysis becomes easier.

An explanation of the properties of the ideal operational amplifier is given in the next section.

2.4.2 Ideal operational amplifier

The ideal operational amplifier has the following characteristics [1].

- $I_{B+} = I_{B-} \rightarrow 0$
- $A \rightarrow \infty$
- $(V_1 \quad V_2) \rightarrow 0$ (Condition only satisfied with negative feedback)

Due to I_B for both inputs $\rightarrow 0$, the input impedance $\rightarrow \infty$. If there is negative feedback in the network, the infinite gain causes the inputs to be consider as virtually connected with zero resistance. In this case, if the positive input is grounded, the negative input is virtually grounded. With this principle, many useful circuit configurations can be developed. Even though the gain is considered to $A \rightarrow \infty$, the output value is limited by the supply voltages.

2.5 Device under test (DUT)

The device under test (DUT) OPA2347YED is a dual CMOS (Complementary Metal Oxide Semiconductor) operational amplifier in a chip scale package (CSP). The suffix YED indicates that the device is CSP. Its main DC electrical characteristics are low power consumption with a quiescent current (I_Q) of 20μA per amplifier, a single or split supply from 2.3V to 5.5V and rail-to-rail inputs and outputs [4].

2.5.1 Product data sheet only with DC parameters to be tested

Table 2.2 contains the DC parameters to be tested with their abbreviated names. The condition column establishes test requirements for every test to ensure results within maximum (max) and minimum (min) limits. These limits, if present, are guaranteed values. Typical values are not guaranteed. They were calculated by design to give a reference.

Table 2.2 Product data sheet DC parameters of the OPA2347

Parameter	Condition	Min	Typ	Max	Units
Input offset voltage V_{OS}	V_S=5.5V V_{CM}=(V-)+0.8V		2	6	mV
Power-Supply Rejection Ratio PSRR	V_S=2.5V to 5.5V V_{CM}<(V+)-1.7V		60	175	μV/V
Common-Mode Rejection Ratio CMRR	V_S=5.5V (V-)-0.2V<V_{CM}<(V+)-1.7V (V-)-0.2V<V_{CM}<(V+)+0.2V	70	80		dB
Input Bias Current I_B			±0.5	±10	pA
Input Offset Current I_{OS}			±0.5	±10	pA
Open-Loop Voltage Gain A_{OL}	V_S=5.5V R_L=100kΩ 0.015<V_O<5.485V	100	115		dB
Voltage Output Swing from Rail	R_L=100kΩ A_{OL}>100dB		5	15	mV
Quiescent Current (per amplifier) I_Q	I_O=0		20	34	μA

Figure 2.3 represents the top view of the typical input/output (I/O) pin configuration for this dual operational amplifier. All previous packages of the OPA2347 have leads to perform board level interconnections. The number and name of every terminal are shown in Figure 2.3.

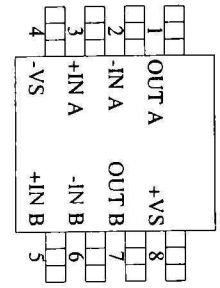

Figure 2.3 Typical top-view configuration of a dual op amp

2.5.2 Package of the DUT

Because the OPA2347YED has a package-to-chip size ratio less than 1.2 and its pitch is less than 1mm, it is categorized as CSP. Wafer level packaging technology is applied to this product. This means that after sawing the wafer the device is already packaged.

This location of the bond pads on the original integrated circuit (IC) layout had to be reconfigured in order to meet bump on pad CSP technology. The original pads were located in line on one side of the die to facilitate wire bonding for packaging. IC redistribution was required to extend interconnections between active circuitry and bond pads for this new package in order to have a final pitch of 0.5mm. In other words, the original IC layout had to be reconfigured without modifying any circuitry. The original circuitry did not suffer any functional modifications. To facilitate metal trace extension to the corresponding bond pad, it was necessary to rotate operational amplifier B 180 degrees as shown in Figure 2.4.

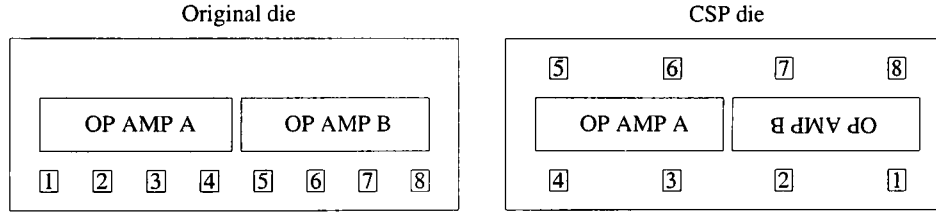

Figure 2.4 Original and CSP OPA2347 die layout

The area of the original die is 358.8μm *1731.2μm. On a 6'' wafer approximately 14,000 die can be built. On the other hand, CSP die had to be increased to 888.85μm *1981.2μm to accommodate solder bumps on pads with a pitch of 0.5mm. As a result, the number of die per wafer was decreased to 7,500. It appears that the cost per die increases for this package, but the original die has to be packaged after sawing and the CSP die does not. This makes wafer level chip scale packaging (WL-CSP) cheaper than other

conventional packaging techniques. It is important to note that the pitch and solder bump size determine the minimum die area for a CSP product.

Wafer-level redistribution is the CSP group to which the OPA2347YED belongs. This group defines the way to interconnect solder bumps to existing I/O pads at the wafer level. Redistribution layer (RDL) and Bump On Pad (BOP) are two approaches used.

RDL and BOP require a passivation layer on top of the active circuitry. Then a Benzocyclobutene (BCB) repassivation layer is required. This BCB polymer layer provides [5]:

- Reconfiguration of perimeter I/O pads,
- Planarization of a severe surface topology,
- Size reduction of perimeter I/O pad openings,
- Stress buffer or scratch protection,
- Lower coupling between redistribution lines and active circuitry.

RDL is a metal layer deposition and patterning technique utilized to interconnect existing I/O pads to a solder-bump array. IC layout reconfiguration is not required. Solder bumps are placed on top of this redistribution layer. RDL was not an option for the OPA2347YED. BOP was used instead because die reconfiguration was possible without affecting the circuitry's functionality [5].

BOP requires IC layout reconfiguration to meet CSP specifications. This is the case of the OPA2347YED. An Under Bump Metallurgy (UBM) is placed on top of the pad before solder bump deposition. UBM's diameter for the OPA2347YED is 247μm. UBM provides [5]:

- A solder wettable terminal,
- Size and area of the solder connection,
- Adhesion between solder and chip,
- Diffusion barrier between solder and chip,
- Electrical contact to the chip I/O.

Solder bump placement is the last procedure to complete. Composition of 63% Sn and 37% Pb is used in this case. Cross section illustrations for both RDL and BOP are presented in Figure 2.5 [6] to help understand the previous explanations.

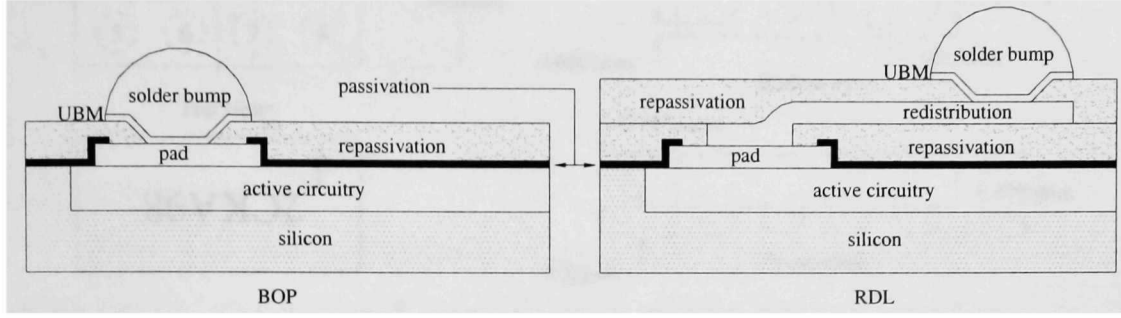

Figure 2.5 Cross-section illustrations for BOP and RDL

Since this is the first time TI-Tucson has introduced an operational amplifier in CSP, a comparison with its first competitor will be discussed. National Semiconductor produces the LM2904 in a micro Solder Mask Defined (uSMD) package. Although National Semiconductor is in the head of CSP technology, the electrical and mechanical performance of the LM2904uSMD does not surpass the OPA2347YED [4] [7].

Starting with the I/O array of 2*4 bumps, the OPA2347YED resembles the conventional pin out for a dual op amp. This is an advantage to the customer since they will be dealing with an identical pin out configuration previously used with the same product in a different package. On the other hand, the LM2904uSMD has an I/O array of 3*3 bumps without a center bump. Figure 2.6 and Figure 2.7 identify the outlines of these products [7].

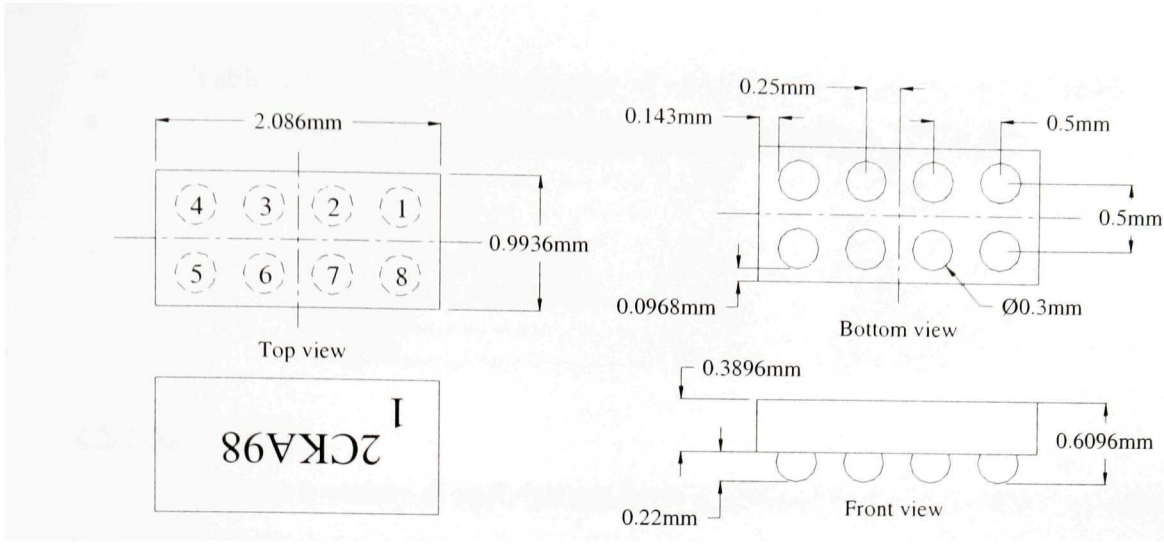

Figure 2.6 OPA2347YED outline

Bump diameters of 0.3 mm against 0.16-0.18mm is another advantage for the OPA2347YED because the larger the bump size makes for easier assemble and visual inspection. Even though both have a pitch of 0.5 mm, the LM2904uSMD occupies more area because of its center bump [7].

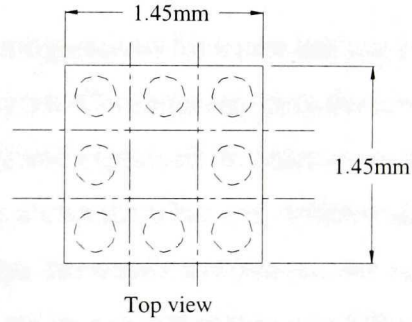

Figure 2.7 LM2904 uSMD outline

Power consumption is a key factor for a product because the larger the quiescent current (I_q) the more expensive to keep the device working. The OPA2347YED consumes 25 times less power than the LM2904uSMD. The electrical performance for both components is illustrated in the following table [4, 7].

Table 2.3 Electrical performance of LM2904uSMD and OPA2347YED

Parameter	LM2904uSMD	OPA2347YED
Quiescent current	500 μA	20 μA
Input bias current	40 nA	±0.5 pA
Input offset voltage	2 mV	2 mV
Power supply rejection ratio	100 dB	85 dB
Common mode rejection ratio	70 dB	80 dB
Bandwidth	1 MHz	350 MHz
Slew rate	0.5 V/μs	0.17 V/μs

2.5.3 Applications

There are a variety of applications for this product including portable equipment, battery-powered equipment, two-wire transmitters, smoke detectors and CO detectors [4].

2.6 Testing DC parameters

2.6.1 Test circuit

Testing DC parameters of a dual operational amplifier is not an easy task. Different circuit configurations and conditions can be applied per parameter. As a result, a general test circuit shown in Figure 2.8 will be used to meet configuration requirements for every test.

Particular circuit configurations for every test can be obtained by closing specific relays of the general test circuit. Consequently only the circuit needed to test each parameter will be displayed and explained. In order to occupy less figure area, two labels separated by a coma or one above the other will differentiate the elements and pins of op amps A and B. Closed relays, parameter definitions, test conditions, with an explanation and special considerations are also included based on OPA2347YED data sheet specifications.

The false summing junction configuration, consisting of five resistors and negative feedback, is used to set the output of an op amp to a desired level by adjusting the input of the circuit [8]. Predominance is granted to this circuit shown in Figure 2.12 because it will help to test the majority of the parameters.

Capacitors are connected as close as possible to each power supply pin of the DUT to ground in order to maintain the voltage applied to each terminal stable. These are called decoupling capacitors.

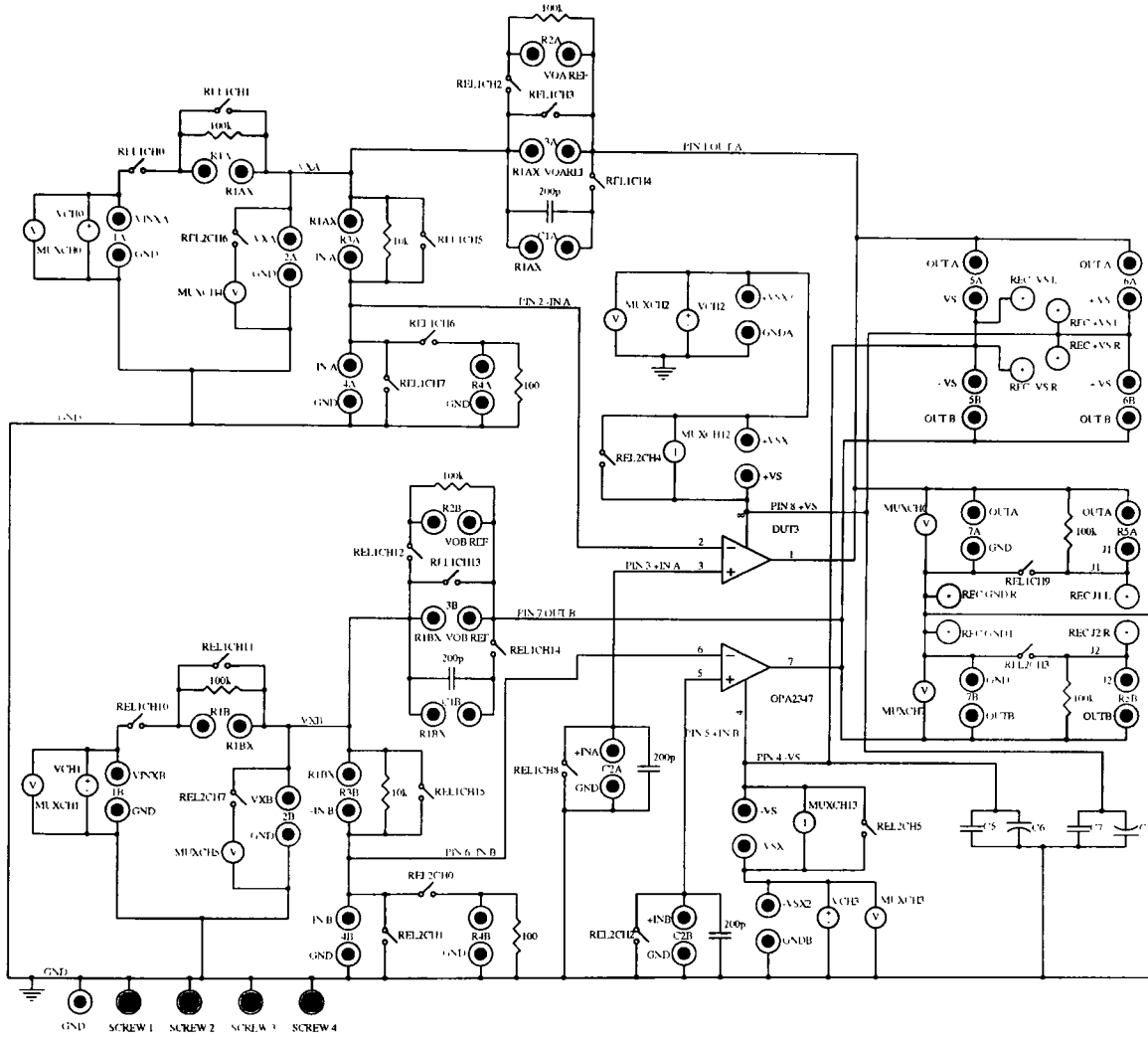

Figure 2.8 General test circuit

MUXCHxx represent the places where voltage and current measurements must be taken. MUXCH0 to MUXCH7 are for voltage. MUXCH12 to MUXCH13 are for current. VCHx indicates the points where voltages are applied. Since this circuit is implemented on a printed circuit board, circle symbols point out the terminals where resistors,

capacitors, relays (RELxCHxx), multiplexer relays (MUXCHxx) and instruments must be connected. The test temperature is 25°C.

2.6.2 Verification routine

Definition: The verification routine verifies if the power supply (AO) and digital multimeter (DMM) are setting and measuring voltages without exceeding an error of 100μV (DMM) and 350μV (AO) with respect to a well known calibrated DMM.

Closed relays: None

Test circuit configuration: None

Test conditions: Connect DMM 1 and DMM 2 in parallel.

Steps: Apply 3 voltage levels (-5, 0 and 5 V) per each voltage channel VCH0, VCH1, VCH2 and VCH3 while measuring them with both DMM 1 and DMM 2 through MUX0, MUX3, MUX6 and MUX7. Having DMM 2 as a reference, readings taken from DMM 1 and the desired voltage level cannot differ by more than 100μV and 350μV.

Special considerations: Make sure all instruments have the same ground reference.

2.6.3 Quiescent current test (I_Q)

Definition: Power supply current of the op amp when its output current is zero [8].

Relays in use: REL1CH3, REL1CH5, REL1CH8, REL1CH13, REL1CH15, , REL2CH2 and REL2CH5.

Test circuit configuration: Voltage follower shown in Figure 2.9.

Test conditions: No load

Expected value: 40μA (20μA per amplifier).

Steps: Apply V_{S+}=2.75 V, V_{S-}=-2.75V, close all relays in use and then measure MUXCH12 current. Divide this reading by 2 to obtain I_Q per amplifier.

Special considerations: Verify if the op amp is oscillating with the use of an oscilloscope connected to the output. If the op amp oscillates due to parasitic elements on

the DIB, a pole-zero analysis previously done by the designer of the DUT must be studied to correct this problem.

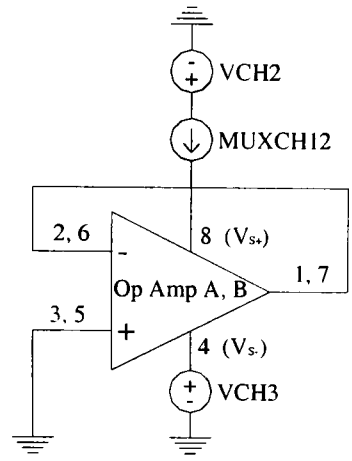

Figure 2.9 Quiescent current (I_Q) test circuit

2.6.4 Positive input bias current (I_{B+})

Definition: The current flowing into the positive input of the op amp [8].

Test configuration: Stop watch integration shown in Figure 2.10.

Relays in use: REL1CH3, REL1CH5, REL1CH8, REL1CH9, REL1CH13, REL1CH15, REL2CH2, REL2CH3, REL2CH4 and REL2CH5.

Test conditions: R_L=R5=100kΩ and C2=200pF.

Expected value: ±0.5pA.

Steps: Apply V_{S+}=2.75 V, V_{S-}=-2.75V, close all the relays, open the relay REL1CH8/REL2CH2, wait for signal settling Δ_{START}>10ms before taking V_{OUT1}, wait Δ_T>500ms, measure V_{OUT2} and then compute I_{B+}=-C2*(V_{OUT1}-V_{OUT2})/(Δ_T). The negative sign corrects polarity of the input bias current.

Explanation: Since the current to be measured is in the order of pA and a DMM capable of measuring it is very expensive, a capacitor is used to integrate this current over a period of time (Δ_T) to obtain the corresponding voltage change (V_{OUT1}-V_{OUT2}). The relationship of the voltage and current through a capacitor is V_C=C*$\int I_C$*dt. C2=200pF

was calculated by using the typical value for I_{B+}=0.5pA, and choosing Δ_T=1sec and (V_{OUT1}-V_{OUT2})=2.5mV.

Special considerations: Connect an oscilloscope at the output to verify the circuit is integrating properly without leaking, saturation or oscillation. Leaking increases the voltage rate of change at the output resulting in a higher measurement. Saturation produces a zero measurement because the output would reach either of the supplies in less than 100ms once the relay is open. Oscillation generates a sine wave at the output of the op amp. Accuracy can be improved by incrementing Δt or decrementing C2. Both ways minimize noise by allowing a larger (V_{OUT1}-V_{OUT2}). Capacitance reduction is a concern when on-board parasitics of the same value are present. When measuring pA a glass capacitor is preferred due to its better performance with respect to any other type.

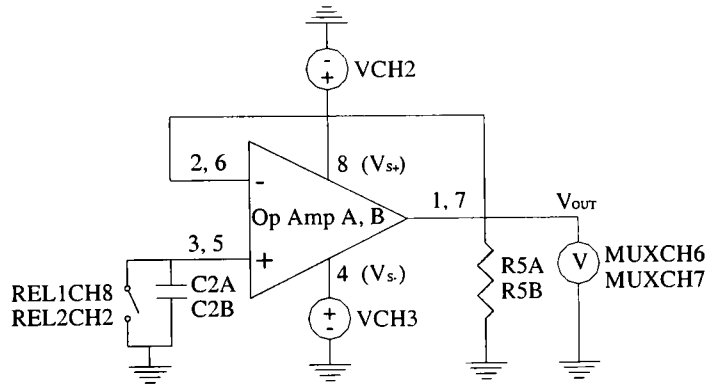

Figure 2.10 Positive input bias current (I_{B+}) test circuit

2.6.5 Negative input bias current (I_{B-})

Definition: The current flowing into the negative input of the op amp [8].

Test configuration: Stop watch integration shown in Figure 2.11.

Relays in use: REL1CH3, REL1CH4, REL1CH5, REL1CH8, REL1CH9, REL1CH13, REL1CH14, REL1CH15, REL2CH2, REL2CH3, REL2CH4 and REL2CH5.

Test conditions: R_L=R5=100kΩ and C1=200pF.

Expected value: ±0.5pA.

Steps: Apply V_{S+}=2.75 V, V_{S-}=-2.75V, close all the relays, open the relay REL1CH3/REL2CH13, wait for signal settling Δ_{START}>10ms before taking V_{OUT1}, measure V_{OUT2} after waiting Δ_T>500ms and then compute I_{B-}=C1*(V_{OUT1}-V_{OUT2})/(Δ_T).

Explanation: Although the capacitor for this test is connected from the output to the negative input of the op amp, the same principle used to obtain I_{B+} is applied for I_{B-}.

Special considerations: Nearby circuitry other than the one in use can be a source of noise. Although glass capacitors are very expensive they provide the best performance for this test.

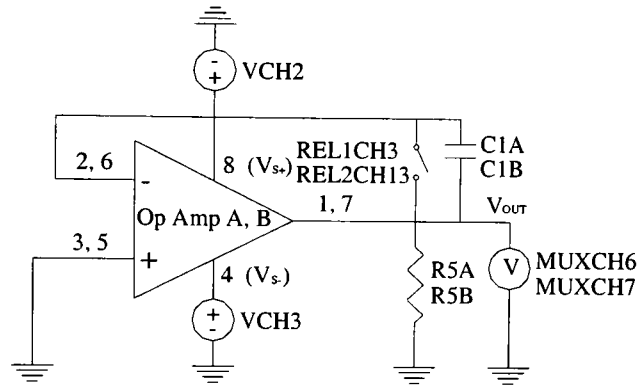

Figure 2.11 Negative input bias current (I_{B-}) test circuit

2.6.6 Input offset current (I_{OS})

Definition: The difference between I_{B+} and I_{B-} [8].

Expected value: Less than ±0.5pA due to the expected values for I_{B+} and I_{B-} are in the same range.

2.6.7 False summing junction test circuit

The false summing junction configuration will be used to test the rest of the DC parameters. Five resistors and negative feedback form the basic idea of this circuit illustrated in Figure 2.12. Both VCH2 and VCH3 can be positive or negative depending on the test conditions [8].

Values for all resistors are shown below:

- $R_1 = R_2 = 100k\Omega$

- R_3 = 10kΩ
- R_4 = 100Ω
- R_5 = disconnected

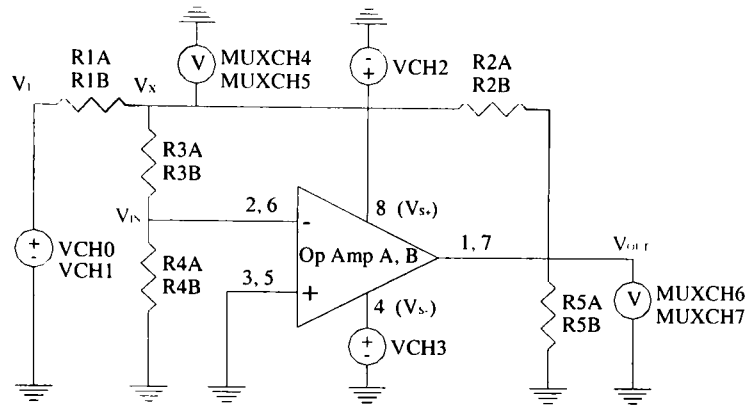

Figure 2.12 False summing junction test circuit

The load resistance R_L specified in the product data sheet (PDS) is 100kΩ. It is not the one connected between the output and ground (R_5) but the parallel combination of R_2 and R_5 (R_L=R_5|| R_2=100kΩ). Therefore if choosing R_2=100kΩ, then R_5 must be disconnected. With these resistor values and considering the ideal behavior of the op amp (I_{B-}=0), the voltage between the two inputs V_{IN} is amplified (1+R_3/R_4) times at V_X.

$$V_{IN} = V_X / (1 + R_3/R_4)$$

Equation 2.2

This circuit is used to set V_{OUT} at a desired voltage by adjusting the input of the circuit (V_1). The relationship between V_{OUT} and V_{IN} is essential for calculating the remaining DC parameters. Even though the positive input is grounded, the common mode voltage (V_{CM}) is not always 0V as for split supplies but the difference between 0V and the output being at the middle point of the supplies. This means that the V_{CM} applied is with respect to the middle point of the supplies. The supplies used for each test are

specified in the PDS with respect to an initial V_{CM}. Since the positive input for the SJC is grounded, this initial V_{CM} is 0V. Substitute V_{CM}=0V to obtain the supplies per test. V_S is the difference between the positive (V_{S+}) and the negative (V_{S-}) supply.

Relays closed for this circuit are REL1CH0, REL2CH6, REL1CH6, REL1CH2, REL1CH8, REL1CH10, REL2CH7, REL2CH0, REL1CH12, REL2CH2, REL2CH4 and REL2CH5.

2.6.8 Input offset voltage (V_{OS})

Definition: V_{IN} when V_{OUT} is at the middle point of the two supplies [8].

Test conditions: V_S=5.5V, V_{CM}=(V-)+0.8V

Expected value: 2mV

Steps: Apply V_{S+}=4.7V, V_{S-}=–0.8V, adjust the input to set the output at 1.95V, measure V_X to calculate V_{IN}=V_{OS}.

Explanation: Measuring the input offset voltage is the easiest test but it varies with the common mode voltage (V_{CM}) applied to the positive and negative input. By setting the output at the middle point of the supplies when adjusting the input as specified in the test conditions, a V_{CM} of -1.95V is obtained.

2.6.9 Power supply rejection ratio (PSRR)

Definition: The change of V_{IN} with V_S [8].

Test conditions: V_S=2.5V to 5.5V, V_{CM}<(V+)-1.7

Expected value: 60μV/V.

Steps: Apply V_{S+}=3.3V=V_{S1+}, V_{S-}=–2.2V=V_{S1-}, adjust the input to have V_{OUT} at 0.55V, measure V_X to calculate V_{IN}=V_{IN1}. Set V_{S+}=1.8V=V_{S2+}, V_{S-}=-0.7V=V_{S2-}, adjust the input to have V_{OUT} at 0.55V, measure V_X to calculate V_{IN}=V_{IN2}, compute PSRR as shown in Equation 2.3.

$$PSRR = (V_{IN1} - V_{IN2}) / 2(V_{S1+} \quad V_{S2+})$$

Equation 2.3

Explanation: PSRR is used to measure the ability of the op amp to reject a symmetrical change in V_S reflected at V_{IN}. The V_{CM} remains at the same level ($V_{CM1}=V_{CM2}=-0.55V$) when changing V_S to eliminate the V_{CM} contribution in the PSRR calculation. This is obtained by changing the supplies symmetrically.

Special considerations: Make sure decoupling capacitors are connected as close as possible from V_{S+} and V_{S-} to ground.

2.6.10 Common-mode rejection ratio half scale (CMRRh)

Definition: The change of V_{IN} with V_{CM} at half scale [8].

Test conditions: $V_S=5.5V$, $(V-)-0.2V<V_{CM}<(V+)-1.7$

Expected value: 100μV/V (80dB).

Steps: Apply $V_{S+}=5.7V=V_{S1+}$, $V_{S-}=0.2V=V_{S1-}$, adjust the input to have V_{OUT} at $2.95V=-V_{CM1}$, measure V_X to calculate $V_{IN}=V_{IN1}$. Set $V_{S+}=1.7V=V_{S2+}$, $V_{S-}=-3.8V=V_{S2-}$, adjust the input to have V_{OUT} at $-1.05V=-V_{CM2}$, measure V_X to calculate V_{IN2}, compute CMRRh as shown in Equation 2.4.

$$CMRRh = (V_{IN1} - V_{IN2}) / (V_{CM1} - V_{CM2})$$

Equation 2.4

Explanation: CMRR is used to measure the ability of the op amp to reject a change in the V_{CM} reflected at V_{IN}. The V_{CM} is not kept at the same level when changing the supplies. The supplies are moved asymmetrically keeping V_S fixed to eliminate the supplies contribution in the CMRR calculation. The V_{CM} change of 4V serves to classify this CMRR measurement as half scale.

2.6.11 Common-mode rejection ratio full scale (CMRRf)

Definition: The change of V_{IN} with V_{CM} at full scale [8].

Test conditions: $V_S=5.5V$, $(V-)-0.2V<V_{CM}<(V+)+0.2$

Expected value: 316.227μV/V (70dB).

Steps: Apply V_{S+}=5.7V=V_{S1+}, V_{S-}=0.2V=V_{S1-}, adjust the input to have V_{OUT} at 2.95V=-V_{CM1}, measure V_X to calculate V_{IN}=V_{IN1}. Set V_{S+}=-0.2V=V_{S2+}, V_{S-}=–5.7V=V_{S2-}, adjust the input to have V_{OUT} at -2.95V=-V_{CM2}, measure V_X to calculate V_{IN}=V_{IN2}, compute CMRRf as shown in Equation 2.5.

$$CMRRf = (V_{IN1} - V_{IN2}) / (V_{CM1} \quad V_{CM2})$$

Equation 2.5

Explanation: The V_{CM} change of 5.9V serves to classify this CMRR measurement as full scale.

2.6.12 Open loop voltage gain (A_{OL})

Definition: The change of V_{OUT} with V_{IN} [8].

Test conditions: V_S=5.5V, (V_-)+0.005V<V_{OUT}<(V_+)-0.005V

Expected value: 1.778μV/V (115dB)

Steps: Apply V_{S+}=2.75V, V_{S-}=–2.75V, adjust the input to have V_{OUT}=2.74V=V_{OUT1}, measure V_X to calculate V_{IN}=V_{IN1}, adjust the input to obtain V_{OUT}=-2.74V=V_{OUT2}, measure V_X to calculate V_{IN}=V_{IN2}, compute A_{OL} as shown in Equation 2.6.

$$A_{OL} = | (V_{OUT1} \quad V_{OUT2}) / (V_{IN1} \quad V_{IN2}) |$$

Equation 2.6

Explanation: The name of this measurement infers that the op amp must be in open loop in order to measure a change in V_{OUT} with V_{IN}. This circuit configuration is not possible because if applying a V_{IN} of ±1mV, which is the typical accuracy of a DMM, the output would be limited by either of the supplies instead of being amplified 562429.69 times. Therefore a fix voltage change in the output divided by the corresponding change

in V_{IN} is used for the A_{OL} calculation. Notice that the swing condition for this test (more than 5mV from the rail) is not the same specified in the PDS (more than 15mV from the rail). This is because the op amp can actually swing to 5mV, based on data collected, maintaining a linear relationship between the output and the V_{OS}.

2.6.13 Voltage output swing from rail ($SW_{out\pm}$)

Definition: The maximum voltage the output of the op amp can swing from each rail maintaining a linear relationship with respect to V_{OS}.

Test circuit configuration: Summing junction configuration when the open loop gain is performed.

Test conditions: R_L=R5=100kΩ, A_{OL}>100dB

Expected value: 5mV (15mV maximum)

Steps: Obtain a plot of VOUT versus VOS by adjusting the input. Determine the values for VOUT in which the plot becomes not linear. These values are the positive and negative voltage output swing from rail. Since this technique is time consuming, one can only do a pass/fail test by setting the output of the op amp at least 15mV from the rail by adjusting the input and verify if the output can be set in that range, otherwise the device fails for this parameter.

Explanation: Since the output set in the A_{OL} test is in the expected range for this parameter, the positive and negative voltage outputs of the op amp used to calculate A_{OL} can be used to verify if the output can swing at least 15mV from each rail.

CHAPTER 3
TEST HARDWARE

3.1 Socketing the DUT

Socketing and surface mounting a device to adapter boards serve to make electrical contact to the I/O. One is as important as the other. Although the customer is going to solder the component to a printed circuit board (PCB), it is cheaper to use a CSP socket for testing. Assembling only 20 units on adapter boards equals the price of a CSP socket. The OPA2347YED is tested on adapter boards and also with a clam shell type CSP socket having springs to provide the board level interconnection. Thus the CSP socket is not soldered to the device interface board (DIB) but mechanically attached with four nuts. This feature protects the DIB from socket replacement because unsoldering usually causes damage. Edge connector and dual in line package (DIP) are the socketing versions for the adapter boards.

3.2 Printed circuit board design

3.2.1 Protel

Protel is the software utilized to design the printed circuit boards. The purpose of this section is not to explain how to use the software, but to provide the key steps to generate a PCB layout from a circuit schematic.

One project database file stores as many schematic, layout, schematic library or layout library type files as wanted. A schematic file contains any kind of circuit diagram. It is built with symbols created and stored in schematic libraries. A layout file is a by-layer physical representation of a circuit diagram. Schematic and layout can be either independent or mutually synchronized so that any change performed in one is updated in the other. It is always easier to draw the schematic first and then Protel generates the layout. For doing this, the user must type on every symbol placed on the schematic file its layout symbol reference. Nodes are also synchronized [9].

Once every symbol of the layout, also called the footprint, has been oriented and located, the trace width has to be set. All interconnection nodes are automatically traced, based on layout rules, when the autoroute command is activated. Then, traces are manually corrected and revised with the error checklist command. Finally, the following files along with board characteristics have to be zipped and sent to the manufacturer [9].

- Gerber files
- NC drill files

3.2.2 Adapter boards

As previously mentioned, two adapter boards are used to attach the OPA2347YED and make electrical contact to the I/O. The circuit schematic created for both is shown in Figure 3.1. Three symbols appear on that circuit. "C" represents the capacitor footprint of the layout. "DESIGNATOR" represents either the 2*4 hole array for the DIP version or the two-sided 4 pad array for the edge connector type. "OPA2347" represents the footprint of the OPA2347YED.

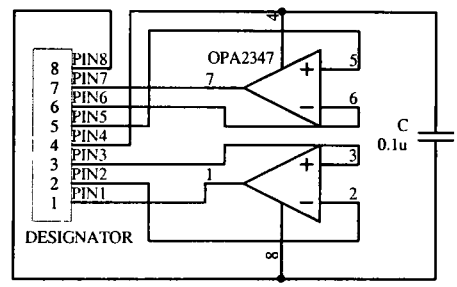

Figure 3.1 Schematic for adapter boards

Then PIN1 to PIN8 labels next to every interconnection wire serves for node identification. This is necessary when performing layout generation based on this circuit schematic.

Top and bottom layer drawings for both adapter boards are shown in Figure 3.2 and Figure 3.3. The capacitor footprint allows either surface mounted or lead based

technologies. Plated holes are indicated as solid black circles with gray contour. Holes are simply solid black holes. CSP pads are solid gray circles with black contour. The 2*4 DIP plated hole array for board PR791 is where pins are inserted and solder to make electrical and mechanical contact to a DIP socket.

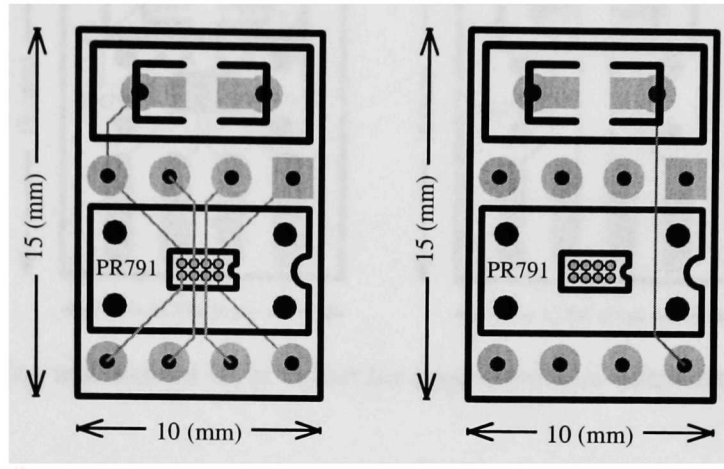

Figure 3.2 Top and bottom layer layout for DIP adapter board PR791

The black contour around CSP pads specifies that the solder mask opening has to be larger than the pad size. It is called non-solder mask defined (NSMD). NSMD prevents solder bridging among solder balls when reflowing is performed. Reflow is the process used to solder the CSP to the board. It consists of applying solder paste on pads, placing the CSP on top of them and generating air hot flux to solder every ball to its respective pad. The amount of solder paste as well as the pad size are based on ball size. The pad size diameter in this case is 0.275mm and solder mask opening is 0.375mm [10].

It is important to know how much down pressure the assembly house will apply when handling the CSPs. Cracks on silicon may be caused if the pick and place piece of equipment is not set up properly. The OPA2347YED handles a pick and place down force of 80 grams (10grams/ball).

Board PR792 (edge connector) is not a common way to adapt a device but a more economical solution. Buying and assembling pins is eliminated with this version. Fabrication cost may be more expensive in comparison with board PR791 (DIP) but the

final cost, including assembly, is less. Four plated holes called vias connect the top and bottom layers. Characteristics for boards PR791 and PR792 is in Table 3.1.

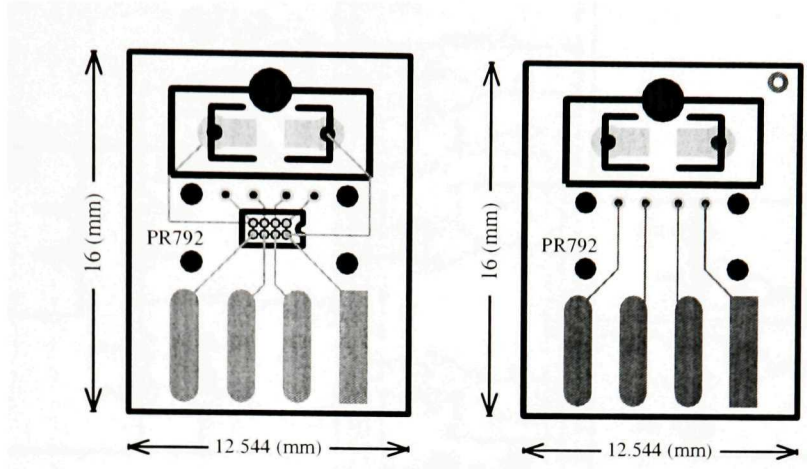

Figure 3.3 Top and bottom layer layout for edge connector adapter board PR792

Table 3.1 Adapter board characteristics

Characteristic	Value
Board material	Polyimide
Board thickness	1.5748mm (62mil)
Trace material	Immersion gold
Trace thickness (T)	25.4μm (1mil)
Trace width (W)	0.1524mm (4mil)
Mask type	LPI-GREEN 2-Sides
CSP pad diameter	0.275mm
Land pattern	Non-solder mask defined (NSMD)
NSMD diameter	0.375mm

3.2.3 Device interface board

As previously stated, the test circuit is implemented on a printed circuit board named bench board or device interface board (DIB). Three socketing options are included on this board: edge connector, DIP and CSP. Symbols for the circuit schematic shown in Figure 3.4 were first created, placed, PCB layout related, and then interconnected including node identifiers.

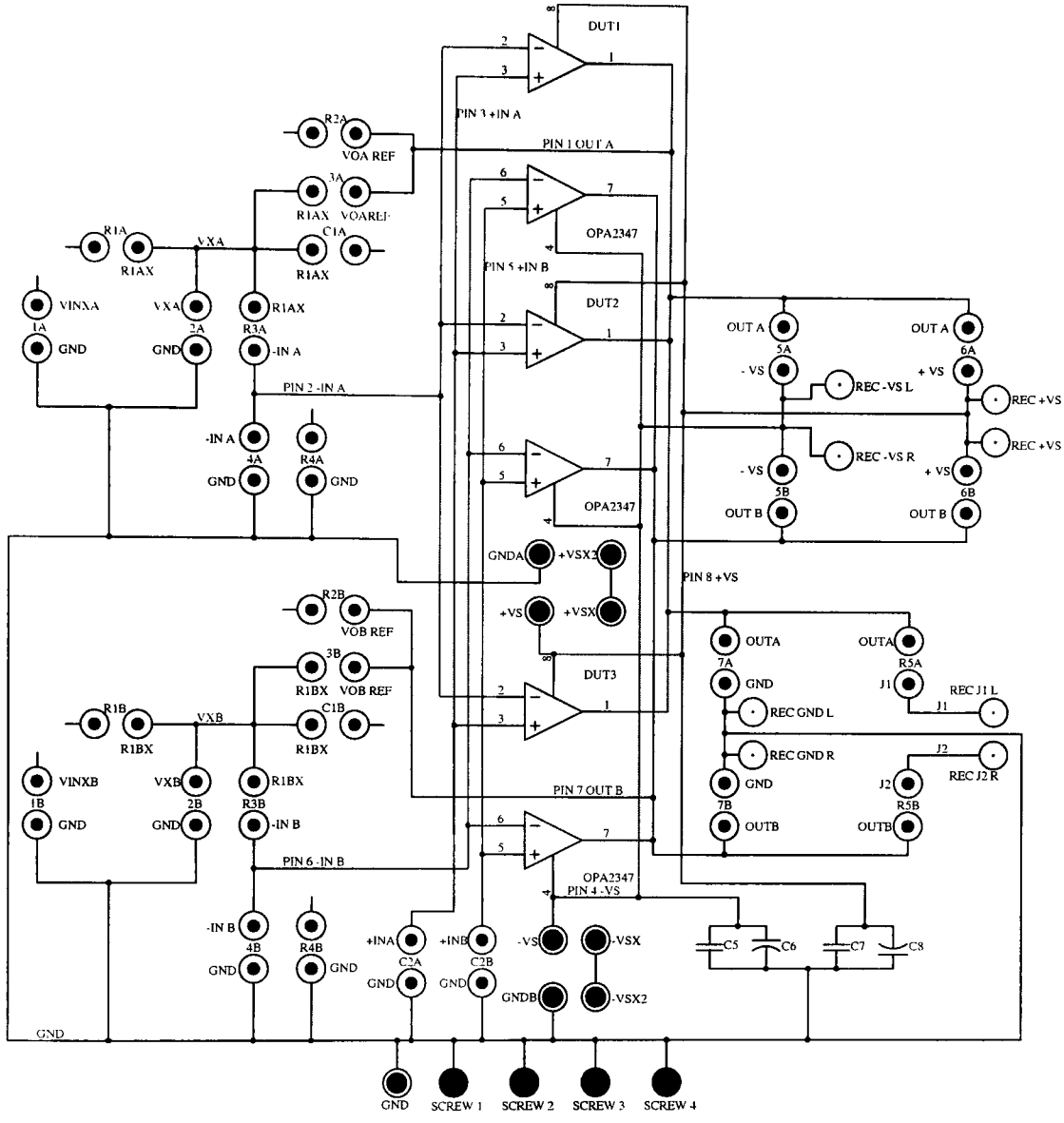

Figure 3.4 Schematic for device interface board PR825

The schematic-to-layout symbol representations are listed below.

- DUT1 → Edge connector socket footprint
- DUT2 → CSP socket footprint
- DUT3 → DIP socket footprint
- Solid circle → Hole for screwing stand off

- Large solid circle → Banana receptacle footprint
- Medium solid circle → Mini banana receptacle footprint
- Small solid circle → Resistor receptacle footprint
- Capacitor → Standard capacitor footprint

All footprints and interconnections are found in Figure 3.5 and Figure 3.6.

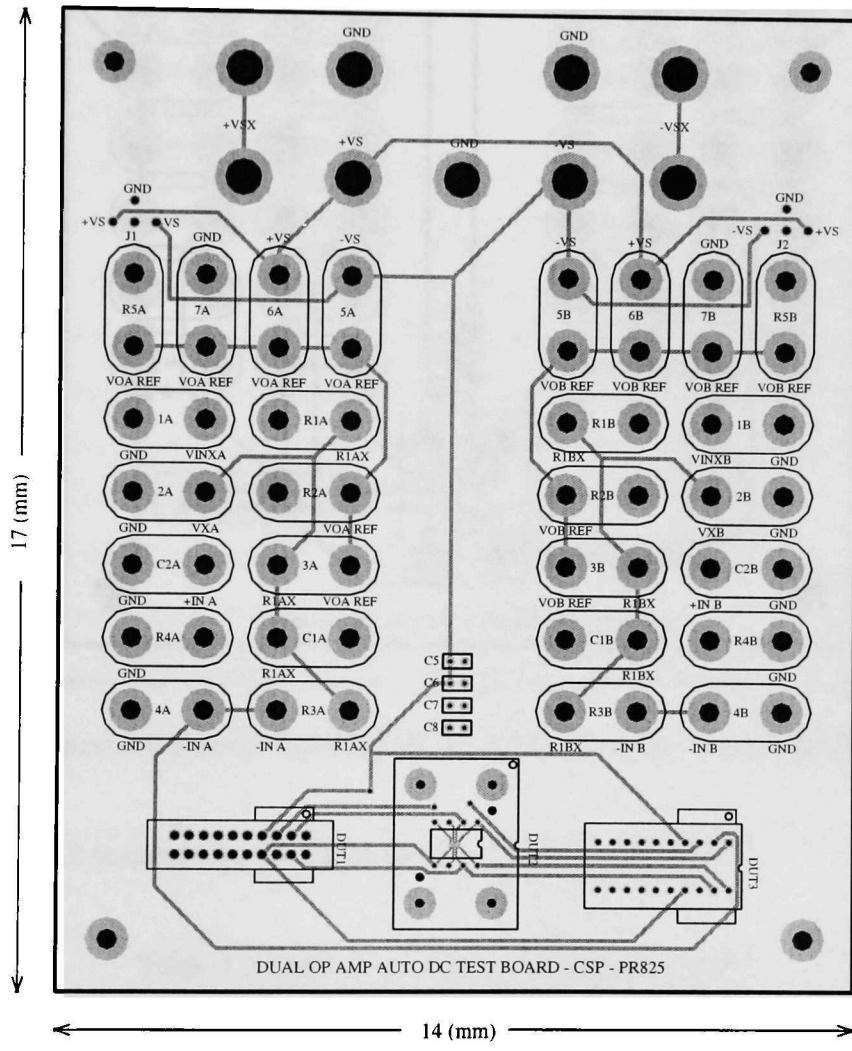

Figure 3.5 Top layer layout for device interface board PR825

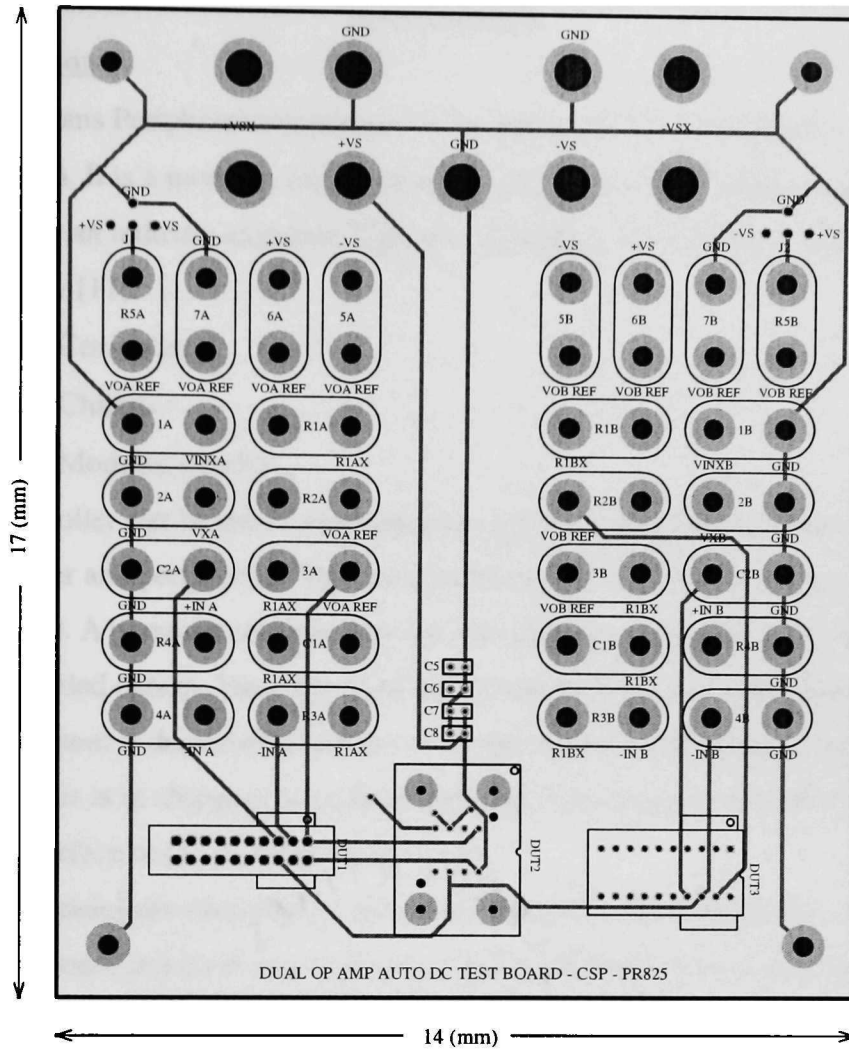

Figure 3.6 Bottom layer layout for device interface board PR825

Table 3.2 summarizes the characteristics of the board PR825.

Table 3.2 Device interface board characteristics

Characteristic	Value
Board material	FR4
Board thickness	1.574mm (62mil)
Trace material	Hard body gold
Trace thickness (T)	25μm (1mil)
Trace width (W)	0.307mm (12mil)
Trace width on DUT2 area (W2)	12 mil (307μm)
Mask type	LPI-GREEN 2-Sides

3.3 PXI system

3.3.1 Introduction

PXI means Peripheral component interconnect (PCI) eXtensions for Instrumentation. It is a modular, computer-based instrumentation platform based on the PCI bus. PCI is an industry-standard, high-speed databus. The elements of a PXI system are listed below [11].

- Controller
- Chassis
- Modules (cards)

A controller can be either a personal computer or an embedded Pentium class or higher computer and peripherals. The main disadvantage between these two options is price and speed. A personal computer can be four times less expensive, but also slower than the embedded option. The embedded option can perform real time applications because the system is dedicated to interact with the modules and nothing else [11].

A chassis is in charge of providing mechanical protection, ventilation, power supply and interface to the modules inserted in it.

PXI modules are classified as multifunction boards and instruments. A multifunction board can be of any type, like a general purpose relay switch, relay multiplexer, analog-to-digital, digital-to-analog, image acquisition, motion control, etc. Instruments can vary from digital multimeters, oscilloscopes, power supplies, spectrum analyzers, and many others [11].

One way to interface a desktop computer with PXI modules is through a link called MXI-3 consisting of a MXI-3 module, cable and PCI card [11].

External instruments like the high resolution 8½ digit DMM HP-3458A or the 6½ digit DMM HP-34401A can communicate with the PXI chassis through a PXI general purpose interface bus (GPIB) card. The instrument receives and sends GPIB commands from and to the controller to perform a specific function [11, 12, 13].

The controller and modules from National Instruments (NI) utilized to test the OPA2347YED with a NI PXI chassis are explained in this section and listed below.

- 1 MXI-3 link
- 1 18-module PXI chassis
- 1 GPIB module with Ethernet port (NI PXI-8212)
- 2 General purpose relay switch card (NI PXI-2565)
- 1 Electromechanical relay multiplexer card (NI PXI-2503)
- 1 6½ Digital multimeter (NI PXI-4070)
- 1 Analog output (NI PXI-6704)

The interconnection among modules and DIB is also covered.

3.3.2 Controller

A personal computer (PC) is the controller for the automated bench system. A Pentium I running at 100MHz with 96Mb of RAM is good enough for the tester. The PC communicates with the PXI modules through a MXI-3 link.

3.3.3 18-slot PXI chassis (PXI-1006 chassis)

In order to have extra slots for future modules, an 18-slot PXI chassis was chosen. The current system comes with PXI and CompactPCI module capability and only occupies 9 slots. Modules are easily plugged into the system, like drawers into a desk. Before connecting the chassis with the MXI-3 cable to the computer, all drivers must be installed on the PC. The PC is turn on after the PXI system, so that all inserted modules are recognized [14].

3.3.4 General purpose relay switch card (NI PXI-2565)

The NI PXI-2565 is a 16-channel general purpose electromechanical relay switch card. The relays can switch 30V DC at 5A DC with a resistive load. They have a contact resistance of 30mΩ and operate (open or close) in no more than 10ms. Figure 3.7 shows the NI PXI-2565 switch architecture [15].

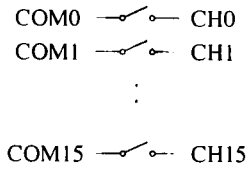

Figure 3.7 NI PXI-2503 Switch architecture

3.3.5 Electromechanical relay multiplexer card (NI PXI-2503)

A multiplexer is a set of electromechanical or semiconductor switches with a common output that can select one of a number of input signals.

The NI PXI-2503 is an electromechanical relay multiplexer card in a PXI/Compact PCI format with 24*1 two-wire multiplexer. It also operates with 4 banks of 6 two-wire channels (2-wire quad 6*1), each bank having its own common two-wire output. The board is software-configurable as shown below [16].

- 1-wire MUX
- 2-wire 12*1 12*1
- 2-wire MUX
- 2-wire quad 6*1
- 4-wire MUX
- 6*4 matrix

The relays have a contact resistance of 100mΩ, operate (open or close) in no more than 5ms and can switch 30V DC at 1A DC with a resistive load. Figure 3.8 shows the NI PXI-2503 switch architecture [16].

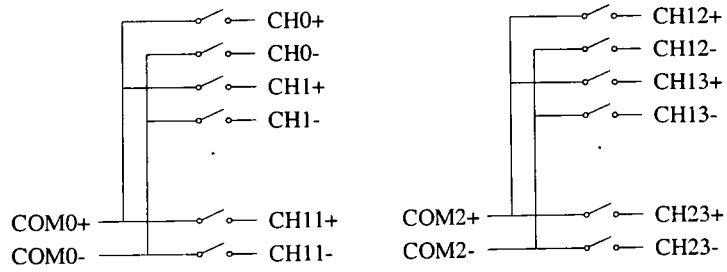

Figure 3.8 NI PXI-2503 2-wire 12*1 12*1 switch architecture

The NI PXI-2503 has a front panel 68-pin female connector. Table 3.3 shows the pin assignments. The NI TB-2505 is a front panel mounting screw terminal block that is plugged into the female connector in order to electrically access the channels, common terminals and other pins of the NI PXI-2503. The pin assignments for the two-wire mode using the NI TB-2505 are shown in Table 3.4 [16].

Table 3.3 NI PXI-2503 front connector pin assignments for two-wire mode

Pin name	Pin #		Pin #	Pin name
CJS0-	34		68	CJS0+
CH0-	33		67	CH0+
CH1-	32		66	CH1+
CH2-	31		65	CH2+
CH3-	30		64	CH3+
CH4-	29		63	CH4+
CH5-	28		62	CH5+
COM0-	27		61	COM0+
COM1-	26		60	COM1+
CH6-	25		59	CH6+
CH7-	24		58	CH7+
CH8-	23		57	CH8+
1_WIRE_LO_REF	22		56	GND
CH9-	21		55	CH9+
CH10-	20		54	CH10+
CH11-	19		53	CH11+
AB0-	18		52	AB0+
AB1-	17		51	AB1+
CH12-	16		50	CH12+
CH13-	15		49	CH13+
CH14-	14		48	CH14+
CH15-	13		47	CH15+
CH16-	12		46	CH16+
CH17-	11		45	CH17+
COM2-	10		44	COM2+
COM3-	9		43	COM3+
+5 V	8		42	SCAN_ADV
GND	7		41	EXT_TRIG_IN
CH18-	6		40	CH18+
CH19-	5		39	CH19+
CH20-	4		38	CH20+
CH21-	3		37	CH21+
CH22-	2		36	CH22+
CH23-	1		35	CH23+

Table 3.4 NI PXI-2503 pin assignments for two-wire mode using the NI TB-2505

Pin #	Pin name	Pin #	Pin name	Pin #	Pin name	Pin #	Pin name
10	COM2-			09	COM3-		
44	COM2+			43	COM3+		
13	CH15-	05	CH19-	01	CH23-		
47	CH15+	39	CH19+	35	CH23+	41	TRIG IN
14	CH14-	06	CH18-	02	CH22-	42	SCANADV
48	CH14+	40	CH18+	36	CH22+		
15	CH13-	11	CH17-	03	CH21-		
49	CH13+	45	CH17+	37	CH21+		
16	CH12-	12	CH16-	04	CH20-		
50	CH12+	46	CH16+	38	CH20+		
19	CH11-	24	CH7-	30	CH3-		
64	CH3+	58	CH7+	53	CH11+		
31	CH2-	25	CH6-	20	CH10-		
65	CH2+	59	CH6+	54	CH10+		
32	CH1-	28	CH5-	21	CH9-		
66	CH1+	62	CH5+	55	CH9+		
33	CH0-	29	CH4-	23	CH8-		
67	CH0+	63	CH4+	57	CH8+		
22	1wireREF	26	COM1-	27	COM0-		
GND	GND	60	COM1+	61	COM0+		
52	AB0+			51	AB1+		
18	AB0-			17	AB1-		

3.3.6 GPIB module with Ethernet port (NI PXI-8212)

The NI PXI-8212 is IEEE 488.2 compatible, Plug and Play, software configurable and capable of transfer rates up to 7.7Mbytes/s. It is built with the Intel 82559 Fast Ethernet controller (10baseT and 100baseTX). The GPIB module is primarily dedicated to communicate with and control GPIB instruments with GPIB commands [11].

3.3.7 PXI-MXI-3 copper link (NI PXI-PCI8330)

The PXI-MXI-3 copper link consists of a NI PXI-MXI-3 module, PCI-MXI-3 card and a 2m copper cable. It is a direct PC control of PXI systems. Once the drivers are installed, the stand-alone PC recognizes the PXI system modules as connected to its PCI bus. Peak and sustained data rate of 132Mbytes/s and 84Mbytes/s can be reached [11].

3.3.8 6½ digital multimeter (NI PXI-4070)

This digital multimeter (DMM) can be configured to measure with either fixed or auto range/resolution. When autorange is set, the DMM takes an adjusting-range reading

first with its highest range and then measures the signal. Autorange time for DC V and DC I is 5ms. Some range/resolution options for voltage and current measurements are 100mV/100nV, 1V/1μV, 10V/10μV and 20mA/10nA [17].

3.3.9 Analog output (NI PXI-6704)

The NI PXI-6704 is a 16-bit analog source. It delivers 16 voltage outputs with ±10V/±1mV (range/accuracy) and ±10mA max, 16 current outputs with 20mA/±2μA (range/ accuracy), and 8 digital I/O lines. Table 3.5 shows the front connector pin assignments [11, 18].

Table 3.5 NI PXI-6704 front connector pin assignments

Pin name	Pin #		Pin #	Pin name
+5V	1		35	DGND
DIO0	2		36	DGND
DIO1	3		37	DGND
DIO2	4		38	RFU
DIO3	5		39	DGND
DIO4	6		40	RFU
DIO5	7		41	DGND
DIO6	8		42	DGND
DIO7	9		43	AGND
ICH3	10		44	VCH15
AGND15/AGND31	11		45	ICH30
VCH14	12		46	AGND14/AGND30
ICH29	13		47	VCH13
AGND13/AGND29	14		48	ICH28
VCH12	15		49	AGND12/AGND28
ICH27	16		50	AGND11/AGND27
VCH11	17		51	ICH26
AGND10/AGND26	18		52	VCH10
AGND	19		53	ICH25
AGND9/AGND25	20		54	VCH9
ICH24	21		55	AGND8/AGND24
VCH8	22		56	AGND
ICH23	23		57	VCH7
AGND7/AGND23	24		58	ICH22
VCH6	25		59	AGND6/AGND22
ICH21	26		60	VCH5
AGND5/AGND21	27		61	ICH20
VCH4	28		62	AGND4/AGND20
ICH19	29		63	VCH3
AGND3/AGND19	30		64	ICH18
VCH2	31		65	AGND2/AGND18
ICH17	32		66	VCH1
AGND1/AGND17	33		67	ICH16
VCH0	34		68	AGND0/AGND16

Its slew rate is 0.5V/μs and 1mA/μs, while its settling time is 5.4ms to ±0.5 LSB for voltage and 7.2ms to ±0.5 LSB for current [11, 18].

The NI SCB-68 is a shielded terminal that is plugged into the front connector of the NI PXI-6704. VCH<0..15> and ICH<16..31>) are the voltage and current output channels respectively. Table 3.6 shows the pin assignments using the NI SCB-68. Every channel is referenced to a ground node AGND<0/16..15/31> which is common to a voltage and current channel [18].

Table 3.6 NI PXI-6704 pin assignments using the NI SCB-68

Pin #	Pin name	Pin #	Pin name	Pin #	Pin name
68	AGND0/AGND16				
34	VCH0				
67	ICH16	12	VCH14	1	+5V
33	AGND1/AGND17	46	AGND14/AGND30	35	DGND
66	VCH1	13	ICH29	2	DIO0
32	ICH17	47	VCH13	36	DGND
65	AGND2/AGND18	14	AGND13/AGND29	3	DIO1
31	VCH2	48	ICH28	37	DGND
64	ICH18	15	VCH12	4	DIO2
30	AGND3/AGND19	49	AGND12/AGND28	38	RFU
63	VCH3	16	ICH27	5	DIO3
29	ICH19	50	AGND11/AGND27	39	DGND
62	AGND4/AGND20	17	VCH11	6	DIO4
28	VCH4	51	ICH26	40	RFU
61	ICH20	18	AGND10/AGND26	7	DIO5
27	AGND5/AGND21	52	VCH10	41	DGND
60	VCH5	19	AGND	8	DIO6
26	ICH21	53	ICH25	42	DGND
59	AGND6/AGND22	20	AGND9/AGND25	9	DIO7
25	VCH6	54	VCH9	43	AGND
58	ICH22	21	ICH24	10	ICH31
24	AGND7/AGND23	55	AGND8/AGND24	44	VCH15
57	VCH7	22	VCH8	11	AGND15/AGND31
23	ICH23	56	AGND	45	ICH30

3.4 Hardware interconnection

Although this thesis is about an automated bench setup, the PXI system modules, GPIB instruments, and bench board must be manually interconnected before starting the test. Twisted pair cables in different colors, mini banana plugs and banana plugs are used for the interconnection. Table 3.7 through Table 3.12 indicate the interconnection.

Table 3.7 Interconnection between NI PXI-4070 DMM and NI PXI-2503 Multiplexer

NI PXI-4070 DMM	NI PXI-2503 Multiplexer (NI TB 2605)		Color identifier
Banana double			Twisted
Voltage Lo	COM0-	27	Black
Voltage Hi	COM0+	61	Red
Current Lo	COM2-	10	Black
Current Hi	COM2+	44	Red white

Table 3.8 Interconnection between NI PXI-2565 REL 1 and bench board

NI PXI-2565 REL 1	Bench board	Color identifier
	Mini banana double	Twisted
CH0	1A VINXA & R1A	Black & blue marine
CH1	R1A	Black & blue marine white
CH2	R2A & 3A R1AX	Black & brown
CH3	3A	Black & brown white
CH4	3A VOA & C1A	Black & gray
CH5	R3A	Black & gray white
CH6	4A -INA & R4A	Black & green
CH7	4A	Black & green white
CH8	C2A	Black & orange
CH9	7A-GND & R5A-J1	Black & orange white
CH10	1B VINXB & R1B	Black & purple
CH11	R1B	Black & purple white
CH12	R2B & 3B R1BX	Black & white
CH13	3B	Black & black white
CH14	3B VOB & C1B	Black & yellow
CH15	R3B	Black & yellow white

Table 3.9 Interconnection between NI PXI-2565 Relay 2 and bench board

NI PXI-2565 REL 2	Bench board	Color identifier
	Mini banana double	Twisted
CH0	4B –INB & R4B	Blue & brown
CH1	4B	Blue & brown white
CH2	C2B	Blue & gray
CH3	7B GND & R5B-J2	Blue & gray white
	Banana double	Twisted
CH4	+VS & +VSX	Blue & green
CH5	-VS & -VSX	Blue & green white
	Mini banana double	Twisted
CH6	2A VXA & Floating mini banana A	Blue & purple
CH7	2B VXB & Floating mini banana B	Blue & purple white

It is important to notice that polarity is not necessary when connecting the relay modules to the bench board because each channel represents the two terminals of a relay.

Table 3.10 Interconnection between NI PXI-2503 Multiplexer and bench board

NI PXI-2503 MUX through NI TB 2605		Bench board	Color identifier
Voltage measurements			
		Mini banana double	Twisted
CH0- CH0+	33 67	1A GND 1A VINXA	Pink Blue marine
CH1- CH1+	32 66	1B GND 1B VINXB	Pink Blue marine white
		Banana double	Twisted
CH2- CH2+	31 65	GND +VSX	Pink Brown
CH3- CH3+	30 64	GND -VSX	Pink Brown white
		Mini banana double	Twisted
CH4- CH4+	29 63	2A GND Floating mini banana A	Pink Gray
CH5- CH5+	28 62	2B GND Floating mini banana B	Pink Gray white
CH6- CH6+	25 59	7A GND 7A VOA	Pink Green
CH7- CH7+	24 58	7B GND 7B VOB	Pink Green white
CH8- CH8+	23 57	6A +VS 6A VOA	Pink Orange
CH9- CH9+	21 55	6B +VS 6B VOB	Pink Orange white
CH10- CH10+	20 54	5A –VS 5A VOA	Pink Purple
CH11- CH11+	19 53	5B –VS 5B VOB	Pink Purple white
Current measurements			
		Banana double	Twisted
CH12- CH12+	16 50	+VS +VSX	Pink White
CH13- CH13+	15 49	-VSX -VS	Pink Black white
		Mini banana double	Twisted
CH14- CH14+	14 48	7A GND 7A VOA	Pink Yellow
CH15- CH15+	13 47	7B GND 7B VOB	Pink Yellow white

Table 3.11 Interconnection between NI PXI-6704 Analog output and bench board

NI PXI-6704 Analog output (NI TB 2605)		Bench board	Color identifier
Voltage supply			
		Mini banana double	Twisted
AGND0	68	1A GND	Pink
VCH0	34	1A VINXA	Red
AGND1	33	1B GND	Pink
VCH1	66	1B VINXB	Red white
Voltage supply			
		Banana single	Single
VCH2	31	+VSX	Red
VCH3	63	-VSX	White
AGND	65	GND	Black

3.4.1 HP DMMs

The HP-3458A achieves a very high resolution of 8½ digits with a reading rate of 100,000 readings/s. Employed for production and bench test, this is the most common DMM used to calibrate DMMs with lower resolution. The HP-34401A is a DMM with 6½ digits of resolution. Both HP DMMs can be controlled with GPIB commands. A calibrated HP-34401A DMM is used to verify that the NI PXI-4070 remains calibrated [12, 13].

Table 3.12 Interconnection between NI PXI-4070 DMM and HP-34401A DMM

NI PXI-4070 DMM	HP-34401A DMM	Color identifier
Banana double	Banana double	Twisted
Voltage Lo	Voltage Lo	Black
Voltage Hi	Voltage Hi	Red

CHAPTER 4
TEST SOFTWARE

4.1 Test program based on LabVIEW

LabVIEW is a graphical programming language based on icons instead of text to develop applications. Data flowing from icon to icon determine the program sequence. On the other hand text-based programming uses lines of instructions to perform execution [19].

Two windows called Front Panel (FP) and Control Diagram (CD) are used to create programs in LabVIEW. Controls and indicators present in the front panel serve to input and output data. The front panel is the user interface. The control panel contains the representation, manipulation and interconnection of these controls and indicators [19].

For example, if two controls and one indicator are created on the front panel, their representations are also on the control diagram. Any mathematical manipulation of the two controls can be performed only in the control diagram. When connecting the addition of the two inputs to the output in the control diagram it is possible to see the result in the indicator of the front panel [19].

A program created in LabVIEW is called a Virtual Instrument (VI). Any VI inserted in another VI is named a subVI. The icon representing a subVI placed in the control diagram of a VI can have input and output terminals around its perimeter for interconnection [19].

The most typical way to sequence subVIs is with the use of input and output error terminals located on the left and right side of the subVI icon. A missing connection can cause an error out message from a subVI. The error will pass through all subsequent subVIs connected unless an error detection subVI stops execution [19].

4.2 Test program subVIs

Since every user-created subVI has an error in control and error out indicator, as shown in Figure 4.1, they are not included when presenting the corresponding front panel in order to save printing area. Built-in LabVIEW subVIs are only mentioned when present in user-created subVIs. Documentation of all the subVIs not explained in this chapter can be found in the help menu of the LabVIEW software.

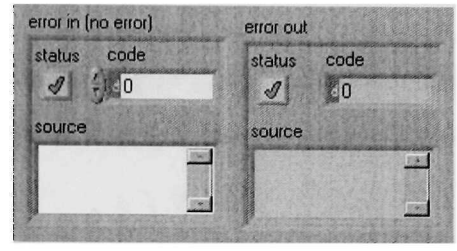

Figure 4.1 Error in control and error out indicator

4.2.1 Delay (mS) subVI

The Delay (mS) subVI introduces a pause in milliseconds during the transition of the program. It has an input named "Delay(mS)". Its icon, FP and CD are shown Figure 4.2.

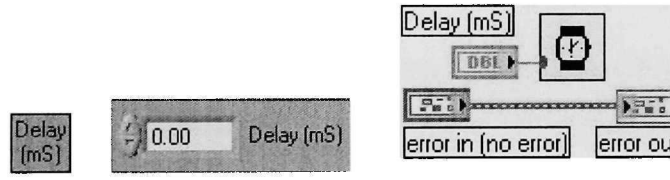

Figure 4.2 Delay subVI icon, FP and CD

4.2.2 NI AO subVI

The NI AO subVI sets a voltage level in a specific channel of the NI-PXI 6704 analog output. It has two inputs called "Channel" and "Voltage". Its icon, FP and CD are shown in Figure 4.3.

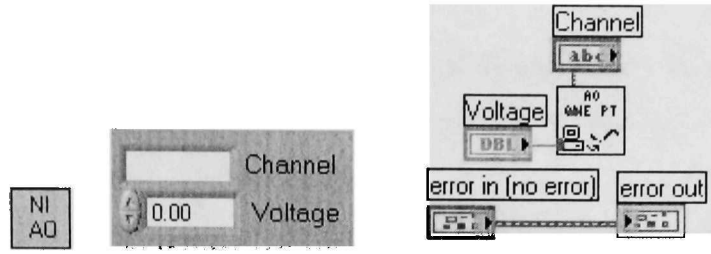

Figure 4.3 NI AO subVI icon, FP and CD

4.2.3 NI DMM I subVI

The NI DMM I subVI configures the NI PXI-4070 DMM to measure dc current with a range/resolution of 20mA/10nA. It has one output named "Current". Figure 4.4 shows its icon, FP and CD.

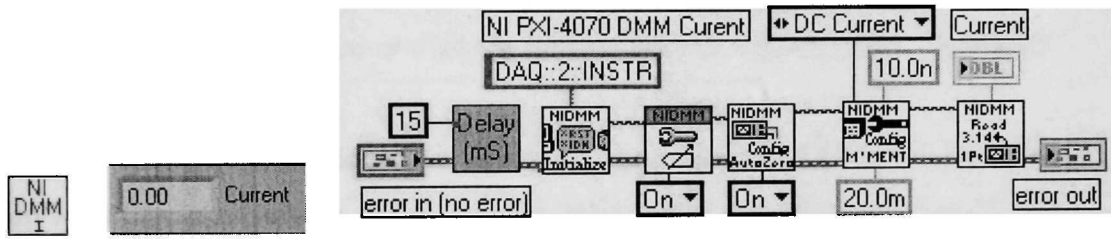

Figure 4.4 NI DMM I subVI icon, FP and CD

4.2.4 NI DMM V subVI

The NI DMM V subVI reads the measurement from the NI PXI-4070 DMM previously configured for dc voltage with auto range/resolution. It has one output named "Volts". Examine Figure 4.5 for its icon, FP and CD.

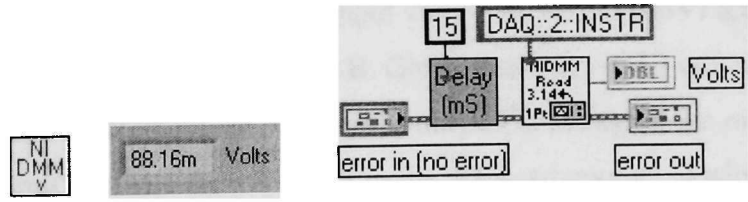

Figure 4.5 NI DMM V subVI icon, FP and CD

4.2.5 HP DMM V subVI

The HP DMM V subVI configures the HP-34401A DMM to measure DC voltage with a range of 10V. It has one output named "Volts". Figure 4.6 shows its icon, FP and CD.

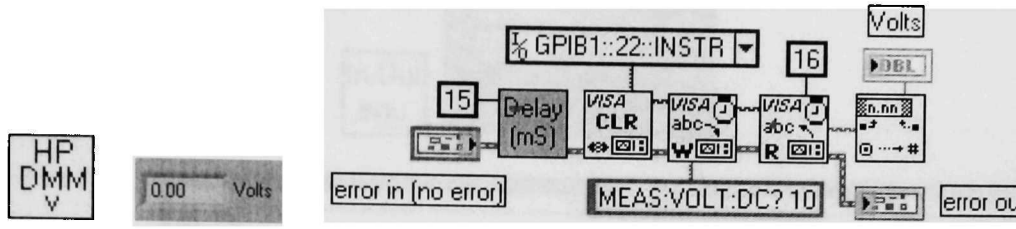

Figure 4.6 HP DMM V subVI icon, FP and CD

4.2.6 In-out equ subVI

The In-out equ subVI calculates the input-output voltage equation for the summing junction configuration with V_{S+} and V_{S-} at a specific potential. Figure 4.7 shows its icon, FP and CD.

The frame 0 of the Sequence Structure (SS) (Figure 4.7 CD 00 00) has a while loop where an input voltage global variable (GV) "Vinx" is applied with the NI AO subVI and the output voltage is measure with the NI DMM V subVI. If the output is larger than "Desired output" GV, "Increment" GV is subtracted from "Vinx" GV, otherwise added. "Increment" GV is divided by 2. When the output voltage is either below V_{S+} or above V_{S-} by 0.25V for both iterations of the For loop without surpassing iteration 15 of the while loop, the frame 0 of the SS ends. In the frame 1 of the SS (Figure 4.7 CD 01 00) coordinates (X1,Y1) and (X2,Y2) are used to calculate the slope of the input-output voltage equation.

Depending on the "AO channel" input value, the NI AO subVI applies the input voltage "Vinx" GV to either op amp A or B. Global variables (GV) initialized previously are "Vinx" at 0 and "Increment" at 5. "Desired output" is always at the middle level of the supplies. "Limit" defines the ±range from the "Desired output" in which the output must be in order to store in-range coordinates (X1,Y1) and (X2,Y2). X1 and X2 are input voltages. Y1 and Y2 are output voltages. "Limit" is always VS/2-0.25. "Cycle flag" GV

outputs 0 only if the while loop surpasses 15 iterations, otherwise it outputs 1. "Slope"=(Y2-Y1)/(X2-X1) outputs the slope of the equation.

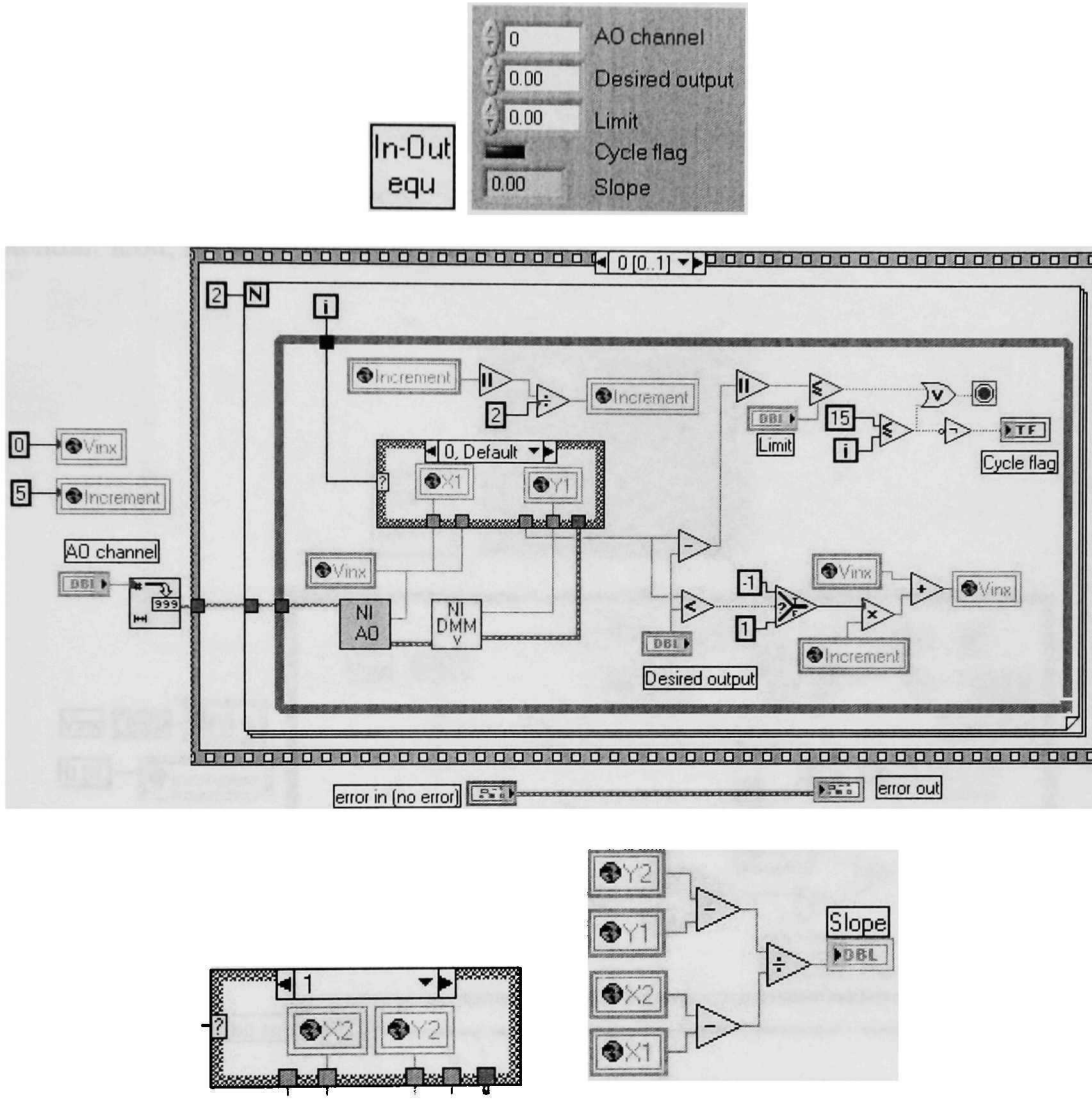

Figure 4.7 In-out equ subVI icon, FP and CD 00 00, CD 00 01 and CD 01 00

By substituting any desired output voltage Y in Equation 4.1 its corresponding input voltage X can be calculated. The slope along with any pair of coordinates (X1,Y1) or (X2,Y2) acquired from the In-out equ subVI are needed for the calculation.

$$X = (Y-Y1)/Slope - X1$$

Equation 4.1

4.2.7 Set out 1 subVI

Based on an initial input voltage "Vinx" GV calculated with the input-output voltage equation from in-out eq subVI, the Set out 1 subVI moves the output at a desired voltage level by adjusting the input with "Increment" GV having V_{S+} and V_{S-} at a specific potential. Icon, FP and CD for this subVI are shown in Figure 4.8.

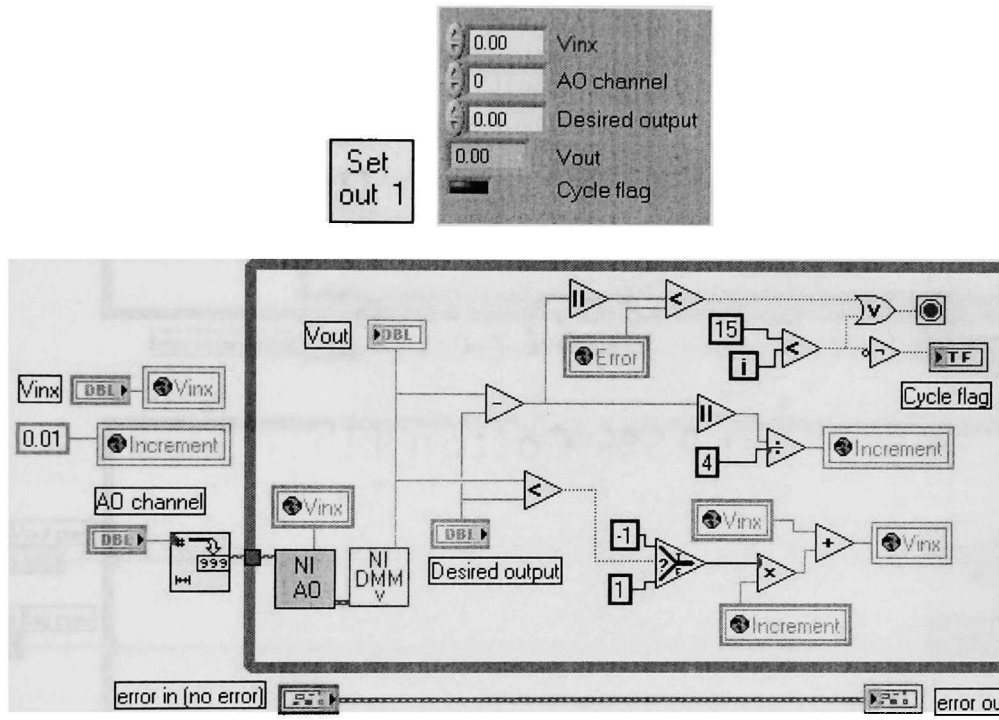

Figure 4.8 Set out 1 subVI icon, FP and CD

4.2.8 Set out 2 subVI

Only if the Set out 1 subVI surpasses 15 iterations, the Set out 2 subVI changes the output to a desired voltage level starting with an initial voltage "Vinx" GV of 0V and an "Increment" GV of 5V. Otherwise the Set out 2 subVI passes "Vout" and "Cycle flag" coming from the Set out 1 subVI. Refer to Figure 4.9 for its icon, FP and CD.

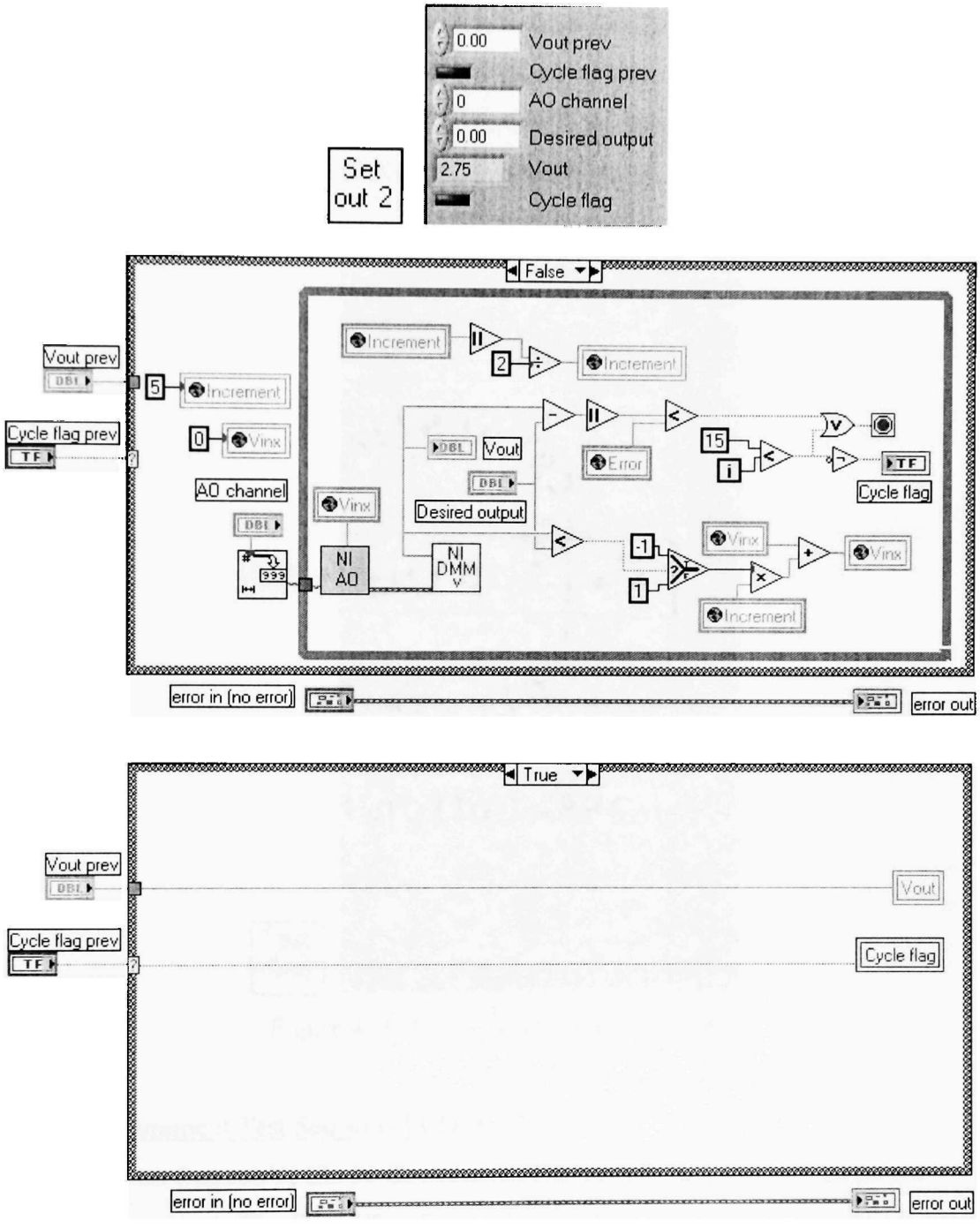

Figure 4.9 Set out 2 subVI icon, FP, CD 00 00 and CD 01 00

4.3 Test Seq subVI

The Test Seq subVI is in charge of testing all DC parameters, writing the results to a *.csv test file, and output the results and pass/fail flags. This is the most important subVI. Global variables (GV) needed for this subVI are previously initialized in the Test program VI. Refer to Figure 4.10 for its icon and FP.

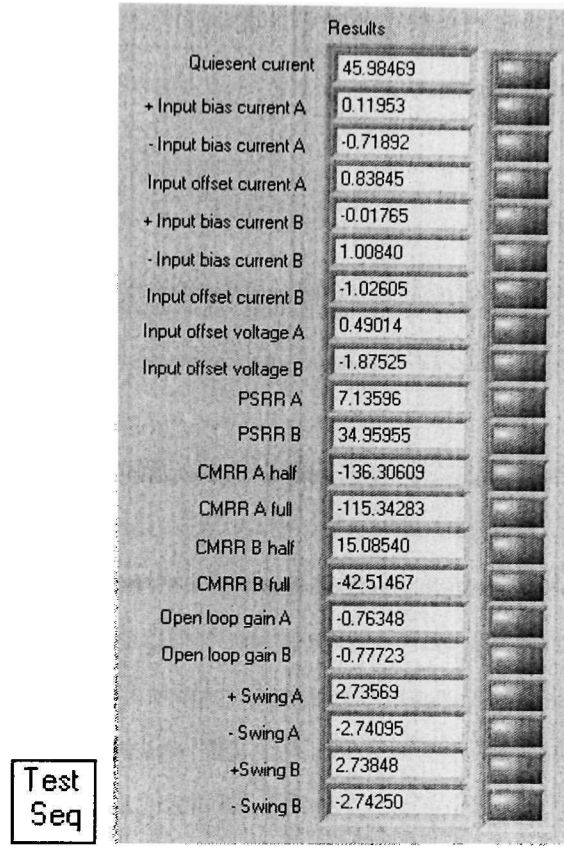

Figure 4.10 Test Seq subVI icon and FP

4.3.1 I_Q measurement Test Seq subVI CD 00 00

The Test Seq subVI CD 00 00 shown in Figure 4.11 performs the quiescent current measurement. The GV "N" indicates that the Test Seq subVI is repeated N times.

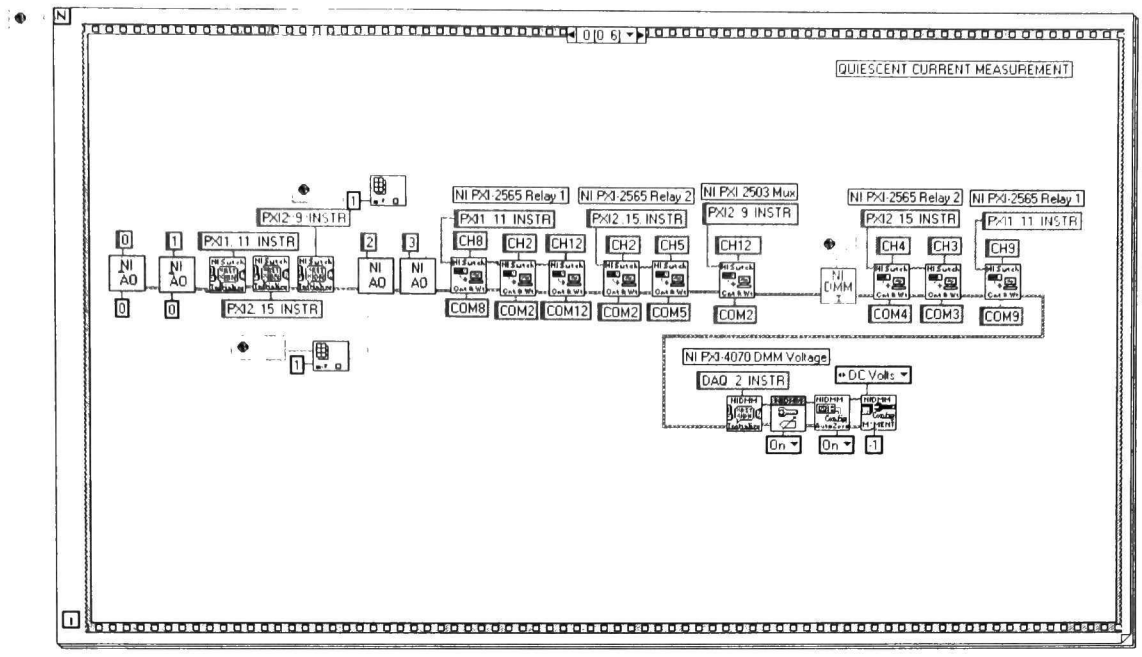

Figure 4.11 Quiescent current measurement Test Seq subVI CD 00 00

REL1, REL2 and MUX relays are open. The two inputs of op amp A and B are set to zero. The power supplies are applied based on the corresponding two values for this test selected from the GV vectors "+VSs" and "-VSs". REL1CH8, REL1CH2, REL1CH12, REL2CH2 and REL2CH5 are closed to have the voltage follower circuit shown in Figure 2.9. MUXCH12 relay is then closed to measure I_Q with the NI DMM I subVI and then the result is stored in "IQ" GV. REL2CH4, REL2CH3, and REL1CH9 are closed to connect VCH2 (V_{S+}) and R5. Finally the NI PXI 4070 is configured to measure voltage with autorange.

4.3.2 I_{B+} A measurement Test Seq subVI CD 01 00

The Test Seq suvVI CD 01 00 shown in Figure 4.12 performs the positive input bias current measurement of op amp A.

The power supplies are applied based on the corresponding two values for this test selected from the GV vectors "+VSs" and "-VSs". All the relays of the MUX are open. MUXCH6 is closed to allow measuring the output of op amp A. REL1CH8 is open

to start the current integration with C2A based on the stop watch integration circuit shown in Figure 2.10. A delay indicated by "IB Delta start" GV is introduced before taking the first output reading for settling. Another delay "IB Delta t" is used before taking the second output reading. I_{B+} for op amp A is calculated by taking the difference of the two output readings multiplied by "IB CAP"/"IB delta t". The result is then stored in "+IB A" GV. The integration status flag "IB Vout flag" is utilized to monitor the output of op amp A with the Test program VI.

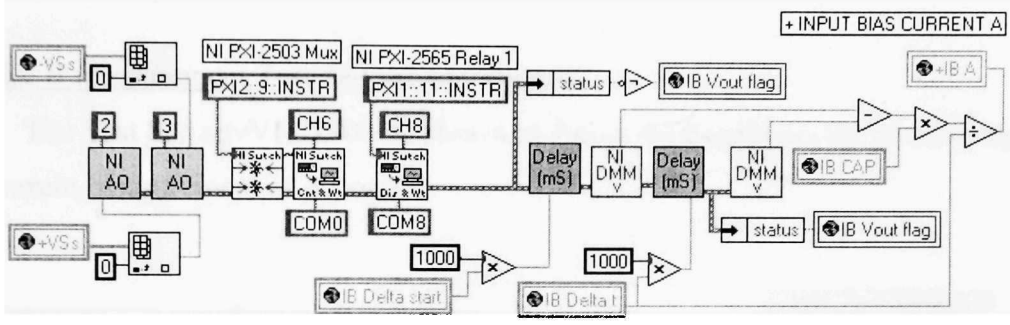

Figure 4.12 Positive input bias current measurement A Test Seq subVI CD 01 00

4.3.3 I_{B-} A measurement Test Seq subVI CD 01 01

The Test Seq suvVI CD 01 01 shown in Figure 4.13 performs the negative input bias current measurement of op amp A and calculates I_{OSA}.

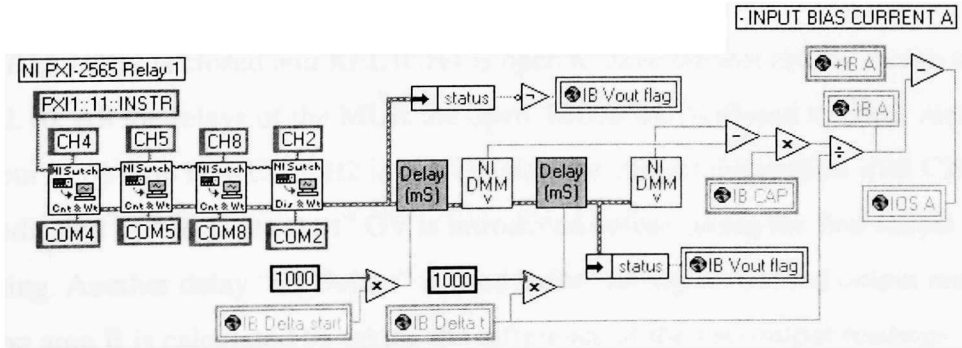

Figure 4.13 Negative input bias current measurement A Test Seq subVI CD 01 01

REL1CH4, REL1CH5 and REL1CH8 are closed to have the test circuit shown in Figure 2.11. REL1CH2 is open to start the current integration with C1A. A delay indicated by "IB Delta start" GV is introduced before taking the first output reading for settling. Another delay "IB Delta t" is used before taking the second output reading. I_{B-} for op amp A is calculated by taking the inverse difference of the two output readings multiplied by "IB CAP"/"IB delta t". The result is then stored in "-IB A" GV. I_{OSA} is calculated and stored in "IOS A". The integration status flag "IB Vout flag" is utilized to monitor the output of op amp A with the Test program VI.

4.3.4 I_{B+} B measurement Test Seq subVI CD 01 02

The Test Seq suvVI CD 01 02 shown in Figure 4.14 performs the positive input bias current measurement of op amp B.

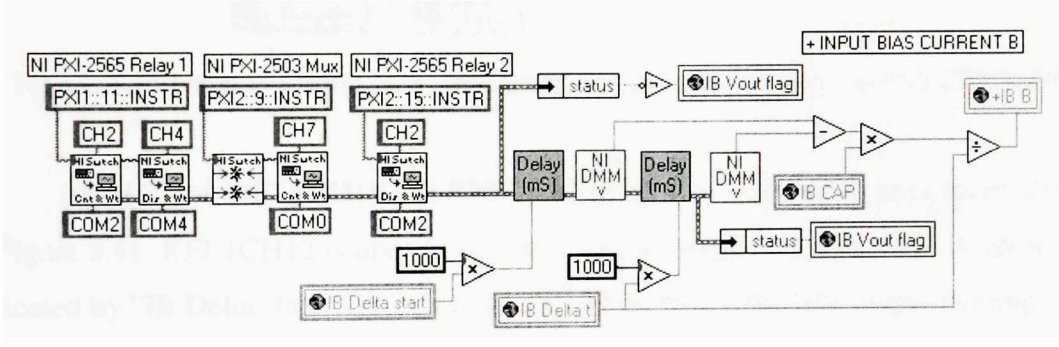

Figure 4.14 Positive input bias current measurement B Test Seq subVI CD 01 02

REL1CH2 is closed and REL1CH4 is open to have the test circuit shown in Figure 2.10. All the relays of the MUX are open. MUXCH7 is closed to allow measuring the output of op amp B. REL2CH2 is open to start the current integration with C2B. A delay indicated by "IB Delta start" GV is introduced before taking the first output reading for settling. Another delay "IB Delta t" is used before taking the second output reading. I_{B+} for op amp B is calculated by taking the difference of the two output readings multiplied by "IB CAP"/"IB delta t". The result is then stored in "+IB B" GV. The

integration status flag "IB Vout flag" is utilized to monitor the output of op amp B with the Test program VI.

4.3.5 I_{B-} B measurement Test Seq subVI CD 01 03

The Test Seq suvVI CD 01 03 shown in Figure 4.15 performs the negative input bias current measurement of op amp B and calculates I_{OSB}.

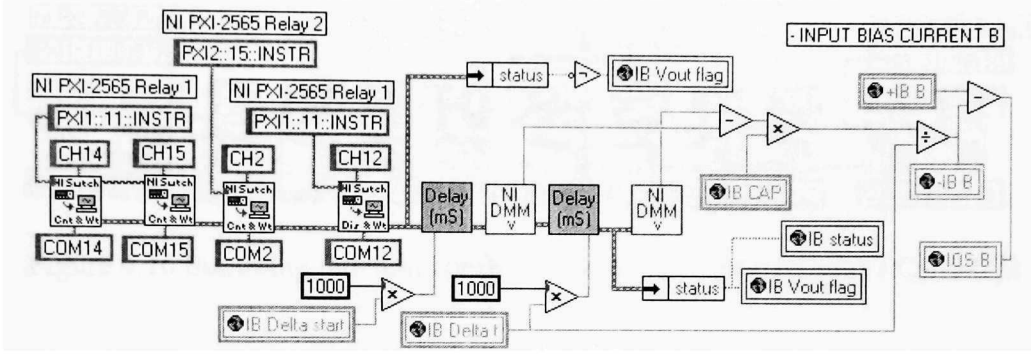

Figure 4.15 Negative input bias current measurement B Test Seq subVI CD 01 03

REL1CH14, REL1CH15 and REL2CH2 are closed to have the test circuit shown in Figure 2.11. REL1CH12 is open to start the current integration with C1B. A delay indicated by "IB Delta start" GV is introduced before taking the first output reading for settling. Another delay "IB Delta t" is used before taking the second output reading. I_{B-} for op amp B is calculated by taking the inverse difference of the two output readings multiplied by "IB CAP"/"IB delta t". The result is then stored in "-IB B" GV. I_{OSB} is calculated and stored in "IOS B". The integration status flag "IB Vout flag" is utilized to monitor the output of op amp B with the Test program VI. The "IB status" GV serves to stop monitoring the output in the Test program VI.

4.3.6 Summing junction configuration set up Test Seq subVI CD 02 00

The Test Seq subVI CD 02 00 shown in Figure 4.16 closes REL1CH12, opens REL1CH14, REL1CH5 and REL1CH15, closes REL1CH6, opens REL1CH9, closes REL2CH0, REL2CH6 and REL2CH7, opens REL2CH3 and closes REL1CH0 and REL1CH10 in order to have the Summing junction configuration.

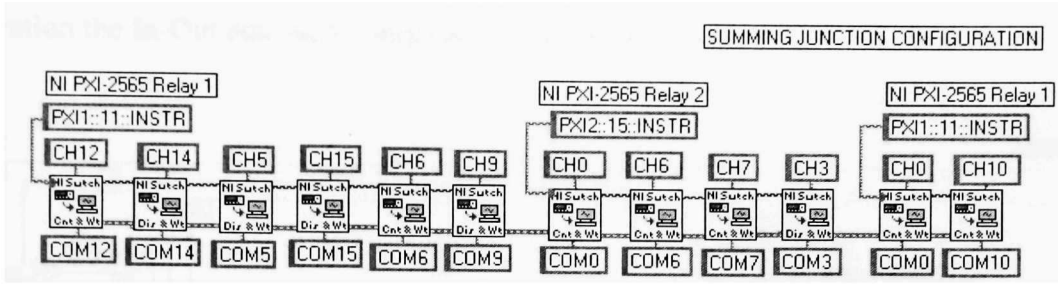

Figure 4.16 Summing junction configuration set up Test Seq subVI CD 02 00

4.3.7 Vin vector Test Seq subVI CD 03 0x

The Test Seq subVI CD 03 0x shown in Figure 4.17 generates the Vin vector used to have initial input voltages when measuring the parameters with the Summing junction configuration.

The two iterations of the first For loop are used to determine whether op amp A or B is being tested by selecting the output MUXCH6 or MUXCH7 to be measured and the input VH0 or VHC1 to be applied with the In-Out equ subVI and the sequence the "Cycle flags" binary vector GV values are stored.

The eight iterations of the second For loop are used to select the power supplies level, store in "Vin vector" GV the calculated input voltages required to set the output of the op amp A and B at a specific voltage level, change the desired output for the A_{OL} inputs calculation when iterations 6 and 7 are present, and sequence the "Cycle flags" binary vector GV values storage.

For every iteration of the second For loop, the inputs and power supplies of the op amp A and B are set to zero. Then the power supplies are set based on the values selected per iteration from the global variables "+VSs" and "-VSs". The middle point of the

supplies and $V_S/2$-0.25 are input to the In-Out equ subVI. The In-Out equ subVI outputs the in-out equation values: slope, input ("X1" GV) and output ("Y1" GV). The Case structure passes the desired output in order to calculate its corresponding input based on the in-out equation values. This desired output is always at the middle point of the supplies except for iterations 6 and 7; corresponding to the open loop gain (A_{OL}) calculation. The "Cycle flags" binary vector GV stores flags to indicate for which iteration the In-Out equ subVI surpassed 15 iterations.

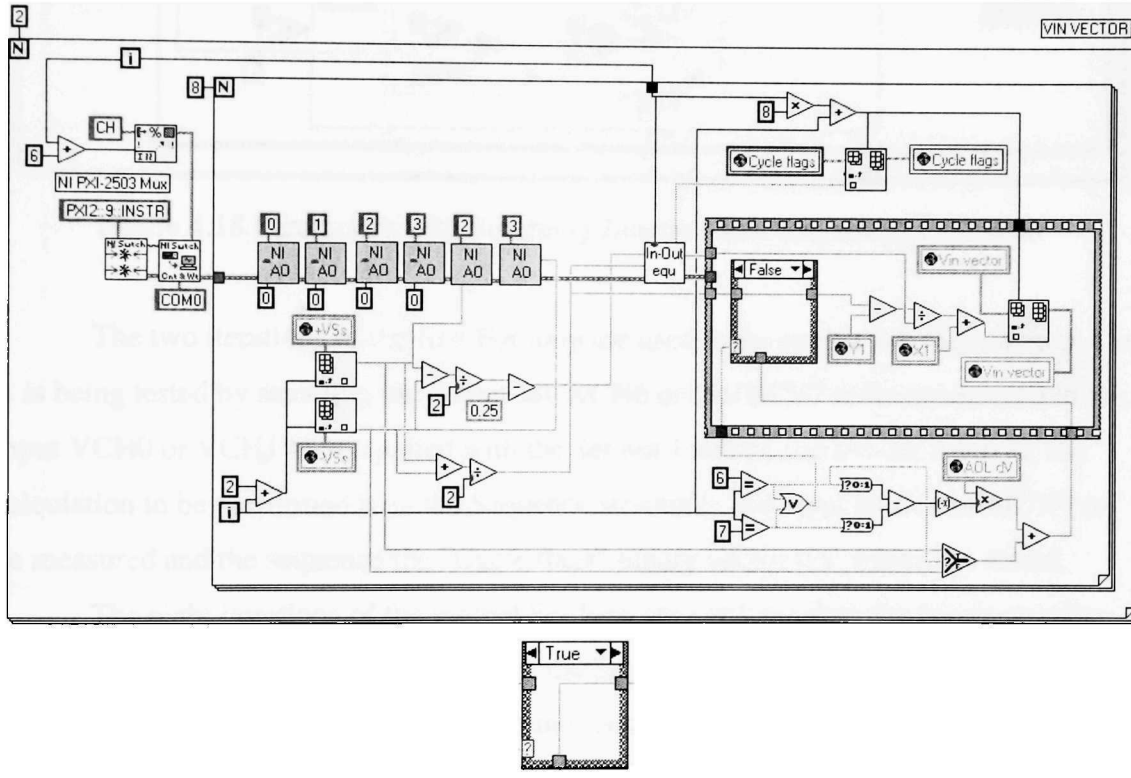

Figure 4.17 Vin vector Test Seq subVI CD 04 00 and CD 03 01

4.3.8 Parameters with Summing Junction Test Seq subVI CD 04 0x

The Test Seq subVI CD 04 0x shown in Figure 4.18 and Figure 4.19 calculates the parameters related to the Summing junction configuration.

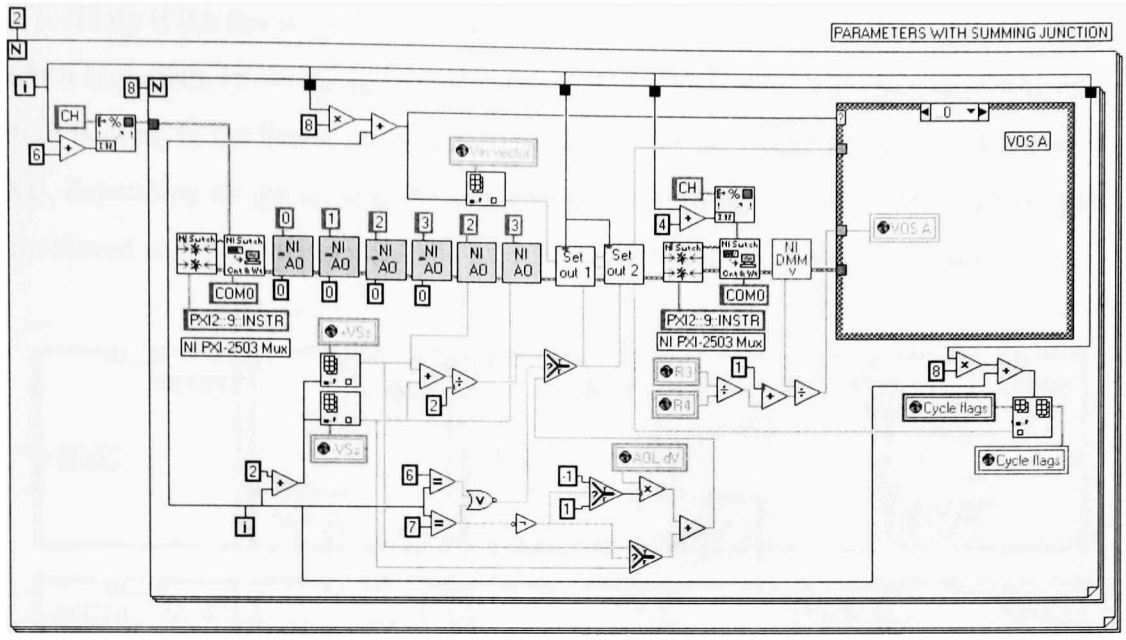

Figure 4.18 Parameters with Summing Junction Test Seq subVI CD 04 00

The two iterations of the first For loop are used to determine whether op amp A or B is being tested by selecting the output MUXCH6 or MUXCH7 to be measured and the input VCH0 or VCH1 to be applied with the Set out 1 subVI and Set out 2 subVI, the calculation to be performed with the Sequence structure, the input MUX4 or MUX5 to be measured and the sequence the "Cycle flags" binary vector GV values are stored.

The eight iterations of the second For loop are used to select the power supplies level, the calculation to be performed with the Sequence structure and the input voltage from the "Vin vector" GV, change the desired output for the A_{OL} calculation when iterations 6 and 7 are present and sequence the "Cycle flags" binary vector GV values storage.

For every iteration of the second For loop, the inputs and power supplies of the op amp A and B are set to zero. Then the power supplies are set based on the values selected per iteration from the global variables "+VSs" and "-VSs". The middle point of the supplies is always input to the Set out 1 and Set out 2 subVIs except for iterations 6 and 7; corresponding to the open loop gain (A_{OL}) calculation.

Only if the Set out 1 subVI cannot put the op amp's output to the desired voltage when it surpasses 15 iterations, the Set out 2 subVI is executed. The measured desired output is input to the Sequence structure. Once the desired output is reached, VXA or VXB, depending on the op amp being tested with MUXCH4 or MUXCH5 respectively, is measured and the voltage between the two inputs of the op amp is calculated.

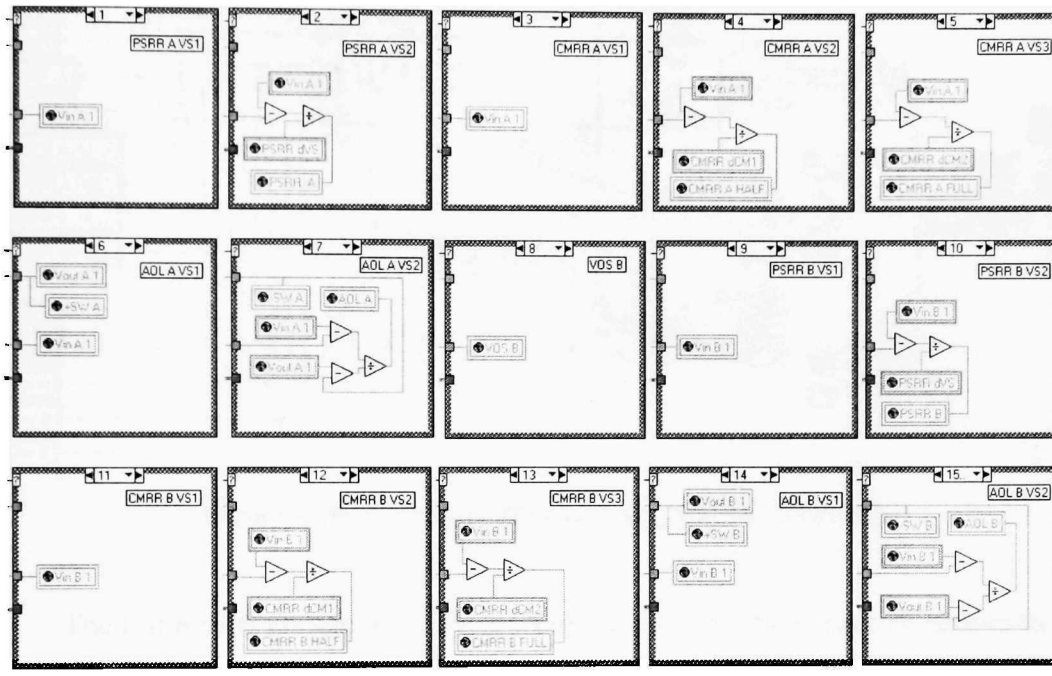

Figure 4.19 Parameters with Summing Junction Test Seq subVI CD 04 01 to CD 04 15

Calculations for every parameter are performed and stored in GVs as shown in Figure 4.19. The "Cycle flags" binary vector GV stores flags to indicate for which iteration the Set out 1 or Set out 2 subVIs surpassed 15 iterations.

4.3.9 Writing results Test Seq subVI CD 05 00

The Test Seq subVI CD 05 00 shown in Figure 4.20 writes to a *.csv file the DUT number, test temperature, pass/fail test label and results of all the calculated DC parameters. The results and pass/fail indicator per parameter is displayed in the front panel of the Test program.

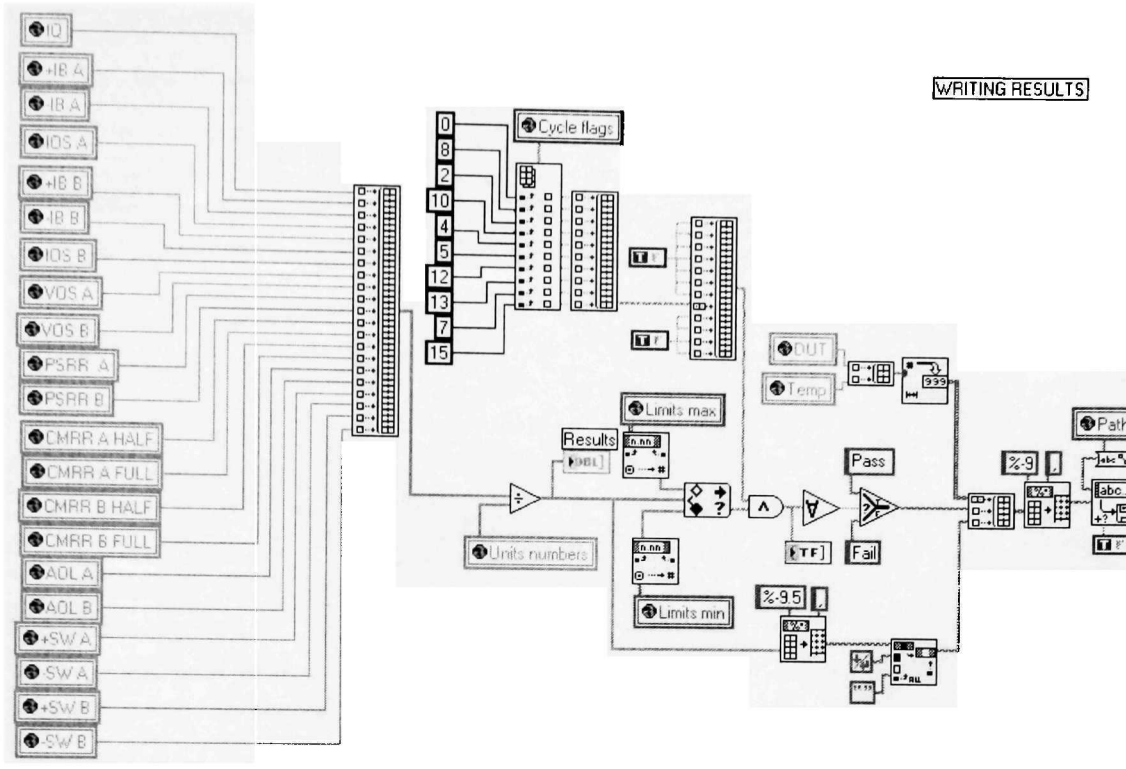

Figure 4.20 Writing results Test Seq subVI CD 05 00

The test results are grouped into a vector, divided by their units, compared to "Limits max" and "Limits min" GVs to obtain the pass/fail test label, grouped again with the DUT number ("DUT" GV) and the test temperature ("Temp" GV) and then written to a *.csv file specified by the "Path" GV. The "Cycle flags" binary vector GV is reorganized to match the test results order in order to indicate in the control panel of the Test program which parameter passed or failed.

4.4 Test Program VI

The Test Program VI performs the verification routine, initializes the global variables required for the entire test, writes to a *.csv file the labels of the DC test results and controls the Test Seq subVI. This VI provides the main user interface. Refer to Figure 4.21 and Figure 4.22 for the control panels (CP) of the Test program and the Verification routine.

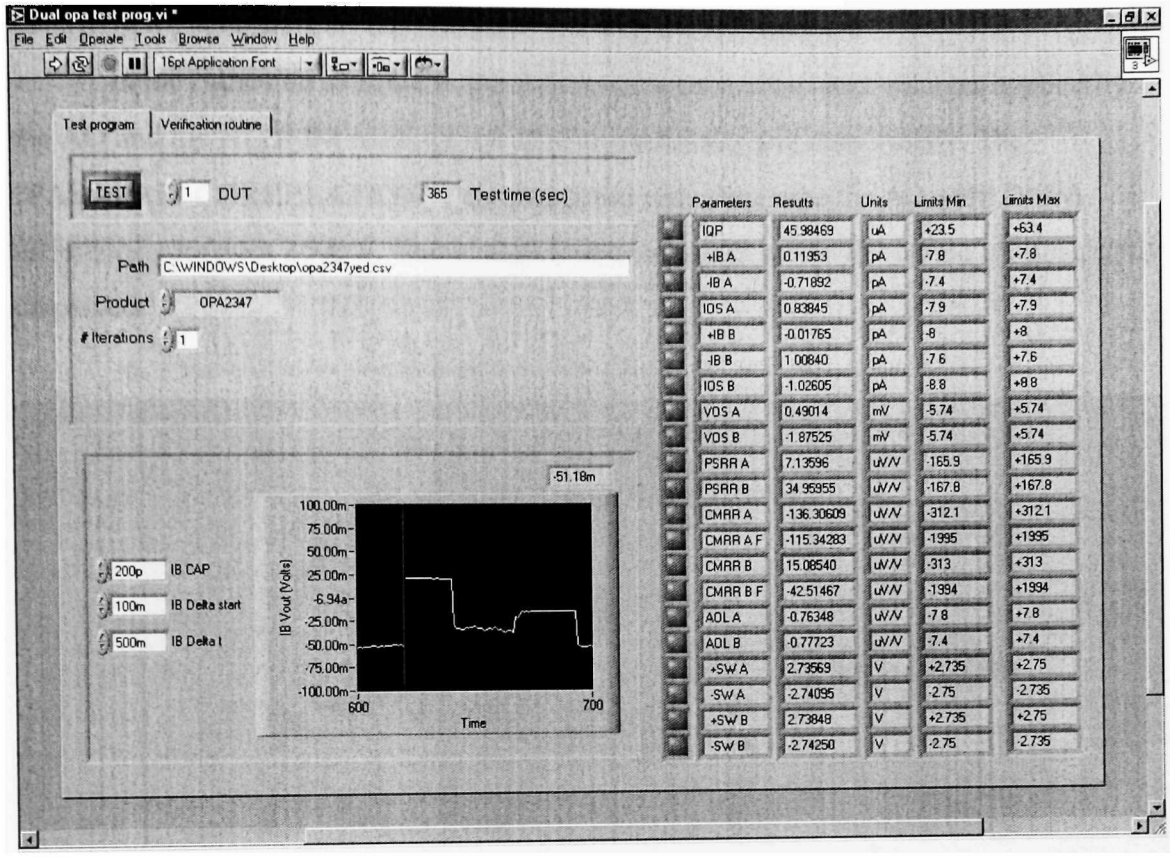

Figure 4.21 Test Program CP 00 00

The Test Program CP 00 00 shown in Figure 4.21 serves to input the "DUT" number, the "Path" and name of the *.csv file, the "Product" to be tested, the number of times "#Iterations" to test the DUT and the parameters used to perform the bias current measurement: "IB CAP", "IB Delta start" and "IB Delta t". This CP also displays the "Test time (sec)", the output voltage of the op amp being tested when the bias current measurement is performed, the test pass/fail flags per parameter, the name of the parameters, the test results and the test limits.

The Test Program CP 00 01 shown in Figure 4.22 displays the results of the Verification routine.

In the left side of this CP, the difference between the NI DMM and the HP DMM readings are shown graphically and numerically. The "PASS/FAIL CORRELATION"

flag changes to red every time the NI DMM HP DMM difference surpasses 350μV. The voltage being measured by the NI DMM is numerically displayed.

In the right side of this CP, the difference between the ideal voltages applied by the AO and the NI DMM readings are shown graphically and numerically. The "PASS/FAIL CORRELATION" flag changes to red every time the AO - HP DMM difference surpasses 350μV. The voltage being measured by the HP DMM is numerically displayed.

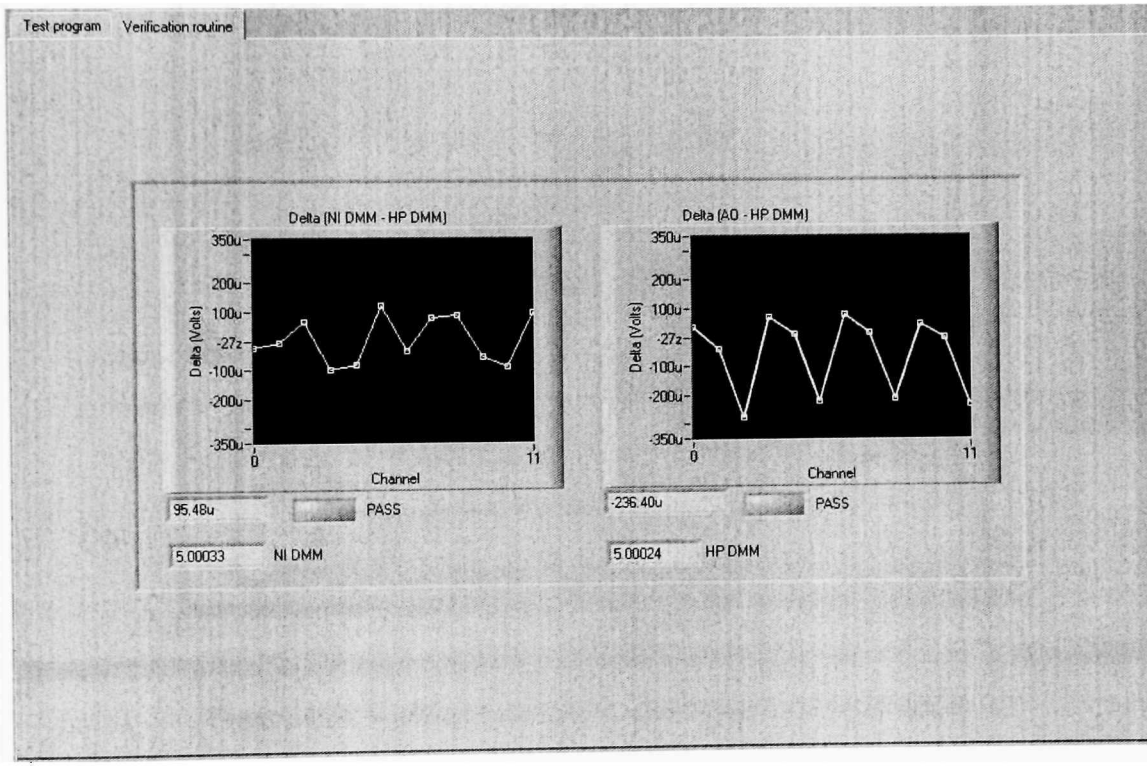

Figure 4.22 Test Program CP 00 01

Before this VI is running the Verification routine tab has to be hit in order for the Verification routine to be executed. Otherwise the Test program starts and once it happens the only variables that can be changed are: "DUT" number, "Path" and "#Iterations".

4.4.1 Verification routine Test Program VI CD 00 00

The Test Program VI CD 00 00 shown in Figure 4.23 performs the verification routine only if "Tab" selects the "Verification routine" state of the case structure. The other sate is empty.

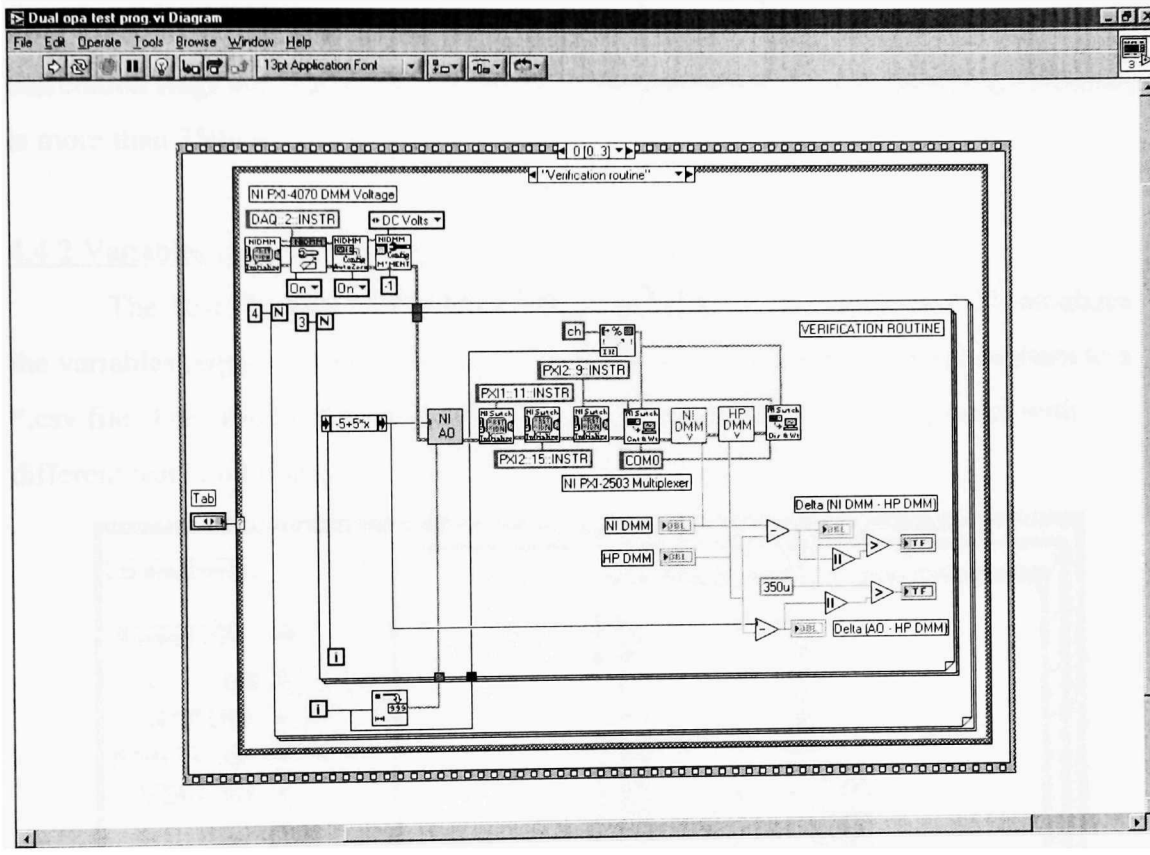

Figure 4.23 Verification routine Test Program VI CD 00 00

The NI DMM is configured to measure in autorange. The four iterations of the first For loop are used to select the places (VCH0, VCH1, VCH2 and VCH3) where the voltages are applied with the NI AO subVI and measured (MUX0, MUX3, MUX6 and MUX7) with the NI DMM and the HP DMM. The three iterations of the second For loop are used to set three voltages (-5, 0 and 5) with the NI AO subVI per every iteration of the first For loop.

For every iteration of the second For loop the NI AO subVI applies a voltage , all relays are open, the MUX is selected, readings from the NI DMM V subVI and the HP DMM V subVI are taken and displayed in the control panel, the difference between the NI DMM V subVI reading and the HP DMM V subVI reading is displayed in the left side of the control panel, the difference between the voltage applied and the HP DMM V subVI reading is displayed in the right side of the control panel, and the pass/fail correlation flags are changed to red in the control panel if their corresponding difference is more than 350μV.

4.4.2 Variables initialization Test Program VI CD 01 0x

The Test Program VI CD 01 0x shown in Figure 4.24 and Figure 4.25 initializes the variables required to perform the test and identify with labels the results written to a *.csv file. The "Product" control allows initializing variables for dual op amps with different test conditions.

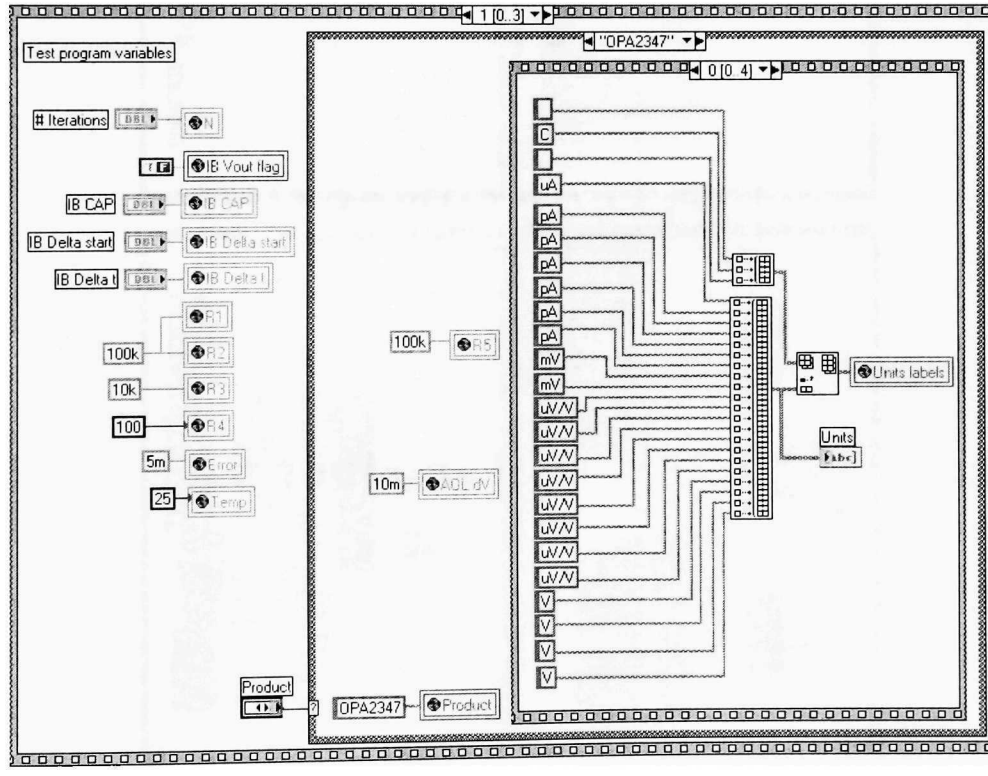

Figure 4.24 Variables initialization Test Program VI CD 01 00

The Test Program VI CD 01 00 shown in Figure 4.24 initializes the "#Iterations" GV used to test the DUT N times in the Test Seq subVI, the GVs required for the input bias current measurement, the resistor values of the Summing junction configuration, the "Error" GV utilized to guard band the desired output, the test temperature "Temp" GV, the "AOL dV" GV used to set the output with respect to the supplies when measuring A_{OL}, the product identifier "Product" GV and the results units labels "Units labels" GV vector.

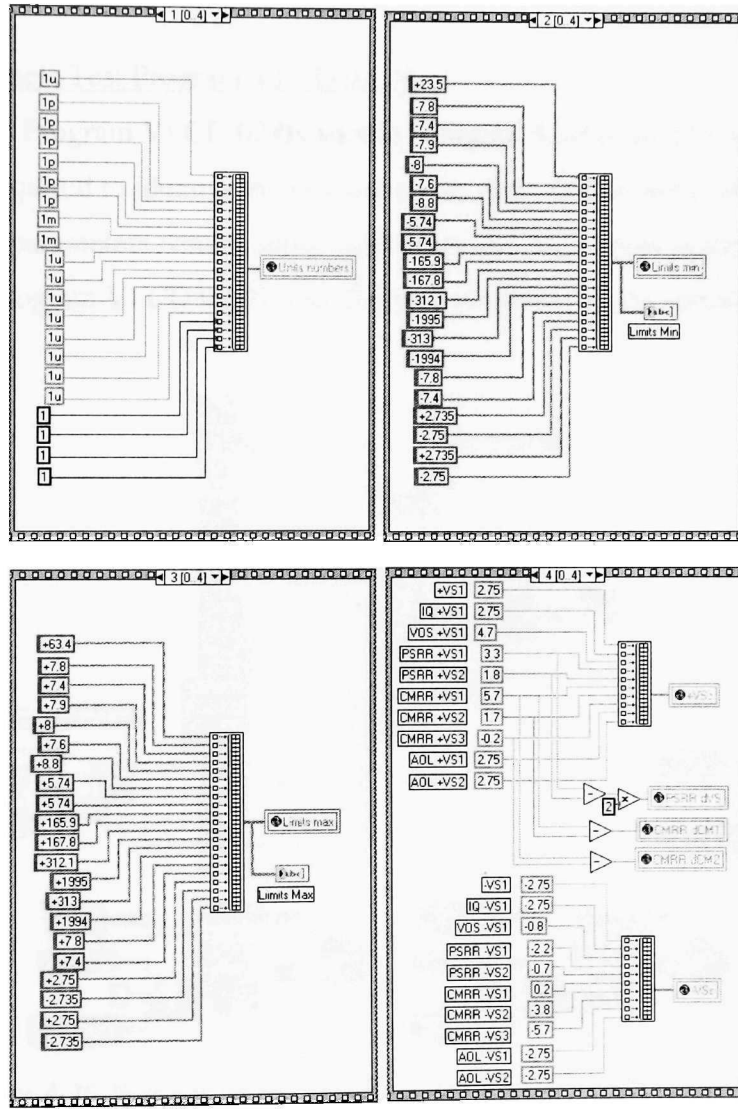

Figure 4.25 Variables initialization Test Program VI CD 01 01 to CD 01 04

The Test Program VI CD 01 01 to CD 01 04 shown in Figure 4.25 initializes the results units "Units numbers" GV vector used to present the results in terms of their units, the minimum "Limits min" GV vector and maximum "Limits max" GV vector limits used to know if the DUT passed or failed, the power supplies levels per test "+VSs" GV vector and "-VSs" GV vector, the power supplies change "PSRR dVS" needed for the PSRR measurement, the common mode voltage change "CMRR dCM1" used for the CMRR half scale measurement and the common mode voltage change "CMRR dCM2" used for the CMRR full scale measurement

4.4.3 Writing labels Test Program VI CD 02 0x

The Test Program VI CD 02 0x shown in Figure 4.26 is used to write to a *.csv file the labels required to identify the product name, date, serialization, temperature, pass/fail status, parameters results, units, limits min and limits max of the devices under test. The Test Program VI CD 02 01 also displays in the CP the parameters labels.

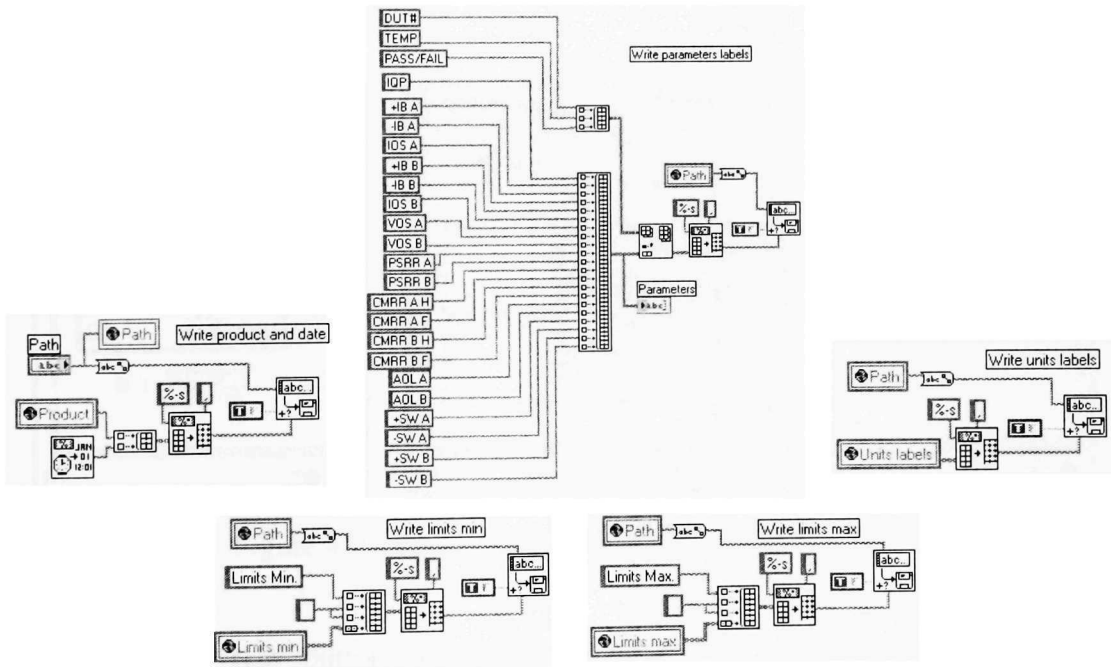

Figure 4.26 Writing labels Test Program VI CD 02 00 to CD 02 04

Every diagram shown in Figure 4.26 indicates one row to be written in the *.csv file. The order in which these rows are written is shown below.

- "Product" GV and date
- "DUT#", "TEMP", "PASS/FAIL" and parameters labels
- "Units labels" GV
- "Limits min" GV
- "Limits max" GV

4.4.4 Test Program VI CD 03 0x

The Test Program VI CD 03 0x shown in Figure 4.27 controls the Test Seq subVI.

In the first Sequence structure the "IB status" flag is set to "true" and the "Test status" flag is set to "false" to indicate in the CP with a green color around the "Test" button control that the DC test can be started. Before hitting the "Test" button control the user can change the "DUT" number in the CP.

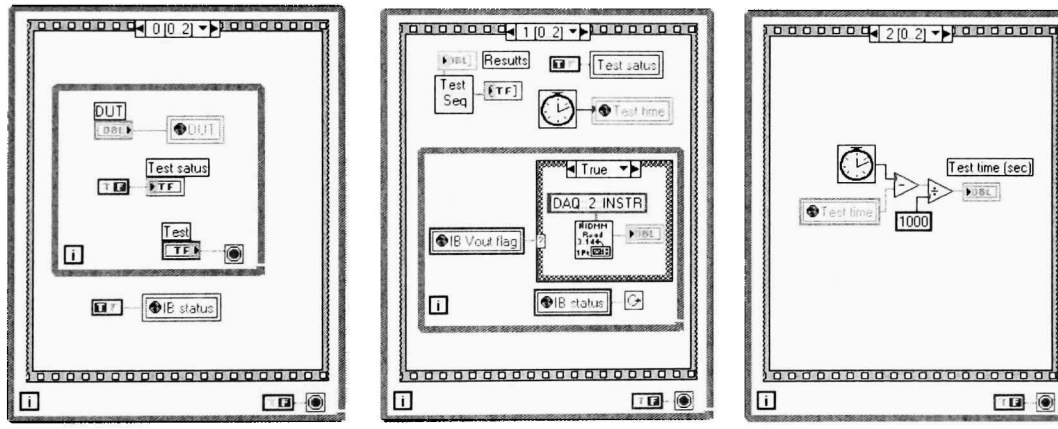

Figure 4.27 Test Program VI CD 03 00 to CD 03 02

Once the "Test" button control is hit the second Sequence structure starts initializing the "Test status" GV to "true" to indicate in the CP with a red color around the "Test" button control that the DC test is running. The "Test time" GV stores the

current counter. The Test Seq subVI starts and the output of the op amp in use is displayed in the CP when the "IB Vout flag" G V changes to "true" during the I_B measurement. After completion of the Test Seq subVI the test results and the pass/fail flags per test are displayed in the CP.

In the third Sequence structure the test time is shown in the CP based on the difference of the current and previous counter values.

The Sequence structure will be running until the stop button in the main menu of the control panel is hit.

CHAPTER 5
DATA ANALYSIS FOR REPEATABILITY AND CORRELATION

Once a test system is working, a statistical data analysis of the test results is required to determine its performance. Measuring the same guardbanded value for a specific parameter every time the DUT is tested does not mean the reading is accurate but repeatable for the test system being used. The measurements may vary from system to system and the task of a test engineer is to determine which system is right by doing readings by hand [2].

In this chapter, an Automated Test Equipment (ATE) system already approved is used to compare the results of the Automated Bench Test Equipment (ABE). Repeatability and accuracy depend on the test instruments characteristics, the expected measurement, maximum (upper test limit UTL) and minimum (lower test limit) test limits, noise and the test circuit design.

The minimum number of samples required to have a normal distribution is 30. The results taken from one device tested 35 times serve to obtain the repeatability of each system. Thirty five devices tested on both systems are used for correlation analysis.

The per-parameter repeatability criterion shown below assures that a device can be tested repeatedly in the ABE without surpassing the test limits.

- $\mu_{ABE} + 3\sigma_{ABE} + 6\sigma_{ABE\_R} < UTL$
- $\mu_{ABE} - 3\sigma_{ABE} - 6\sigma_{ABE\_R} > LTL$

where

μ_{ABE} is the mean of the 35 devices tested at the ABE

σ_{ABE} is the standard deviation of the 35 devices tested at the ABE

σ_{ABE_R} is the standard deviation of the same device tested 35 times at the ABE.

The ABE is considered repeatable for a specific parameter if meeting at least the last two repeatability conditions shown below.

- $\sigma_{ABE\_R} \leq \sigma_{ATE\_R}$
- $6\sigma_{ABE\_R} < 3\%$ of (UTL-LTL)

- $\mu_{ABE} + 3\sigma_{ABE} + 6\sigma_{ABE\_R} < UTL$
- $\mu_{ABE}\ \ 3\sigma_{ABE} - 6\sigma_{ABE\_R} > LTL.$

If the second repeatability condition is met, the parameter can be used to determine if the system's repeatability has changed every time a test is perform.

The per-parameter correlation criterion shown below assures that the same device can be tested at the ATE and the ABE without surpassing the test limits.

- $\mu_{ABE} + 3\sigma_{ABE} + |\mu_C| + 3\sigma_C < UTL$
- $\mu_{ABE} - 3\sigma_{ABE}\ \ |\mu_C| - 3\sigma_C > LTL$

where

μ_C is the mean of the ATE and ABE delta results of the 35 devices

σ_C is the standard deviation of the ATE and ABE delta results of the 35 devices.

The ABE correlates with the ATE if the three correlation conditions shown below are met for a specific parameter.

- $|\mu_C| + 3\sigma_C < 3\%$ of (UTL-LTL)
- $\mu_{ABE} + 3\sigma_{ABE} + |\mu_C| + 3\sigma_C < UTL$
- $\mu_{ABE}\ \ 3\sigma_{ABE}\ \ |\mu_C| - 3\sigma_C > LTL$

σ_{ATE_R} is the standard deviation of the same device tested 35 times at the ATE

μ_{ABE} is the mean of the 35 devices tested at the ATE

σ_{ABE} is the standard deviation of the 35 devices tested at the ATE.

If the second repeatability condition is met, the parameter can be used to determine if the correlation between systems has changed every time a test is perform.

The highlighted cells in the repeatability and correlation results tables indicate the failures for that particular condition of the parameter.

5.1.1 I_Q data analysis

Based on the data of Table 5.1, the I_Q repeatability and correlation results are calculated and shown in Table 5.2 and

Table 5.3. This parameter is repeatable at the ABE because the last two repeatability conditions are met. Since the second repeatability condition is met this

parameter can be used to determine a change in the ABE's repeatability. All correlation conditions are met, therefore the ABE correlates with the ATE for this parameter.

Table 5.1 I_Q statistical data

	(I_Q) μA
σ_{ABE_R}	0.058
σ_{ATE_R}	0.033
μ_{ABE}	42.824
σ_{ABE}	2.638
μ_{ATE}	42.742
σ_{ATE}	2.135
μ_C	-0.082
σ_C	0.303
LTL	23.5
UTL	63.4

Table 5.2 I_Q repeatability results

Conditions	I_Q (μA)
$\sigma_{ABE\_R} \leq \sigma_{ATE\_R}$	0.058>0.033
$6\sigma_{ABE\_R}$<3% (UTL-LTL)	0.34<1.197
$\mu_{ABE}+3\sigma_{ABE}+6\sigma_{ABE\_R}$<UTL	50.174<63.4
$\mu_{ABE}-3\sigma_{ABE}-6\sigma_{ABE\_R}$>LTL	34.562>23.5
Result	pass

Table 5.3 I_Q correlation results

Conditions	I_Q (μA)
$\lvert\mu_C\rvert+3\sigma_C$<3% (UTL-LTL)	0.991<1.197
$\mu_{ABE}+3\sigma_{ABE}+\lvert\mu_C\rvert+3\sigma_C$<UTL	51.729<63.4
$\mu_{ABE}-3\sigma_{ABE}-\lvert\mu_C\rvert-3\sigma_C$>LTL	33.919>23.5
Result	pass

5.1.2 I_B data analysis

Based on the data of Table 5.4, the I_B repeatability and correlation results are calculated and shown in Table 5.5 and Table 5.6.

Since the last two repeatability conditions are met for all the I_B parameters there is confidence that a device can be tested repeatedly in the ABE without surpassing the test limits and therefore the ABE is considered repeatable for I_B.

Even though the ABE does not correlate with the ATE for this parameter, the same device can be tested at the ATE and the ABE without surpassing the test limits because the last two correlation conditions are met as shown in Table 5.6.

Table 5.4 I_B statistical data

	(I_{B+} A) pA	(I_{B-} A) pA	(I_{OS} A) pA	(I_{B+} B) pA	(I_{B+} B) pA	(I_{OS} B) pA
σ_{ABE_R}	0.29	0.77	0.93	0.55	0.52	0.78
σ_{ATE_R}	0.32	0.26	0.41	0.32	0.23	0.38
μ_{ABE}	0.17	0.38	-0.21	0.13	0.31	-0.18
σ_{ABE}	0.09	0.44	0.48	0.04	0.11	0.11
μ_{ATE}	1.62	4.58	-2.95	3.41	5.13	-1.72
σ_{ATE}	0.12	0.33	0.32	0.32	0.15	0.27
μ_C	1.45	4.19	-2.74	3.27	4.82	-1.54
σ_C	0.17	0.53	0.59	0.31	0.14	0.31
LTL	-7.8	-7.8	-7.8	-7.8	-7.8	-7.8
UTL	7.8	7.8	7.8	7.8	7.8	7.8

Table 5.5 I_B repeatability results

Conditions	(I_{B+} A) pA	(I_{B-} A) pA	(I_{OS} A) pA	(I_{B+} B) pA	(I_{B-} B) pA	(IOS B) pA
$\sigma_{ABE\_R} \leq \sigma_{ATE\_R}$	0.29<0.32	0.77>0.26	0.93>0.41	0.55>0.32	0.52>0.23	0.78>0.38
$6\sigma_{ABE\_R}$<3% (UTL-LTL)	1.74<0.23	4.6>0.23	5.61>0.23	3.29>0.23	3.13>0.23	4.68>0.23
$\mu_{ABE}+3\sigma_{ABE}+6\sigma_{ABE\_R}$<UTL	2.19<7.8	6.32<7.8	6.85<7.8	3.56<7.8	3.76<7.8	4.84<7.8
$\mu_{ABE}-3\sigma_{ABE}-6\sigma_{ABE\_R}$>LTL	-1.84>-7.8	-5.51>-7.8	-7.26>-7.8	-3.29>-7.8	-3.06>-7.8	-5.14>-7.8
Results	pass	pass	pass	pass	pass	Pass

Table 5.6 I_B correlation results

Conditions	(I_{B+} A) pA	(I_{B-} A) pA	(I_{OS} A) pA	(I_{B+} B) pA	(I_{B-} B) pA	(I_{OS} B) pA
$\lvert\mu_C\rvert+3\sigma_C$<5% UTL	1.966<0.39	5.785<0.39	4.524<0.39	4.215<0.39	5.231<0.39	2.48<0.39
$\mu_{ABE}+3\sigma_{ABE}+\lvert\mu_C\rvert+3\sigma_C$<UTL	2.417<7.8	7.49<7.8	5.778<7.8	4.485<7.8	5.864<7.8	2.645<7.8
$\mu_{ABE}-3\sigma_{ABE}-\lvert\mu_C\rvert-3\sigma_C$>LTL	-2.067>-7.8	-6.726>-7.8	-6.192>-7.8	-4.215>-7.8	-5.24>-7.8	-2.999>-7.8
Results	fail	fail	fail	fail	fail	fail

Based on the means for all the I_B parameters tested on the ATE, it is noticeable that a leakage is present in the measurement. Instead of obtaining the typical value of 0.5pA for the OPA2347 on the ATE, a mean of more than 1.5pA is being measured for all the I_B parameters. On the other hand, the ABE has a leakage only for I_{B-} A.

Under these circumstances the only way to determine if the systems are reliable enough to detect if the I_B parameters of the device surpass the test limits is by using a device with a higher value of I_B. A well-known device with a typical I_B of 10pA was used. Both systems measured the typical value with a discrepancy of 3pA.

5.1.3 SW_{OUT} from rail data analysis

Since this purpose of this test is to corroborate if the output of the op amp can swing at least 15mV from each rail, it is considered a pass/fail test and no repeatability and correlation study have to be performed.

In order to verify if the output can be in the range of ±2.735V to ±2.75V, the ATE sets the output at 2.736V with a tolerance of less than ±0.5mV and the ABE sets the output at 2.74V with a tolerance of less than ±5mV.

5.1.4 V_{OS} data analysis

Based on the data of Table 5.7 the ABE meets all the repeatability and correlation conditions for V_{OS} as shown in Table 5.8 and Table 5.9. As a result the ABE is considered repeatable and correlates with the ATE for this parameter.

Table 5.7 V_{OS} statistical data

	(V_{OS} A) mV	(V_{OS} B) mV
σ_{ABE_R}	0.007	0.004
σ_{ATE_R}	0.007	0.006
μ_{ABE}	-0.429	-0.558
σ_{ABE}	1.407	1.212
μ_{ATE}	-0.419	-0.561
σ_{ATE}	1.417	1.229
μ_C	0.010	-0.003
σ_C	0.098	0.091
LTL	-5.740	-5.740
UTL	5.740	5.740

Table 5.8 V_{OS} repeatability results

Conditions	(V_{OS} A) mV	(V_{OS} B) mV
$\sigma_{ABE\_R} \leq \sigma_{ATE\_R}$	0.007=0.007	0.004<0.006
$6\sigma_{ABE\_R} < 3\%$ (UTL-LTL)	0.042<0.344	0.024<0.344
$\mu_{ABE}+3\sigma_{ABE}+6\sigma_{ABE\_R} < UTL$	3.834<5.740	3.102<5.740
$\mu_{ABE}-3\sigma_{ABE}-6\sigma_{ABE\_R} > LTL$	-4.692>-5.740	-4.218>-5.740
Results	pass	pass

Table 5.9 V_{OS} correlation results

Conditions	(V_{OS} A) mV	(V_{OS} B) mV
$\|\mu_C\|+3\sigma_C<3\%$ (UTL-LTL)	0.304<0.344	0.276<0.344
$\mu_{ABE}+3\sigma_{ABE}+\|\mu_C\|+3\sigma_C<$UTL	4.096<5.740	3.354<5.740
$\mu_{ABE}-3\sigma_{ABE}-\|\mu_C\|-3\sigma_C>$LTL	-4.954>-5.740	-4.470>-5.740
Results	pass	pass

5.1.5 PSRR data analysis

Based on the data of Table 5.10, the ABE meets all the PSRR repeatability and correlation conditions except for the first repeatability condition as shown in Table 5.11 and Table 5.12. The ABE is considered repeatable and correlates with the ATE for PSRR.

Table 5.10 PSRR statistical data

	(PSRR A) μV/V	(PSRR B) μV/V
σ_{ABE_R}	1.6	1.5
σ_{ATE_R}	0.7	0.9
μ_{ABE}	16.3	22.1
σ_{ABE}	32.6	41.3
μ_{ATE}	17.8	22.7
σ_{ATE}	32.5	41.8
μ_C	1.5	0.6
σ_C	1.6	1.7
LTL	-165.9	-167.8
UTL	165.9	167.8

Table 5.11 PSRR repeatability results

Conditions	(PSRR A) μV/V	(PSRR B) μV/V
$\sigma_{ABE\_R}\leq\sigma_{ATE\_R}$	1.6>0.7	1.5>0.9
$6\sigma_{ABE\_R}<3\%$ (UTL-LTL)	9.8<10	8.7<10.1
$\mu_{ABE}+3\sigma_{ABE}+6\sigma_{ABE_R}<$UTL	123.7<165.9	154.6<167.8
$\mu_{ABE}-3\sigma_{ABE}-6\sigma_{ABE_R}>$LTL	-91.1>-165.9	-110.4>-167.8
Results	pass	pass

Table 5.12 PSRR correlation results

Conditions	(PSRR A) μV/V	(PSRR B) μV/V
$\|\mu_C\|+3\sigma_C<3\%$ (UTL-LTL)	6<10	6<10
$\mu_{ABE}+3\sigma_{ABE}+\|\mu_C\|+3\sigma_C<UTL$	120<166	152<168
$\mu_{ABE}-3\sigma_{ABE}-\|\mu_C\|-3\sigma_C>LTL$	-88>-168	-107>-168
Results	pass	pass

5.1.6 CMRR data analysis

Based on the data of Table 5.13 the ABE meets all the CMRR repeatability and correlation conditions except for the first repeatability condition as shown in Table 5.14 and Table 5.15. The ABE is considered repeatable and correlates with the ATE for CMRR.

Table 5.13 CMRR statistical data

	(CMRR half A) μV/V	(CMRR full A) μV/V	(CMRR half B) μV/V	(CMRR full B) μV/V
σ_{ABE_R}	1.0	0.9	1.1	0.9
σ_{ATE_R}	0.8	0.8	0.6	0.7
μ_{ABE}	21.6	-1.3	12.2	2.8
σ_{ABE}	49.6	168.3	43.1	190.4
μ_{ATE}	23.4	-5.2	12.7	1.5
σ_{ATE}	49.7	170.2	43.8	192.3
μ_C	1.9	-3.9	0.6	-1.4
σ_C	1.1	2.4	1.6	2.6
LTL	-312.1	-1995.0	-313.0	-1994.0
UTL	312.1	1995.0	313.0	1994.0

Table 5.14 CMRR repeatability results

	(CMRR half A) μV/V	(CMRR full A) μV/V	(CMRR half B) μV/V	(CMRR full B) μV/V
$\sigma_{ABE\_R}\leq\sigma_{ATE\_R}$	1.0>0.8	0.9>0.8	1.1>0.6	0.9>0.7
$6\sigma_{ABE\_R}<3\%$ (UTL-LTL)	6.1<18.7	5.3<119.7	6.5<18.8	5.5<119.6
$\mu_{ABE}+3\sigma_{ABE}+6\sigma_{ABE\_R}<UTL$	176.3<312.1	508.8<1995.0	148<313.0	579.5<1994.0
$\mu_{ABE}-3\sigma_{ABE}-6\sigma_{ABE\_R}>LTL$	-133.2>-312.1	-511.4>-1995.0	-123.7>-313.0	-573.8>-1994.0
Results	pass	pass	pass	pass

Table 5.15 CMRR correlation results

Conditions	(CMRR half A) μV/V	(CMRR full A) μV/V	(CMRR half B) μV/V	(CMRR full B) μV/V
$\|\mu_C\|+3\sigma_C<3\%$ (UTL-LTL)	5.2<18.7	11.2<119.7	5.5<18.8	9.1<119.6
$\mu_{ABE}+3\sigma_{ABE}+\|\mu_C\|+3\sigma_C<$UTL	175.5<312.1	514.7<1995.0	147.0<313.0	583.1<1994.0
$\mu_{ABE}-3\sigma_{ABE}-\|\mu_C\|-3\sigma_C>$LTL	-132.4>-312.1	-517.2>-1995.0	-122.6>-313.0	-577.4>-1994.0
Results	pass	pass	pass	pass

5.1.7 A_{OL} data analysis

Based on the data of Table 5.16, the A_{OL} repeatability and correlation results are calculated and shown in Table 5.17 and Table 5.18.

Table 5.16 A_{OL} statistical data

	(A_{OL} A) μV/V	(A_{OL} B) μV/V
σ_{ABE_R}	0.6	0.5
σ_{ATE_R}	0.5	0.5
μ_{ABE}	-0.5	-0.6
σ_{ABE}	0.7	0.6
μ_{ATE}	-0.9	-0.7
σ_{ATE}	0.6	0.6
μ_C	-0.3	0.0
σ_C	0.9	0.7
LTL	-7.8	-7.4
UTL	7.8	7.4

The ABE is considered repeatable for A_{OL} only because the last two repeatability conditions are met as shown in Table 5.17.

Table 5.17 A_{OL} repeatability results

Conditions	(A_{OL} A) μV/V	(A_{OL} B) μV/V
$\sigma_{ABE\_R}\leq\sigma_{ATE\_R}$	0.6>0.5	0.5=0.5
$6\sigma_{ABE\_R}<3\%$ (UTL-LTL)	3.6>0.5	2.7>0.5
$\mu_{ABE}+3\sigma_{ABE}+3\sigma_{ABE_R}<$UTL	5.2<7.8	4<7.8
$\mu_{ABE}-3\sigma_{ABE}-3\sigma_{ABE_R}>$LTL	-6.2>-7.8	-5.3>-7.4
Results	pass	pass

Even though the ABE does not correlate with the ATE for this parameter, the same device can be tested at the ATE and the ABE without surpassing the test limits because the last two correlation conditions are met as shown in Table 5.18.

Table 5.18 A_{OL} correlation results

Conditions	(A_{OL} A) μV/V	(A_{OL} B) μV/V
$\lvert\mu_C\rvert+3\sigma_C<3\%$ (UTL-LTL)	3.1>0.5	2.3>0.4
$\mu_{ABE}+3\sigma_{ABE}+\lvert\mu_C\rvert+3\sigma_C<$UTL	4.7<7.8	3.6<7.4
$\mu_{ABE}-3\sigma_{ABE}-\lvert\mu_C\rvert-3\sigma_C>$LTL	-5.7>-7.8	-4.8>-7.4
Results		

5.1.8 Test time

Test time is the main difference between the two systems because the test circuit is not the same for both. The ATE circuit design sets the output of the op amp at once with an input voltage while the bench solution circuit configuration sets the output by adjusting an input voltage based on the output feedback. The ATE can test either a good or bad device in two seconds. In contrast, the bench solution spends 11 seconds if the part is good and 50 seconds in the worst case of having the socket empty. Although it is a disadvantage to spend more time testing, it is a big advantage to have two different test circuit configurations in order to provide correlation.

CHAPTER 6
CONCLUSIONS

Wafer level CSP is a potential packaging technology that demands an extra effort due to the recent development. The problem starts when handling this package of 1 by 2 mm with a vacuum tip and orienting it to be tested. A wrong movement can make the device jump and be lost. Determining if either the device or the board assembly is the cause of the failure adds difficultness to the qualification process.

Understanding the electrical and mechanical properties of the OPA2347YED, the test conditions and the test circuit in detail are necessary in order to build an efficient test system. The most difficult test of this thesis is the input bias current since it is sensible to any movement close to the device. A parasitic capacitance was found from the negative input of the device to ground. This capacitance introduced by the multiplexer was producing a leakage of 5pA. A relay had to be placed between the multiplexer and the negative input to avoid the leakage. The sequence in which the power supplies and relays are changed from test to test had to be analyzed to prevent damage to the DUT with an over voltage situation.

The voltage range (10±V) and the maximum current (20mA) delivered by the PXI analog output are the most critical limitations of the test hardware when trying to test a dual op amp with higher I_Q current.

Changing the standard way of programming with LabView drives to a change in reasoning the algorithms. There is a text-to-icons programming translation process before becoming familiar with the mechanics of this software. Calculating the input vector before starting to test the parameters with the summing junction configuration was essential to increase considerably the test time of the program. Configuring the NI DMM with autorange instead of with a fix range makes the program five times faster.

A further improvement to this automated bench solution can be the test at temperature software implementation with the use of two extra PXI multiplexer modules,

a pin-to-pin 12 DUT high temperature board, a software-controlled oven and the corresponding hardware interconnection.

Given the statistical results of Chapter 5, the ABE is repeatable according to the repeatability conditions and correlates for the majority of the parameters with the ATE based on the correlation conditions. As a result the ABE can be used in conjunction with the ATE to qualify the OPA2347YED.

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