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MC68330

Addendum to

MC68330 Integrated CPU32 Processor User's Manual

26 January 1996

This addendum to the initial release of the MC68330UM/AD User's Manual provides corrections to the original text, plus additional information not included in the original. This document and other information on this product is maintained on the AESOP BBS, which can be reached at (800) 843-3451 (from the U.S. and Canada) or (512) 891-3650. Configure modem for up to 14.4Kbaud, 8 bits, 1 stop bit, and no parity. Terminal software should support VT100 emulation. Internet access is provided by telneting to pirs.aus.sps.mot.com [129.38.233.1] or through the World Wide Web at http://pirs.aus.sps.mot.com.

1. OPERAND ALIGNMENT

On page 3-7, third paragraph (under 3.2.2), change the first two lines to: "The CPU32 restricts all operands (both data and instructions) to be word-aligned. That is, word and long-word operands must be located on a word boundary." Longword operands do not have to be longword aligned.

2. TYPO IN FAST TERMINATION TIMING DIAGRAM

On page 3-16: UWE and LWE in Figure 3-6 do not assert during a fast termination write. The signals should remain high.

3. ADDITIONAL NOTE ON MBAR DECODE

Add to the CPU Space Cycles description on page 3-22: The CPU space decode logic allocates the 256-byte block from $3FF00-3FFFF to the SIM module. An internal two-clock termination is provided by this initial decode for any access to this range, but selection of specific registers depends on additional decode.

Accesses to the MBAR register at longword $3FF00 are internal only, and are only visible by enabling show cycles. Users should directly access only the MBAR register and use the LPSTOP instruction to generate the LPSTOP broadcast access to $3FFFE. The remaining address range $3FF04-3FFFD is Motorola reserved and should not be accessed.

4. ADDITIONAL NOTES ON CPU SPACE ADDRESS ENCODING

On page 3-22, Figure 3-10, the BKPT field for the Breakpoint Acknowledge address encoding is on bits 4-2, and the T bit is on bit 1. The Interrupt Acknowledge LEVEL field is on bits 3-1.

5. BREAKPOINTS

On page 3-21, the first paragraph implies that either a software breakpoint (BKPT instruction) or hardware breakpoint can insert an instruction. As noted in the following paragraphs, only a software breakpoint can insert an instruction on the breakpoint acknowledge cycle.

6. INTERRUPT LATENCY

Add to the Interrupt Acknowledge Bus Cycles section on page 3-27: Interrupt latency from IRQx asserted to the prefetch of the first instruction in the interrupt handler is about 37 clocks + worst-case instruction length in clocks (using two-clock memory and autovector termination). From the instruction timing tables, this gives 37+71 (DIVS.L with worst-case <fea>) = 108 clocks worst-case interrupt latency time. For applications requiring shorter interrupt response time, use simpler addressing modes and/or avoid using longer instructions (specifically DIVS.L, DIVU.L, MUL.L) to reduce latency.

7. INTERRUPT HOLD TIME AND SPURIOUS INTERRUPTS

Add to the Interrupt Acknowledge Bus Cycles section on page 3-27: All interrupts (including level 7) are level sensitive and must remain asserted until the corresponding IACK cycle; otherwise, a spurious interrupt exception may result or the interrupt may be ignored entirely. This is also true for external interrupts that are autovectored using either the AVEC signal or the AVEC register, because the SIM will not respond to an interrupt arbitration cycle on the IMB if the external interrupt at that level has been removed.

8. ADDITIONAL NOTE ON INTERNAL AUTOVECTOR OPERATION

Add to the Autovector Interrupt Acknowledge Cycle section on page 3-30: If an external interrupt level is autovectored either by the AVEC register programming or the external AVEC signal, an external IACK will be started and terminated internally. The interrupting device should not respond to this IACK in any way, or the resulting operation is undefined.

9. ADDITIONAL NOTES ON RETRY TERMINATION

On page 3-34, Table 3-4: When $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are asserted together in case #5 to force a retry of the current bus cycle, relative timing of $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ must be controlled to avoid inadvertantly causing bus error termination case #3. This can be done several ways: (1) by asserting $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ either synchronously to the clock to directly controlling which edge each is recognized on, or (2) asynchronously with $\overline{\text{HALT}}$ asserted for time [spec 47A+spec 47B] ns before $\overline{\text{BERR}}$ to guarantee recognition on or before the same clock edge as $\overline{\text{BERR}}$.

10. NEGATION OF $\overline{\text{HALT}}$ AND $\overline{\text{BERR}}$ FOR RETRY SEQUENCE AND LATE RETRY SEQUENCE.

Figure 3-19 and Figure 3-20 on pages 3-37 and 3-38, respectively, should show $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ being negated one-half clock cycle earlier.

11. ACTIVE NEGATE ON BUS ARBITRATION

The 68330 actively pulls up all three-stateable bus pins other than the data bus before three-stating them during bus arbitration. This pullup function is not guaranteed to result in spec VOH levels before three-stating, but will help reduce rise time on these signals when using weak external bus pullups.

12. ADDITIONAL NOTE ON BUS ARBITRATION PRIORITY

For the bus arbitration description beginning on page 3-40: The arbitration priority between possible bus masters for this device is external request via $\overline{\text{BR}}$ (highest priority), then CPU (lowest).

13. ADDITIONAL NOTE ON BUS ARBITRATION AND OPERAND COHERENCY

For the bus arbitration description beginning on page 3-40: Each bus master maintains operand coherency when a higher priority request is recognized. For example, a CPU write of a longword operand to a byte port results in a sequence of four bus cycles to complete the operand transfer—the CPU will not release the bus until the completion of the fourth bus cycle. The RMC read/write sequences for a TAS instruction are also indivisible to guarantee data coherency. Arbitration is allowed between each operand transfer of a multi-operand operation such as a MOVEM instruction or exception stacking.

14. ADDITIONAL NOTES ON RESET INTERACTION WITH CURRENT BUS CYCLE

Add to the Reset Operation description beginning page 3-47:

Hardware resets are delayed until completion of the current operand transfer for maintaining operand coherency. The processor resets at the end of the bus cycle in which the last portion of the operand is transfered or after the bus monitor has timed out. The bus monitor operates whether or not it is enabled for the time period to which the BMT bits are set.

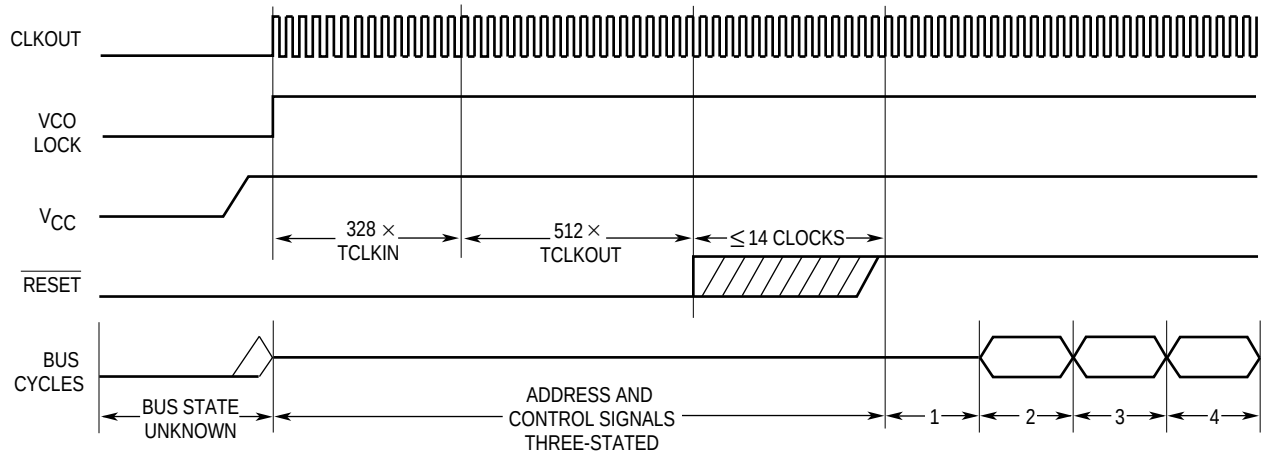
The following reset sources initialize all internal registers to their reset state: external, POR, software watchdog, double bus fault, loss of clock. Execution of a RESET instruction does not effect any of the SIM40 registers or the CPU state.

15. EXTERNAL RESET

On page 3-48, Figure 3-27, the $\overline{\text{RESET}}$ signal negates for two clocks between internal and external assertions, not one. $\overline{\text{RESET}}$ is not actively negated and its rise time depends on the pullup resistor used.

16. POWER-ON-RESET

The figure on page 3-49 is incorrectly labeled as Figure 3-27. The figure should be labeled as Figure 3-28. Also, the figure is incorrect and should be replaced with Figure 1 below.



NOTES:
1. Internal start-up time.
2. SSP read here.
3. PC read here.
4. First instruction fetched here.

Figure 1. Initial Reset Operation Timing

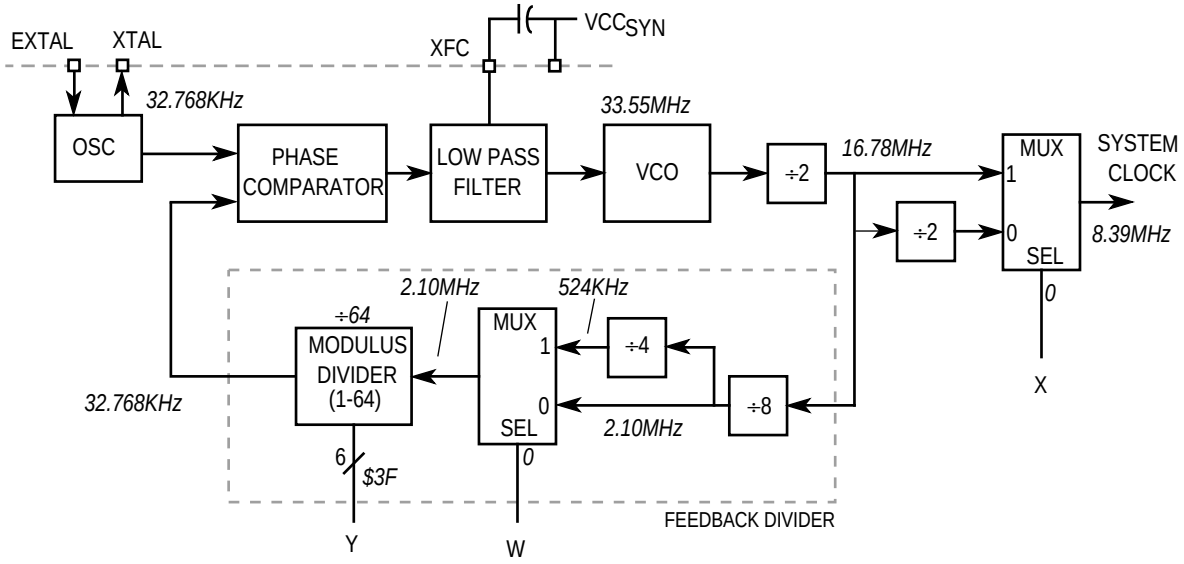
In Figure 1 above, Initial Reset Operation Timing, CLKOUT is not gated by VCO lock or other internal control signals, and can begin toggling as soon as VCC is high enough for the internal logic to begin operating. For crystal mode and external clock with VCO mode, after the VCO frequency has reached an initial stable value, the 328*TCLKIN delay is counted down, and VCO lock is set after completion of the 328 clock delay. For external clock mode without VCO, the 328*TCLKIN delay starts as soon as EXTAL clock transitions are recognized. See ‘‘Additional Notes on Power-On Reset’’ on page 9 for more POR information.

17. ADDITIONAL NOTE FOR EXTERNAL CLOCK MODE WITH PLL

On page 4-8 External Clock Mode with PLL: the PLL phase locks the CLKOUT falling edge to the falling edge of the EXTAL input clock. Maximum skew between falling edges of the EXTAL and CLKOUT signals is specified in AC ELECTRICAL SPECIFICATIONS CONTROL TIMING on page 15.

18. VCO BLOCK DIAGRAM

The clock output from the VCO block shown in Figure 4-4 on page 4-9 is actually the VCO output divided by 2. See the corrected figure below—default values for W,X, and Y SYNCR bits and resulting clock frequencies are shown in italics.



Default bit values after reset (and resulting frequencies) are shown in italics for VCO operation with a 32.768KHz crystal oscillator circuit.

Figure 2. Clock Block Diagram for Crystal Operation

19. RECOMMENDED XFC CAPACITOR VALUES

On page 4-11, second paragraph of **4.2.3.1 Phase Comparator and Filter**, and page 7-2, last paragraph: The XFC capacitor recommendation of 0.01µF to 0.1µF applies specifically to crystal mode operation. When using external clock with VCO mode, for frequencies > 1MHz start with a capacitance value of 10000pf/F_MHz. For example, at 16.0MHz the recommended XFC capacitance is approximately 10000pf/16.0 = 625pf—choose the next higher standard value available.

20. VCO FREQUENCY LIMIT

On page 4-11, last paragraph: although clearing the X bit does affect the system frequency, it has no affect on the VCO frequency because the divider that X controls lies outside the feedback loop. Changing the W or Y bits does change the VCO frequency. Users should consider the maximum VCO frequency limit when programming these bits.

21. CLKOUT AND VCO FREQUENCY PROGRAMMING

On page 4-12, Table 4-2 should be replaced by the following full table of frequencies. Although a complete table is shown for all W:X:Y combinations, users must observe both CLKOUT and VCO frequency limits when programming the SYNCR. For example, a system operating frequency (CLKOUT) of 25.16MHz can be selected with W:X:Y=1:1:23, resulting in a VCO frequency of 50.3MHz. However, programming W:X:Y=1:0:47 to achieve the same system frequency would result in a VCO frequency of >100MHz, which is outside the spec VCO frequency operating range. Programming that violates current 25MHz electrical specs is shown in italics.

Table 1. System Frequencies From 32.768-kHz Reference

Y[2]	CLKOUT (KHZ)[1]		VCO (KHZ)[1]	CLKOUT (KHZ)[1]		VCO (KHZ)[1]
	W=0[2]		W=0[2]	W=1[2]		W=1[2]
	X=0	X=1	X=X	X=0	X=1	X=X
0	131	262	524	524	1049	2097
1	262	524	1049	1049	2097	4194
2	393	786	1573	1573	3146	6291
3	524	1049	2097	2097	4194	8389
4	655	1311	2621	2621	5243	10486
5	786	1573	3146	3146	6291	12583
6	918	1835	3670	3670	7340	14680
7	1049	2097	4194	4194	8389	16777
8	1180	2359	4719	4719	9437	18874
9	1311	2621	5243	5243	10486	20972
10	1442	2884	5767	5767	11534	23069
11	1573	3146	6291	6291	12583	25166
12	1704	3408	6816	6816	13631	27263
13	1835	3670	7340	7340	14680	29360
14	1966	3932	7864	7864	15729	31457
15	2097	4194	8389	8389	16777	33554
16	2228	4456	8913	8913	17826	35652
17	2359	4719	9437	9437	18874	37749
18	2490	4981	9961	9961	19923	39846
19	2621	5243	10486	10486	20972	41943
20	2753	5505	11010	11010	22020	44040
21	2884	5767	11534	11534	23069	46137
22	3015	6029	12059	12059	24117	48234
23	3146	6291	12583	12583	25166	50332
24	3277	6554	13107	*13107*	*26214*	*52429*

Y[2]	CLKOUT (KHZ)		VCO (KHZ)	CLKOUT (KHZ)		VCO (KHZ)
	W=0		W=0	W=1		W=1
	X=0	X=1	X=X	X=0	X=1	X=X
32	4325	8651	17302	*17302*	*34603*	*69206*
33	4456	8913	17826	*17826*	*35652*	*71303*
34	4588	9175	18350	*18350*	*36700*	*73400*
35	4719	9437	18874	*18874*	*37749*	*75497*
36	4850	9699	19399	*19399*	*38797*	*77595*
37	4981	9961	19923	*19923*	*39846*	*79692*
38	5112	10224	20447	*20447*	*40894*	*81789*
39	5243	10486	20972	*20972*	*41943*	*83886*
40	5374	10748	21496	*21496*	*42992*	*85983*
41	5505	11010	22020	*22020*	*44040*	*88080*
42	5636	11272	22544	*22544*	*45089*	*90178*
43	5767	11534	23069	*23069*	*46137*	*92275*
44	5898	11796	23593	*23593*	*47186*	*94372*
45	6029	12059	24117	*24117*	*48234*	*96469*
46	6160	12321	24642	*24642*	*49283*	*98566*
47	6291	12583	25166	*25166*	*50332*	*100663*
48	6423	12845	25690	*25690*	*51380*	*102760*
49	6554	13107	26214	*26214*	*52429*	*104858*
50	6685	13369	26739	*26739*	*53477*	*106955*
51	6816	13631	27263	*27263*	*54526*	*109052*
52	6947	13894	27787	*27787*	*55575*	*111149*
53	7078	14156	28312	*28312*	*56623*	*113246*
54	7209	14418	28836	*28836*	*57672*	*115343*
55	7340	14680	29360	*29360*	*58720*	*117441*
56	7471	14942	29884	*29884*	*59769*	*119538*

Table 1. System Frequencies From 32.768-kHz Reference

Y[2]	CLKOUT (KHZ)[1]		VCO (KHZ)[1]	CLKOUT (KHZ)[1]		VCO (KHZ)[1]
	W=0[2]		W=0[2]	W=1[2]		W=1[2]
	X=0	X=1	X=X	X=0	X=1	X=X
25	3408	6816	13631	*13631*	*27263*	*54526*
26	3539	7078	14156	*14156*	*28312*	*56623*
27	3670	7340	14680	*14680*	*29360*	*58720*
28	3801	7602	15204	*15204*	*30409*	*60817*
29	3932	7864	15729	*15729*	*31457*	*62915*
30	4063	8126	16253	*16253*	*32506*	*65012*
31	4194	8389	16777	*16777*	*33554*	*67109*

Y[2]	CLKOUT (KHZ)		VCO (KHZ)	CLKOUT (KHZ)		VCO (KHZ)
	W=0		W=0	W=1		W=1
	X=0	X=1	X=X	X=0	X=1	X=X
57	7602	15204	30409	*30409*	*60817*	*121635*
58	7733	15466	30933	*30933*	*61866*	*123732*
59	7864	15729	31457	*31457*	*62915*	*125829*
60	7995	15991	31982	*31982*	*63963*	*127926*
61	8126	16253	32506	*32506*	*65012*	*130023*
62	8258	16515	33030	*33030*	*66060*	*132121*
63	8389	16777	33554	*33554*	*67109*	*134218*

1. Some W/X/Y bit combinations shown may select a CLKOUT or VCO frequency higher than spec. Refer to **Section 11 Electrical Characteristics** for CLKOUT and VCO frequency limits.
2. Any change to W or Y results in a change in the VCO frequency - the VCO should be allowed time to relock if necessary.
3. Programming which violates current 25MHz electrical specs is shown in italics (any combination of W = 1 and Y > 23.

22. ADDITIONAL NOTE FOR GLOBAL CHIP-SELECT

On page 4-13, last paragraph: When operating as a global chip-select, CS0 does not assert for accesses to either the MBAR or to internal peripheral module registers.

23. TYPO IN GLOBAL CHIP-SELECT OPERATION

On page 4-13, the last sentence of the last paragraph is incorrect. It should read " When the CPU32 begins fetching after reset, $\overline{CS0}$ is asserted for every address until the V-bit in the chip-select base address register is set."

24. ADDITIONAL NOTE ON PORT A/B OUTPUT TIMING

Add to the External Bus Interface Operation description on page 4-14: The Port A and Port B output pins transition after the S4 falling edge for the internal write to the respective data register. This places port pin transitions at roughly the same time DS negates for the data register write—note this output delay is not currently specified in the Electrical Specifications.

25. MBAR REGISTER RESET VALUES

On page 4-17, the reset values for MBAR bits 31-12 are undefined.

26. MBAR AS7 BIT AND IACK CYCLES

On page 4-18, for the second code sequence, change the "MOVE.L #$FFFFF001,D0" to "MOVE.L #$FFFFF101,D0". This sets AS7 in the MBAR to prevent the address decode for the internal 4K register block from responding to CPU space accesses. In particular, it prevents the register block decode of $FFFFFxxx from interfering with IACK cycles (address $FFFFFFFx) and possibly corrupting the vector number returned. This change does not affect normal interrupt acknowledge operation for the internal modules.

27. ADDITIONAL NOTE ON VCO OVERSHOOT

On page 4-25, place the following note under the Y-bits description:

NOTE

A VCO overshoot can occur when increasing the operating frequency by changing the Y bits in the SYNCR register. The following procedure controls the effects of this overshoot:

1. Write the X bit to zero. This will reduce the previous frequency by one half.
2. Write the Y bits to the desired frequency divided by 2.
3. After the VCO lock has occurred, write the X bit to one. This changes the clock frequency to the desired frequency.

Steps 1 and 2 may be combined.

28. BUS ERROR STACK FRAME

On page 5-82, in the next-to-last paragraph, delete "(the internal transfer count register is located at SP+$10 and the SSW is located at SP+12)". The stack space allocation is the same for both faults—the location of the internal count register and SSW remains the same. The only difference is that the faulted instruction program counter location SP+10 and SP+12 will contain invalid data. To tell the difference between the two stack frames, look at the first nibble of the faulted exception format vector word located at SP+$E—it will be $0 for the four-word frame and $2 for the six-word frame.

29. DSO TIMING

On page 5-92, Figure 5-32, DSO transitions one clock later than shown.

30. TYPO ON BDM RSREG COMMAND

On page 5-98, Section 5.7.2.8.6, RSREG register bit #8 should be a "1."

31. IPIPE TIMING

On page 5-109, Figure 5-38 shows the third IPIPE assertion low, lasting for 1.5 CLKs. It actually asserts for an additional 0.5 CLKs. IPIPE transitions occur after the falling edge of CLKOUT.

32. ADDITIONAL NOTE ON OSCILLATOR LAYOUT GUIDELINES

Add to the Processor Clock Circuitry (page 7-1) and Serial Interface (page 7-4) sections: In general, use short connections and place external oscillator components close to the processor. Do not route other signals through or near the oscillator circuit, especially high-frequency signals like CLKOUT and $\overline{AS}$. Place a ground shield around the oscillator logic; use a separate trace for ground to the oscillator so that it does not carry any digital switching noise.

33. RECOMMENDED 32KHZ OSCILLATOR CIRCUIT

On page 7-2, Figure 7-2, the component values shown in the example 32kHz oscillator circuit may not provide enough loop gain for all crystals. For a more generally robust oscillator circuit, change C1 and C2 as shown below. Users can substitute a10M resistor for the 20M R2 bias resistor as shown.

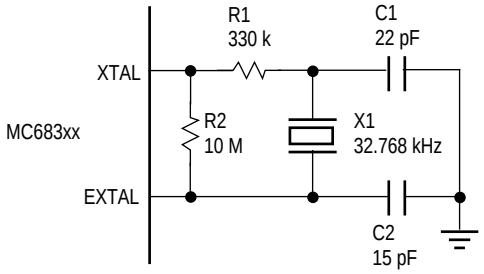


Figure 3. Sample Crystal Circuit

34. ADDITIONAL NOTES ON POWER-ON RESET

Replace **Section 7.1.2 Reset Circuitry** on page 7-3 with the following paragraphs:

The SIM module generates a power-on reset (POR) when it detects a positive going V_{CC} transition—the V_{CC} threshold is typically in the range 2.0–2.7V and varies depending on processing and environmental variables. Hysteresis is included in the reset circuit to prevent reassertion for a monotonically increasing V_{CC} voltage; however, excessively long V_{CC} rise times (>100 ms) may allow the reset logic to release RESET before V_{CC} has stabilized. Users should not rely on the reset thresholds provided in the SIM to monitor V_{CC} because internal logic may fail at voltages between spec V_{CCmin} and the reset trigger threshold. Instead, use an external low voltage monitor circuit such as the MC34064.

When the processor is used in crystal clock mode, the simplest external reset logic consists of simply a 1K pullup resistor from RESET to V_{CC}. This solution relies on a monotonically increasing V_{CC} that has a rise time on the order of 100ms or less—the actual allowable rise time depends on the startup time of the 32.768kHz oscillator circuit. As noted above, this does not provide rigorous V_{CC} monitoring and may be susceptible to sags or glitches in the V_{CC} supply voltage.

In external clock mode, either with or without the PLL, the POR time delay of 328 * T_{clkin} does not provide adequate time for V_{CC} to stabilize before allowing reset to negate. Applications using these two clocking modes should include an external reset circuit that generates an appropriate delay for the power source being used as well as a voltage monitor, if needed.

35. SRAM INTERFACE

The SRAM interface shown in Figure 7-4, page 70-3 is incorrect. The corrected drawing is shown below in Figure 4.

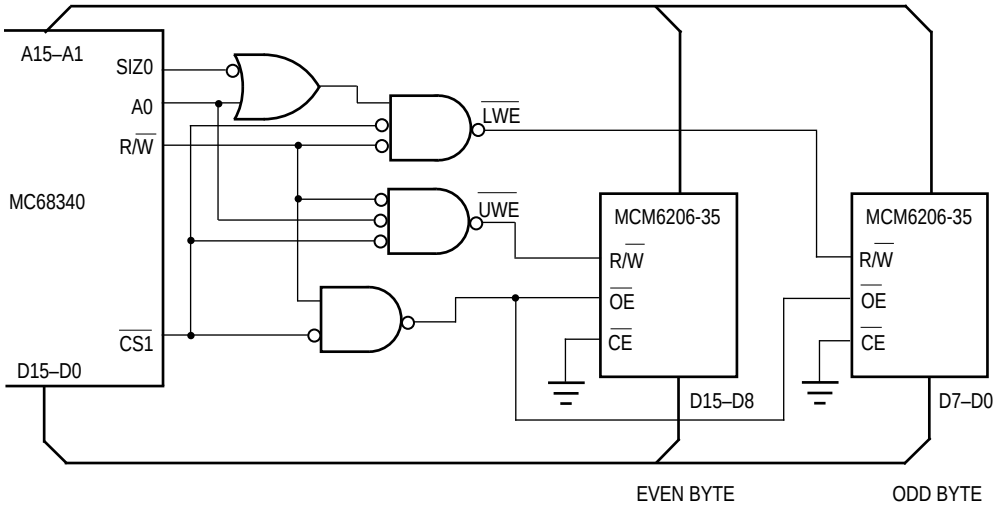


Figure 4. SRAM Interface

36. ADDITIONAL NOTES ON ROM INTERFACE

On page 7-4 Figure 7-5 EPROM interface: Connect $\overline{OE}$ to $\overline{CS0}$ and $\overline{CE}$ to ground to maximize available access time (at the expense of power consumption). Alternatively, connect $\overline{OE}$ and $\overline{CE}$ to $\overline{CS0}$ to deselect the EPROM between accesses and lower power consumption.

37. STANDARD MC68330 ORDERING INFORMATION

Update table 12.1 as shown in Table 2 below.

Table 2. Standard MC68330 Ordering Information

SUPPLY VOLTAGE	PACKAGE TYPE	FREQUENCY (MHZ)	TEMPERATURE	ORDER NUMBER
5.0 V	Plastic Quad Flat Pack FC Suffix	0 – 16 0 – 16 0 – 25	0° C to +70° C -40° C to +85° C 0° C to +70° C	MC68330FC16 MC68330CFC16 MC68330FC25
5.0 V	Thin Quad Flat Pack PV Suffix	0 – 16 0 – 16 0 – 25	0° C to 70° C -40° C to +85° C 0° C to 70° C	MC68330PV16 MC68330CPV16 MC68330PV25
3.3 V	Plastic Quad Flat Pack FC Suffix	0 – 16	0° C to +70° C	MC68330FC16V
3.3 V	Thin Quad Flat Pack PV Suffix	0 – 16	0° C to 70° C	MC68330PV16V

38. ELECTRICAL CHARACTERISTICS

Most of the electrical characteristics are not printed in the *MC68330 Integrated CPU32 Processor User's Manual*. They are reprinted here for your convenience.

39. MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	–0.3 to +7.0	V
Input Voltage	V_{in}	–0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C

The following ratings define a range of conditions in which the device will operate without being damaged. However, sections of the device may not operate normally while being exposed to the electrical extremes. This device contains circuitry to protect against damage due to high static voltages or electrical fields; however, Motorola advises users to take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

40. POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from Equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

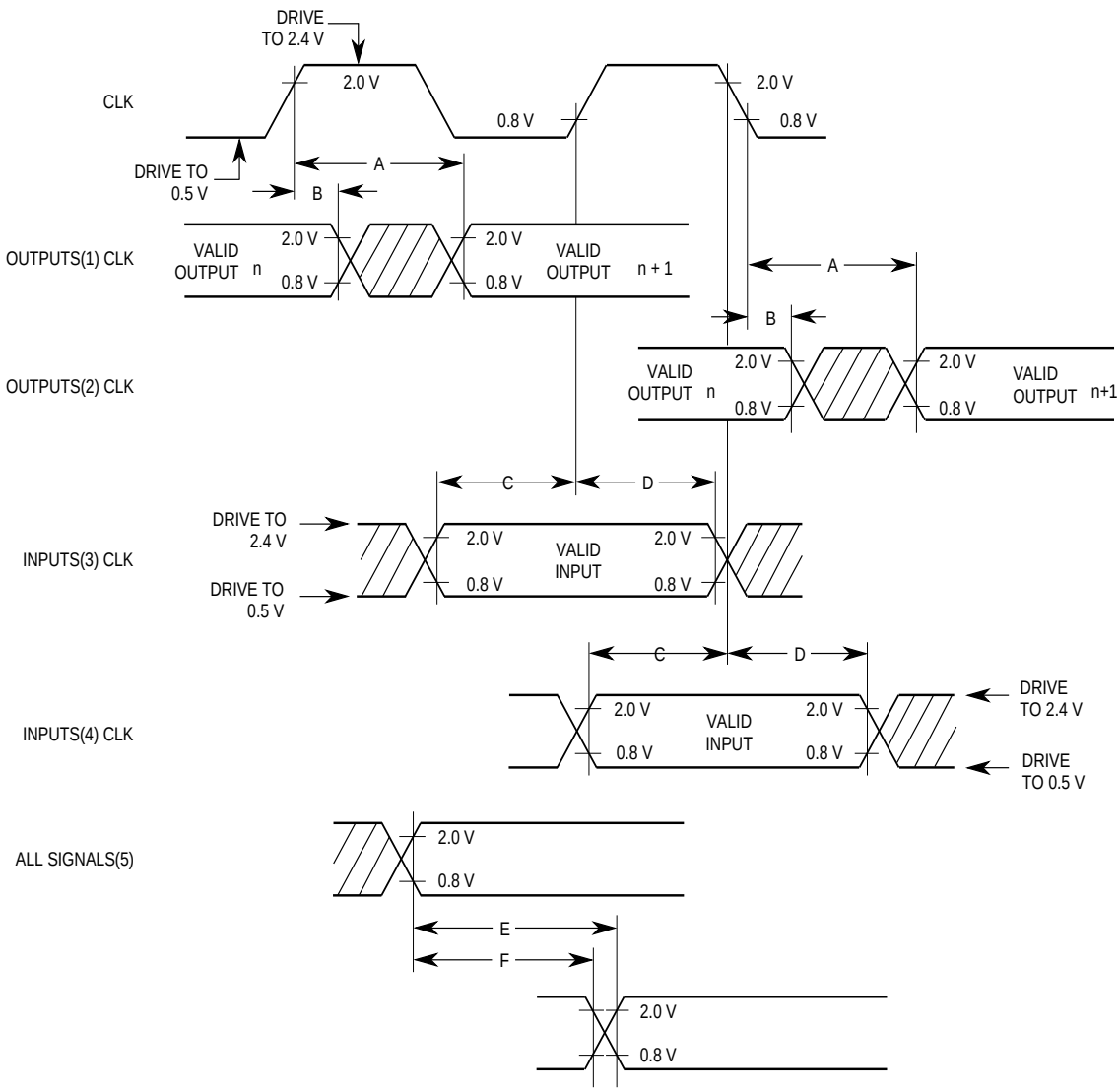
41. AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The waveforms shown in Figure 5 define the measurement of the AC specifications. To test the parameters guaranteed by Motorola, drive inputs to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times and are measured as shown. Finally, the measurement for signal-to-signal specifications is shown.

NOTE

The testing levels used to verify conformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 5. Drive Levels and Test Points for AC Specifications

42. DC ELECTRICAL SPECIFICATIONS

(See notes (a), (b), (c), and (d) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70°C; see numbered notes)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage (except clock)	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Clock Input High Voltage (EXTAL, X1)	V_{IHC}	0.7*(V_{CC})	V_{CC}+0.3	V
Undershoot	—	—	–0.8	V
Input Leakage Current (All Input Only Pins) V_{in} = V_{CC} or GND	I_{in}	–2.5	2.5	µA
Hi-Z(Off-State) Leakage Current (All Non-Crystal Outputs and I/O Pins – See Note 1) V_{in}=0.5/2.4 V	I_{OZ}	–20	20	µA
Signal Low Input Current V_{IL}=0.8 V TMS, TDI Signal High Input Current V_{IH}=2.0 V TMS, TDI	I_L I_H	–0.015 –0.015	0.2 0.2	mA mA
Output High Voltage (See Notes 1 and 2) I_{OH} = –0.8 mA, V_{CC} = 4.75 V (All Noncrystal Outputs except HALT, RESET)	V_{OH}	2.4	—	V
Output Low Voltage (See Note 1) I_{OL} = 2.0 mACLKOUT, FREEZE, IPIPE, IFETCH I_{OL} = 3.2 mAA23–A0, D15–D0, FC2–FC0, SIZ1, SIZ0 I_{OL} = 5.3 mAAll Other Output Only and Group 2 I/O Pins I_{OL} = 15.3 mAHALT, RESET	V_{OL}	—	 0.5 0.5 0.5 0.5	V
Total Supply Current at 5 V +5% @ 16.78 MHz RUN (see Note 3) STOP (VCO Off)	 I_{DD} S_{IDD}	—	 120 300	 mA µA
Power Dissipation at 5 V +5% @ 16.78 MHz	P_D	—	630	mW
Input Capacitance (See Note 1 and 4) All Input-Only Pins All I/O Pins	C_{in}	—	 10 20	pF
Load Capacitance (See Note 4)	C_L	—	100	pF

(a) The electrical specifications in this document for both the 16.78 MHz @ 3.3 V±0.3 V are preliminary and apply only to the appropriate MC68330V low voltage part.
(b) The 16.78-MHz specifications apply to the MC68330 @ 5.0 V ±5% operation.
(c) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.
(d) For extended temperature parts TA = –40 to +85∞C. These specifications are preliminary.

1. Input-Only Pins:
   BERR, BGACK, BKPT, BR, DSACK1, DSACK0, EXTAL, TCK, TDI, TMS
   Output-Only Pins:
   A23–A0, AS, BG, CLKOUT, CS3–CS1, DS, FC2–FC0, FREEZE, IFETCH, IPIPE, LWE, RMC, R/W, SIZ1, SIZ0, TDO, UWE
   Input/Output Pins:
   Group 1: D15–D0
   Group 2: A31–A24, CS0, IRQ7 – IRQ1, MODCK
   Group 3: HALT, RESET
2. VOH specification for HALT and RESET is not applicable because they are open-drain pins.
3. Supply current measured with system clock frequency of 16.78 MHz.
4. Capacitance is periodically sampled rather than 100% tested.

43. AC ELECTRICAL SPECIFICATIONS CONTROL TIMING

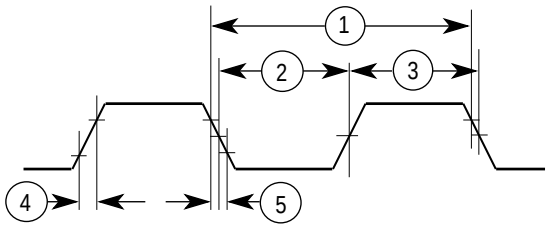
(See notes (a), (b), (c), and (d) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70∞C; see numbered notes; see Figure 6)

NUM.	CHARACTERISTIC	SYMBOL	3.3 V OR 5.0 V 16.78 MHZ MIN	3.3 V OR 5.0 V 16.78 MHZ MAX	5.0 V 25.16 MHZ MIN	5.0 V 25.16 MHZ MAX	UNIT
	System Frequency[1]	f_{sys}	dc	16.78	dc	25.16	MHz
	Crystal Frequency	f_{XTAL}	25	50	25	50	kHz
	On-Chip VCO System Frequency	f_{sys}	0.13	16.78	0.13	25.16	MHz
	On-Chip VCO Frequency Range	f_{VCO}	0.1	33.5	0.1	50.3	MHz
	External Clock Operation	f_{sys}	0	16	0	25	MHz
	PLL Start-up Time[2]	t_{rc}	—	20	—	20	ms
	Limp Mode Clock Frequency[3]	f_{limp}					kHz
	SYNCR X-bit = 0		—	$f_{sys}/2$	—	$f_{sys}/2$	
	SYNCR X-bit = 1		—	f_{sys}	—	f_{sys}	
	CLKOUT stability[4]	ΔCLK	–1	+1	–1	+1	%
1[5]	CLKOUT Period in Crystal Mode	t_{cyc}	59.6	—	40	—	ns
1B[6]	External Clock Input Period	t_{EXTcyc}	62.5	—	40	—	ns
1C[7]	External Clock Input Period with PLL	t_{EXTcyc}	62.5	—	40	—	ns
2,3[8]	CLKOUT Pulse Width in Crystal Mode	t_{CW}	28	—	19	—	ns
2B, 3B[9]	CLKOUT Pulse Width in External Mode	t_{EXTCW}	28	—	18	—	ns
2C, 3C[10]	CLKOUT Pulse Width in External w/PLL Mode	t_{EXTCW}	31	—	20	—	ns
4,5	CLKOUT Rise and Fall Times	t_{Crf}	—	5	—	4	ns

(a) The electrical specifications in this document for both the 8.39 and 16.78 MHz @ 3.3 V±0.3 V are preliminary and apply only to the appropriate MC68330V low voltage part.
(b) The 16.78-MHz specifications apply to the MC68330 @ 5.0 V ±5% operation.

(c) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.
(d) For extended temperature parts TA = –40 to +85∞C. These specifications are preliminary.

1. All internal registers retain data at 0 Hz.
2. Assumes that a stable V_{CCSYN} is applied, that an external filter capacitor with a value of 0.1 µF is attached to the XFC pin, and that the crystal oscillator is stable. Lock time is measured from power-up to RESET release. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
3. Determined by the initial control voltage applied to the on-chip VCO. The X-bit in the SYNCR controls a divide-by-two scaler on the system clock output.
4. CLKOUT stability is the average deviation from programmed frequency measured at maximum f_{sys}. Measurement is made with a stable external clock input applied using the PLL.
5. All crystal mode clock specifications are based on using a 32.768-kHz crystal for the input.
6. When using the external clock input mode (MODCK reset value = 0 V), the minimum allowable t_{EXTcyc} period will be reduced when the duty cycle of the signal applied to EXTAL exceeds 5% tolerance. The relationship between external clock input duty cycle and minimum t_{EXTcyc} is expressed:
   Minimum t_{EXTcyc} period = minimum t_{EXTCW} / (50% – external clock input duty cycle tolerance).
   Minimum external clock low and high times are based on a 45% duty cycle.
7. When using the external clock input mode with the PLL (MODCK reset value = 0 V), the external clock input duty cycle can be at minimum 20% to produce a CLKOUT with a 50% duty cycle.
8. For crystal mode operation, the minimum CLKOUT pulse width is based on a 47% duty cycle.
9. For external clock mode operation, the minimum CLKOUT pulse width is based on a 45% duty cycle, with a 50% duty cycle input clock.
10. For external clock w/PLL mode operation, the minimum CLKOUT pulse width is based on a 50% duty cycle.
11. For external clock mode, there is a 10–40 ns skew between the input clock signal and the output CLKOUT signal from the MC68330. Clock skew is measured from the rising edges of the clock signals.
12. For external clock mode w/PLL, there is a 5 ns skew between the input clock signal and the output CLKOUT signal from the MC68330. Clock skew is measured from the rising edges of the clock signals.



NOTES: 1. All timing except two and three is measured with respect to 0.8 V and 2.0 V.
2. Two and three are measured from 1.5 V to 1.5 V.

Figure 6. Clock Output Timing Diagram

44. AC TIMING SPECIFICATIONS

(See notes (a), (b), (c), and (d) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70∞C; see numbered notes; see Figure 7–Figure 16)

NUM	CHARACTERISTIC	SYMBOL	3.3 V OR 5.0 V 16.78 MHZ MIN	3.3 V OR 5.0 V 16.78 MHZ MAX	5.0 V 25.16 MHZ MIN	5.0 V 25.16 MHZ MAX	UNIT
6	CLKOUT High to Address, FC, SIZ, Valid	t_{CHAV}	0	30	0	20	ns
6A	CLKOUT High to $\overline{RMC}$ Valid	t_{CHAVB}	0	35	0	25	ns
7	CLKOUT High to Address, Data, FC, SIZ, RMC High Impedance	t_{CHAZx}	0	60	0	40	ns
8	CLKOUT High to Address, FC, SIZ, RMC Invalid	t_{CHAZn}	0	—	0	—	ns
9[9]	CLKOUT Low to AS, DS, CS, UWE, LWE, IFETCH, IPIPE, IACK[a] Asserted	t_{CLSA}	3	30	3	20	ns
9A[2]	AS to DS or CS Asserted (Read)	t_{STSA}	–15	15	–6	6	ns
11	Address, FC, SIZ, RMC Valid to AS, CS (and DS Read) UWE, LWE Asserted	t_{AVSA}	15	—	10	—	ns
12	CLKOUT Low to AS, DS, CS, UWE, LWE, IFETCH, IPIPE, IACK[a] Negated	t_{CLSN}	3	30	3	20	ns
13	AS, DS, CS, UWE, LWE, IACK[a] Negated to Address, FC, SIZ Invalid (Address Hold)	t_{SNAI}	15	—	10	—	ns
14	AS, CS, UWE, LWE, (and DS Read) Width Asserted	t_{SWA}	100	—	70	—	ns
14A	DS Width Asserted (Write)	t_{SWAW}	45	—	30	—	ns
14B	AS, CS, UWE, LWE, IACK[a] (and DS Read) Width Asserted (Fast Termination Cycle)	t_{SWDW}	40	—	30	—	ns
15[3]	AS, DS, CS, UWE, LWE Width Negated	t_{SN}	40	—	30	—	ns
16	CLKOUT High to AS, DS, UWE, LWE, R/W High Impedance	t_{CHSZ}	—	60	—	40	ns
17	AS, DS, CS, UWE, LWE Negated to R/W High	t_{SNRN}	15	—	10	—	ns
18	CLKOUT High to R/W High	t_{CHRH}	0	30	0	20	ns
20	CLKOUT High to R/W Low	t_{CHRL}	0	30	0	20	ns
21[9]	R/W High to AS, CS Asserted	t_{RAAA}	15	—	10	—	ns
22	R/W Low to DS Asserted (Write)	t_{RASA}	70	—	47	—	ns
23	CLKOUT High to Data-Out Valid	t_{CHDO}	—	30	—	20	ns
24	Data-Out Valid to Negating Edge of AS, CS, UWE, LWE (Fast Termination Write)	t_{DVASN}	15	—	10	—	ns
25	DS, CS, Negated to Data-Out Invalid (Data-Out Hold)	t_{SNDOI}	15	—	10	—	ns
26	Data-Out Valid to DS Asserted (Write)	t_{DVSA}	15	—	10	—	ns
27	Data-In Valid to CLKOUT Low (Data Setup)	t_{DICL}	5	—	5	—	ns
27A	Late BERR, HALT, BKPT Asserted to CLKOUT Low (Setup Time)	t_{BELCL}	20	—	10	—	ns
28	AS, DS, UWE, LWE Negated to DSACK[a], BERR, HALT Negated	t_{SNDN}	0	80	0	50	ns
29[4]	DS, CS Negated to Data-In Invalid (Data-In Hold)	t_{SNDI}	0	—	0	—	ns
29A[4]	DS, CS Negated to Data-In High Impedance	t_{SHDI}	—	60	—	40	ns
30[4]	CLKOUT Low to Data-In Invalid (Fast Termination Hold)	t_{CLDI}	15	—	10	—	ns

44. AC TIMING SPECIFICATIONS (CONTINUED)

(See notes (a), (b), (c), and (d) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70∞C; see numbered notes; see Figure 7–Figure 16)

NUM	CHARACTERISTIC	SYMBOL	3.3 V OR 5.0 V 16.78 MHZ MIN	3.3 V OR 5.0 V 16.78 MHZ MAX	5.0 V 25.16 MHZ MIN	5.0 V 25.16 MHZ MAX	UNIT
30A[4]	CLKOUT Low to Data-In High Impendance	t_{CLDH}	—	90	—	60	ns
31[5]	DSACK[a] Asserted to Data-In Valid	t_{DADI}	—	50	—	32	ns
31A	DSACK[a] Asserted to DSACK[a] Valid (Skew)	t_{DADV}	—	30	—	20	ns
32	HALT and RESET Input Transition Time	t_{HRrf}	—	200	—	140	ns
33	CLKOUT Low to BG Asserted	t_{CLBA}	—	30	—	20	ns
34	CLKOUT Low to BG Negated	t_{CLBN}	—	30	—	20	ns
35[6]	BR Asserted to BG Asserted (RMC Not Asserted)	t_{BRAGA}	1	—	1	—	CLK OUT
37	BGACK Asserted to BG Negated	t_{GAGN}	1	2.5	1	2.5	CLK OUT
39	BG Width Negated	t_{GH}	2	—	2	—	CLK OUT
39A	BG Width Asserted	t_{GA}	1	—	1	—	CLK OUT
46	R/W Width Asserted (Write or Read)	t_{RWA}	150	—	100	—	ns
46A	R/W Width Asserted (Fast Termination Write or Read)	t_{RWAS}	90	—	60	—	ns
47A[8]	Asynchronous Input Setup Time	t_{AIST}	8, 5	—	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	15	—	10	—	ns
48[5,7]	DSACK[a] Asserted to BERR, HALT Asserted	t_{DABA}	—	30	—	20	ns
53	Data-Out Hold from CLKOUT High	t_{DOCH}	0	—	0	—	ns
54	CLKOUT High to Data-Out High Impedance	t_{CHDH}	—	30	—	20	ns
55	R/W Asserted to Data Bus Impedance Change	t_{RADC}	40	—	25	—	ns
56	RESET Pulse Width (Reset Instruction)	t_{HRPW}	512	—	512	—	CLK OUT
56A	RESET Pulse Width (Input from External Device)	t_{RPWI}	590	—	590	—	CLK OUT
57	BERR Negated to HALT Negated (Rerun)	t_{BNHN}	0	—	0	—	ns
70	CLKOUT Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	30	0	20	ns
71	Data Setup Time to CLKOUT Low (Show Cycle)	t_{SCLDS}	15	—	10	—	ns
72	Data Hold from CLKOUT Low (Show Cycle)	t_{SCLDH}	10	—	6	—	ns
80	DSI Input Setup Time	t_{DSISU}	15	—	10	—	ns
81	DSI Input Hold Time	t_{DSIH}	10	—	6	—	ns
82	DSCLK Setup Time	t_{DSCSU}	15	—	10	—	ns
83	DSCLK Hold Time	t_{DSCH}	10	—	6	—	ns

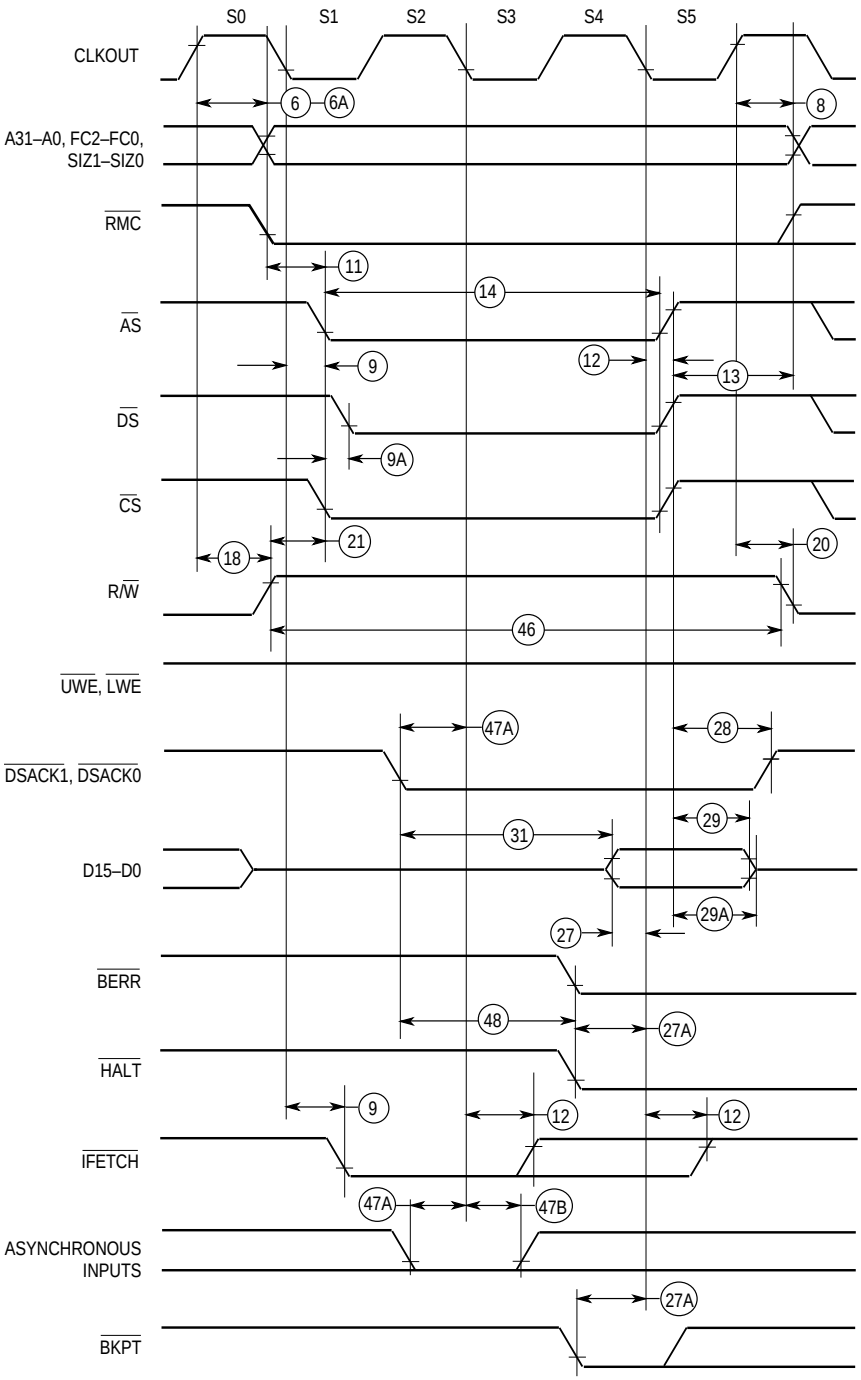
44. AC TIMING SPECIFICATIONS (CONTINUED)

(See notes (a), (b), (c), and (d) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70∞C; see numbered notes; see Figure 7–Figure 16)

NUM	CHARACTERISTIC	SYMBOL	3.3 V OR 5.0 V 16.78 MHZ MIN	3.3 V OR 5.0 V 16.78 MHZ MAX	5.0 V 25.16 MHZ MIN	5.0 V 25.16 MHZ MAX	UNIT
84	DSO Delay Time	t_{DSOD}	—	t_{cyc} + 25	—	t_{cyc} + 16	ns
85	DSCLK Cycle	t_{DSCCYC}	2	—	2	—	CLK OUT
86	CLKOUT High to FREEZE Asserted	t_{FRZA}	0	50	0	35	ns
87	CLKOUT High to FREEZE Negated	t_{FRZN}	0	50	0	35	ns
88	CLKOUT High to IFETCH High Impedance	t_{IFZ}	0	50	0	35	ns
89	CLKOUT High to IFETCH Valid	t_{IF}	0	50	0	35	ns

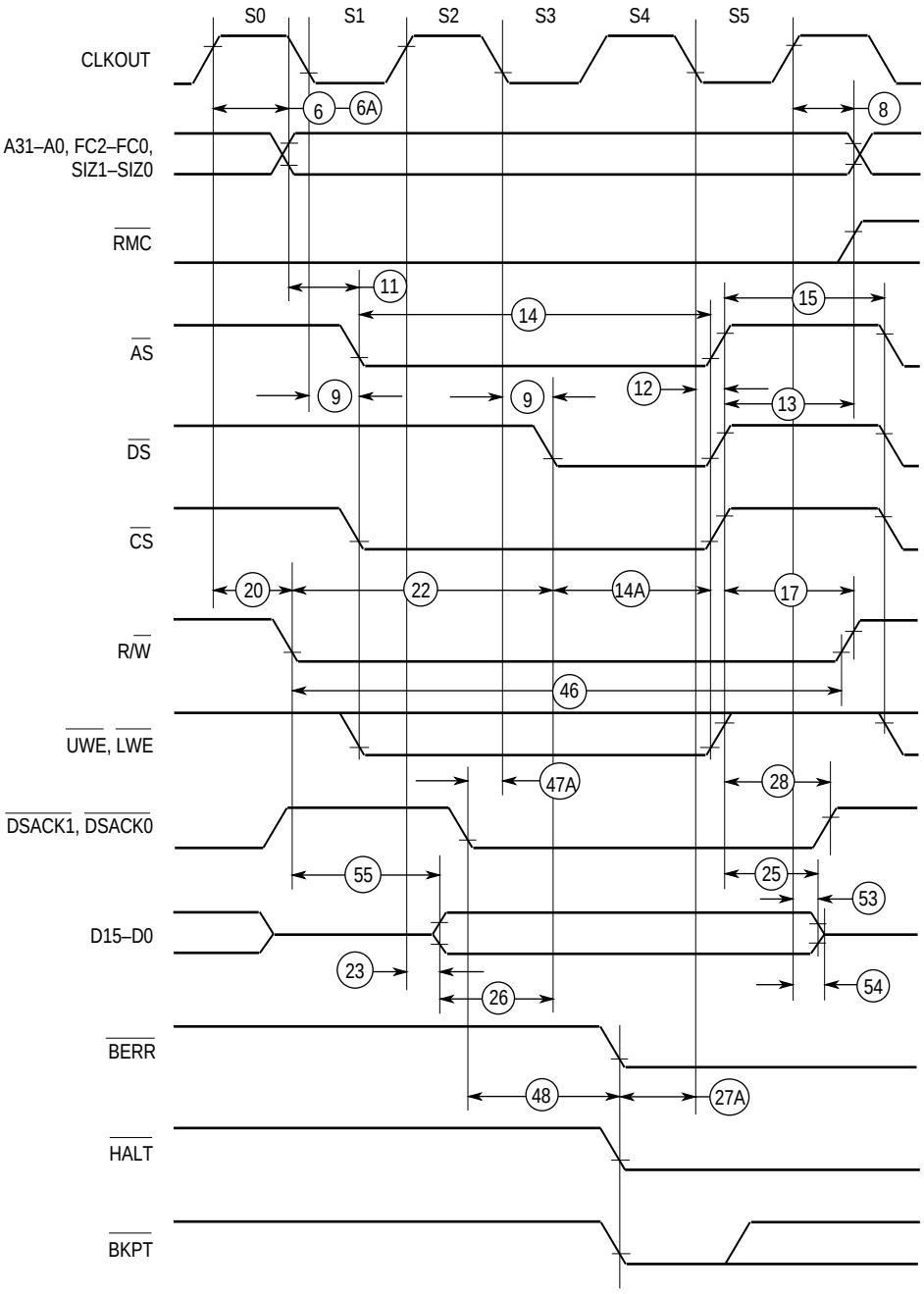
(a) The electrical specifications in this document for both the 8.39 and 16.78 MHz @ 3.3 V±0.3 V are preliminary and apply only to the appropriate MC68330V low voltage part.
(b) The 16.78-MHz specifications apply to the MC68330 @ 5.0 V ±5% operation.
(c) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.
(d) For extended temperature parts T_A = –40 to +85°C. These specifications are preliminary.

1. All AC timing is shown with respect to 0.8 V and 2.0 V levels unless otherwise noted.
2. This number can be reduced to 5 ns if strobes have equal loads.
3. If multiple chip selects are used, the CS width negated (#15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select.
4. These hold times are specified with respect to DS or CS on asynchronous reads and with respect to CLKOUT on fast termination reads. The user is free to use either hold time for fast termination reads.
5. If the asynchronous setup time (#47) requirements are satisfied, the DSACK≈ low to data setup time (#31) and DSACK≈ low to BERR low setup time (#48) can be ignored. The data must only satisfy the data-in to CLKOUT low setup time (#27) for the following clock cycle: BERR must only satisfy the late BERR low to CLKOUT low setup time (#27A) for the following clock cycle.
6. To ensure coherency during every operand transfer, BG will not be asserted in response to BR until after cycles of the current operand transfer are complete and RMC is negated.
7. In the absence of DSACK[a], BERR is an asynchronous input using the asynchronous setup time (#47).
8. Specification #47A for 16.78 MHz @ 3.3 V ±0.3V will be 8 ns.
9. During interrupt acknowledge cycles up to two wait states may be inserted by the processor between states S0 and S1.
10. Address Access Time = $2t_{cyc} + t_{CW} – t_{CHAV} – t_{DICL}$ = 112.2 ns (@ 16.78-MHz clock). Chip-Select Access Time = $2t_{cyc} – t_{CLSA} – t_{DICL}$ = 84.2 ns (@ 16.78-MHz clock).



NOTE: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7. Read Cycle Timing Diagram



NOTE: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 8. Write Cycle Timing Diagram

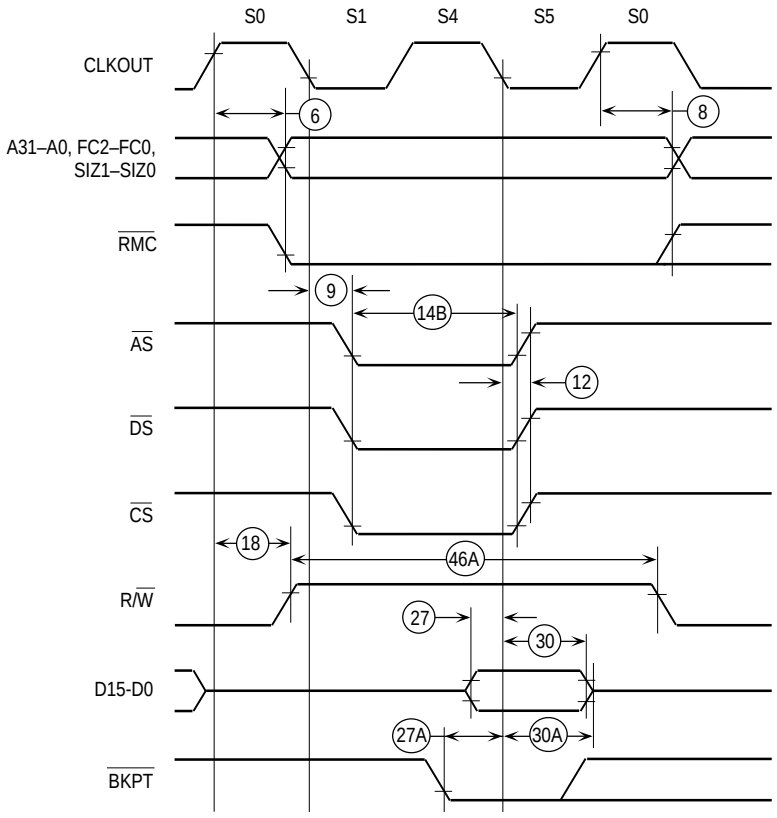


Figure 9. Fast Termination Read Cycle Timing Diagram

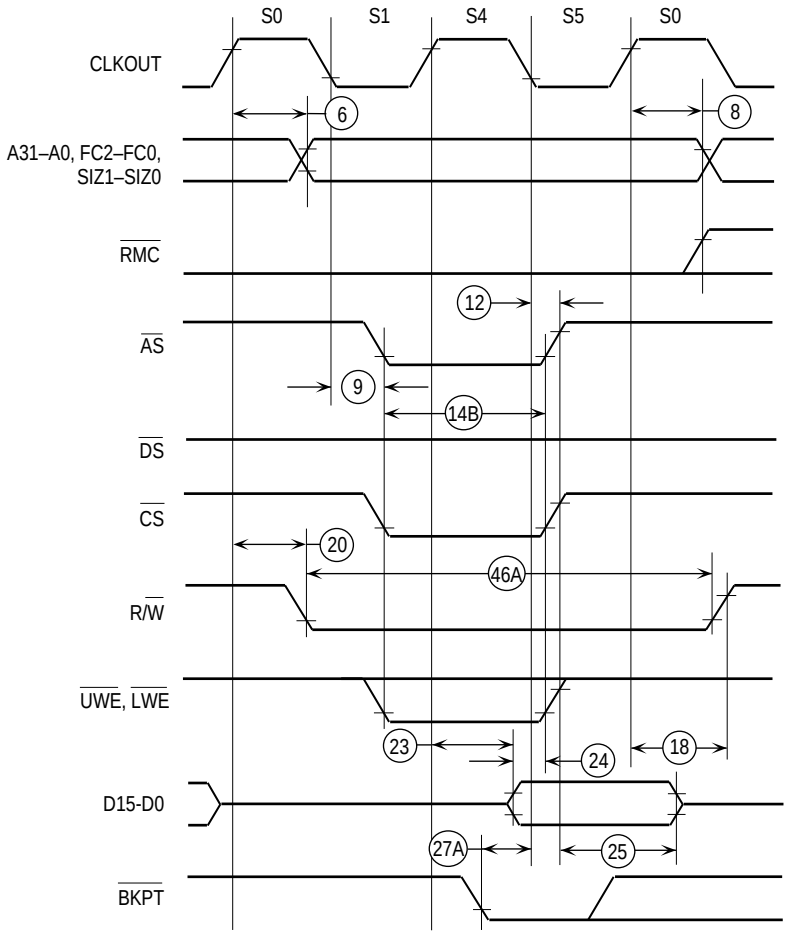


Figure 10. Fast Termination Write Cycle Timing Diagram

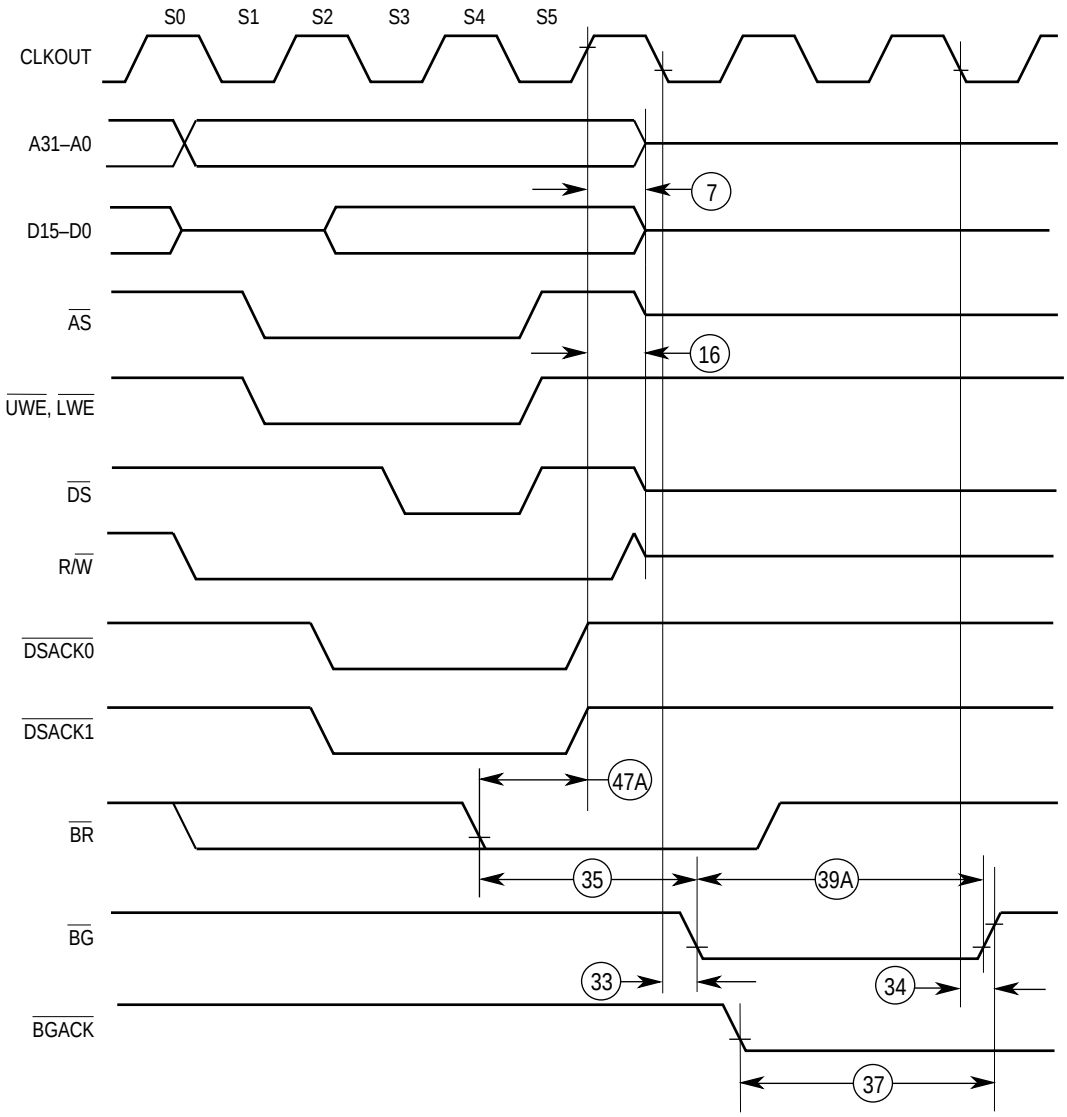


Figure 11. Bus Arbitration Timing—Active Bus Case

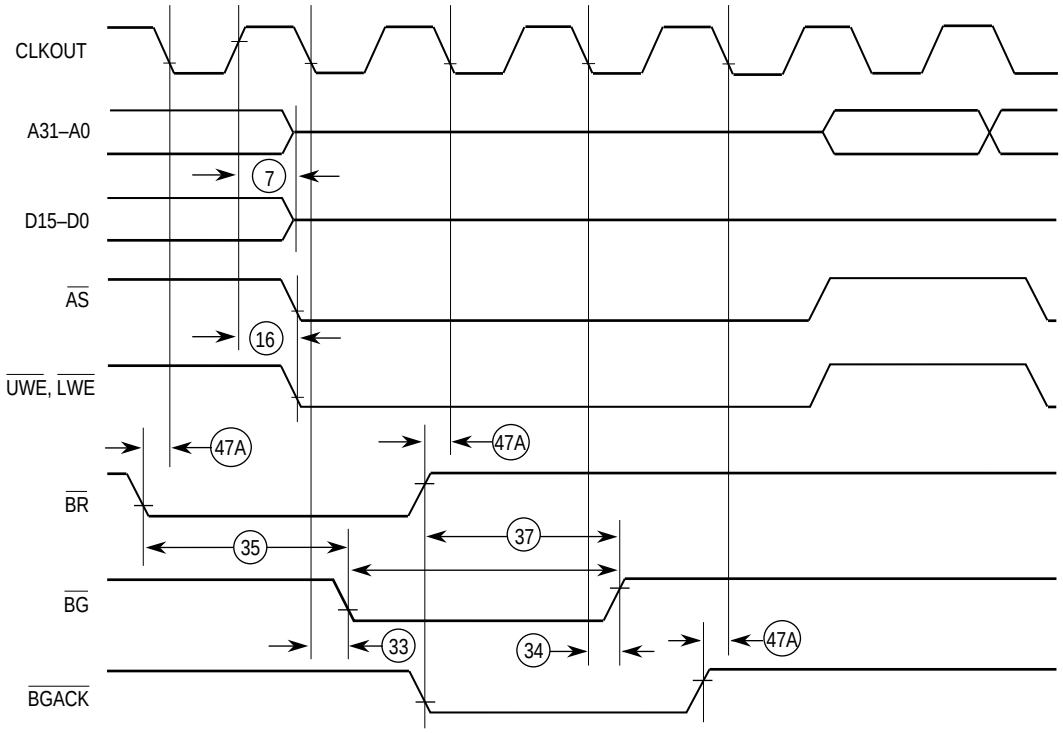


Figure 12. Bus Arbitration Timing—Idle Bus Case

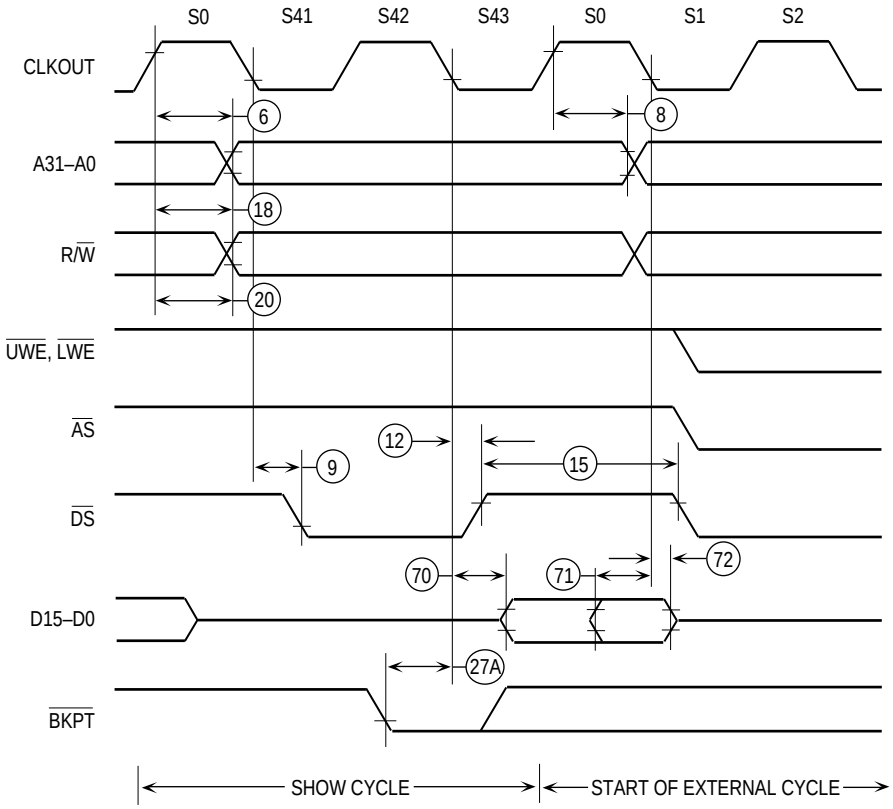
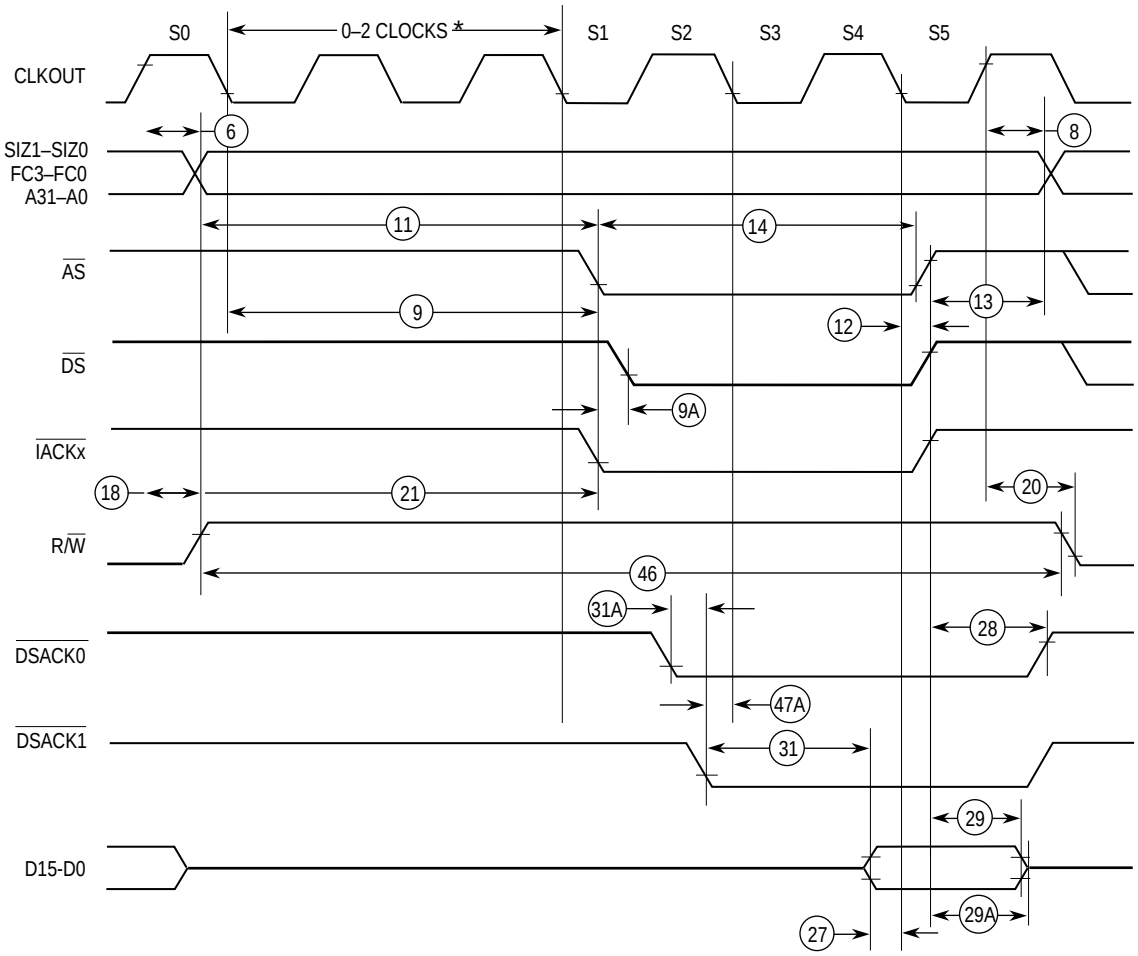


Figure 13. Show Cycle Timing Diagram



*Up to two wait states may be inserted by the processor between states S0 and S1.

Figure 14. IACK Cycle Timing Diagram

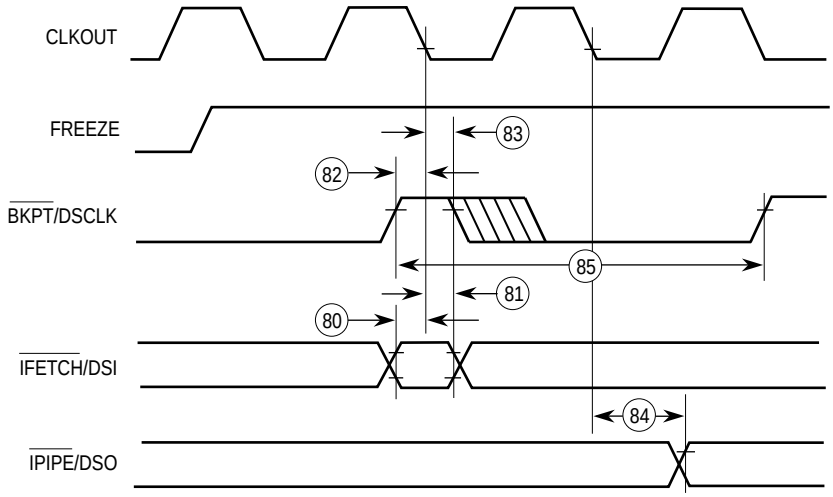


Figure 15. Background Debug Mode Serial Port Timing

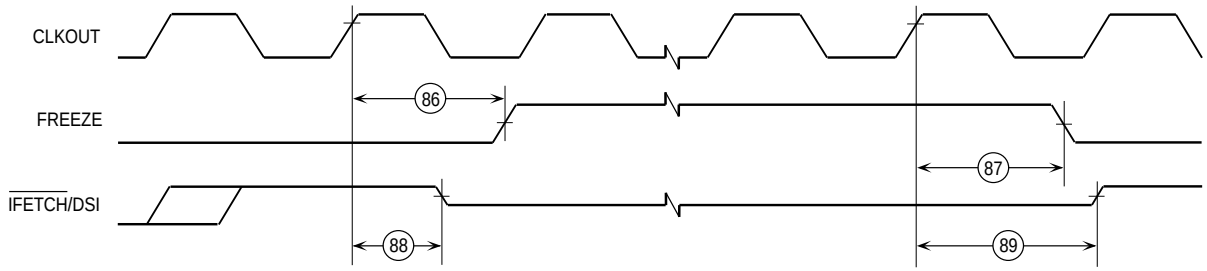


Figure 16. Background Debug Mode FREEZE Timing

IEEE 1149.1 ELECTRICAL SPECIFICATIONS

(See notes (a), (b), (c), and (d) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70°C(see Figures 20, 21, and 22)

NUM.	CHARACTERISTIC	3.3 V OR 5.0 V 16.78 MHZ MIN	3.3 V OR 5.0 V 16.78 MHZ MAX	5.0 V 25.16 MHZ MIN	5.0 V 25.16 MHZ MAX	UNIT
	TCK Frequency of Operation	0	16.78	0	25	MHz
1	TCK Cycle Time in Crystal Mode	59.6	—	40	—	ns
2	TCK Clock Pulse Width Measured at 1.5 V	28	—	18	—	ns
3	TCK Rise and Fall Times	0	5	0	3	ns
6	Boundary Scan Input Data Setup Time	16	—	10	—	ns
7	Boundary Scan Input Data Hold Time	26	—	18	—	ns
8	TCK Low to Output Data Valid	0	40	0	26	ns
9	TCK Low to Output High Impedance	0	60	0	40	ns
10	TMS, TDI Data Setup Time	15	—	10	—	ns
11	TMS, TDI Data Hold Time	15	—	10	—	ns
12	TCK Low to TDO Data Valid	0	25	0	16	ns
13	TCK Low to TDO High Impedance	0	25	0	16	ns

(a) The electrical specifications in this document for both the 8.39 and 16.78 MHz @ 3.3 V±0.3 V are preliminary, and apply only to the appropriate MC68330V low voltage part.
(b) The 16.78-MHz specifications apply to the MC68330 @ 5.0 V ±5% operation.
(c) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.
(d) For extended temperature parts T_A = –40 to +85°C. These specifications are preliminary.

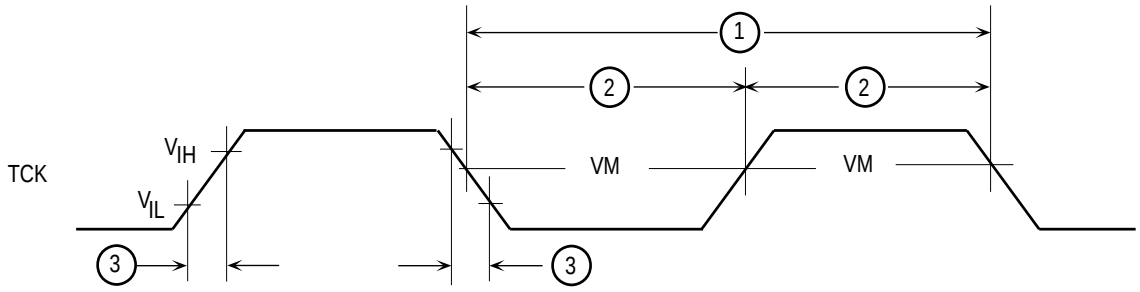


Figure 17. TCK Input Timing Diagram

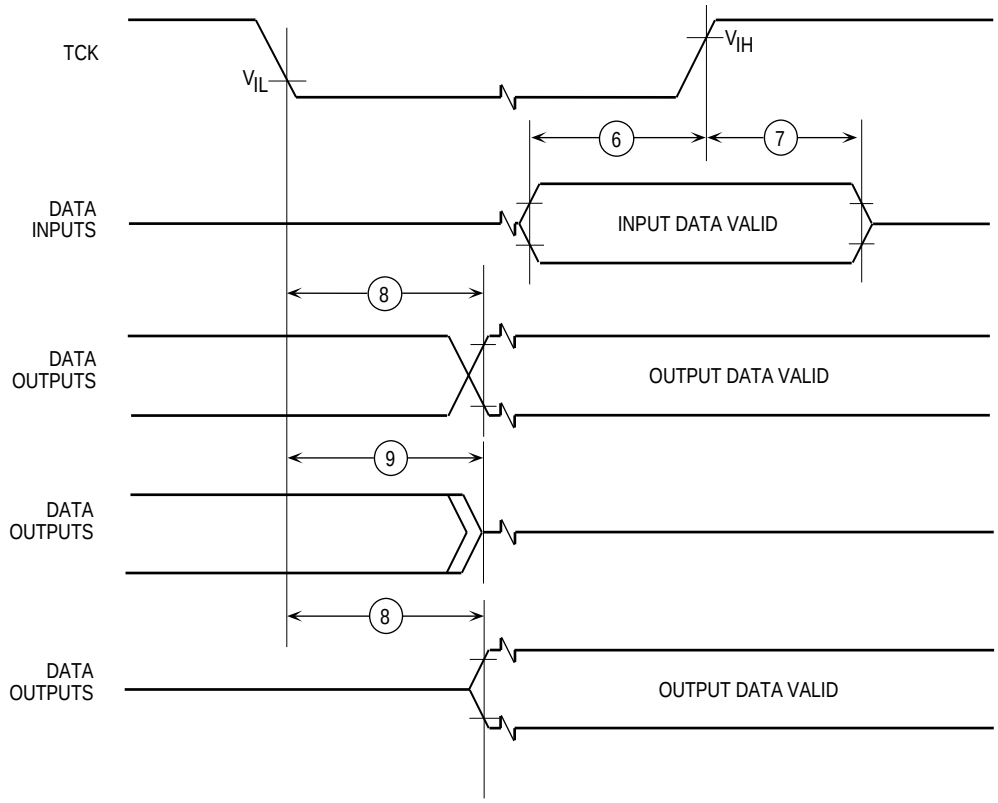


Figure 18. Boundary Scan Timing Diagram

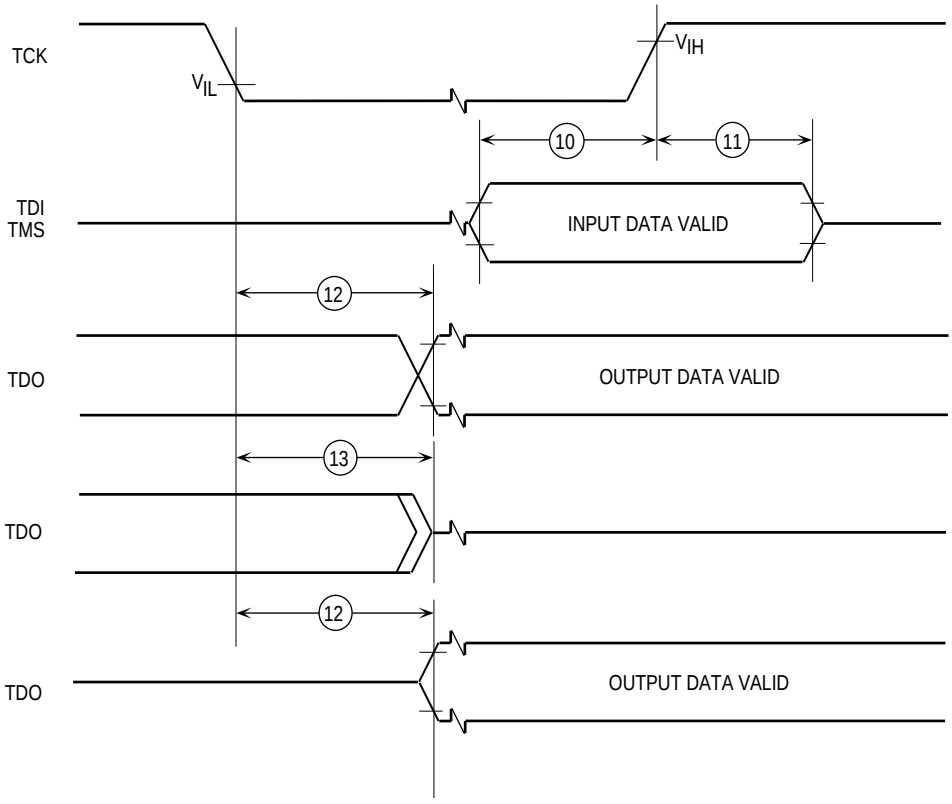


Figure 19. Test Access Port Timing Diagram

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