PHYTEC

miniMODUL-537/509

Hardware-Manual

Edition June 1999

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	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 255 Ericksen Avenue NE Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	+1 (800) 278-9913 order@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	+1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	+1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

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Index of Figures and Tables

Preface

This miniMODUL-537/509 Hardware Manual describes the board's design and functions. Precise specifications for the SAB80C537 microcontroller can be found in the enclosed microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding EMV-Conformity of the PHYTEC miniMODUL-537/509

CE

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

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The miniMODUL-537/509 is one of a series of PHYTEC nano-/micro-/miniMODULs which can be fitted with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common Infineon 8- and 16-bit controllers in two ways:

(1) as the basis for Starter Kits in which user-designed hardware can be implemented on a wrap-field around the controller and

(2) as insert-ready, fully functional micro- and miniMODULS which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. Please contact PHYTEC for additional information:

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Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 255 Ericksen Avenue NE Bainbridge Island, WA 98110 USA
Web Site:	http://www.phytec.de	http://www.phytec.com
e-mail:	info@phytec.de	info@phytec.com
Voice:	+49 (6131) 9221-0	+1 (800) 278-9913
Fax:	+49 (6131) 9221-33	+1 (206) 780-9135

1 Introduction

The miniMODUL-537/509 is a continuation of PHYTEC's successful line of credit card-sized microcomputers. The core of the miniMODUL-537 version is the Infineon SAB80C537 8-bit controller, which is closely compatible to the 80C535 yet boasts the following integrated hardware additions: 4 timers, a 12-channel A/D-converter, two serial interfaces, a Watchdog-Timer, eight data-pointers, six ports and a high-performance arithmetic unit. The miniMODUL-509 version is based on the 80C509 controller which, in turn, extends the functionality of the C537. The C509 has a standard internal frequency booster which doubles its clock speed from 12 to 24 MHz. Its maximum clock frequency of 16 MHz. allows it to attain the processing speed of an 8032 board running at a 32 MHz frequency (delivering an instruction cycle in 375 ns.). It also offers 3 kByte on-chip RAM and Boot-ROM, as well as a 15-bit A/D-converter with 10-bit resolution. Refer to the corresponding Controller User's Manual for detailed information. The module itself features 32 kByte SRAM and 128 kByte Flash, which can be programmed on-board using the PHYTEC FlashTools. All board components are addressable, with signals available at the pin rows aligning three edges of the board. The miniMODUL-509/537 can also accommodate an external address decoder. One of two RS-232 serial interfaces can be optionally configured as an RS-485 transceiver, hence allowing the module to be networked with other boards with RS-485 connectivity. The module is easily programmable with the included 8051-compatible evaluation software development tools. These versatile on-chip and peripheral characteristics of the miniMODUL-537/509 render the module a complete microprocessor-system. Insertion of the miniMODUL-537/509 into a project allows engineers to forgo development of a digital microprocessor system to be embedded within application hardware, hence shortening development time horizons. The miniMODUL-537/509 can also be inserted as a "big chip" into application hardware. Compare the cost-performance of PHYTEC's insert-ready miniMODUL-537/509 with the development, design and testing costs of your internal development.

The miniMODUL-537/509 offers the following features:

- SBC in credit card-size dimensions (55 x 85 mm.) achieved through advanced SMD technology
- fitted with Infineon 8051-compatible SAB80C509 in a QFP-100 socket or C537 controller in a PLCC-84 socket
- improved interference safety through multi-layer technology
- controller signals and ports extend to standard-width (2.54 mm.) pins aligning board edges, allowing the board to be plugged into any target application like a “big chip”
- requires a single low power supply 5 V/typ. < 100 mA
- 128 (to 512) kByte Flash on-board (PLCC)
- on-board Flash programming
- no dedicated Flash programming voltage required through use of 5 V Flash devices
- 32 (to 160) kByte RAM on-board (SMD)
- 32 kByte EEPROM (SMD) can also be accommodated on the board
- supplemental 3 kByte XRAM on-chip and BOOT-ROM with the C509
- flexible software-configured address decoding through complex logic device
- bank latches for Flash and RAM integrated in address decoder
- 2 serial interfaces via RS-232 (one of which is optionally configurable as an RS-485 transceiver to enable networking)
- Real Time Clock (RTC8583 or RTC72423)
- SRAM and Real-Time Clock buffered by external battery
- 3 free Chip-Select signals for easy connection external peripherals
- operates within a standard range of 0 to 70 degrees C°.

1.1 Block Diagram

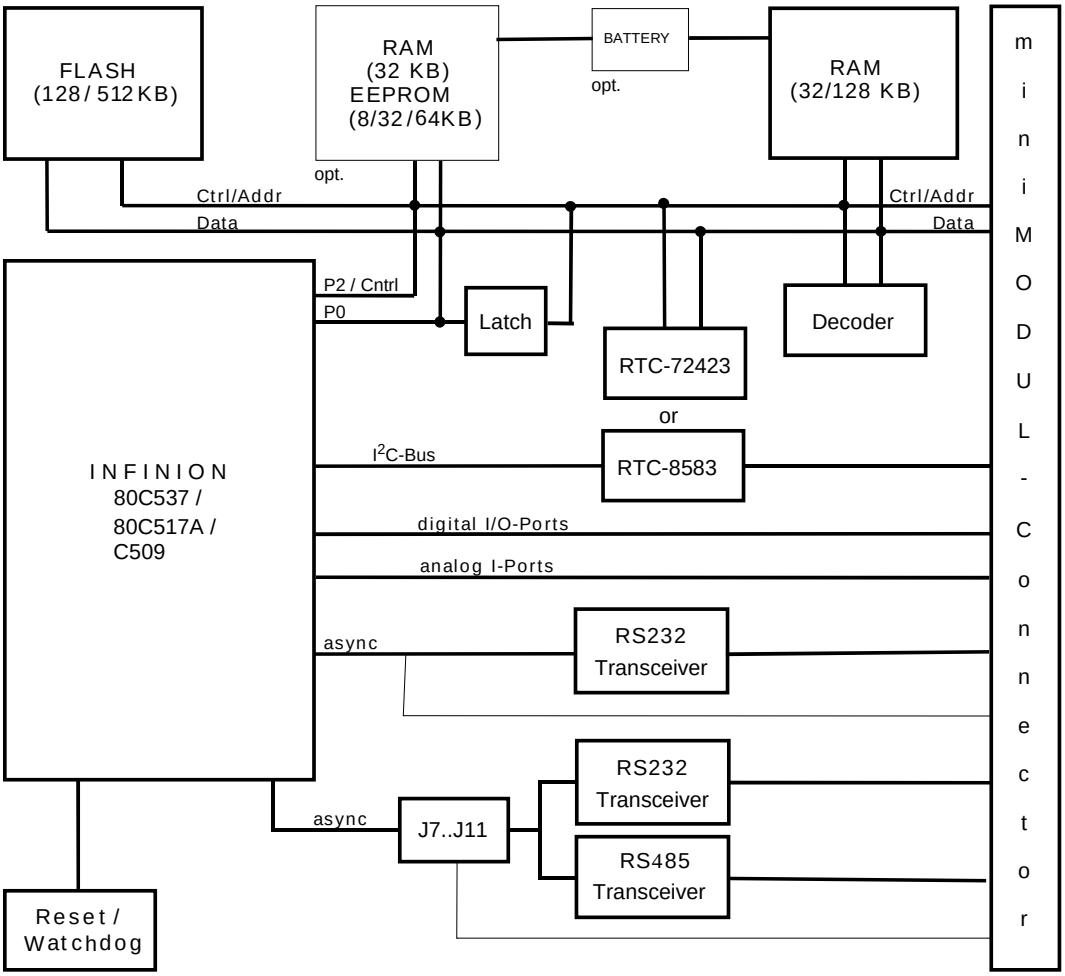


Figure 1: Block Diagram

2 Pinout

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.
As
Figure 2 indicates, all controller signals extend to standard-width (2.54 mm) pin rows lining three sides the board (referred to as miniMODUL-Connector). This allows the board to be plugged into any target application like a "big chip". *Table 1* provides an overview of the pinout of the miniMODUL-Connector

Attention:
The miniMODUL-537/509 has been reengineered for Flash technology in an manner ensuring the highest possible compatibility to earlier non-Flash fitted versions of the miniMODUL-537. However some differences in pinout to earlier versions, as described in the, chapter *9* were unavoidable.

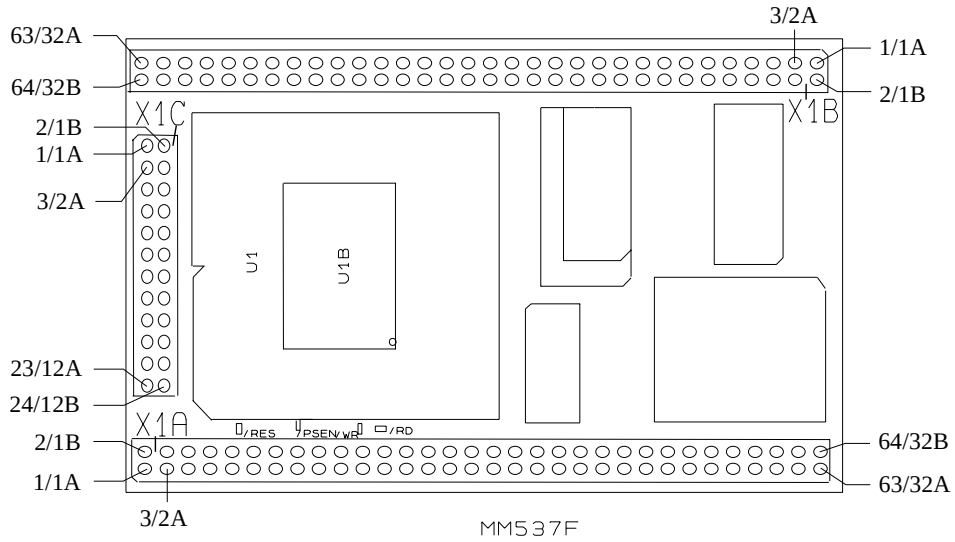


Figure 2: Pinout of the miniMODUL-537/509

PIN #	Connection	Comments
Pin row X1A		
1, 2/ 1A, 1B	NC	Not used
3..10/ 2A..5B	P4.0...P4.7	Port 4
11/ 6A	MDIS	Memory-Disable-Input for U4 and U5
12/ 6B	/PSEP	separable Program-Store-Enable-signal of the controller
13/ 7A	/WRP	separable /WR-signal of the controller[1]
14/ 7B	/RDP	separable /RD-signal of the controller[1]
15..20/ 8A..10B	P3.0...P3.5	Port 3
21/ 11A	/WR , P3.6	separable /WR-signal of the module[1]
22/ 11B	/RD , P3.7	separable /RD-signal of the module[1]
23..30/ 12A 15B	P1.7...P1.0	Port 1
31/ 16A	/PSEN	separable Program-Store-Enable-signal of the module[1]
32/ 16B	VPD	Voltage-output for external buffer
33/ 17A	RES	Reset-output of the module
34/ 17B	/RES	separable Reset-Input/Output of the module[1]
35/ 18A	/CS1	predecoded Chip-Select-signal #1
36/ 18B	/CS2	predecoded Chip-Select-signal #2
37/ 19A	/CS3	predecoded Chip-Select-signal #3
38/ 19B	/PFO	Power-Fail Output
39/ 20A	PFI	Power-Fail Input
40/ 20B	/HPD	optional HWPD-Input for the C509/C517A
41, 43, 51, 52/ 21A, 22A, 26A, 26B	TI1...TI4	Transmitter-Inputs 1-4 of the RS-232 driver (TI1 and TI2 conected via Jumpers J5 and J8 to the serial interface of the controller)
42/ 21B	VBAT	Input for conection to external buffer battery
44, 54, 50/ 22B, 27B, 25B	RO1...RO3	Receiver-Outputs 1-3 of the RS-232 driver (RO1 and RO2 are connected via Jumpers J6 and J7 to the serial interface of the controller)
45 ,55 ,49/ 23A, 28A, 25A	RI1...RI3	Receiver-Inputs 1-3 of the RS-232 driver
47, 46, 48, 56/ 24A, 23B, 24B, 28B	TO1...TO4	Transmitter Outputs 1-4 of the RS-232 driver
53/ 27A	RSDIS	RS-232 driver Disable-Input
57/ 29A	ALE	Address-Latch-Enable Output
58/ 29B	/RESP	separable Reset-signal of the controller[1]
59/ 30A	/CSRTC	Chip-Select-signal of RTC72423 (connected via Jumper J13 to /CS1
60/ 30B	/IRTC	Interrupt-Output of both RTCs
61/ 31A	/RESI	/Reset-Input of the module
62/ 31B	WDP	Watchdog-Input of the module
63, 64/ 32A, 32B	NC	not used

[1]: In order to implement an emulator, the controller signals /*XX*P can be separated from the /XX signals used in the module, enabling external input. Applicable signals are /PSEN, /RD, /WR and /RES

PIN #	Connection	Comments
Pin row X1B		
1, 2/ 1A, 1B	VCC	Voltage input +5 V.
3..10/ 2A..5B	AD7...AD0	Data-bus (Port 0), multiplexed with low-byte of address-bus
11..18/ 6A..9B	A7...A0	Address-bus (low-byte)
19, 20....26/ / 10A, 10B..13B	A9 ,A8, A11, A10, A13, A12, A15, A14	Address-bus (high-byte)
27/ 14A	PRGEN	Program-Enable-Input (only C509)
28/ 14B	NC	Not used
29/ 15A	DE	Data-Enable-Input of the RS-485 driver (connected via Pin 13 to U11)
30/ 15B	D	Data-input of the RS-485 transmitter (connected via Jumper J8 to the serial interface of the controller)
31/ 16A	B	differentiated B-line of the RS-485 driver
32/ 16B	R	Data-output of the RS-485 receiver (connected via Jumper J7 to the serial interface of the controller)
33/ 17A	A	differentiated A-line of the RS-485 driver
34/ 17B	/R	inverted Data-output of the RS-485 receiver (connected via Jumper J11 to P3.2 of the controller)
35/ 18A	/DE	inverted Data-Enable-input of the RS-485 transmitter (connected via Jumper J9 with P5.1 of the controller)
36/ 18B	/RE	Receive-Enable-input of the RS-485 receiver (connected via Jumper J10 to GND)
37..44/ 19A 22B	P9.7...P9.0	Port 9 (of the C509 controller)
45..52/ 23A 26B	P5.7...P5.0	Port 5
53/ 27A	/RO	Reset-Output of the controller
54/ 27B	/PE	Watchdog Timer/Power-Save mode of the controller (connected via Jumper J3 to GND)
55..62/ 28A 31B	P6.0...P6.7	Port 6
63, 64/ 32A, 32B	GND	Ground 0 V.
Pin row X1C		
1, 5, 9, 13, 15, 17, 19, 21/ 1A, 3A, 5A, 7A, 8A, 9A, 10A, 11A	AGND	Analog-input 0 V.
3, 7, 11/ 2A, 4A, 6A	P8.4 ..P8.6/ AN12...AN14	Analog-inputs AN12...AN14 (only for the C509 controller)
8, 6, 4, 2, 24, 22, 20, 18, 16, 14, 12, 10/ 4B, 3B, 2B, 1B, 12B, 11B, 10B, 9B, 8B, 7B, 6B, 5B	P8.3..P8.0, P7.7.. P7.0/ AN11.AN0	Analog-inputs AN11...AN0
23/ 12A	AREF	Reference Voltage: Analog inputs + 5 V.

Table 1: Pinout with Explanations

3 Jumpers

For configuration purposes, the miniMODUL-537/509 has 14 soldering jumpers, some of which have been installed prior to delivery. *Figure 3* illustrates the numbering of the jumper-pads, while *Figure 4* and *Figure 5* indicates the location of the jumpers on the board.

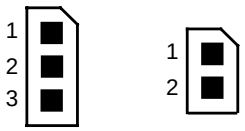


Figure 3: Numbering of the jumper-pads

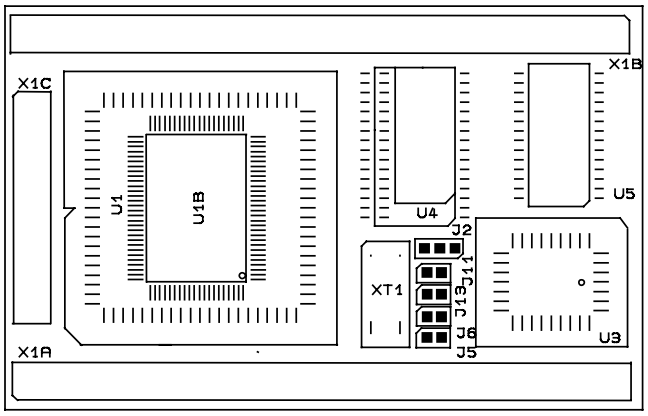


Figure 4: Location of the Jumper (view of the component side)

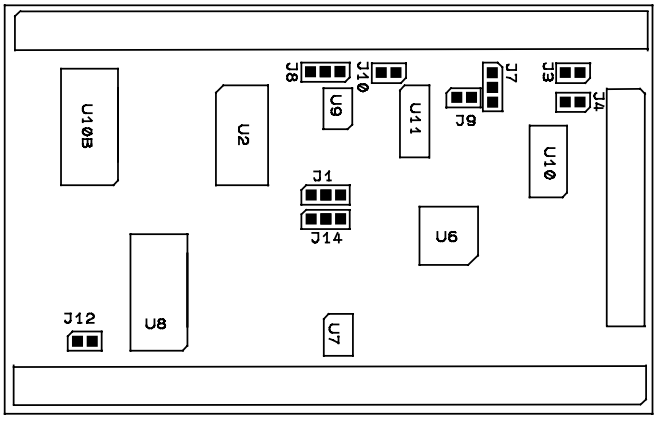


Figure 5: Location of the Jumper (view of the soldering side)

The jumpers can be divided into three groups:

1. Serial Interface Jumpers J5, J6, J7, J8, J9, J10, J11 and J12
2. Memory Model Selection Jumper J2 (U5)
3. Special Features Jumpers J1, J3, J4, J13 and J14

3.1 Serial Interface Jumpers

Jumpers J5 and J6: Jumpers J5 and J6 connect both signals of the controller's serial interface 0 (Serial0) with the RS-232 transceiver of the miniMODUL at pins 45(23A) and 47(24A) at X1A. Additionally, a TTL connection is enabled when controller signals are directly connected to pins 15(8A) and 16(8B) of the module (P3.0 and P3.1). At the time of delivery the RS-232 interface is active by default.
The following signal qualities can be configured for serial interface 0:

Signal Quality - Serial0	J5	J6
RS-232 (modul pins 45(23A) and 47(24A) at X1A)	closed	closed
TTL (modul pins 15(8A) and 16(8B) at X1A)	open	open

Jumpers J7 and J8: Jumpers J7 and J8 connect both pins of the controller's serial interface 1 (Serial1) with an RS-232 or RS-485 transceiver of the miniMODUL. Likewise, a TTL connection is enabled when controller signals are directly connected to pins 56(28B) and 57(29A) at X1B (P6.1 and P6.2).

The following signal qualities can be configured for serial interface 1:

Signal Quality - Serial1	J7	J8
RS-232 (modul pins 46(23B) and 55(28A) at X1A)	2+3	2+3
TTL (modul pins 56(28B) and 57(29A) at X1B)	open	open
RS-485 (modul pins 31(16A) and 33(17A) at X1B)	1+2	1+2

Jumper J9: Closing Jumper J9 connects the Data-Enable-Input of the RS-485 transceiver to pin P5.1 of the controller. This allows software-configuration of the RS-485 transmitter for networking purposes (such as networking the module within the proprietary PHYTEC µNET RS-485 network).

RS-485-Transmitter	J9	P5.1	RES
Enabled	closed	Low	Low
Disabled	closed	High	*n.a.*
	closed	*n.a.*	High
	open	*n.a.*	*n.a.*

Jumper J10: Closing Jumper J10 enables receptivity of the RS-485 Receiver.

RS-485-Receiver	J10
Reception Enabled	closed
Reception Disabled	open

Jumper J11: Closing Jumper J11 connects the inverted Data-Output of the RS-485 receiver with pin P3.2 of the controller. As this pin is bit-addressable, Jumper J11 enables bit-addressed commands regarding the status of the data-output.

Controller Pin P3.2	J11
Connected with the inverted Data-Output	closed
Disconnected with the inverted Data-Output	open

If the module is to be routed in the proprietary PHYTEC µNET RS-485 network, then the jumpers J9, J10 and J11 must be closed in order to enable µNET network connectivity.

Jumper J12: Opening Jumper J12 deactivates the RS-232 transceiver. If this transceiver is deactivated, it is possible to control the transceiver's activities via the RSDIS input of the module (module pin 53(27A) at X1A). Upon delivery of the module, Jumper J12 is closed and, hence, the RS-232 transceiver is activated.

RS-232 Transceiver	J12	RSDIS
Activated	closed	N.C.
	open	Low
Deactivated	open	N.C.
	open	High

3.2 Memory Model Selection Jumper J2 (U5)

Jumper J2: Jumper J2 enables selection of a power source for the specific memory device installed at U5. If an EEPROM is installed at U5, a power source via Vcc (J2 = 1+2) is required in order to prevent a expedited depletion of any external battery buffer. Installation of a RAM device at U5, however, requires sourcing power via VPD (J2 = 2+3).

Memory Device at U5	J2
EEPROM	1+2
RAM	2+3

3.3 Special Features Jumpers

Jumpers J1, J3, J4, J13 and J14 are used to activate the special features of the particular controller fitted on the module.

- **Execution out of internal or external program memory**

  At the time of delivery, Jumper J1 is preconnected at pads 1+2. This default configuration means that the program stored in the external program memory is executed after a Hardware-Reset. In order to allow the execution of a specific controller's internal program memory, the pads 2+3 on jumper J1 must be connected.
  The following configurations are possible:

Code-Fetch	J1
Execution from external program memory	1+2
Execution from internal program memory	2+3

- **Power-Saving Modes/Watchdog Timer**

Opening Jumper J3 deactivates the Power-Save mode. This also automatically starts the Watchdog timer after a Hardware-Reset. Upon delivery, the Watchdog timer is deactivated. Jumper J3 allows activation of either the timer or the Power-Save mode.

Power-Save Mode	Watchdog Timer	J3
Activated	Deactivated	closed
Deactivated	Activated	open

- **Oscillator-Watchdog**

Upon delivery of the module, the Oscillator-Watchdog is activated, enabling a quick Power-On-Reset of and stable operation of the controller.

Oscillator-Watchdog	J4
Deactivated	closed
Activated	open

- **Chip-Enable of the RTC72423**

Closing Jumper J13 connects the Real-Time-Clock RTC2423 with the address decoder's pre-decoded Chip-Select signal /CS1. Opening Jumper J13 allows the user to connect any desired Chip-Select signal via the /CSRTC signal of the module (module pin 59(30A) at X1A).

Chip-Enable RTC-72423	J13
/CS1 of the address decoder	closed
external/CSRTC at module pin 59(30A) at X1A	open

- Internal Progamming-Mode of the C509

Jumper J14 is only relevant for modules fitted with the C509 controller. Connecting jumper pads 2+3 enables an optional programming mode for the C509, which can be activated per software. This exchanges XDATA and CODE memory areas and enables an application running from the RAM to program the Flash-Memory. This is facilitated by a special /WRF-signal, which writes to Flash. The design of the board, however, does not utilize this mode for programming the Flash-Memory. This is done via the FlashTools (refer to Sections *5* and the Quickstart-Instructions). Hence, it is recommended that J14 remain closed at 1+2.

Programming Mode - C509	J14
Deactivated	1+2
Activated	2+3

4 Memory Models

The miniMODUL-537/509 allows for flexible address decoding which can be adjusted by software to different memory models. A Hardware-RESET activates a default memory configuration that is suitable for a variety of applications. However, this memory model can be changed or adjusted at the beginning of a particular application.

Configuration of the memory is done within the address decoder by means of decoder internal registers: two control registers, one address register and one mask register. All named registers are carried out as Write-Only-Registers with access to the XDATA-memory of the controller. There are two distinct address areas - selectable by means of the bit IO-SW in control register 1 - by which the registers can be accessed (refer to the description of the bit IO-SW below). Due to a lack of read-access, a copy of all register contents should be maintained within the application. Reserved bits may not be changed during the writing of the register; contents must remain at 0. A Hardware-RESET erases all registers while preserving the configuration of the default memory.

Attention:
In the event that you use the FlashTools – PHYTEC's proprietary firmware allowing convenient on-board Flash-programming - the address FA16 is preset at the start of your application software. This is to be noted upon installation of the software copy of the register contents.

The following Figure displays the default memory model:

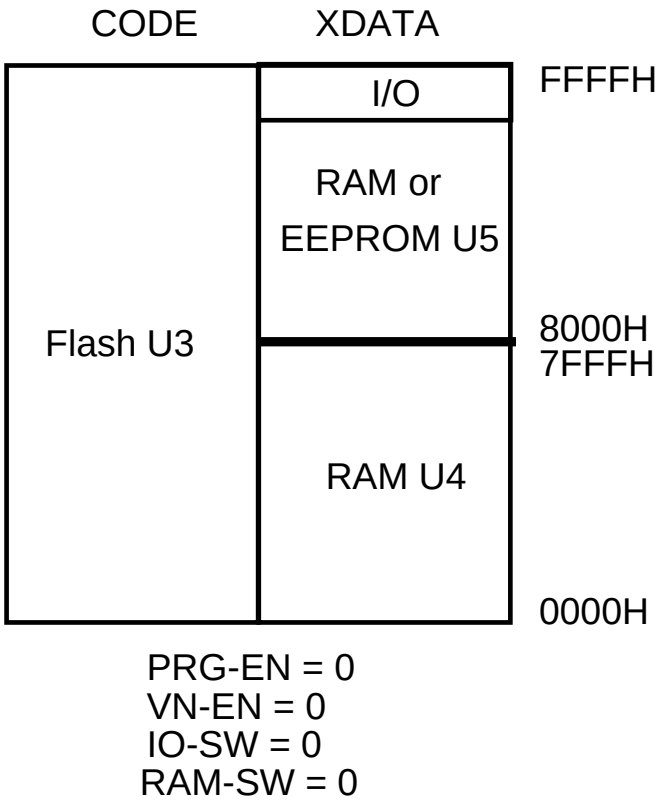


Figure 6: Default-memory model after Hardware-Reset

It should be noted that the memory block U4 and U5 comprise separate 32 kByte memory areas in the XDATA address-area of the controller. In the event that a 128 kByte RAM device is installed at U4, then blocks of 32 kByte can be accessed and switched via bank-latching. In the event that U4 and U5 are not populated by memory devices, then there is no possible access to the corresponding XDATA memories. The corresponding current I/O area is concentrated in an XDATA-address area in which there is no access to any existing RAM.

In the following sections the registers of the address decoder for configuration of the memory are explained:

4.1 Control Register 1

Control Register 1 (Address 7C00H / FC00H)							
Bit 7							Bit 0
PRG-EN	IO-SW	RAM-SW	VN-EN	FA18	FA17	FA16[1]	FA15

Bit invalid in programming-model (refer to PRG-EN)
Bit valid only in programming-model (refer to PRG-EN)

PRG-EN: Activates the special Flash-programming memory model (PRG-EN = 1). This configuration is used within the FlashTools[2] for Flash-programming. On account of existing restrictions it is either of no or of restricted use in your application.
In this model, 32 kByte Flash-Memory located within the address range 0000H - 7FFFH is accessible, as well as 32 kByte RAM within the range 8000H - FFFFH. The Flash-Memory can only be written in the XDATA-area and can only be read from the CODE-area. The RAM can be read and written in the XDATA-area. RAM can also be read from the CODE-area. The address line A15 of the Flash is derived from the Control Register 1 (Bit 0, FA15) only in the programming configuration. In the Run-time-configuration (PRG-EN = 0), the address line A15 of the controller leads directly to the Flash device.

1: In the event that you use the FlashTools - a firmware allowing convenient on-board Flash-programming - it should be noted that the Bit FA16 will be preset at the start of your application software. This is to be noted upon installation of the software copy of the register contents.

2: A firmware allowing convenient on-board Flash-programming, at purchase of the module including a Flash device this software is already installed in the Flash device.

The bits IO-SW and VN-EN is also relevant to the programming configuration; whereas the bit VN-EN is not relevant. The following Figure illustrates the programming configuration (the I/O-field is not represented):

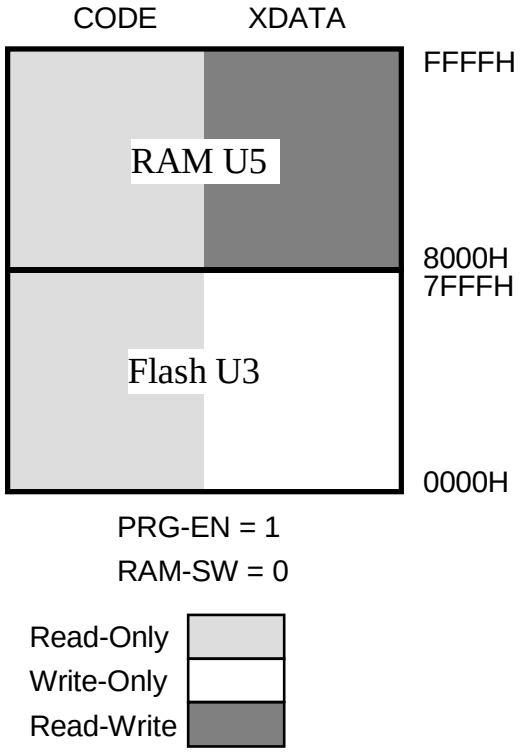
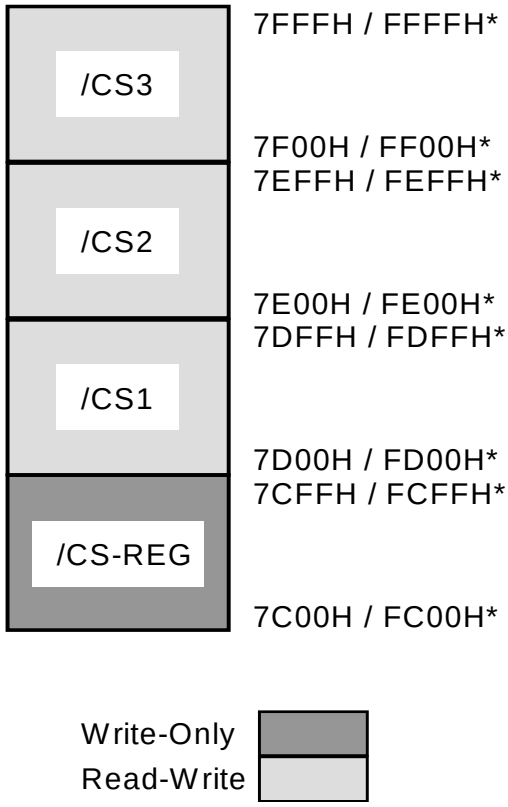


Figure 7: Memory model for Flash-Programming

IO-SW: By means of this bit, the I/O-area of the module can be selectively mapped either to the upper or to the lower 32 kByte of the address space. After a Hardware-Reset (IO-SW = 0) the I/O-area is located in the address area from FC00H to FFFFH. Following setting of the IO-SW-bit, the I/O-area is located in the address area from 7C00H to 7FFFH. This I/O-area generally consists of 4 blocks of 256 bytes each. In three of these blocks the address decoder provides a predecoded Chip-Select-Signal which simplifies the connection of peripheral hardware to the module.

This Chip-Select-Signals are activated by XDATA-access (Read-Write access) to the corresponding address area. The fourth block is reserved for accessing the register internal to the decoder (Write-Only access). Hence, this block is not available for connection of peripheral hardware to the module.
The following diagram illustrates the partitioning of the I/O-area:



* = Default-Setting

Figure 8: Partitioning of the I/O-Area

Given this partition, /CS1 through /CS3 function as the available free Chip Select Signals. The signal /CS-REG is solely a signal internal to the decoder, which is necessary in order to access the internal register. This latter signal is not available.

Connection of peripheral devices to the area of /CS-REG should not take place under any circumstances in order to maintain the correct function of the FlashTools[1] for programming of the Flash. The internal register is to occupy only the address ranges 7C00H - 7C03H and/or FC00H - FC03H. The rest of the /CS-REG block remains unused and is reserved for future expansion.

RAM-SW: This bit enables exchange of 32 kByte memory areas of the devices installed at U4 and U5. Following a hardware-reset (RAM-SW = 0) the RAM U4 is mirrored in the area from 0000H to 7FFFh and the RAM/EEPROM at U5 is addressable from 8000H to FFFH. After setting the RAM-SW bit, the RAM at U4 populates the area from 8000H-FFFFH. Likewise, the RAM/EEPROM U5 populates the area from 0000H-7FFFH. In the corresponding I/O areas, there is no access to the memory devices.

VN-EN: This bit enables free selection of von-Neumann memory[2] within the address space of the controller. A Reset renders a Harvard[3]-Architecture available as the default configuration. Von-Neumann memory is especially useful when programming code is to be downloaded and subsequently run during running time, as is the case with a Monitor program.
The location of the optional von-Neumann memory is defined through the address- and mask registers (see below).

1: Software-tools for on-board Flash-programming are pre-installed in the Flash device upon delivery.

2: Memory area in which no difference is made between CODE- and XDATA-access. This means that both accesses use the same physical memory device, usually a RAM.

3: Memory area in which CODE and XDATA-accesses use physical different memory devices. CODE-access typically uses a ROM or Flash device, whereas XDATA-access uses a RAM.

Following a hardware-reset (VN-EN = 0) the settings in the address- and mask registers are not released, which means that no von-Neumann-memory is available. After setting the bit (VN-EN = 1), the settings in the address- and mask registers are valid and incorporated in access addressing. This bit is only relevant in the Runtime-model (PRG-EN = 0). In the Programming-model (PRG-EN=1) it is unimportant and ignored.

FA[18..15]: The module can be equipped with an optional 512 kByte Flash-Memory. As the controller's address space is limited to 64 kByte, the remainder of the Flash-Memory can only be accessed by means of bank memory switching.
In the Runtime-model (PRG-EN = 0), 64 kByte banks can be switched by controlling the high address lines A[18..16] for the Flash through software. For this purpose, register bits FA[18..16] of the address decoder provide a Latch to which the desired higher addresses can be written.
Of particular note is the bit FA15, which is solely relevant in the programming-model (PRG-EN = 1). As in this model only 32 kByte of Flash can be accessed, it serves as address line A15 for the Flash-Memory. In the Runtime-model (PRG-EN = 0) with a 64 kByte Flash-Memory area, to contrast, the address line A15 of the controller is attached directly to the Flash.
The function of the bits FA[18..16] is dependent on the hardware configuration of the module and functions, as described above, only in connection with Flash devices of 512 kByte.

4.2 Control Register 2

Control Register 2 (Address 7C01H / FC01H)							
Bit 7							Bit 0
N/A[1]	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	RA16	RA15

RA16: The module can optionally accommodate a 128 kByte RAM device at U4. As the address space at U4 is limited to 32 kByte in the XDATA area of the controller, the remainder of the RAM can only be accessed by means of bank switching.
Four memory banks of 32 kByte banks can be switched by setting the high address-lines A[16..15] through software. For this purpose, register bit RA[16..15] of the address decoder provides a Latch to which the desired higher addresses can be written.
The function of this bit is dependent on the hardware configuration of the module and functions, as described above, only in connection with RAM devices of at least 128 kByte at U4.

[1]: N/A: Not Accessible

4.3 Address Register

The address register 7C02H / FC02H functions in conjunction with the mask register (see below) to define the von-Neumann[1]- and Harvard[2]-memory in the controller's addressing area. By setting the bit VN-EN in control register 1, the values of the address and the mask register become valid for the definition of the von-Neumann and the Harvard addressing space and incorporated in access addressing (refer to control register 1).
The location of one or more Harvard areas can be configured with both registers. The remaining sections of the addressing area is configured as von-Neumann area in which RAM is accessible through XDATA as well as through CODE.
The mechanism through which the areas are differentiated is based on a comparison of the current address with a predefined address pattern of variable width. If the relevant bit position of the addresses conform to one another, access occurs according to the Harvard-architecture. In the case of non-conformity, access occurs according to the von-Neumann-architecture.

Address Register (Address 7C02H / FC02H)							
Bit 7							Bit 0
HA15	HA14	HA13	HA12	HA11	HA10	*Res.*[3]	*Res.*

The address register holds the address pattern mentioned above. Each bit of the pattern is compared with the corresponding address line of the controller (HA15 with A15, ..., HA10 with A10). As address lines A15 .. A10 are used to define Harvard addressing space, only Harvard-fields of at least 1 kByte can be configured. Areas smaller than 1 kByte can not be configured.

1: Memory area in which no difference exists between CODE- and XDATA-access. This means that both accesses use the same physical memory device, usually a RAM.

2: Memory area in which CODE and XDATA-accesses use different physical memory devices, usually CODE-access uses a ROM or Flash device, whereas XDATA-access uses a RAM.

3: Reserved bits are not to be changed, the default value (0) must remain.

4.4 Mask Register

The mask register (addresses 7C03H / FC03H) serves the masking of single bits in the address register (see above). Following a hardware-reset, all bits within the address register are relevant. By setting the individual bits in the mask register, all corresponding bits in the address register will *no* longer be subject to an address comparison.

Mask Register (Address 7C03H / FC03H)							
Bit 7							Bit 0
MA15	MA14	MA13	MA12	MA11	MA10	*Res.*[1]	*Res.*

It is to be noted that in the case of a single 32 kByte RAM, the memory area is mirrored within the controller's addressing area. On account of the insufficient utilization of A15 in this configuration, memory accesses to addresses higher than 8000H are reduced to accesses to the memory area from 0000H to 7FFFH. This should be taken into consideration when choosing the memory model. Otherwise, function failure could result from overlapping access.

[1]: Reserved bits are not to be changed, the default value (0) must remain.

The following examples of different combinations of the address- and mask registers illustrate these functions (X=specific bit irrelevant):

Address-Reg.	Mask-Reg.	Comments (only for VN-EN = 1)	
1XXXXX00b	01111100b	Harvard Von-Neumann	8000H-FFFFH, 0000H-7FFFH
0XXXXX00b	01111100b	Harvard Von-Neumann	0000H-7FFFH, 8000H-FFFFH
11111100b	00000000b	Harvard Von-Neumann	FC00H-FFFFH, 0000H-FBFFH
010X0000b	00010000b	Harvard and Von-Neumann and	4000H-43FFH 5000H-53FFH, 0000H-3FFFH, 4400H-4FFFH 5400H-FFFFH
10000000b	00000000b	Harvard Von-Neumann and	8000H-83FFH, 0000H-7FFFH 8400H-FFFFH
10100X00b	00000100b	Harvard Von-Neumann and	A000H-A7FFH, 0000H-9FFFH A800H-FFFFH

Reserved bits without function for address decoding (refer to description of the register)

X = irrelevant (on account of a bit set in the mask register)

The last example in the Table is further illustrated by the following Figure:

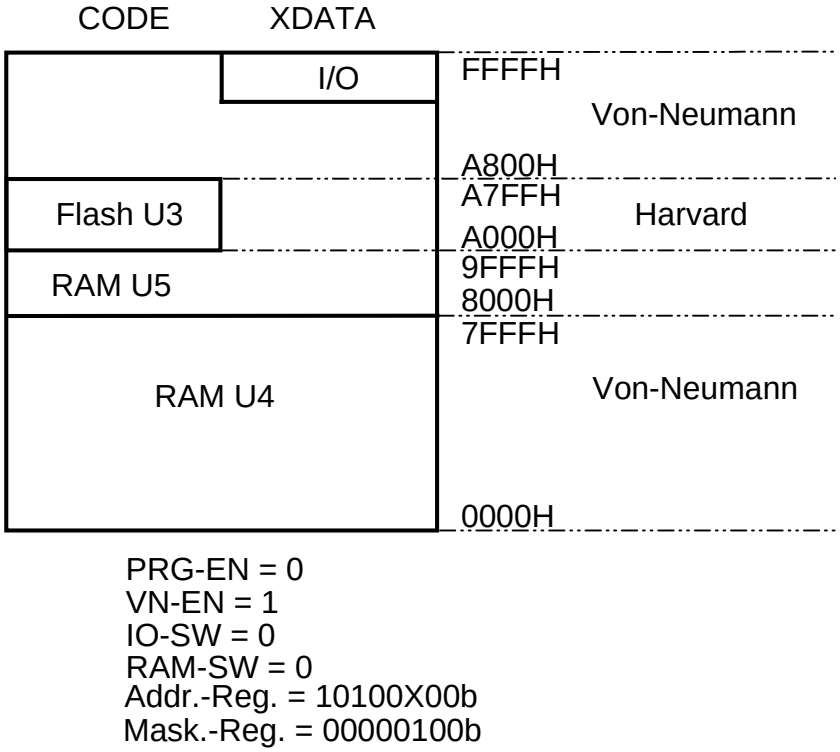


Figure 9: Example of a Memory model

5 Flash-Memory

Flash is a highly functional means of storing non-volatile data. Having the miniMODUL-537/509 equipped with a Flash device makes this modern technique available. The miniMODUL-537/509 can house a Flash device of type 29F010 with two banks of 64 kByte each or of type 29F040 with 8 banks of 64 kByte each.

Use of Flash devices allows incorporation of on-board programming capability. The Flash devices are programmable with 5V=. Consequently, no dedicated programming voltage is required. A firmware to programm the Flash device (the so-called FlashTools) is pre-installed in the first bank (bank 0) of the Flash device. Hence the total memory available is 64 kByte or 448 kByte (*refer to Figure 10*).

Attention:
Should this software be erased from the Flash device without having a back-up or an equivalent replacement, reprogramming is no longer possible!

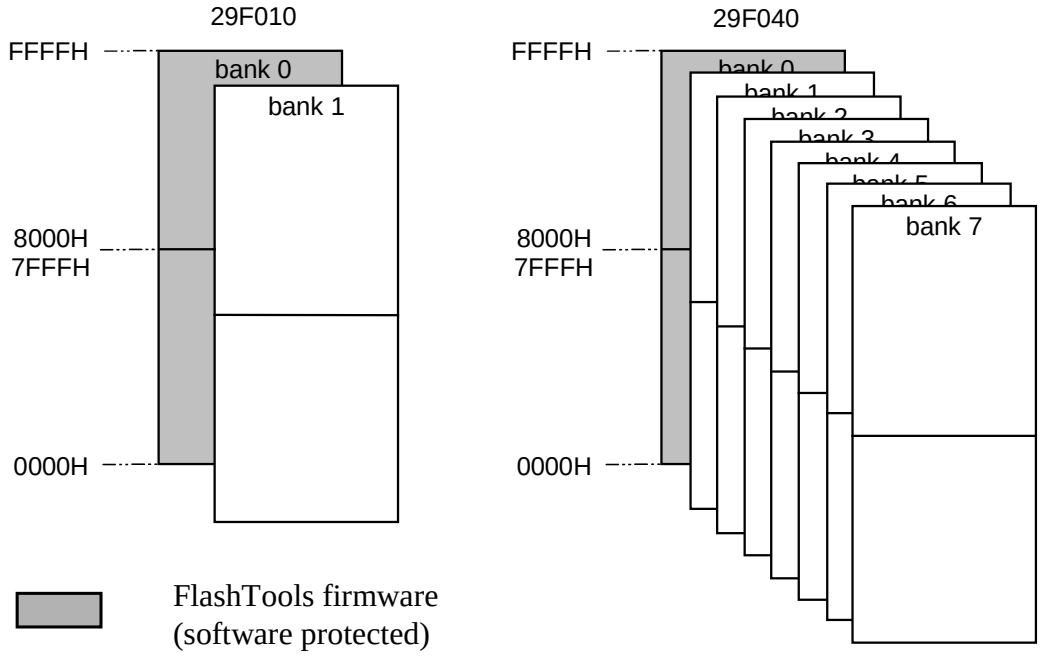


Figure 10: Memory Areas of the Flash Device

Please note that this firmware protects itself against any intentional or accidental erasure or copy-over. As the Flash device’s hardware protection mechanism is not utilized, protection is limited to the software level. In the event that you might wish to download your own programming algorithms or tools into the Flash, please ensure that a programming tool remains in the Flash-Memory. Refer to the “QuickStart Instructions" for a detailed description of the on-board programming.

Use of a Flash device as the only code memory results in no or only a limited usability of the Flash-Memory as non-volatile memory for data. This is due to the internal structure of the Flash device as, during the Flash-internal programming process, the reading of data from Flash is not possible. Hence, for Flash programming, program execution must be transferred out of Flash (such as into von-Neumann RAM). This usually equals the interruption of a "normal" program execution cycle.

As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 Erase-/Program-cycles.

6 The Battery Buffer

The battery which buffers the memory is not otherwise essential to the functioning of the miniMODUL-537/509. However, this battery buffer embodies an economical and practical means of storing nonvolatile data.

The VBAT-input (pin 42(21B) at X1A) is provided for connecting the external battery. As of the pressing of this manual, a lithium battery is recommended as it offers relatively high capacity at low discharge. In the event of a power failure at Vcc, the RAM memory blocks will be buffered by a connected battery via VBAT.

Attention:
The battery device on the miniMODUL-537/509 is not appropriate to supply an EEPROM if installed at U5. Therefore jumper J2 has to be closed at 1+2 in order to avoid fast discharge of the battery.

Power consumption depends on the components used and memory size. This is typically < 1 µA per 32 kByte RAM device installed on the miniMODUL.

For reasons of operating safety, please be advised that despite the battery buffer, changes in the data content within the RAM can occur given disturbances. The battery buffer does not completely remove the danger of data destruction.

7 Technical Specifications

The physical dimensions of the miniMODUL-537/509 are represented in *Figure 11*. The module's profile is ca. 10 mm. thick, with a maximum component height of 3 mm. on the back-side of the PCB and approximately 5 mm. on the front-side. The board itself is approximately 1.5 mm thick.

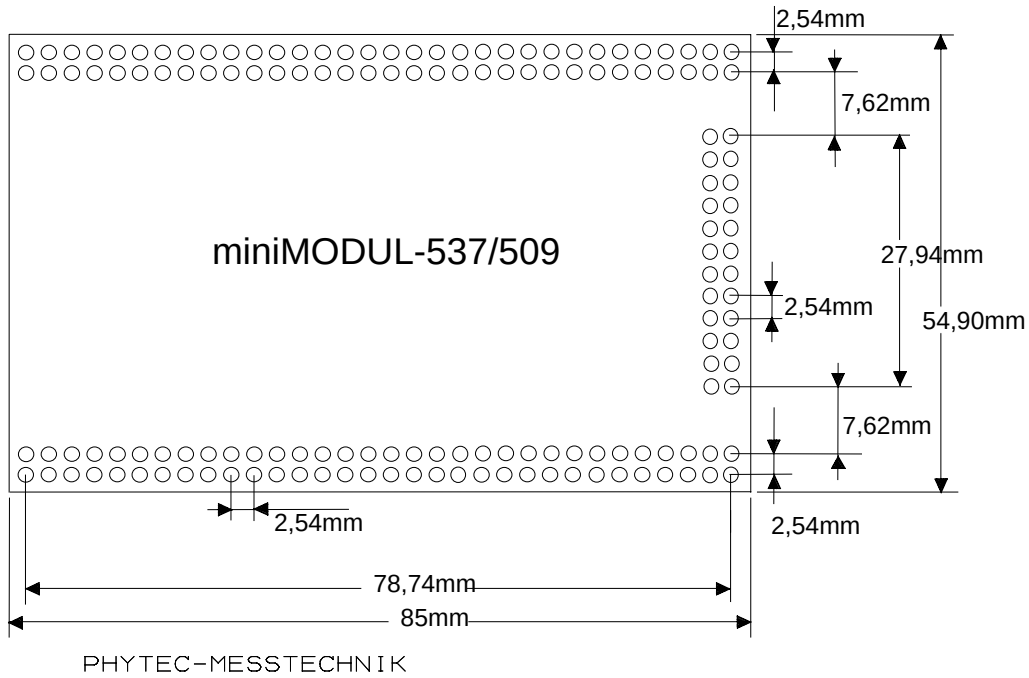


Figure 11: Physical Dimensions (not shown at scale)

Additional specifications:

- Dimensions: 54.9 x 85 mm., ±0,01mm
- Weight: approximately 32 g with 32 kByte RAM device, 128 kByte Flash device
- Storage temperature: -40°C to +90°C
- Operating temperature: standard 0°C to +70°C, extended -40°C to +85°C
- Humidity: maximum 95% r.F. not condensed
- Operating voltage: 5 V. ±5%, VBAT 3V ±20%
- Power consumption: maximum 140 mA, typ. 100 mA at 12 MHz oscillator frequency and 128 kByte RAM at +20°C
- Power consumption with battery buffer: maximum 10 µA per RAM-device, typically 1 µA per RAM-device at +20°C

These specifications describe the standard configuration of the miniMODUL-537/509 as of the pressing of this manual.

Please note that utilizing the battery buffer for the RAMs the storage temperature is only 0°C to +70°C.

8 Hints for Handling the Module

When changing controllers please ensure that appropriate PLCC extraction tools are used and that the socket and all components remain free from intrusive damage. It is also advisable to ensure that all insertable controllers are pin-compatible with the 80C32, and that all special hardware features are compatible with the layout of the board.

Removal of the standard quartz or oscillator is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remains undamaged while unsweating. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

9 Revision-History of miniMODUL-537/509

Due to the conversion to Flash-Memories, some changes appeared in regard to the specifications of the miniMODUL-537/509. PHYTEC tried to gain as much compatibility as possible but some differences are necessary. The Table below shows the differences in function and pinout and points out the interchangeability between the versions MM-101 ‘miniMODUL-537’ and MM-103 ‘miniMODUL-537/509’:

	miniMODUL-537 (old) (MM-101)	miniMODUL-537/509 (new) (MM-103)
Pin 1+2	VCC	No connection. Use Pins 65+66 only. (this improves radio interference behavior)
Pin 12	/OFF	/PSEP
Pin 13	BRES	/WRP
Pin 14	RES2	/RDP
Pin 35	/WDO	/CS1
Pin 36	/WRO	/CS2
Pin 37	/PWR	/CS3
Pin 40	/Low-Line	/HPD
Pin 58	ROM_A15	/RESP
Pin 60	STDP	/IRTC
Pin 63+64	GND	No connection. Use Pins 127+128 only. (this improves radio interference behavior)
Pin 91	B0	PRGEN
Pin 92	B1	No connection
Pin 93	RS-485 Vcc	DE
Pin 101	/XCERAM2	Port9.7 of C509
Pin 102	XRAM2	Port9.6 of C509
Pin 103	/XCERAM1	Port9.5 of C509
Pin 104	XRAM1	Port9.4 of C509
Pin 105	/XOEROM	Port9.3 of C509
Pin 106	XROM	Port9.2 of C509
Pin 107	/XCEROM	Port9.1 of C509
Pin 108	/	Port9.0 of C509
U3	suitable for OTPs/EPROMs with 32Kx8/64Kx8 in PLCC-/LCC-case	Suitable for Flash-Memories 29F010/29F040 with 128Kx8/512Kx8 or OTPs with 128Kx8 in PLCC-case

Table 2: Revisions

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Document number: **L-244e_4, June 1999**

How would you improve this manual?

Did you find any mistakes in this manual? page

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PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

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