OKI Semiconductor

FEDL86V7666-01
Issue Date: Apr. 21, 2004

ML86V7666

NTSC/PAL Digital Video Decoder

USES AND APPLICATION EXAMPLES

The ML86V7666 is an IC that can be used as an interface for video signal input of any digital video processing system. The device can be operated with a digital PLL line lock clock for applications where image quality is of utmost importance. Further, for application where sync speed is important, such as switching between multiple input channels, an asynchronous clock allows high-speed synchronous operation.

APPLICATION EXAMPLES

- TVs and TV reception equipment
  Panel TVs such as TFT/PDP, PC TVs, digital TVs, set top boxes for receiving TV broadcasts
- Video recording equipment
  DVD-R/W, HDD recorders, digital VTRs, digital video cameras, and digital cameras
- Monitoring systems
  Multi-display equipment, long-playing video recording equipment, and transmission equipment for remote monitoring
- PC peripheral equipment
  Video capture boards, video editing equipment, and internet monitoring cameras

GENERAL DESCRIPTION

The ML86V7666 is an LSI that converts NTSC or PAL analog video signals into the YCbCr standard digital format defined by ITU-R recommendations BT.601/BT.656 and RGB digital data.
The device has two built-in 10-bit A/D converter channels and can accept composite video and S-video signals as input.
The composite video signal is separated into a luminance signal and chrominance signals by a 2-dimensional Y/C separation filter (2-line or 3-line adaptive comb filter) and are then converted to a general-purpose video data format.
With 1/4, 1/9, and 1/16 screen scaling features, the ML86V7666 is compatible with interfaces for a wide variety of applications.
In addition to the asynchronous sampling that is a special feature of Oki decoders, video signals can also be sampled using digital PLL for line lock clock sampling.
With asynchronous sampling, high-speed locking is available for synchronization and color bursts.
Further, due to the built-in pixel position correction circuit and the FIFO for correcting the pixel count, the video jitter that can be a problem with asynchronous sampling is eliminated and jitter-free output data is ensured.

FEATURES

(●: New features not found in the MSM7664B; ◎: Improved/altered features)

Input Section

- ○ Accepts NTSC/PAL composite video signals and S-video signals
- ○ Maximum 5 composite or 2 S-video + 2 composite inputs can be connected
- ○ Built-in clamp circuits and video amps
- ● Built-in 10-bit A/D converters (2 channels)
- ● Switchable between line lock clock sampling mode and asynchronous sampling mode

○ Operation mode : pixel frequencies (sampling clock: normal/double-speed)
NTSC/PAL ITU-R BT.601 : 13.5 MHz (13.5/27 MHz)
NTSC Square Pixel : 12.272727 MHz (12.272727/24.545454 MHz)
NTSC 4fsc : 14.31818 MHz (14.31818/28.63636 MHz)
PAL Square Pixel : 14.75 MHz (14.75/29.5 MHz)

Digital Processing Section

◎ 2-dimensional Y/C separation using an adaptive comb filter (this filter is bypassed for S-video signal input)
NTSC/PAL system: 2-line or 3-line adaptive comb filter
◎ Recognition of data in the VBI period (closed caption, CGMS, WSS) and function of reading from I^2C-bus (detection possible in all operating modes)
○ Copy protection (e.g., macrovision AGC and color stripe) detection
● Capable of decoding specially standardized signals such as NTSC443 and PAL-NM
○ Built-in AGC/ACC circuits (automatic luminance level control/automatic color level control)
○ Automatic NTSC/PAL recognition (only in the 27MHz mode)

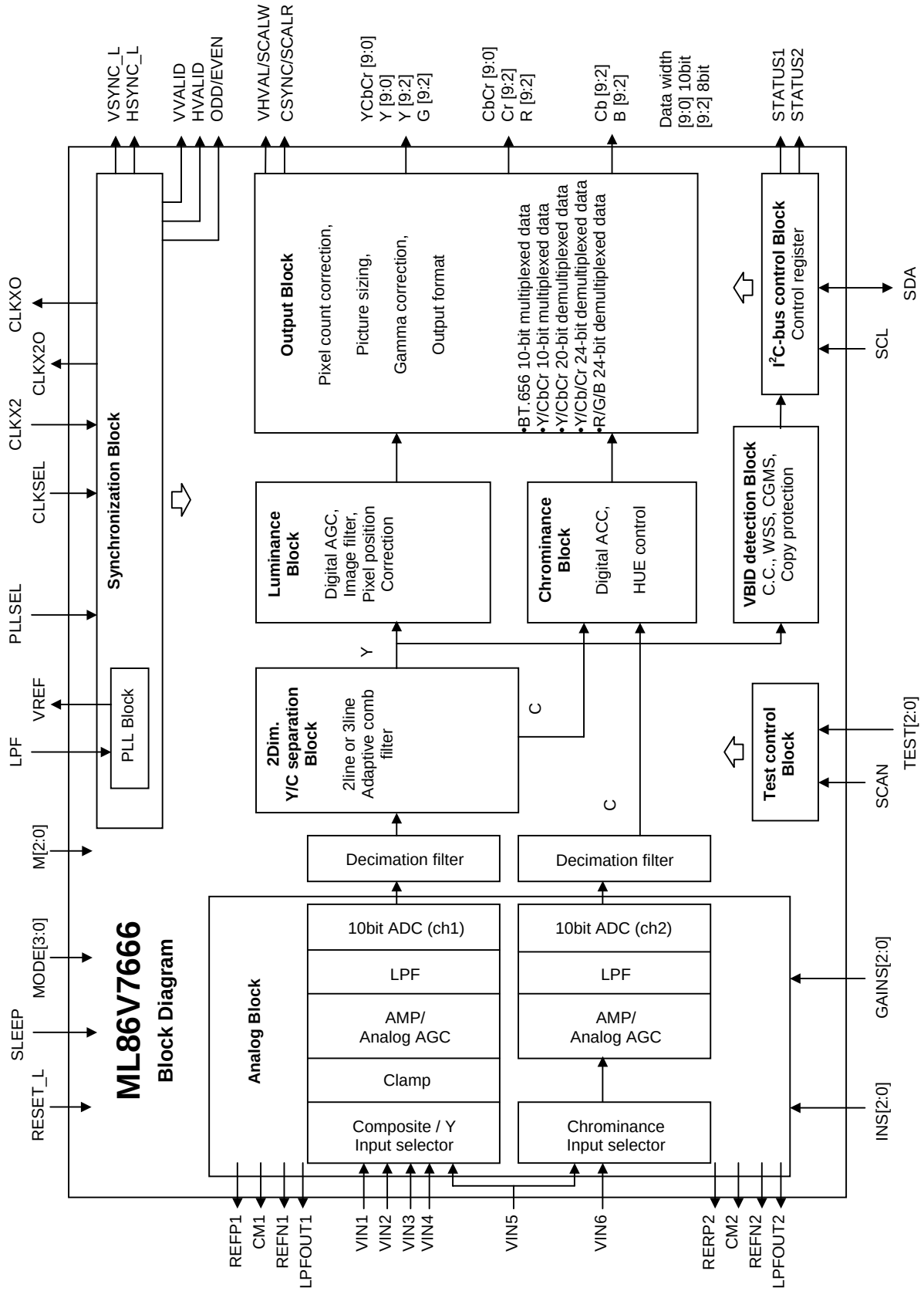
Output Section

◎ 5 selectable output interfaces
ITU-R BT.656-4 : 10-bit(Y/CbCr) multiplexed data With sync signals
10-bit Y/CbCr : 10-bit(Y/CbCr) multiplexed data YCbCr = 4:2:2 / YCbCr = 4:1:1
20-bit Y/CbCr : 10-bit (Y) + 10-bit (CbCr) demultiplexed data YCbCr = 4:2:2 / YCbCr = 4:1:1
24-bit RGB : 8-bit (R) + 8-bit (G) + 8-bit (B) demultiplexed data
24-bit component : 8-bit (Y) + 8-bit (Cb) + 8-bit (Cr) demultiplexed data
◎ Output pixel count correction function via internal FIFO
○ Automatic FIFO/FIFO-through switching feature
● Screen scaling feature (fixed sizes: 1/4, 1/9, 1/16 and QVGA)
● Gamma correction function (only RGB output mode)
○ Sleep mode
○ Output pin Hi-Z mode

Other Sections

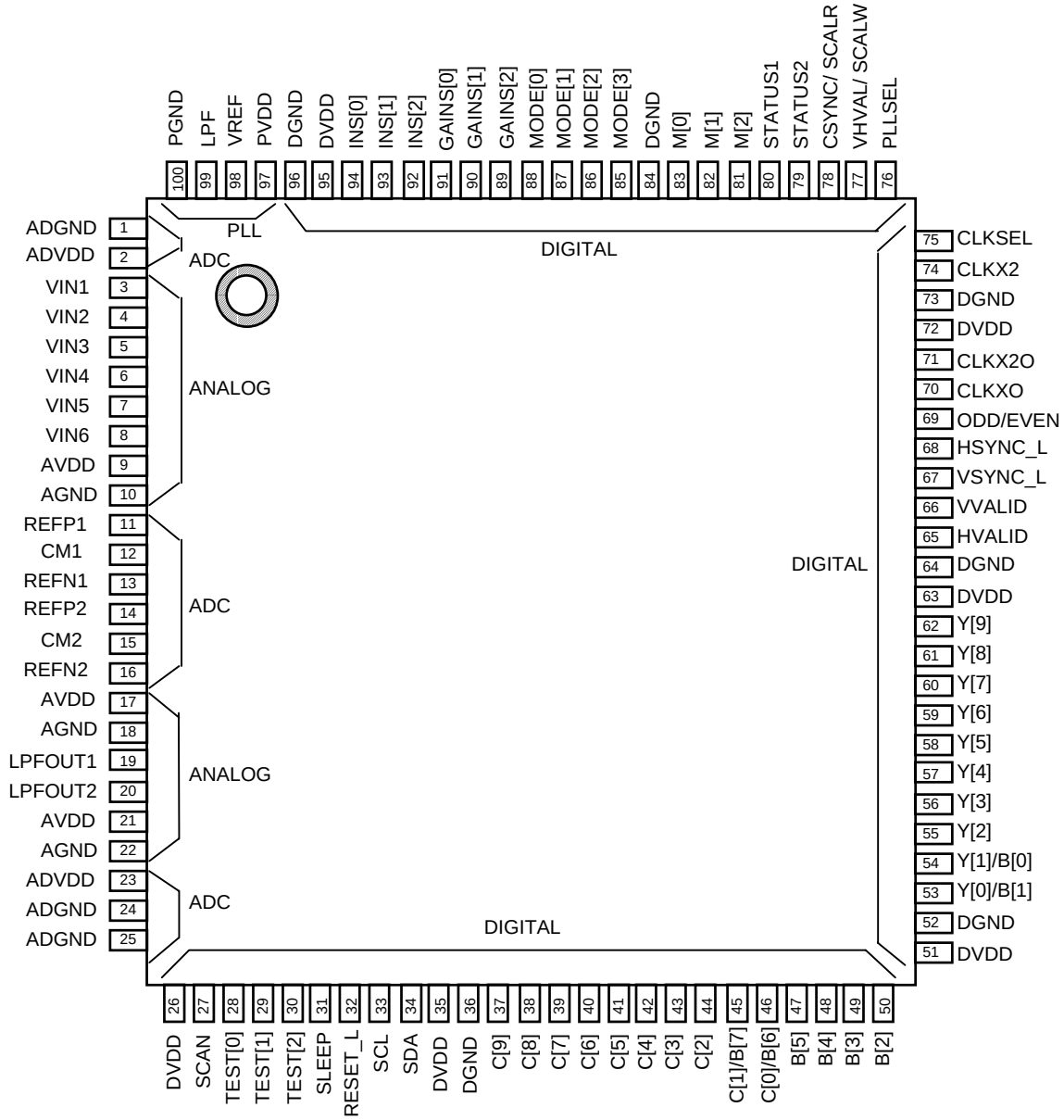
○ I^2C-bus interface
○ 3.3V single power supply (5V input tolerance)
○ Package: 100-pin plastic TQFP (TQFP100-P-1414-0.50-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

100-Pin Plastic TQFP (TQFP100-P-1414-0.50-K)



PIN DESCRIPTIONS

Attention: The input pin is not pull-down or pull-up in internal circuit.

Pin	Symbol	I/O	Description
1	ADGND	—	ADC ground
2	ADVDD	—	ADC power supply
3	VIN1	I	Composite-1 or S-video 1 luminance signal (Y-1) input Connect to AGND when not used.
4	VIN2	I	Composite-2 or S-video 2 luminance signal (Y-2) input Connect to AGND when not used.
5	VIN3	I	Composite-3 input Connect to AGND when not used.
6	VIN4	I	Composite-4 input Connect to AGND when not used.
7	VIN5	I	Composite-5 or S-video 1 chroma signal (C-1) input Connect to AGND when not used.
8	VIN6	I	S-video 2 chroma signal (C-2) input Connect to AGND when not used.
9	AVDD	—	Analog power supply
10	AGND	—	Analog ground
11	REFP1	O	Ch1 ADC reference voltage (high) Open
12	CM1	O	Ch1 ADC reference voltage (middle) Open
13	REFN1	O	Ch1 ADC reference voltage (low) Open
14	REFP2	O	Ch2 ADC reference voltage (high) Open
15	CM2	O	Ch2 ADC reference voltage (middle) Open
16	REFN2	O	Ch2 ADC reference voltage (low) Open
17	AVDD	—	Analog power supply
18	AGND	—	Analog ground
19	LPFOUT1	O	Not used. Open
20	LPFOUT2	O	Not used. Open
21	AVDD	—	Analog power supply
22	AGND	—	Analog ground
23	ADVDD	—	ADC power supply
24	ADGND	—	ADC ground
25	ADGND	—	ADC ground
26	DVDD	—	Digital power supply
27	SCAN	I	Not used. Fixed at "0".
28	TEST [0]	I	Not used. Fixed at "0".
29	TEST [1]	I	Not used. Fixed at "0".
30	TEST [2]	I	Not used. Fixed at "0".
31	SLEEP	I	Sleep signal input. 0: Normal operation, 1: Sleep operation The Input pin becomes ineffective at the sleep mode.
32	RESET_L	I	Reset signal input. 0: Reset, 1: Normal operation After powering ON, be sure to reset.
33	SCL	I	I^2C-bus clock input. "0" when not used.
34	SDA	I/O	I^2C-bus data I/O pin. External pull up at 4.7 kΩ. "0" when not used.
35	DVDD	—	Digital power supply
36	DGND	—	Digital ground
37 | 44	C [9] | C [2]	O	Data output C[9]:MSB - C[2] *) ITU-R BT.656 mode: Hi-Z 10-bit Y/CbCr mode: Hi-Z 20-bit Y/CbCr mode: CbCr upper 8-bit data output 24-bit RGB mode: R 8-bit data output 24-bit component mode: Cr 8-bit data output Add pins 45 and 46 in the 20-pin output mode. The output mode is set by pins 85 and 86, or register $00/MRA[7:6].

Pin	Symbol	I/O	Description
45 46	C[1]/B[7] C[0]/B[6]	O	Data output C[1]-C[0]LSB or B[7]MSB-B[6] *) ITU-R BT.656 mode: Hi-Z 10-bit Y/CbCr mode: Hi-Z 20-bit Y/CbCr mode: CbCr lower 2-bit output 24-bit RGB mode: B upper 2-bit output 24-bit component mode: Cb upper 2-bit output The output mode is set by pins 85 and 86, or register $00/MRA[7:6].
47 | 50	B [5] | B [2]	O	Data output B[5] - B[2] *) ITU-R BT.656 mode: Hi-Z 10-bit Y/CbCr mode: Hi-Z 20-bit Y/CbCr mode: Hi-Z 24-bit RGB mode: B intermediate 4-bit output 24-bit component mode: Cb intermediate 4-bit output For upper 2 bits, pins 45 and 46 are used, for lower 2 bits, pins 53 and 54 are used. The output mode is set by pins 85 and 86, or register $00/MRA[7:6].
51	DVDD	—	Digital power supply
52	DGND	—	Digital ground
53 54	Y [0]/B [1] Y [1]/B [0]	O	Data output Y[1]-Y[0]LSB or B[1]-B[0]LSB *) ITU-R BT.656 mode: YCbCr lower 2-bit data output 10-bit Y/CbCr mode: YCbCr lower 2-bit data output 20-bit Y/CbCr mode: Y lower 2-bit data output 24-bit RGB mode: B lower 2-bit data output 24-bit component mode: Cb lower 2-bit data output The output mode is set by pins 85 and 86, or register $00/MRA[7:6].
55 | 62	Y [2] | Y [9]	O	Data output Y[9]: MSB - Y[2] *) ITU-R BT.656 mode: YCbCr upper 8-bit data output 10-bit Y/CbCr mode: YCbCr upper 8-bit data output 20-bit Y/CbCr mode: Y upper 8-bit data output 24-bit RGB mode: G 8-bit data output 24-bit component mode: Y 8-bit data output When performing 10-bit output in BT.656 / (Y/CbCr) output mode, add pins 53 and 54. The output mode is set by pins 85 and 86, or register $00/MRA[7:6].
63	DVDD	—	Digital power supply
64	DGND	—	Digital ground
65	HVALID	O	Horizontal valid pixel timing signal output *) "H" is output for horizontal valid data section.
66	VVALID	O	Vertical valid line timing signal output *) "H" is output for vertical valid data section.
67	VSYNC_L	O	Vertical sync signal output (V sync) *)
68	HSYNC_L	O	Horizontal sync signal output (H sync) *)
69	ODD/EVEN	O	Field display output *) "H" is output for ODD field section.
70	CLKXO	O	Pixel clock output Double-speed clock mode (Pin 75 =0) One half of system clock frequency is output. Normal clock mode (Pin 75 = 1) The same frequency as system clock frequency is output.
71	CLKX2O	O	Operating clock output The same frequency as the Operating mode clock frequency is output.
72	DVDD	—	Digital power supply
73	DGND	—	Digital ground

Pin	Symbol	I/O	Description
74	CLKX2	I	System clock input Input a fixed clock or a PLL reference clock. Fixed clock (Pin 76 = 0) Operating mode / Normal clock (Pin 75 = 1) / Double-speed clock (Pin 75 = 0) NTSC ITU-R BT. 601: 13.5 MHz / 27 MHz NTSC Square Pixel: 12.272727 MHz / 24.545454 MHz NTSC 4Fsc: 14.31818 MHz / 28.63636 MHz PAL ITU-R BT. 601: 13.5 MHz / 27 MHz PAL Square Pixel: 14.75 MHz / 29.5 MHz PLL reference clock (Pin 76 = 1) Register $1F/PLLR[0] 0:32 MHz(default) 1: 25 MHz
75	CLKSEL	I	Double-speed clock select pin 0: Double-speed clock mode 1: Normal clock mode When the double-speed clock mode is set, input a doubled frequency to the system clock. When Pin 76 PLLSEL = 1 (PLL clock mode), set to 0 to select the double-speed clock mode.
76	PLLSEL	I	PLL clock select pin 0: Fixed clock 1: PLL clock
77	VHVAL /SCALW	O	Register $1A/SCR[7:6] = 00 (When scaling is not used.) VHVAL (VVALID ∧ HVALID) output Register $1A/SCR[7:6] = 01-11 (scaling mode) External memory writing control signal output Register $18/OMRD[5:4] = 01-11 (QVGA mode) QVGA clock is output.
78	CSYNC /SCALR	O	Register $1A/SCR[7:6] = 00 (When scaling is not used.) CSYNC (Composite SYNC) output Register $1A/SCR[7:6] = 01-11 (scaling mode) External memory read control signal output
79	STATUS2	O	Status signal output Selected by register $15/OMRA[0]. OMR[0]:0 NTSC-PAL recognition output (default) 0: NTSC 1: PAL OMR[0]:1 HLOCK sync detection output 0: Non-detection 1: Detection
80	STATUS1	O	Status signal output Selected by register $15/OMRA[1] OMR[1]: 0 FIFO overflow detection output (default) 0: Non-detection 1: Detection OMR[1]: 1 PLL sync detection output
81	M [2]	I	I2C-bus slave address select "0" when not used. 0: 1000 001X (X: 0 = Write, 1 = Read) 1: 1000 011X (X: 0 = Write, 1 = Reed)
82	M [1]	I	Amplifier gain setting and input pin switch setting control select pin 0: External pin mode Amplifier gain setting: Pins 89 to 91 GAINS[2:0] are used Input pin setting: Pins 92 to 94 INS[2:0]) are used 1: Register mode Amplifier gain setting: Register $1E/ADC2[6:4] Input pin setting: Register $1D/ADC1[2:0] The internal register setting is invalid when the external pin mode is set.
83	M [0]	I	Not used. Fixed at "0".
84	DGND	—	Digital ground

Pin	Symbol	I/O	Description
85 86	MODE [3] MODE [2]	I	Output mode external setting pins "0" when not used. Valid when register $00/MRA[0] = 0 (default). MODE [3:2] 00: ITU-R BT.656 (10-bit Y/CbCr + SAV, EAV, blank) 01: 10-bit Y/CbCr (10-bit Y/CbCr multiplexed data) 10: 20-bit Y/CbCr (10-bit Y + 10-bit CbCr demultiplexed data) 11: 24-bit RGB/YCbCr (RGB or YCbCr 8+8+8-bit demultiplexed data) Register $10/CHRCB[1] = 0: 24-bit RGB, 1: 24-bit YCbCr
87 88	MODE [1] MODE [0]	I	Operation mode external setting pins "0" when not used. Valid when register $00/MRA[0] = 0 (default). MODE [1] 0: NTSC, 1: PAL Invalid when register $02/MRC[7] = 1 (NTSC/PAL automatic recognition). MODE [0] 0: ITU-R BT. 601, 1: Square Pixel NTSC 4fsc can be set by register $00/MRA[5:3] only.
89 | 91	GAINS [2] | GAINS [0]	I	Amplifier gain external setting pins "0" when not used. Valid when external pin 82 M[1]=0. GAINS [2:0] Gain value (x times) [000] 0.55 [001] 0.70 [010] 0.93 [011] 1.21 [100] 1.60 [101] 2.09 [110] 2.65 [111] 3.45
92 | 94	INS [2] | INS [0]	I	Input pin switch external setting pins "0" when not used. Valid when external pin 82 M[1]=0. INS[2:0] Input pin [000] VIN1(Pin 3) Composite-1 [001] VIN2(Pin 4) Composite-2 [010] VIN3(Pin 5) Composite-3 [011] VIN4(Pin 6) Composite-4 [100] VIN5(Pin 7) Composite-5 [101] VIN1(Pin 3) Y-1 VIN5(Pin 7) C-1 [110] VIN2(Pin 4) Y-2 VIN6(Pin 8) C-2 [111] Prohibited setting (ADC enters sleep mode)
95	DV_{DD}	—	Digital power supply
96	DGND	—	Digital ground
97	PV_{DD}	—	PLL power supply
98	VREF	O	Center frequency setting pin "0" when not used.
99	LPF	I	Analog PLL loop filter connection pin "0" when not used. Refer to the sample circuits provided in the User's Manual.
100	PGND	—	PLL ground

*) Leave open when not used.
Connect a pull-up resistor in High-Z output mode .

FUNCTIONAL DESCRIPTION

This section explains the basic functions of the IC in terms of the blocks shown in the block diagram.
Refer to the User's manual for detailed explanations of the internal registers and any functions that are not covered in this data sheet.

Analog Section

The analog section inputs video signals. The analog section uses the video signal channel selector, AMP and 10-bit ADC to select the desired channel from among several video signals and convert the input to digital video data.

Analog input selector:

The analog input selector is compatible with composite signals and S-video signals. The maximum number of input connections is 5 channels of composite signals or 2 channels of S-video signals + 2 channels of composite signals. The selection of these input connections can be changed by external pins or by register controls using the I^2C-bus.

Related register: $1D/ADC1[2:0]

Analog Input Conditions

Input signal	Control pin	Register	Input pin						ADC operation	
	Pin 82 M[1]=0	Pin 82 M[1]=1								
	INS[2:0]	ADC1[2:0]	VIN1	VIN2	VIN3	VIN4	VIN5	VIN6	Y ADC	C ADC
Composite-1 input*	[000]	[000]*	Composite						ON	OFF
Composite-2 input	[001]	[001]		Composite					ON	OFF
Composite-3 input	[010]	[010]			Composite				ON	OFF
Composite-4 input	[011]	[011]				Composite			ON	OFF
Composite-5 input	[100]	[100]					Composite		ON	OFF
S-video-1 input	[101]	[101]	Luminance				Chroma		ON	ON
S-video-2 input	[110]	[110]		Luminance				Chroma	ON	ON
All inputs OFF	[111]	[111]	OFF (ADC sleep)						OFF	OFF

Blank spaces: Non-selectable; *: Register default setting after LSI reset

Clamp function:

The clamp fixes the video input signal in the ADC input range. Clamping is performed by sync chip clamp.

AMP/analog AGC function:

This function converts video input signals to the optimum level for the ADC using the analog AMP of the AGC function. The AGC function has an output level adjust function in the luminance block of the digital section in addition to the AMP input level adjust function. Manual setting of the AMP gain is also possible.

Related register: $1E/ADC2

Analog AMP Manual Gain Control

82-pin M[1] = 0	82-pin M[1] = 1	Gain setting value Typical value (multiplication factor)
Gain setting pin GAINS[2:0]	Register $1E/ADC2[6:4]	
[000]	[000]	0.55
[001]	[001]	0.70
[010]	[010]*	0.93
[011]	[011]	1.21
[100]	[100]	1.60
[101]	[101]	2.09
[110]	[110]	2.65
[111]	[111]	3.45

82-pin M[1] pin = "0": External pin analog gain setting mode
"1": Internal register analog gain setting mode

A/D converter:

This 10-bit A/D converter (ADC) converts analog video signals to digital video data. There are 2 channels built into the ADC. Sampling is performed at the pixel frequency or double-speed. In the S-video input mode, both channels of the A/D converter operate; in the composite input mode, only one channel operates, and the A/D converter on the chrominance signal input side goes OFF.

Related registers: $00/MRA, $1D/ADC1

Digital Section

The digital section separates the video data digitized by the ADC into Y and C data, converts these data to various data formats and outputs them. The digital section also performs output level adjustment, image quality adjustment and various corrections.

Decimation filter:

The decimation filter is used in the double-speed sampling mode. Because internal processing is performed at single speed also in the double-speed sampling mode, this filter is needed to reduce the data that has been doubled by one-half. Using the decimation filter after double-speed sampling reduces high-frequency noise and makes it possible to obtain data with a good high-frequency characteristic.

Related register: $02/MRC[4]

2-dimensional Y/C separation block:

This block separates composite data into Y (luminance) data and C (chrominance) data. For S pin input, Y/C separation circuit is bypassed.

• 2-Dimensional Y/C Separation Function

With the Y/C separation filter, composite data is separated into Y (luminance) data and C (chrominance) data. There are various Y/C separation filters available, which can be selected in an internal register.

Related register: $01/MRB

$01/MRB[5:3]	NTSC Y/C separation	PAL Y/C separation
*000	2-line/3-line adaptive comb filter	2-line comb/trap adaptive transition filter
001	3-line comb filter	2-line comb filter
010	Trap filter	Trap filter
011	3-line comb/trap adaptive filter	Undefined
100	3-line comb/trap adaptive filter 2	Undefined
101	2-line/3-line adaptive transition filter	Undefined
110	Undefined	Undefined
111	Undefined	2-line/3-line adaptive comb filter

• Special Broadcast Standards Decoder Function

In addition to normal NTSC/PAL signals, this decoder can decode the following specialized signals.
Set register $01/MRB[5:3] to ”010”, ”011”, “100”, or “111” when using the PAL M,N mode.

Related register: MRA[2:1] $00
MRA[2:1] = 00 Normal mode *
MRA[2:1] = 01 NTSC443
MRA[2:1] = 10 PAL M, N
MRA[2:1] = 11 Undefined

Luminance block:

The luminance block removes sync signals from the luminance data after Y/C separation, and performs adjustments such as luminance level adjustment and luminance image quality correction and adjustment. The digital decoded data that is output conforms with ITU-R BT601.

• Pixel Position Correction Function
This function corrects sampling error in asynchronous sampling and loss of PLL synchronization. Error correction is made in the horizontal direction, which improves vertical line jitter on the screen.
Related register: $02/ MRC[6]

• Digital AGC Function
This function adjusts the output level of luminance signals. Adjustment is automatically performed by the digital AGC (Auto Gain Control), but the adjustment can also be set manually by using an internal register to set digital MGC (Manual Gain Control). In the digital AGC mode, the sync level is compared with a reference value to determine the amplification rate of the luminance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted in an internal register. In the digital MGC mode, the signal amplification rate and the black level are adjusted with register settings. The black level is adjusted by means of pedestal level adjustment (register $0E/SSEPL[7] = "1").

Regarding the AGC function, in addition to the output level adjust function in the digital section, the input level adjust function of the AMP in the analog section also operate independently.
Related registers: $0B/AGCL, $0C/AGCRC, $0E/SSEPL, $0D/CLC

• Image Quality Adjustment
The following image filters are provided for adjusting luminance image quality.
Refer to the User's Manual for the characteristics of each filter.
Edge enhancement pre-filter
This pre-filter enhances the edges of luminance component signals; the pre-filter and the sharp filter operate at the same time.
Related register: $0A/LUMC[7]
Aperture bandpass filter and coring filter for contour compensation
Adjustment is made through a combination of the following registers:
Aperture bandpass filter coefficient setting
Related register: $0A/LUMC[6:5]
Coring range setting
Related register: $0A/LUMC[4:3]
Aperture weighting coefficient setting
Related register: $0A/LUMC[2:0]

Chrominance block:
This block decodes chroma data to Cb/Cr data and performs level adjustment and color adjustment. To eliminate unnecessary bands, this block first passes data through a bandpass filter (bypass is possible) and then through an ACC correction circuit to maintain a stable chroma level, before performing UV decoding. The result of the UV decoding is passed through a low-pass filter and output as a chrominance signal.
Related registers: $0F/CHRCA, $10/CHRCB

• Digital ACC Function
The digital ACC is the gain adjustment for the chrominance signal output level. Adjustment is automatically performed by the digital ACC (Auto Chrominance Control), but the adjustment can also be set manually by using an internal register to set digital MCC (Manual Chrominance Control). In the digital ACC mode, the burst level is compared with a reference value to determine the amplification rate of the chrominance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted in an internal register. Separate U/V level adjustment is also possible.
Related registers: $0F/CHRCA, $11/ACCC, $12/ACCRC

• Hue Adjust Function
Hues can be adjusted in the HUE register.
Related register: $13/HUE

Output block:
The output block performs output timing adjustment, picture sizing, output format conversion, and other types of output conversion.

• Pixel Count Correction Function
This function uses the internal FIFO to correct the total number of pixels in a line. It corrects the 1-line sampling error generated when in asynchronous sampling mode or PLL synchronization is lost, and fixes the pixel count for a line within the active screen. Refer to **Active Pixel Timing** for more on the pixel count for one line.
Related registers: $03/MRD[7:6], $16/OMRB

In the FIFO mode, register $03/MRD[7:6] can be set to bypass the FIFO.

MRD[7:6] = 00: FIFO-1 mode * (default)
Uses the internal FIFO to output data with the pixel count for 1H in the active screen as the reference value.

MRD[7:6] = 01: FIFO-2 mode *
Uses the internal FIFO to set and output the pixel count per 1H as the reference value. The internal processing method is different from the FIFO-1 mode. This mode is effective for non-standard signals.

MRD[7:6] = 10: FIFO through mode
This mode does not use the internal FIFO for pixel count correction, but outputs the decoded input signal as it is.

MRD[7:6] = 11: Undefined

• Scaling Function
This function shrinks the screen (fixed value).

Scaling
This function converts the input image to 1/4, 1/9, or 1/16 size for output.
Field memory control signals (pin 77 SCALW and pin 78 SCALR) are provided, so in connection with the Oki 4M-FIFO, a sub-screen can be output at any location on the screen.
Related registers: $1A/SCR, $1B/SCVPR, and $1C/SCHPR

QVGA output
This function performs QVGA conversion where the operating clock was used in the Square Pixel mode.
QVGA data is output by decimating the pixels.
Related register: $18/OMRD

• Gamma Correction Function
This function, which is only effective for RGB output, corrects gamma as part of the correction of monitor characteristics.
Five stages can be selected in an internal register.
Related register: $18/OMRD

• Output Format Conversion Function
This function converts the output data to the desired output format.
The following output formats are possible.
Related registers: $00/MRA, $02/MRC, $03/MRD, $10/CHRCB, $18/OMRD, and $1A/SCR

Output Formats

Output mode (i): interlace	Register $00/MRA[0]=0	Register $00/MRA[0]=1	Register	
	Control pin (Pins 85, 86)	Register		
	MODE[3:2]	$00/MRA[7:6]	$02/MRC[5]	$10/CHRCB[1]
ITU-R BT.656 (i) 4:2:2	[00]	[00]	0	0
Y/CbCr 10-bit multiplex (i) 4:2:2	[01]	[01]	0	0
Y/CbCr 20-bit de-multiplex (i) 4:2:2	[10]	[10]	0	0
Y/CbCr 20-bit de-multiplex (i) 4:1:1	[10]	[10]	1	0
RGB-24bit de-multiplex (i) 4:4:4	[11]	[11]	0	0
not use	[11]	[11]	0	0
Component (YCbCr) 24-bit de-multiplex (i) 4:4:4	[11]	[11]	0	1
not use	[11]	[11]	0	1

• Synchronization Block

This block controls the sync signals for internal operation, output sync signals, and the timing for each block. Synchronization detection levels, output timing, and various other functions can be adjusted by the registers listed below.

Related registers: $03/MRD, $04/SYDR, $06/STHR, $07/HSDL, $08/HVALT, $09/VVALT, $0F/CHRCA, $10/CHRCB, $14/BBHC, $15/OMRA, $17/OMRC, and $18/OMRD

PLL Function

The digital PLL circuit generates an operating clock synchronized with the horizontal sync signals of the video signals. With the input of a 25 MHz or 32 MHz standard clock, the double-speed sampling clock for each mode is provided as a line lock clock and used as the system clock.

The asynchronous sampling mode, which uses an asynchronous clock directly, can be used without using PLL.

Related registers: $17/OMRC, $1F/PLLR

Input Clock Settings

<table>
<tr><th>76pin
PLLSEL</th><th colspan="2">Input clock</th><th>Sampling clock</th></tr>
<tr><td>PLLSEL=0
Fixed clock mode</td><td colspan="2">Sampling clock input according to the operating mode
(See the table below)</td><td>Asynchronous clock</td></tr>
<tr><td rowspan="2">PLLSEL=1
PLL clock mode</td><td rowspan="2">$1F/ PLLR[0]=0*
32 MHz</td><td rowspan="2">$1F/ PLLR[0]=1
25 MHz</td><td>$1F/ PLLR[7]=0*
PLL ON
Line lock clock</td></tr>
<tr><td>$1F/ PLLR[7]=1
PLL OFF
Asynchronous clock</td></tr>
</table>

*: Default

In the PLL clock mode, a double-speed line lock clock is generated by setting the operating mode.

Operating Modes / Sampling Clock Settings

Operating mode	MRA[0] = 0 *	MRA[0] = 1	Sampling clock (double-speed/normal)	
	Control pin (pin 87 or 88)	Register		
	MODE[1:0]	MRA[5:3]	75-pin CLKSEL=0	75-pin CLKSEL=1
NTSC ITU-R BT.601 13.5 MHz	[00]	[000]	27 MHz	13.5 MHz
NTSC Square pixel 12.272727 MHz	[01]	[001] *	24.545454 MHz	12.272727 MHz
NTSC 4fsc 14.31818 MHz	—	[010]	28.63636 MHz	14.31818 MHz
—	—	[011]	—	—
PAL ITU-R BT.601 13.5 MHz	[10]	[100]	27 MHz	13.5 MHz
PAL Square pixel 14.75 MHz	[11]	[101]	29.5 MHz	14.75 MHz
—	—	[110]	—	—
—	—	[111]	—	—

— : Not used *: Default

VBID detection block:
This block detects data information and copy protection information from the VBI (Vertical Blanking Interval) of the input luminance signals. The following four types of VBID data can be detected, and the detection line and detection level can be changed by altering register settings.
*Note: VBID detection may not provide 100% detection, depending on the signal status.

VBID Detection Function

(1) AGC copy protection
Detects whether specified lines include a macrovision AGC pulse (NTSC/PAL) and sets a flag.
Related registers: $24/AGCD1, $25/AGCD2, $27/AIREG, $29/VFLAG

(2) C. C. (Closed Caption)
Detects whether specified lines include closed caption data (NTSC/PAL), keeps separately the data of even and odd lines, and sets individual flags.
Related registers: $20/CCD1, $21/CCD2, $27/AIREG, $29/VFLAG, $2A/CCDO0, $2B/CCDO1, $2C/CCDE0, and $2D/CCDE1

(3) WSS (Wide Screen Signaling)
Detects the WSS data in the lines specified by ETSC and sets a flag (PAL only).
Related registers: $26/WSSD, $27/AIREG, $29/VFLAG, $34/WSSD0, $35/WSSD1

(4) CGMS (Copy Generation Management System)
Detects the CGMS data in the lines specified by IEC61880 and sets a flag (NTSC only).
Related registers: $22/CGMS1, $23/CGMS2, $27/AIREG, $29/VFLAG, $2E/CGMSO0, $2F/CGMSO1, $30/CGMSO2, $31/CGMSE0, $32/CGMSE1, $33/CGMSE2

(5) Other copy protection detection functions
Detects the color stripes, false pulses, and MV protection and sets flags.
Related registers: $27/AIREG, $28/STATUS, $29/VFLAG

I^2C-bus control block:
This serial interface block is based on the I^2C standard of the Phillips Corporation. The registers at up to subaddress 27h are write/read, while the registers from 28h on are read-only.

Normally, a license from the Phillips Corporation allowing the use of its I^2C patent is required to use an I^2C bus. However, the license to use this LSI chip as a slave is granted by the Phillips Corporation upon purchasing this LSI chip. There is no need for a license if the decoder is used alone, without I##2C control, but if this I##2C-bus is used to control this LSI, a license for use as a master is required.

As of 2001, the I^2C patent expired in Japan and the rest of the Asian region, so there have been no costs with regard to license fees. However, in the USA and Canada, there is still a requirement for the payment of license fees, so if this product is intended for overseas trade, it may be necessary to pay the Phillips Corporation license fees for the use of its patent. For more information, contact the Phillips Corporation.

Test control block:
This block is used to test the LSI chip. It is not intended for user use.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to 4.5	V
Input voltage	Vi	V_{DD} = 3.3 V	–0.3 to 5.5	V
Power consumption	Pw	—	1	W
Storage temperature	Tstr	—	–55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	—	3.0	3.3	3.6	V
Power supply voltage	GND	—	—	0	—	V
Analog video signal input	Vain	SYNC tip to white peak level	0.8		1.1	Vp-p
Operating temperature (*)	Ta	—	-40	—	85	°C

(*): The Operating temperature is the ambient temperature.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = -40 to +85°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.0 V to 3.6 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level input voltage (*3)	Vih1	—	2.2	—	V_{DD}(*2)	V
	Vih2 (*1)	—	0.8 V_{DD}	—	V_{DD}(*2)	V
"L" level input voltage (*3)	Vil	—	0	—	0.8	V
"H" level output voltage	Voh	Ioh = –4 mA (*4)	0.7 V_{DD}	—	V_{DD}	V
		Ioh = –8 mA (*5)				
"L" level output voltage	Vol	Iol = 4mA (*4)	0	—	0.6	V
		Iol = 8 mA (*5)				
Input leakage current	Ii	Vi = GND to V_{DD}	–10	—	10	μA
Output leakage current	Io	Vi = GND to V_{DD}	–10	—	10	μA
Analog input	Avin	C Coupling	0.4	—	1.3	Vp-p

*1. SDA, CLKX2
*2. The inputs have a tolerance of 5V, so applying 5V to the inputs will not cause a problem.
*3. The input pins are not pulled down internally, so they should not be left open; at either a “L” or a “H” level.
*4: Y[9:0],C[9:0],B[5:2],HSYNC_L, VSYNC_L, SYSSEL, ODD, VVALID, HVALID, CLKXO, STATUS1, STATUS2, SCALW, SCALR, SDA, SCL
*5: CLKX2O

Current Characteristics

(Ta = -40 to +85°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.0 V to 3.6 V, GND = 0 V)

Parameter	Symbol	Condition	Operating clock	Min. V_{DD} = 3.0 V	Typ. V_{DD} = 3.3 V	Max. V_{DD} = 3.6 V	Unit
Digital power supply current (DV_{DD}) 1 channel operating	I_{DD1}	PLL Mode CLKX2 = 32 MHz AD1 on AD2 off	24.545454 MHz	75	105	155	mA
			27 MHz	80	110	160	
			28.63636 MHz	85	115	165	
			29.5 MHz	85	120	170	
Analog power supply current (AV_{DD} + ADV_{DD}) 1 channel operating	I_{DA1}		24.545454 MHz	30	45	65	mA
			27 MHz				
			28.63636 MHz				
			29.5 MHz				
Digital power supply current (DV_{DD}) 2 channel operating	I_{DD2}	PLL Mode CLKX2 = 32 MHz AD1 on AD2 on	24.545454 MHz	70	95	145	mA
			27 MHz	75	100	150	
			28.63636 MHz	80	105	155	
			29.5 MHz	85	110	160	
Analog power supply current (AV_{DD} + ADV_{DD}) 2 channel operating	I_{DA2}		24.545454 MHz	55	75	95	mA
			27 MHz				
			28.63636 MHz				
			29.5 MHz				
Digital power supply current (DV_{DD}) 1 channel operating	I_{DD1}	Fixed Clock Mode AD1 on AD2 off	24.545454 MHz	70	95	150	mA
			27 MHz	75	100	155	
			28.63636 MHz	80	105	160	
			29.5 MHz	80	110	165	
Analog power supply current (AV_{DD} + ADV_{DD}) 1 channel operating	I_{DA1}		24.545454 MHz	30	45	65	mA
			27 MHz				
			28.63636 MHz				
			29.5 MHz				
Digital power supply current (DV_{DD}) 2 channel operating	I_{DD2}	Fixed Clock Mode AD1 on AD2 on	24.545454 MHz	65	90	140	mA
			27 MHz	70	95	145	
			28.63636 MHz	75	100	150	
			29.5 MHz	80	105	155	
Analog power supply current (AV_{DD} + ADV_{DD}) 2 channel operating	I_{DA2}		24.545454 MHz	55	75	95	mA
			27 MHz				
			28.63636 MHz				
			29.5 MHz				
Power supply current (inactive)	I_{Doff}	Vi = 1.5 V		—	—	20	mA

AC Characteristics (Double-Speed Mode)

(Ta = -40 to +85°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) = 3.0 V to 3.6 V, GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Cycle Frequency	1/tclkx2	ITU-RBT601	—	27.0	—	MHz
		NTSC 4Fsc	—	28.63636	—	MHz
		NTSC Square Pixel	—	24.545454	—	MHz
		PAL Square Pixel	—	29.5	—	MHz
Input Frequency Tolerance (**)	—	—	—	—	±100	ppm
CLKX2 Duty	td_d2	—	45	—	55	%
CLKX2 Rise/Fall Time	tr, tf	CLKSEL:L	—	—	5	ns
Output Data Delay Time 1(*)	tod21	CLKSEL:L	7	—	24	ns
Output Data Delay Time 2(*)	tod22	CLKSEL:L	7	—	22	ns
Output Data Delay Time 3(*)	tod23	CLKSEL:L	5	—	25	ns
Output Data Delay Time 1x1(*)	todx21	CLKSEL:L	1	—	10	ns
Output Data Delay Time 1x2(*)	todx22	CLKSEL:L	1	—	8	ns
Output Data Delay Time 1x3(*)	todx23	CLKSEL:L	1	—	12	ns
Output Data Delay Time 2x1(*)	tod2x21	CLKSEL:L	1	—	9	ns
Output Data Delay Time 2x2(*)	tod2x22	CLKSEL:L	1	—	8	ns
Output Data Delay Time 2x3(*)	tod2x23	CLKSEL:L	1	—	11	ns
Output Clock Delay Time (*) (CLKX2-CLKXO)	tcxd21	CLKSEL:L	4	—	17	ns
Output Clock Delay Time (*) (CLKX2-CLKX2O)	tcxd22	CLKSEL:L	4	—	16	ns
SCL Clock Cycle Time	tc_scl	pull up = 4.7kΩ	200	—	—	ns
Low Level Cycle	tl_scl	pull up = 4.7kΩ	100	—	—	ns
RESET_L width	rst_w		200	—	—	ns

(*) Output load: 40 pF

(**) Use accuracy of ± 50 ppm when emphasizing characteristics such as vector waveforms. If ± 100 ppm is used, jitter will increase in the vector waveform as accuracy deteriorates due to the thermal characteristic.

Values in parentheses indicate the delay time when 8-bit YCbCr format data is output from the Y pin.

AC Characteristics (Single-Speed Mode)

(Ta = -40 to +85°C, V_{DD} (DV_{DD}, ADV_{DD}, AV_{DD}) =3 .0 V to 3.6 V, GND = 0 V)

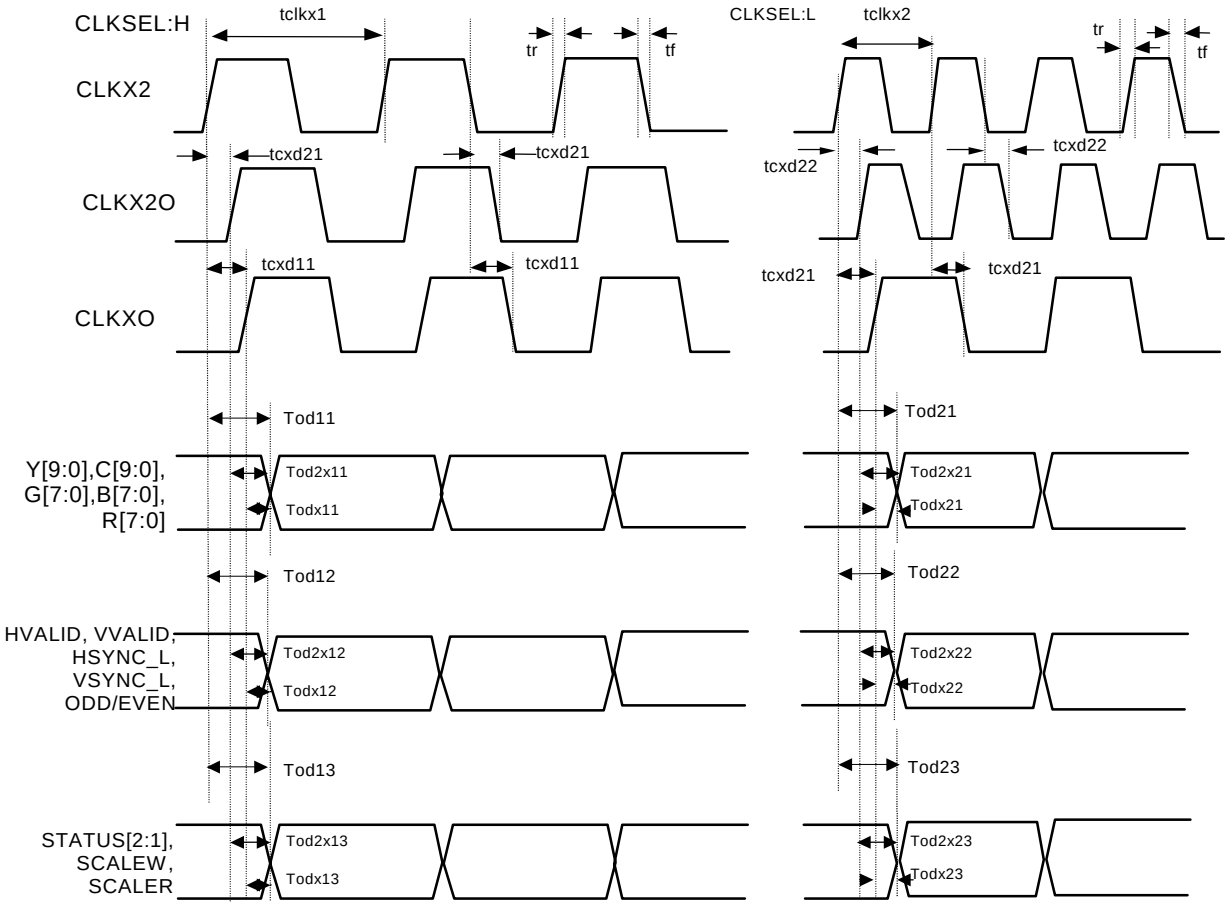
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Cycle Frequency	1/tclk x 2	ITU-RBT601	—	13.5	—	MHz
		NTSC 4Fsc	—	14.31818	—	MHz
		NTSC Square Pixel	—	12.272727	—	MHz
		PAL Square Pixel	—	14.75	—	MHz
Input Frequency Tolerance (**)	—	—	—	—	±100	ppm
CLKX2 Duty	td_d1	CLKSEL:H	40		60	%
CLKX2 Rise/Fall Time	tr, tf	CLKSEL:H	—	—	5	ns
Output Data Delay Time 1(*)	tod11	CLKSEL:H	7	—	24	ns
Output Data Delay Time 2(*)	tod12	CLKSEL:H	7	—	22	ns
Output Data Delay Time 3(*)	tod13	CLKSEL:H	5	—	25	ns
Output Data Delay Time 1x1(*)	todx11	CLKSEL:H	1	—	10	ns
Output Data Delay Time 1x2(*)	todx12	CLKSEL:H	1	—	8	ns
Output Data Delay Time 1x3(*)	todx13	CLKSEL:H	1	—	12	ns
Output Data Delay Time 2x1(*)	tod2x11	CLKSEL:H	1	—	9	ns
Output Data Delay Time 2x2(*)	tod2x12	CLKSEL:H	1	—	8	ns
Output Data Delay Time 2x3(*)	tod2x13	CLKSEL:H	1	—	11	ns
Output Clock Delay Time (*) (CLKX2-CLKXO)	tcxd11	CLKSEL:H	4	—	17	ns
Output Clock Delay Time (*) (CLKX2-CLKX2O)	tcxd12	CLKSEL:H	4	—	16	ns
SCL Clock Cycle Time	tc_sc1	pull up = 4.7kΩ	200	—	—	ns
Low Level Cycle	tl_sc1	pull up = 4.7kΩ	100	—	—	ns
RESET_L width	rst_w		200	—	—	ns

(*) Output load: 40 pF

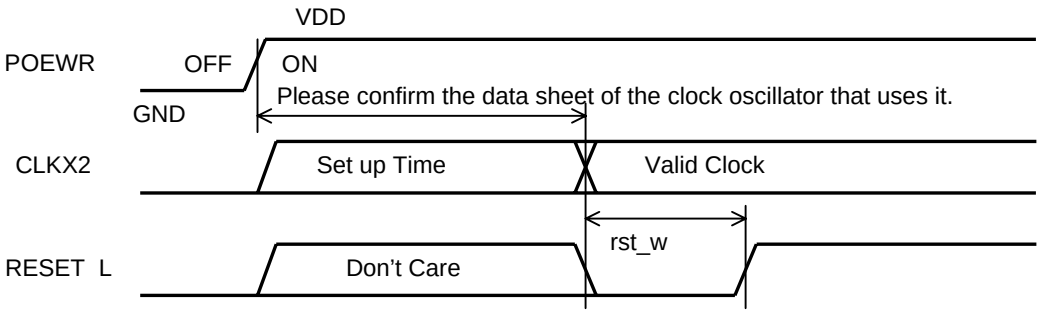
(**) Use accuracy of ± 50 ppm when emphasizing characteristics such as vector waveforms. If ± 100 ppm is used, jitter will increase in the vector waveform as accuracy deteriorates due to the thermal characteristic.

INPUT AND OUTPUT TIMINGS

Data Output Timing

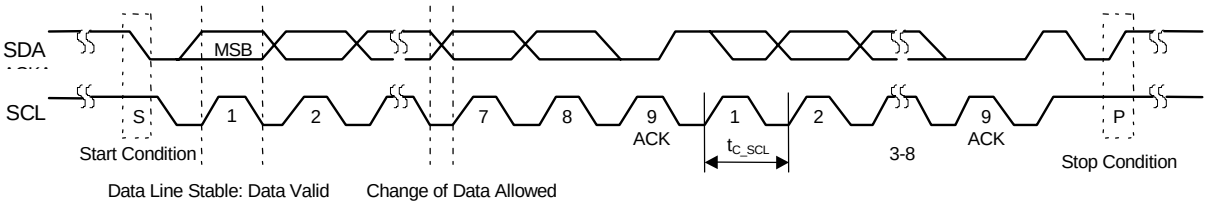


Reset Timing

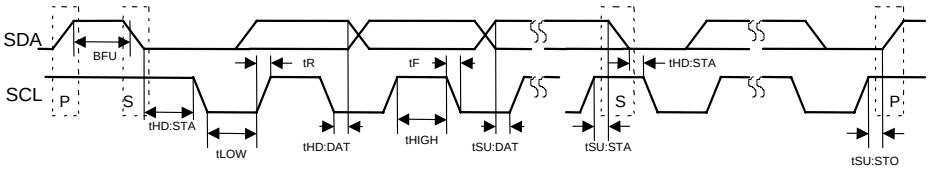


The input terminal at the time of the reset is uncertain.

I²C-bus Interface Timing



I²C-bus Timing

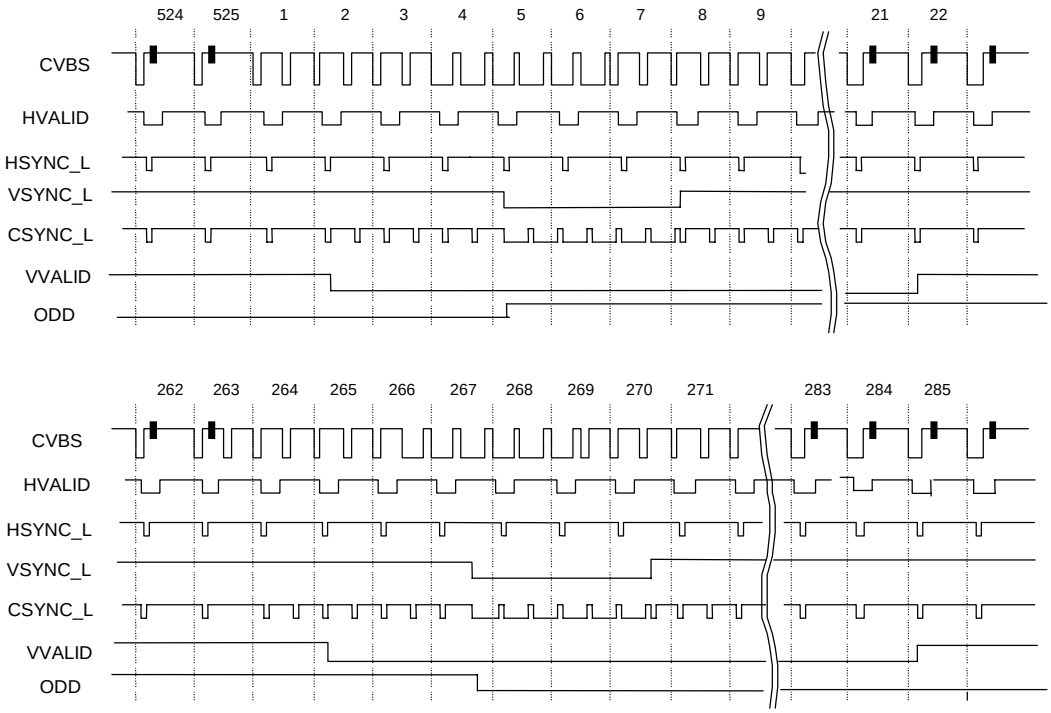


Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL frequency	0	100	400	KHz
tBUF	Bus open time	4.7			µs
tHD:STA	Start condition hold time	4.0			µs
tLOW	Clock LOW period	4.7			µs
tHIGH	Clock HIGH period	4.0			µs
tSU:STA	Start condition setup time	4.7			µs
tHD:DAT	Data hold time	300			ns
tSU:DAT	Data setup time	250			ns
tR	Line rise time			1	µs
tF	Line fall time			300	ns
tSU:STO	Stop condition setup time	4.7			µs

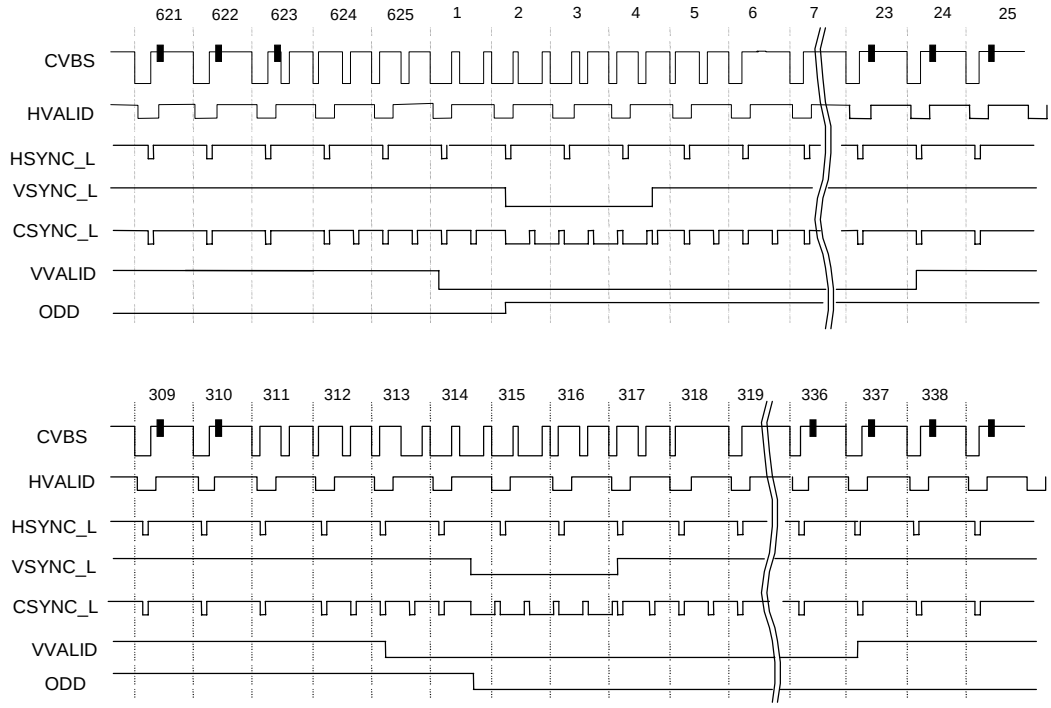
The I²C-bus timing is based on the table above.

Sync Signal Input and Output Timings (Default)

The following illustrations show the timing of vertical sync signals. The sync signal is output after approximately 1.5H.



Vertical Sync Signals (60 Hz)

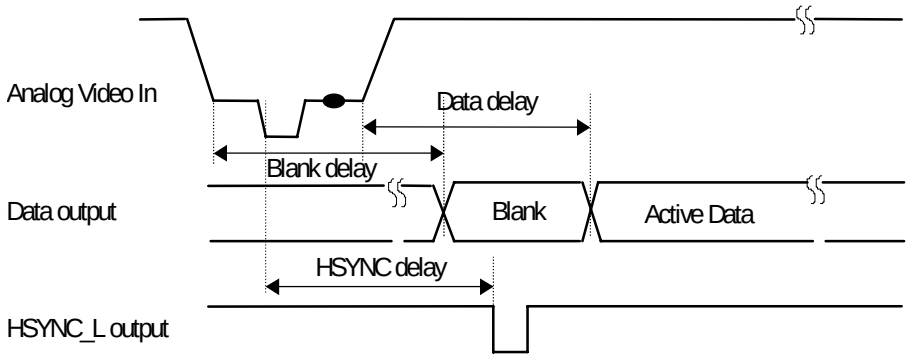


PAL VSYNC_L : $04/SYDR[6] = ”1” 2.5H , “0” 3H (default)

Vertical Sync Signals (50 Hz)

Input/Output Delays (at Standard Signal Input)

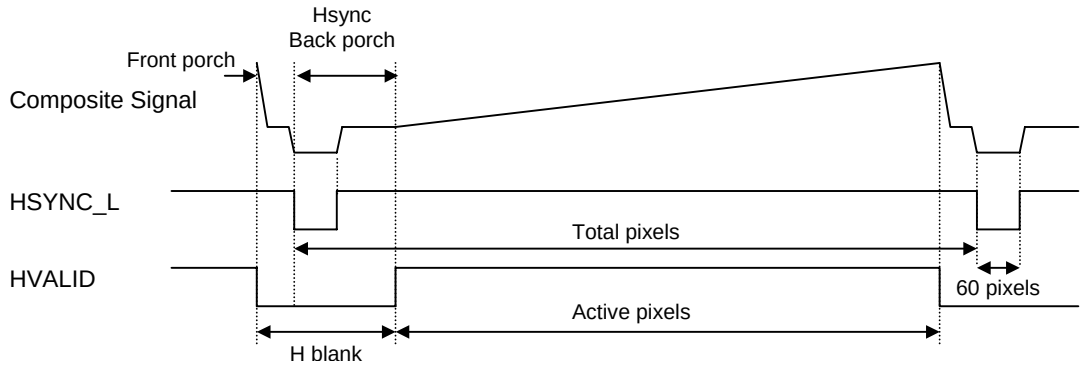
The illustration below shows the time delay between the input of a video signal and the output of digital data.



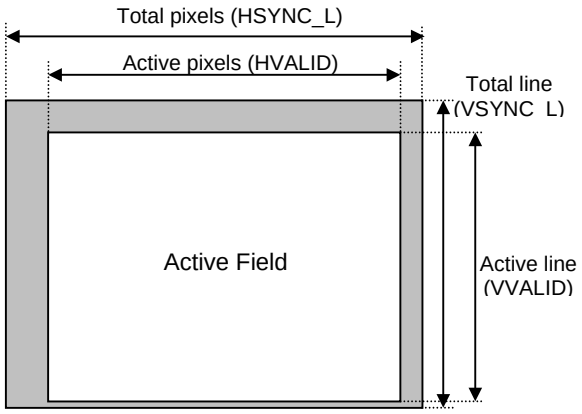
Video mode	Input signal	FIFO/FM mode	Delay
NTSC	Composite	FIFO-1	about 1.5H
NTSC	Composite	FM	
PAL	Composite	FIFO-1	
PAL	Composite	FM	
NTSC, PAL	S-Video	FIFO-1	
NTSC, PAL	S-Video	FM	

The data delay, blank delay, and sync signal delay are the same length.
Depending on the mode status, the numeric Delay value may vary.

Active Pixel Timing



Note: Actually, there is an output delay of about 1H after video signal input.



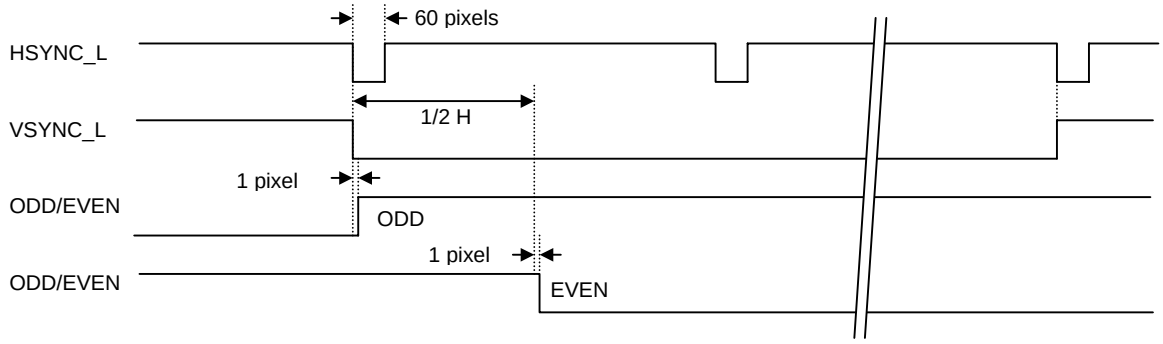
Video Modes and Pixel/Line Counts (at Standard Signal Input)

Video mode	Sampling Pixel mode	Output Pixel rate (MHz)	H					V		
			Front porch	Hsync Back porch	H blank	Active pixels	Total pixels	V blank	Active line	Total line
NTSC	ITUR.601	13.5	16	122	138	720	858	odd/20 even/20	odd/243 even/242	odd/263 even/262
	square pixel	12.272727	28	112	140	640	780			
	4fsc	14.31818	8	134	142	768	910			
PAL	ITUR.601	13.5	12	132	144	720	864	odd/23 even/24	odd/289 even/289	odd/312 even/313
	square pixel	14.75	34	142	176	768	944			

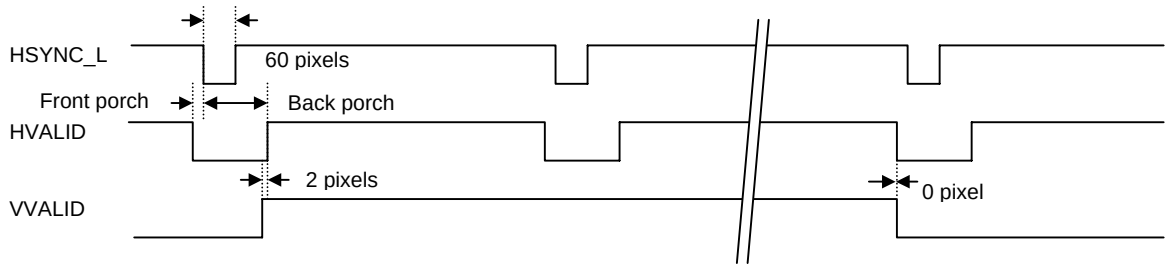
Note: Where the FIFO mode is used in asynchronous sampling operations with fixed clock, the 1-field sampling error accumulated in the line immediately following the fall of VVALID is reset. Therefore, the pixel count for the line that was reset will change. In addition, where the condition of VTR and other signals is poor in the FIFO-2 mode, the FIFO reset line might break in before the fall of VVALID.

Sync Signals Output Timing (at Default/Standard Signal Input)

VSYNC_L, ODD/EVEN

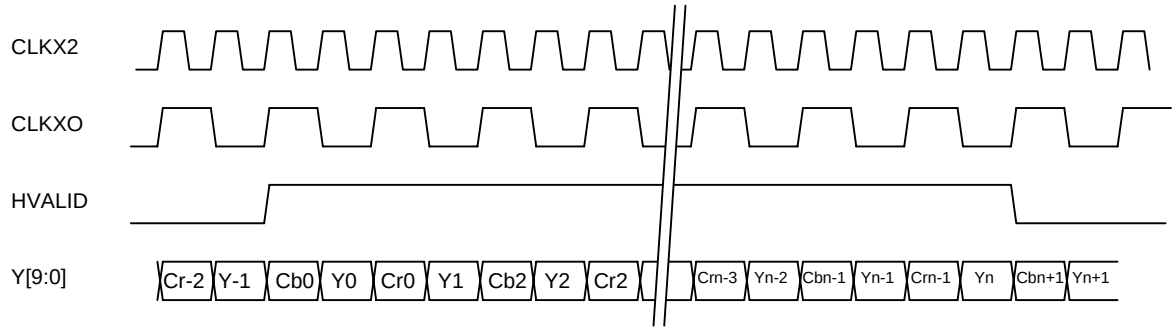


VALID Signal

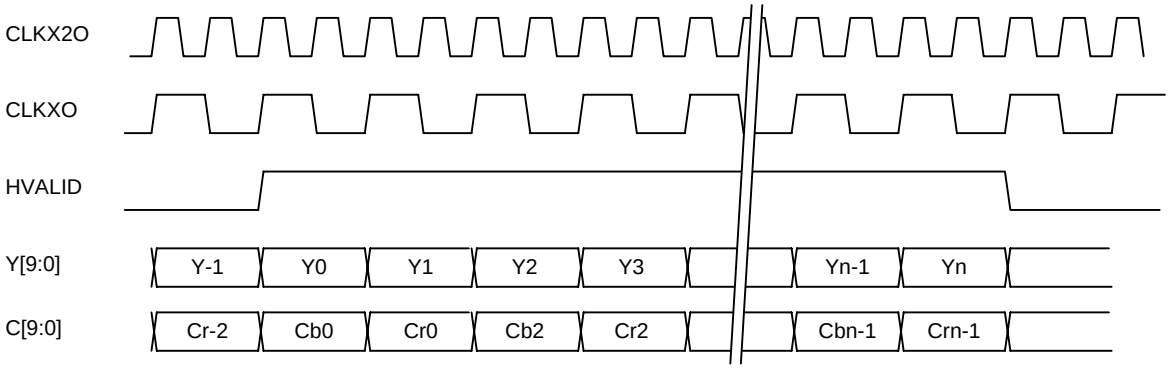


Output Timing by Mode

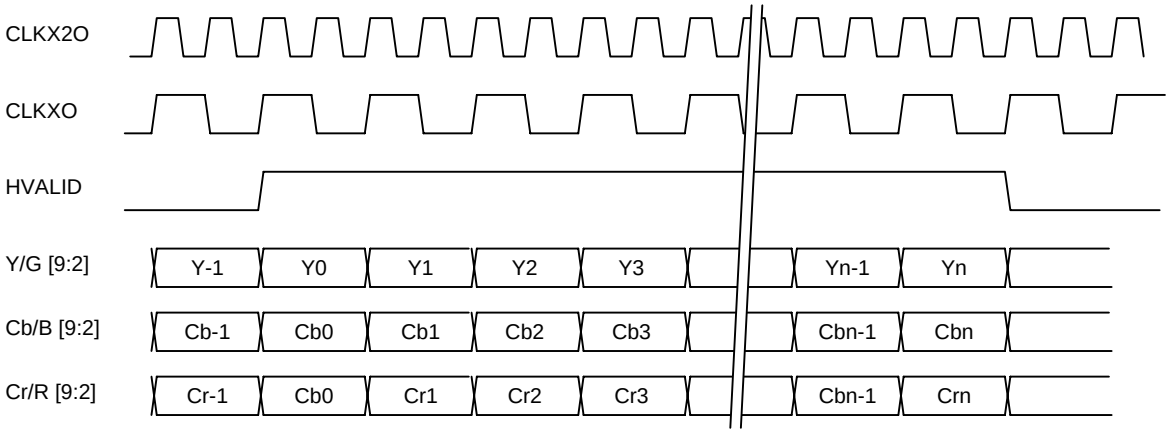
10-bit Y/CbCr serial output



20-bit Y/CbCr parallel output



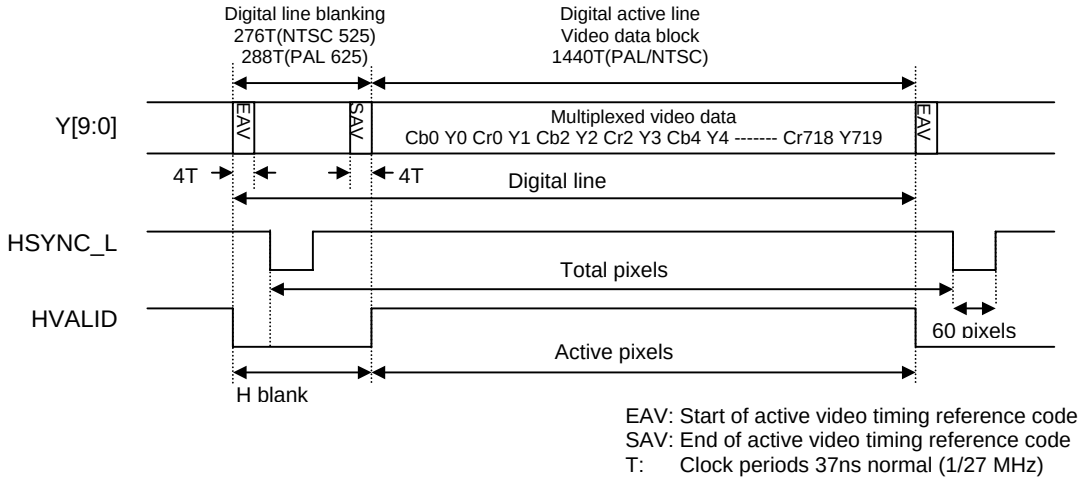
24-bit Y/CbCr and RGB parallel output



Note: Where single-speed (e.g., 13.5 MHz) is input as the input clock in the 16-bit or 24-bit (RGB) output mode, the waveform of CLKX2 is single-speed, but the format after that is not changed.

ITU-R BT.656-4 output:

Output is performed based on BT.656 of the ITU standards. If sync signal information (SAV, EAV) is multiplexed with video data and the interface complies with BT.656, data can be transferred by connecting to Y data, without connecting to the sync signal. The data in the blanking period is masked, but the Y data can be output.



EAV: Start of active video timing reference code
SAV: End of active video timing reference code
T: Clock periods 37ns normal (1/27 MHz)

Note: When operating in the asynchronous sampling mode, digital lines 1716T (NTSC,525) and 1728T (PAL, 625) will change due to the sampling error.
In the FIFO mode, the pixels count correction function ensures that there is no fluctuation in the pixel count between active lines, but the line immediately following the fall of VVALID will change due to the FIFO reset.
In particular, when non-standard signals such as VTR signals are input, the line immediately following the fall of VVALID will vary greatly in accordance with the degree of the instability of the input signal. Where the sampling error is large, the line will change immediately before the fall of VVALID.
In some cases where the line count increases or decreases with respect to the reference, such as non-standard signals, EAV and SAV may not be guaranteed.

INTERNAL REGISTERS

The following is a list of registers. Refer to the User's Manual for details of each register.

Register name	W/R	Sub ADD.	Register bit number / Default value								Hex value
Mode Register A (MRA)	W/R	00	MRA7	MRA6	MRA5	MRA4	MRA3	MRA2	MRA1	MRA0	
			0	1	0	0	0	0	0	0	40
Mode Register B (MRB)	W/R	01	MRB7	MRB6	MRB5	MRB4	MRB3	MRB2	MRB1	MRB0	
			0	0	0	0	0	0	0	0	00
Mode Register C (MRC)	W/R	02	MRC7	MRC6	MRC5	MRC4	MRC3	MRC2	MRC1	MRC0	
			1	0	0	0	0	0	0	0	80
Mode Register D (MRD)	W/R	03	MRD7	MRD6	MRD5	MRD4	MRD3	MRD2	MRD1	MRD0	
			0	1	0	0	0	0	0	0	40
Synchronous Detect Register (SYDR)	W/R	04	SYDR7	SYDR6	SYDR5	SYDR4	SYDR3	SYDR2	SYDR1	SYDR0	
			0	0	0	0	1	0	0	0	08
Not use	W/R	05	-	-	-	-	-	-	-	-	
			1	1	1	1	0	0	1	0	F2
Sync Threshold Level Adjust (STHR)	W/R	06	STHR7	STHR6	STHR5	STHR4	STHR3	STHR2	STHR1	STHR0	
			0	0	1	0	1	1	0	1	2D
Horizontal Sync Delay (HSDL)	W/R	07	HSDL7	HSDL6	HSDL5	HSDL4	HSDL3	HSDL2	HSDL1	HSDL0	
			0	0	0	0	0	0	0	0	00
Horizontal Valid Trimmer (HVALT)	W/R	08	HVALT7	HVALT6	HVALT5	HVALT4	HVALT3	HVALT2	HVALT1	HVALT0	
			0	0	0	0	0	0	0	0	00
Vertical Valid Trimmer (VVALT)	W/R	09	VVALT7	VVALT6	VVALT5	VVALT4	VVALT3	VVALT2	VVALT1	VVALT0	
			0	0	0	0	0	0	0	0	00
Luminance Control (LUMC)	W/R	0A	LUMC7	LUMC6	LUMC5	LUMC4	LUMC3	LUMC2	LUMC1	LUMC0	
			0	0	0	0	0	0	0	0	00
AGC Loop filter Control & Lum. Control Register (AGCL)	W/R	0B	AGCL7	AGCL6	AGCL5	AGCL4	AGCL3	AGCL2	AGCL1	AGCL0	
			0	1	0	0	0	0	0	0	40
AGC Reference Control (AGCRC)	W/R	0C	AGCRC7	AGCRC6	AGCRC5	AGCRC4	AGCRC3	AGCRC2	AGCRC1	AGCRC0	
			0	0	0	0	0	0	0	0	00
Contrast Level Control (CLC)	W/R	0D	CLC7	CLC6	CLC5	CLC4	CLC3	CLC2	CLC1	CLC0	
			1	0	0	0	0	0	0	0	80

Register name	W/R	Sub ADD.	Register bit number								Hex value
			Default value								
Sync Separation Level (SSEPL)	W/R	0E	SSEPL7	SSEPL6	SSEPL5	SSEPL4	SSEPL3	SSEPL2	SSEPL1	SSEPL0	
			0	0	0	0	0	0	0	0	00
Chrominance Control A (CHRCA)	W/R	0F	CHRCA7	CHRCA6	CHRCA5	CHRCA4	CHRCA3	CHRCA2	CHRCA1	CHRCA0	
			0	0	0	1	0	0	0	0	10
Chrominance Control B (CHRCB)	W/R	10	CHRCB7	CHRCB6	CHRCB5	CHRCB4	CHRCB3	CHRCB2	CHRCB1	CHRCB0	
			0	0	0	0	0	0	0	0	00
ACC Loop Filter & Chrominance Control C (ACCC)	W/R	11	ACCC7	ACCC6	ACCC5	ACCC4	ACCC3	ACCC2	ACCC1	ACCC0	
			0	1	0	0	0	0	0	0	40
ACC Reference Control (ACCRC)	W/R	12	ACCRC7	ACCRC6	ACCRC5	ACCRC4	ACCRC3	ACCRC2	ACCRC1	ACCRC0	
			0	0	0	0	0	0	0	0	00
Hue Control (HUE)	W/R	13	HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0	
			0	0	0	0	0	0	0	0	00
Blue Back & HDET Control (BBHC)	W/R	14	BBHC7	BBHC6	BBHC5	BBHC4	BBHC3	BBHC2	BBHC1	BBHC0	
			1	0	0	1	0	0	0	0	90
Optional Mode Register A (OMRA)	W/R	15	OMRA7	OMRA6	OMRA5	OMRA4	OMRA3	OMRA2	OMRA1	OMRA0	
			1	0	0	0	0	0	0	0	80
Optional Mode Register B (OMRB)	W/R	16	OMRB7	OMRB6	OMRB5	OMRB4	OMRB3	OMRB2	OMRB1	OMRB0	
			0	0	1	0	1	0	1	0	2A
Optional Mode Register C (OMRC)	W/R	17	OMRC7	OMRC6	OMRC5	OMRC4	OMRC3	OMRC2	OMRC1	OMRC0	
			0	1	1	0	1	0	0	0	68
Optional Mode Register D (OMRD)	W/R	18	OMRD7	OMRD6	OMRD5	OMRD4	OMRD3	OMRD2	OMRD1	OMRD0	
			0	0	0	0	0	0	0	0	00
Optional Mode Register E (OMRE)	W/R	19	OMRE7	OMRE6	OMRE5	OMRE4	OMRE3	OMRE2	OMRE1	OMRE0	
			0	0	0	0	0	0	0	0	00
Scalar Register (SCR)	W/R	1A	SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0	
			0	0	0	0	0	0	0	0	00

Register name	W/R	Sub ADD.	Register bit number								Hex value
			Default value								
Scalar V-Position Register (SCVPR)	W/R	1B	SCVPR7	SCVPR6	SCVPR5	SCVPR4	SCVPR3	SCVPR2	SCVPR1	SCVPR0	
			0	0	0	0	0	0	0	0	00
Scalar H-Position Register (SCHPR)	W/R	1C	SCHPR7	SCHPR6	SCHPR5	SCHPR4	SCHPR3	SCHPR2	SCHPR1	SCHPR0	
			0	0	0	0	0	0	0	0	00
ADC Register 1 (ADC1)	W/R	1D	ADC17	ADC16	ADC15	ADC14	ADC13	ADC12	ADC11	ADC10	
			0	0	0	0	0	0	0	0	00
ADC Register 2 (ADC2)	W/R	1E	ADC27	ADC26	ADC25	ADC24	ADC23	ADC22	ADC21	ADC20	
			1	0	0	1	0	0	0	1	91
PLL Resister (PLLR)	W/R	1F	PLLR7	PLLR6	PLLR5	PLLR4	PLLR3	PLLR2	PLLR1	PLLR0	
			0	0	0	0	0	0	0	0	00
Closed Caption Detected-1 Register (CCD1)	W/R	20	CCD17	CCD16	CCD15	CCD14	CCD13	CCD12	CCD11	CCD10	
			0	0	0	0	0	0	0	0	00
Closed Caption Detected-2 Register (CCD2)	W/R	21	CCD27	CCD26	CCD25	CCD24	CCD23	CCD22	CCD21	CCD20	
			0	0	0	0	0	0	0	0	00
CGMS Detected-1 Register (CGMS1)	W/R	22	CGMS17	CGMS16	CGMS15	CGMS14	CGMS13	CGMS12	CGMS11	CGMS10	
			0	0	0	0	0	0	0	0	00
CGMS Detected-2 Register (CGMS2)	W/R	23	CGMS27	CGMS26	CGMS25	CGMS24	CGMS23	CGMS22	CGMS21	CGMS20	
			0	0	0	0	0	0	0	0	00
AGC pulse Detected-1 Register (AGCD1)	W/R	24	AGCD17	AGCD16	AGCD15	AGCD14	AGCD13	AGCD12	AGCD11	AGCD10	
			0	0	0	0	0	0	0	0	00
AGC pulse Detected-2 Register (AGCD2)	W/R	25	AGCD27	AGCD26	AGCD25	AGCD24	AGCD23	AGCD22	AGCD21	AGCD20	
			0	0	0	0	0	0	0	0	00
0WSS data Detected-1 Register (WSSD1)	W/R	26	WSSD7	WSSD6	WSSD5	WSSD4	WSSD3	WSSD2	WSSD1	WSSD0	
			0	0	0	0	0	0	0	0	00
Reset data Request for VBID Function Register (AIREG)	W/R	27	AIREG7	AIREG6	AIREG5	AIREG4	AIREG3	AIREG2	AIREG1	AIREG0	
			0	0	0	0	0	0	0	0	00
Status Register (STATUS)	Read	28	STATUS7	STATUS6	STATUS5	STATUS4	STATUS3	STATUS2	STATUS1	STATUS0	
			—	—	—	—	—	—	—	—	

Register name	W/R	Sub ADD.	Register bit number								Hex value
			Default value								
VBID Flag Register (VFLAG)	Read	29	VFLAG7	VFLAG6	VFLAG5	VFLAG4	VFLAG3	VFLAG2	VFLAG1	VFLAG0	
			—	—	—	—	—	—	—	—	
C.C. Data Buffer Register in Odd Field (CCDO0)	Read	2A	CCDO07	CCDO06	CCDO05	CCDO04	CCDO03	CCDO02	CCDO01	CCDO00	
			—	—	—	—	—	—	—	—	
C.C. Data Buffer Register in Odd Field (CCDO1)	Read	2B	CCDO17	CCDO16	CCDO15	CCDO14	CCDO13	CCDO12	CCDO11	CCDO10	
			—	—	—	—	—	—	—	—	
C.C. Data Buffer Register in Even Field (CCDE0)	Read	2C	CCDE07	CCDE06	CCDE05	CCDE04	CCDE03	CCDE02	CCDE01	CCDE00	
			—	—	—	—	—	—	—	—	
C.C. Data Buffer Register in Even Field (CCDE1)	Read	2D	CCDE17	CCDE16	CCDE15	CCDE14	CCDE13	CCDE12	CCDE11	CCDE10	
			—	—	—	—	—	—	—	—	
CGMS Data Buffer Register in Odd Field (CGMSO0)	Read	2E	CGMSO07	CGMSO06	CGMSO05	CGMSO04	CGMSO03	CGMSO02	CGMSO01	CGMSO00	
			—	—	—	—	—	—	—	—	
CGMS Data Buffer Register in Odd Field (CGMSO1)	Read	2F	CGMSO17	CGMSO16	CGMSO15	CGMSO14	CGMSO13	CGMSO12	CGMSO11	CGMSO10	
			—	—	—	—	—	—	—	—	
CGMS Data Buffer Register in Odd Field (CGMSO2)	Read	30	CGMSO27	CGMSO26	CGMSO25	CGMSO24	CGMSO23	CGMSO22	CGMSO21	CGMSO20	
			—	—	—	—	—	—	—	—	
CGMS Data Buffer Register in Even Field (CGMSE0)	Read	31	CGMSE07	CGMSE06	CGMSE05	CGMSE04	CGMSE03	CGMSE02	CGMSE01	CGMSE00	
			—	—	—	—	—	—	—	—	
CGMS Data Buffer Register in Even Field (CGMSE1)	Read	32	CGMSE17	CGMSE16	CGMSE15	CGMSE14	CGMSE13	CGMSE12	CGMSE11	CGMSE10	
			—	—	—	—	—	—	—	—	
CGMS Data Buffer Register in Even Field (CGMSE2)	Read	33	CGMSE27	CGMSE26	CGMSE25	CGMSE24	CGMSE23	CGMSE22	CGMSE21	CGMSE20	
			—	—	—	—	—	—	—	—	
WSS Data Buffer Register (WSS0)	Read	34	WSS07	WSS06	WSS05	WSS04	WSS03	WSS02	WSS01	WSS00	
			—	—	—	—	—	—	—	—	
WSS Data Buffer Register (WSS1)	Read	35	WSS17	WSS16	WSS15	WSS14	WSS13	WSS12	WSS11	WSS10	
			—	—	—	—	—	—	—	—	

NOTES ON USE

The ML86V7666 Video Decoder is being developed based on standard signals. Improvements are being made to ensure stable operation even with non-standard signals. However, the signal conditions and usage environments differ widely for signals such as those having a weak electromagnetic field, VTR playback signals, signals with numerous signal switching or a large amount of noise, and simple video signals from various cameras. As a result, stable operation for all signals has not yet been confirmed. Before using the decoder, please carefully evaluate and consider the signal conditions and usage environment of the intended use.

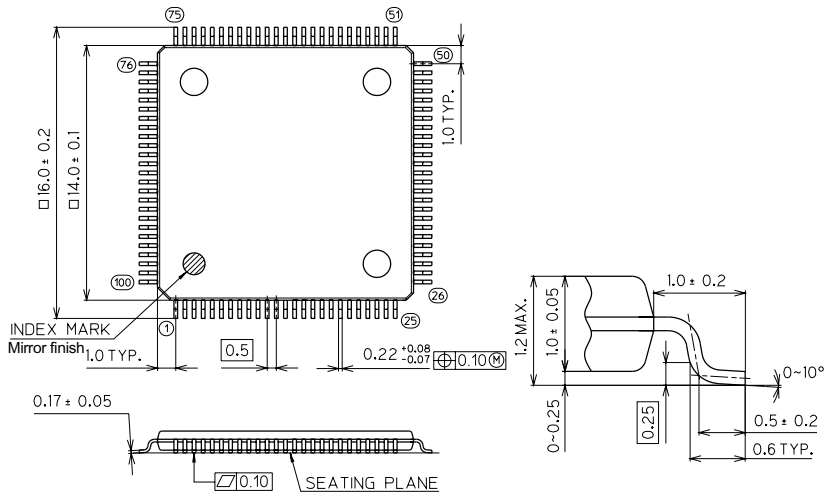
In addition to this Data Sheet, a ML86V7666 User's Manual is also available. The User's Manual explains each register and provides examples of adapted circuits as well as other information helpful in the design phase. Please read the User's Manual before embarking on design work.

Users are also requested to regularly download the most recent versions of this Data Sheet and the User's Manual from the Oki web site. As the newest information, not included in printed materials, and the answers to frequently asked questions are published on the web site, users are recommended to check the site regularly for updates.

PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

5

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code, and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
Version 1	Oct. 30, 2002	–	–	Preliminary edition 1
Version 2	Jun. 5. 2003	–	–	Preliminary edition 2
Version 3	Apr. 9. 2004	36	36	Preliminary edition 3
FEDL86V7666-01	Apr. 20. 2004	36	36	Final edition 1

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by Oki, authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.