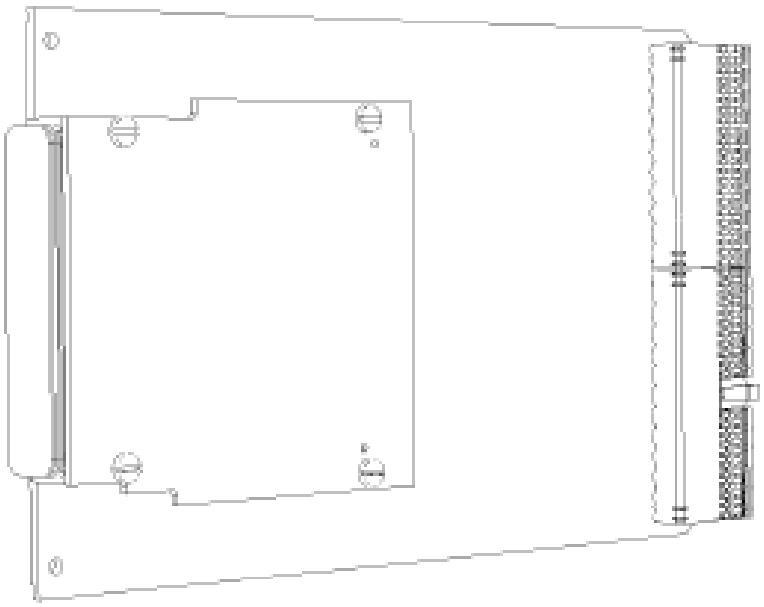
# FMC30RF
## User Manual



4DSP LLC, USA

Email: support@4dsp.com

# Revision History

| Date | Revision | Revision |
|---|---|---|
| 2012-05-30 | Draft | 0.1 |
| 2012-05-30 | Release after review | 1.0 |
| 2012-10-05 | Additional info on LNA and reference oscillator | 1.1 |
| 2014-06-11 | Update voltage monitoring section<br>Additional info in Figure 5 and pin out. | 1.2 |
| 2015-02-12 | Added RF input analog line-up description, updated RF in/out characteristics. | 1.3 |
| | | |
| | | |
| | | |

# Table of Contents

# 1 Acronyms and related documents

## 1.1 Acronyms

| | |
|---|---|
| ADC | Analog to Digital Converter |
| DDR | Double Data Rate |
| EPROM | Erasable Programmable Read-Only Memory |
| FBGA | Fineline Ball Grid Array |
| FMC | FPGA Mezzanine Card |
| FPGA | Field Programmable Gate Array |
| JTAG | Join Test Action Group |
| LED | Light Emitting Diode |
| LVTTL | Low Voltage Transistor Logic level |
| LSB | Least Significant Bit(s) |
| LVDS | Low Voltage Differential Signaling |
| MGT | Multi-Gigabit Transceiver |
| MSB | Most Significant Bit(s) |
| PCB | Printed Circuit Board |
| PLL | Phase Locked Loop |
| PSSR | Power Supply Rejection Ratio |

**Table 1: Glossary**

## 1.2 Related Documents

- FPGA Mezzanine Card (FMC) standard ANSI/VITA 57.1-2010
- CDCE62005 datasheet, TI, August 2011
- TRF3765 datasheet, TI, November 2011
- TRF371109 datasheet, TI, May 2011
- TRF371125 datasheet, TI, December 2010
- TRF372017 datasheet, TI, August 2010
- AMC7823 datasheet, TI, January 2010

# 2 General description

The FMC30RF is an FMC Daughter Card which is fully compliant with the VITA 57.1-2010 standard. The FMC30RF offers in a small footprint a low power and fully featured Rx/Tx signal path for the development and deployment of advanced RF solutions. With a frequency range coverage from 400MHz to 3.0GHz (two ranges) and up to 60MHz bandwidth the FMC30RF provides flexibility and reconfigurability to a host of applications.

Based on Texas Instruments RF technology the FMC30RF comprises of a dual DAC Tx IQ modulator, a dual ADC Rx IQ demodulator with PGA and LNA front-end and on-board clocking with integrated PLL/VCO. The FMC30RF allows flexible control on sampling frequency through serial communication busses. Furthermore the card is equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions.

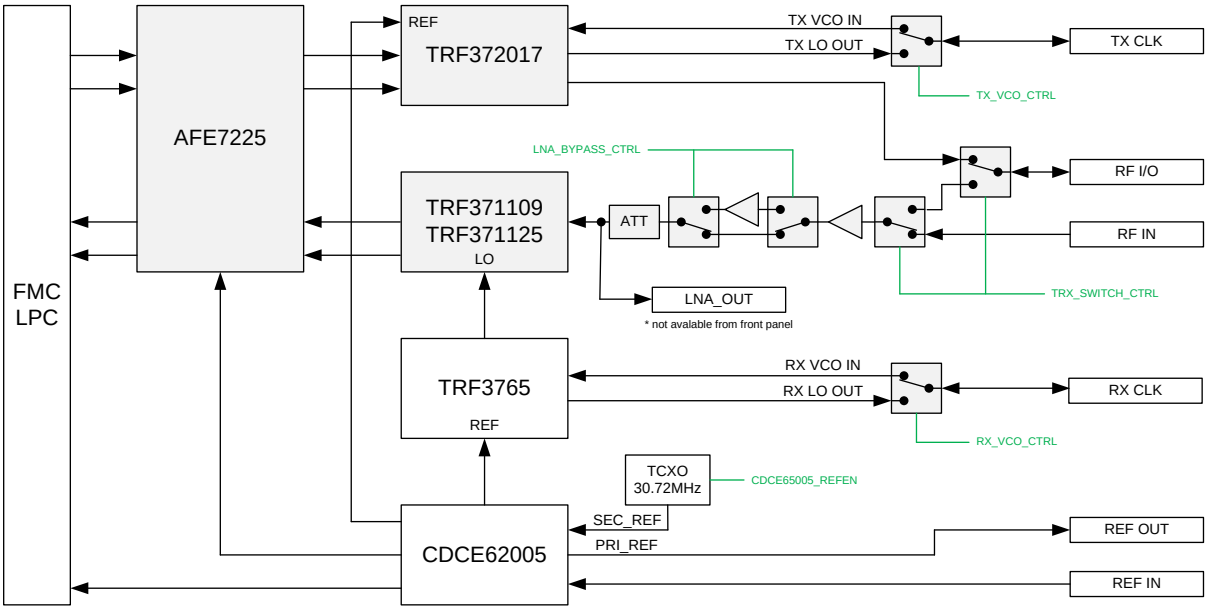



**Figure 1: FMC30RF block diagram**

# 3 Installation

## 3.1 Requirements and handling instructions

- The FMC30RF daughter card must be installed on a carrier card compliant to the FMC standard.
- The FMC carrier card must support the low-pin count connector (LPC 160-pins). High pin count is permitted.
- The FMC carrier card must support VADJ/VIO_B voltage between +1.65V and +5.5V.
- Do not flex the card and prevent electrostatic discharges by observing ESD precautions when handling the card.

# 4 Design

## 4.1 Phycisal specifications

### 4.1.1 Board Dimensions

The FMC30RF card complies with the FMC standard known as ANSI/VITA 57.1. The card is a single width conduction cooled mezzanine module (with region 1 and front panel I/O). A front rib on the carrier hardware is not supported. The stacking height is 10mm.

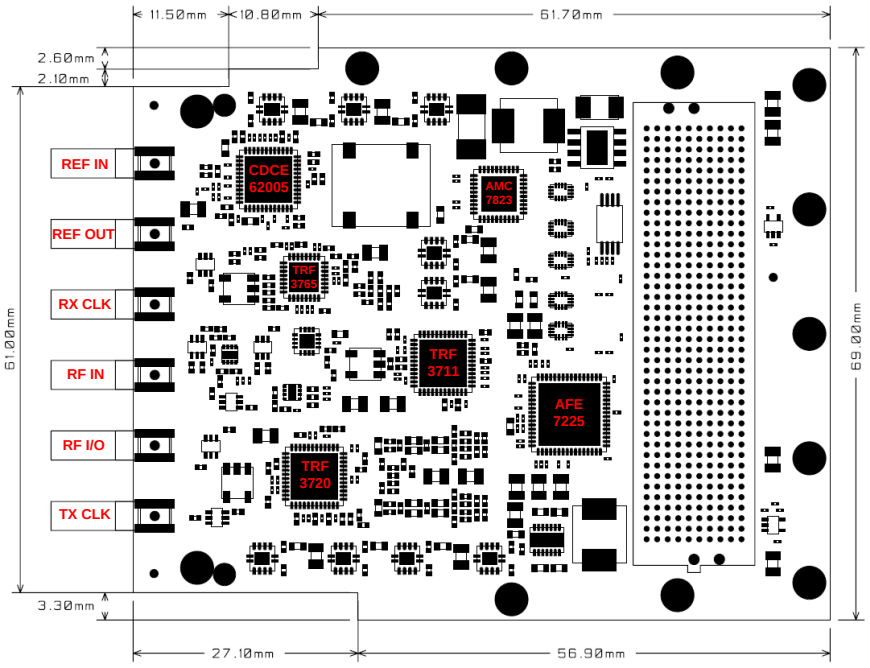



**Figure 2: FMC30RF dimensions**

### 4.1.2 Front panel coax inputs

The FMC30RF can be ordered with MMCX or SSMC connector type. Six connectors are available on the front panel.

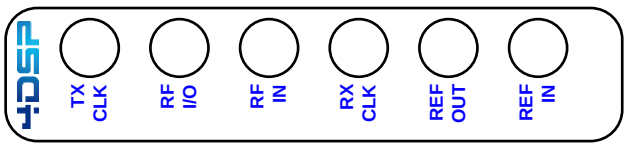



**Figure 3: FMC30RF bezel layout**

## 4.2 Electrical specifications

The FMC30RF card uses a mix of LVDS and LVCMOS signals. According to the FMC standard VADJ should be +2.5V to support LVDS, but the FMC30RF is designed to accept any level on VADJ ranging between 1.65V and 5.5V. VIO_B_M2C connections are connected to VADJ on the FMC30RF. Level translators are implemented to guarantee VADJ level on the FMC connector for all single ended communication and control signals.

### 4.2.1 EEPROM

The FMC30RF card carries a 2Kbit EEPROM (24LC02B) which is accessible from the carrier card through the $I^2C$ bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01µA when SCL and SDA are kept at 3P3VAUX level. These signals may also be left floating since pull-up resistors are present on the card.

### 4.2.2 JTAG

The FMC30RF card TDO pin is connected to the TDI pin (through an SN74LVC1G126 buffer) to ensure continuity of the JTAG chain. TCK, TMS and TRST are left unconnected on the FMC30RF.

### 4.2.3 FMC connector

The low-pin count connector has only bank LA available and two dedicated LVDS clock pairs. The recommendations from AV57.1-2010 Table 14 have been taking into account resulting in the following arrangement:

- The ADC data clock pair (ADC_DCLKOUT) and ADC frame clock pair (ADC_FCLKOUT) are connected to clock capable pins LA00_CC and LA01_CC respectively. The ADC data pairs are mapped to LA02 to LA05.
- The DAC clock, frame and data pairs are mapped to LA06 to LA12. Since all pairs are outputs as seen from the FPGA, there is no need to have the clock and frame pair on clock capable pins.
- LA13 to LA31 are used for low speed single ended communication and control signals.
- The remaining connections (LA32-LA33) are used left unconnected.
- An LVDS output of the CDCE62005 is connected to a dedicated LVDS connections on the FMC (CLK0_M2C). The other dedicated LVDS connection is not used.

Refer also to the appendix for the detailed LPC connector pinout.

### 4.2.4 RF input

The RF input circuit comprises tuneable and fixed gain stages. The analog line-up is depicted in Figure 4.

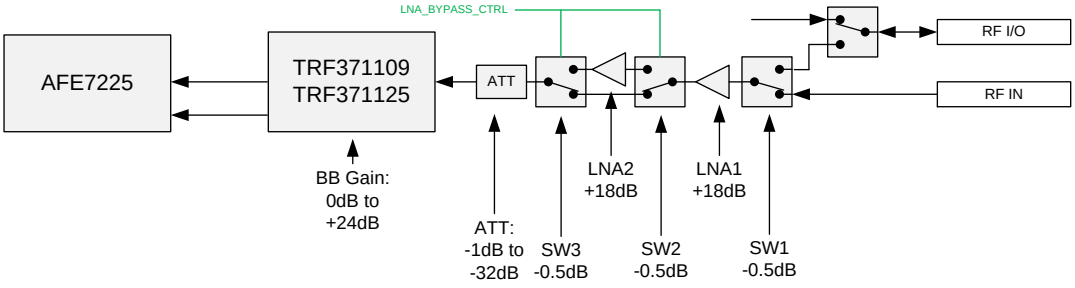



**Figure 4: RF input analog line-up**

Guidelines of controlling tuneable gain and attenuators are provided in section 6. The maximum input level at the RF input is +3dBm and can be applied to the board when the total gain of the analog line-up is set to minimum. This is done by:

- Bypass LNA2
- Set the stepped attenuator to 32dB attenuation
- Set the BB gain of the TRF3711 to 0dB (default setting is 15dB, refer to the datasheet of the TRF3711)

Applying a signal of +3dBm to the first stage LNA drives the LNA close to its input 1dB compression point.

## 4.3 Main characteristic

| | |
|---|---|
| **RF IN** | |
| **LO Range** | Low range option: 400MHz – 1200MHz<br>High range option: 1200MHz – 3000MHz |
| **Bandwidth** | 60MHz (when LPF in TRF3711xx bypassed) |
| **Input Impedance** | 50Ω |
| **Maximum Input Level** | +3dBm[1] |
| **RF OUT** | |
| **LO Range** | 300MHz – 4800MHz |
| **Bandwidth** | 70MHz |
| **Output Impedance** | 50Ω |
| **Full Scale Maximum Output Level** | +3dBm (depending on LO frequency) |
| **Receiver LO (RX CLK)** | |
| **Output Frequency Range** | Programmable trough fractional PLL (TRF3765):<br>300MHz to 4800MHz |
| **Output Impedance** | 50Ω |
| **Output Level** | -0.5dBm typ. |
| **Input Frequency Range** | 300MHz to 4800MHz |
| **Input Impedance** | High-impedance |
| **Input Level** | 0dBm |
| **Transmitter LO (TX CLK)** | |
| **Output Frequency Range** | Programmable trough fractional PLL (TRF372017):<br>300MHz to 4800MHz |
| **Output Impedance** | 50Ω |
| **Output Level** | -0.5dBm typ. |
| **Input Frequency Range** | 300MHz to 4800MHz |
| **Input Impedance** | High-impedance |
| **Input Level** | 0dBm |
| **External Reference Input (REF IN)** | |
| **Input Level** | $0.2V_{PP}$ - $3.3V_{PP}$ |
| **Input Frequency** | 10MHz – 250MHz |
| **Input Impedance** | 50Ω |
| **External Reference Output (REF OUT)** | |
| **Output Level** | $3.3V_{PP}$ (AC coupled LVCMOS) |
| **Output Frequency** | 10MHz – 250MHz |

**Table 2: FMC30RF daughter card main characteristics**

[1] Make sure minimum gain is configured, refer to section 4.2.4.

# 5 Modes of operation

The FMC30RF support different modes of operation; TDD and FDD.

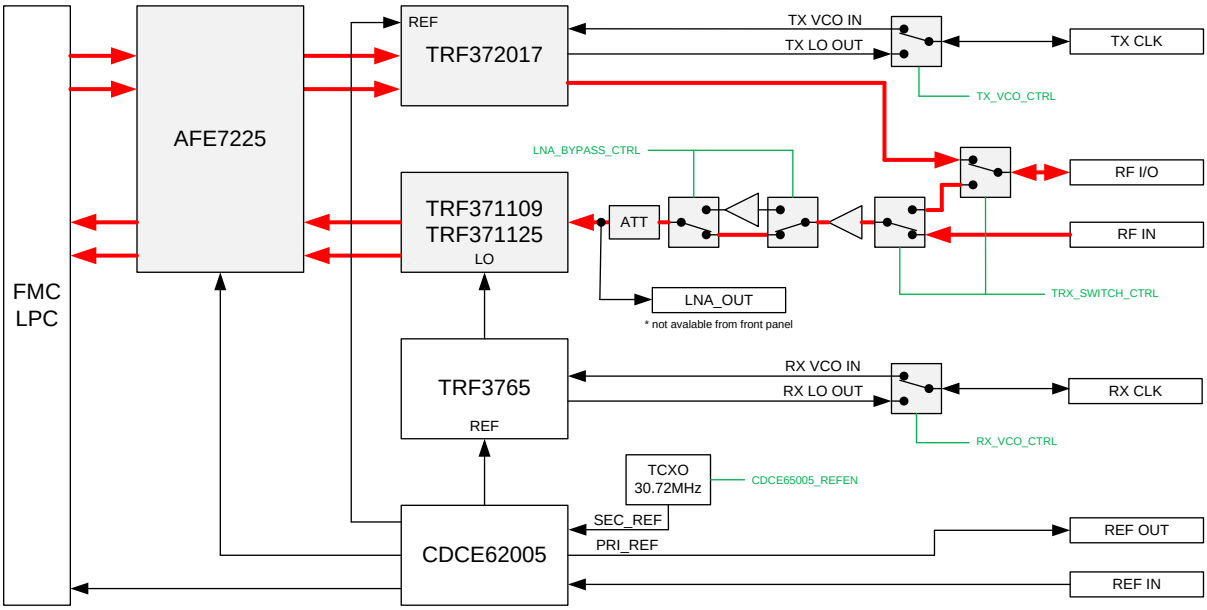



**Figure 5: Signal Path**

## 5.1 Time-Division Duplex (TDD)

The FMC30RF supports TDD using the RF I/O connector. The RF I/O connector is either receiving (TRX_SWITCH_CTRL=0) or transmitting (TRX_SWITCH_CTRL=1). The TRX_SWITCH_CTRL signal should be driven by the FPGA trough the FMC connector.

## 5.2 Frequency-Division Duplex (FDD)

The FMC30RF supports FDD using the RF I/O connector for transmitting and the RF IN connector for receiving. The TRX_SWITCH_CTRL signal should be driven high by the FPGA trough the FMC connector.

## 5.3 Multiple-Input Multiple-Output (MIMO)

With two FMC30RF boards a 2x2 MIMO setup can be realised.

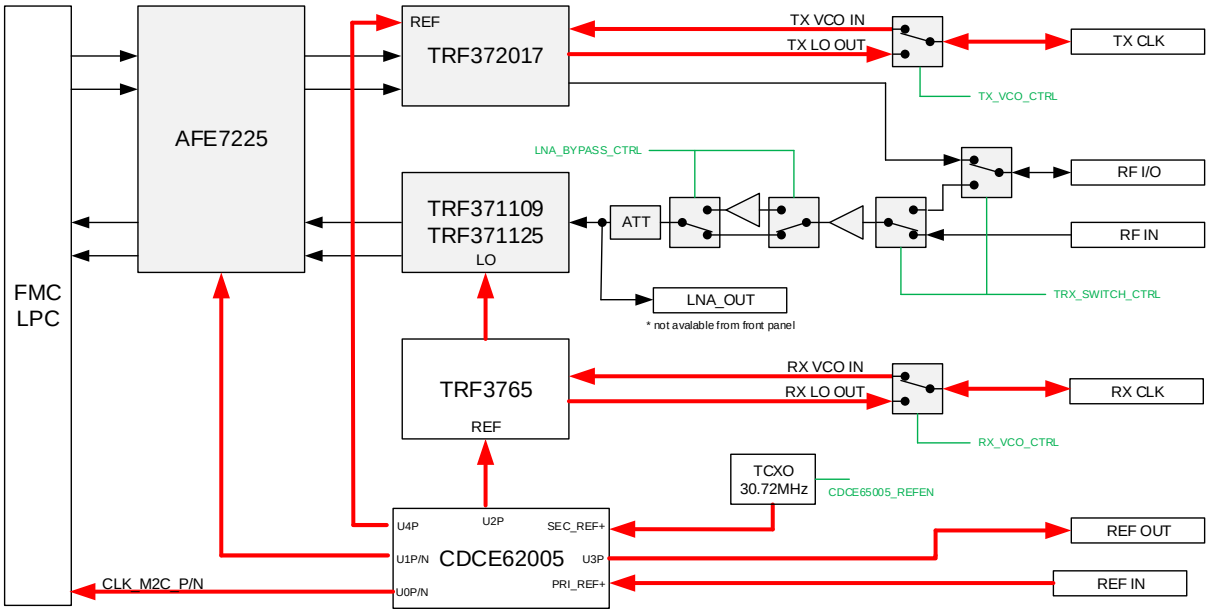



**Figure 6: Clock paths**

# 6 Controlling the FMC30RF

Good knowledge of the internal structure and communication protocol of relevant on-board devices is required for controlling the FMC30RF. This document only provides guidelines for programming the devices. For detailed information it is recommended to refer to the datasheets listed in the related documents section of this document.

## 6.1 Guidelines for controlling the RF path

The following control signals controls the RF frontend;

- TRX_SWITCH_CTRL
- LNA_BYPASS_CTRL
- RF_ATT_V[1..5]

Refer to Appendix A for a description of these signals.

The LNA in the RX path depends on the RF coverage specified at the time of order:

- RF coverage option 1 (400MHz – 1200MHz): SKY67101-396LF
- RF coverage option 2 (1200MHz – 3000MHz): SKY67100-396LF

The gain is 18-20dB for each LNA stage.

## 6.2 Guidelines for controlling the CDCE62005

The following control signals connect from the FMC connector to the CDCE62005;

- SCLK (shared with other devices)
- SDATA (shared with other devices)
- CDCE62005_CS#
- CDCE62005_SDOUT
- CDCE62005_PD#

- CDCE62005_SYNC#
- CDCE62005_LOCK
- CDCE62005_REFEN

Refer to Appendix A for a description of these signals.

### 6.3 Guidelines for controlling the TRF3765

The following control signals connect from the FMC connector to the TRF3765;

- SCLK (shared with other devices)
- SDATA (shared with other devices)
- TRF3765_CS#
- TRF3765_SDOUT
- TRF3765_LOCK
- RX_VCO_CTRL

Refer to Appendix A for a description of these signals.

### 6.4 Guidelines for controlling the TRF3711

The following control signals connect from the FMC connector to the TRF3711;

- SCLK (shared with other devices)
- SDATA (shared with other devices)
- TRF3711_CS#
- TRF3711_SDOUT
- TRF3711_PD#
- TRF3711_GAIN_B[0..2]

Refer to Appendix A for a description of these signals.

### 6.5 Guidelines for controlling the TRF3720

The following control signals connect from the FMC connector to the TRF3720;

- SCLK (shared with other devices)
- SDATA (shared with other devices)
- TRF3720_CS#
- TRF3720_SDOUT
- TRF3720_PS
- TRF3720_LOCK
- TX_VCO_CTRL

Refer to Appendix A for a description of these signals.

### 6.6 Guidelines for controlling the AFE7225

The following control signals connect from the FMC connector to the AFE7225;

- SCLK (shared with other devices)
- SDATA (shared with other devices)
- AFE7225_CS#

- AFE7225_SDOUT
- AFE7225_RESET
- AFE7225_PD

Refer to Appendix A for a description of these signals.

### 6.7 Guidelines for controlling the AMC7823

The following control signals connect from the FMC connector to the AMC7823;

- SCLK (shared with other devices)
- SDATA (shared with other devices)
- AMC7823_CS#
- AMC7823_SDOUT
- AMC7823_GALR#
- AMC7823_RESET#

Refer to Appendix A for a description of these signals.

## 7 Power supply

Power is supplied to the FMC30RF card through the FMC connector. The pin current rating is 2.7A, but the overall maximum as specified by the FMC standard is limited according to Table 3.

| Voltage | # pins | Max Amps | Max Watt |
|---|---|---|---|
| +3.3V | 4 | 3 A | 10 W |
| +12V | 2 | 1 A | 12 W |
| VADJ (+2.5V) | 4 | 4 A | 10 W |
| VIO_B (+2.5V) | 2 | 1.15 A | 2.3 W |

**Table 3: FMC standard power specification**

The power provided by the carrier card can be very noisy. Special care is taken with the power supply generation on the FMC30RF card to minimize the effect of power supply noise on clock generation, (de-)modulation, and data conversion.

Clean supply is derived from +3.3V and 12V in two steps for maximum efficiency. The first step uses a high efficient switched regulators to generate +3.8V and +5.5V power rails. From these power rail the analog and digital supplies are derived with a low dropout, low noise, high PSRR, linear regulator. At several stages in the power supply there is additional noise filtering with beads and capacitance. Power supplies for different devices are isolated where necessary.

| Power plane | Typical | Maximum |
|---|---|---|
| VADJ | 100mA | 200mA |
| 3P3V | 1.3A | 1.6A |
| 12P0V | 0.5A | 0.6A |
| 3P3VAUX (Operating)<br>3P3VAUX (Standby) | 0.1 mA<br>0.01 µA | 3 mA<br>1 µA |

**Table 4: Typical/Maximum current drawn from FMC carrier card**

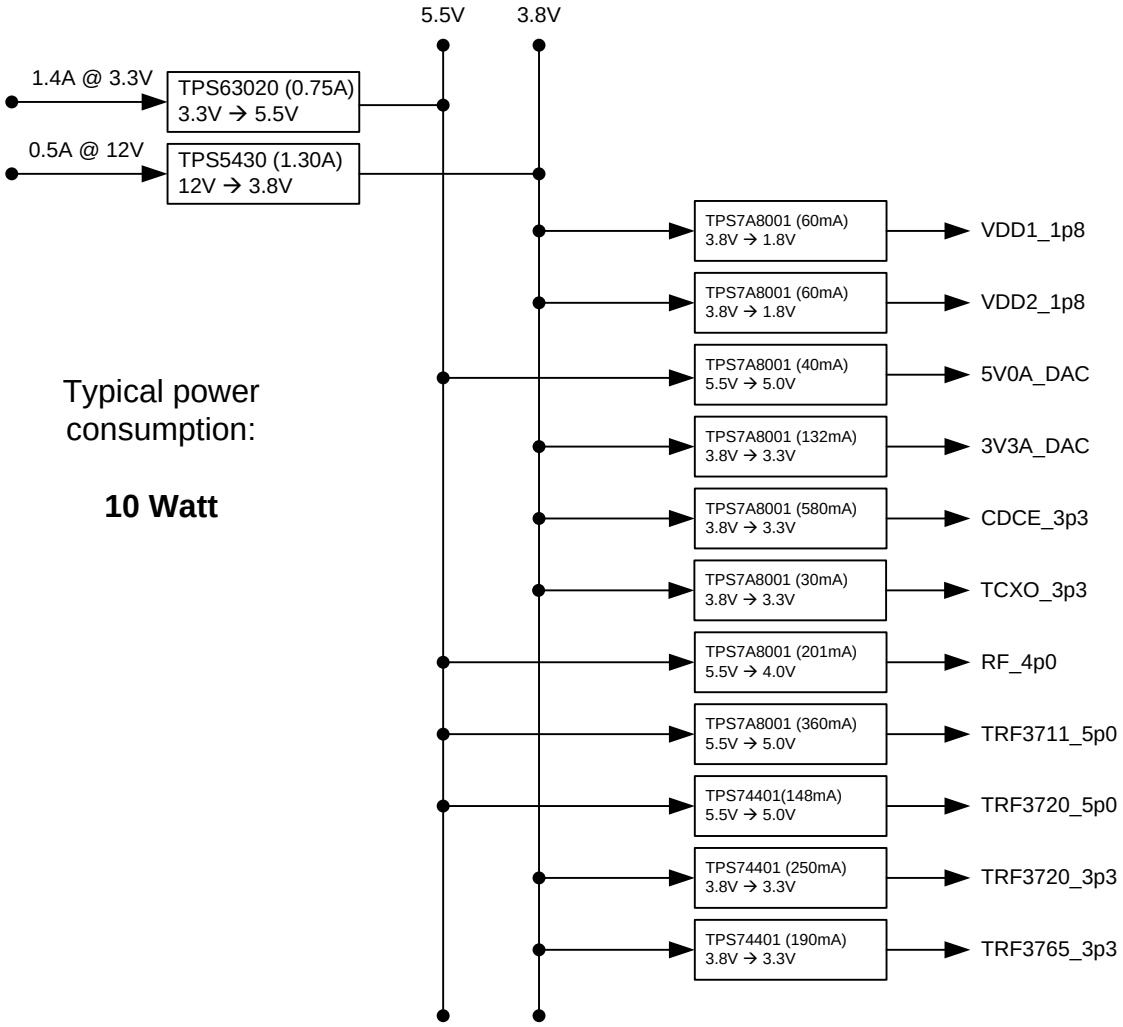



**Figure 7: FMC30RF Power Supply Architecture**

# 8 Environment

## 8.1 Temperature

Operating temperature:

- -40˚C to +85˚C (Industrial)

Storage temperature:

- -40˚C to +120˚C

## 8.2 Monitoring

The AMC7823 device may be used to monitor the voltage on the different power rails as well as the temperature. It is recommended that the carrier card and/or host software uses the power-down features in the devices in the case the temperature is too high. Normal operations can resume once the temperature is within the operating conditions boundaries.

| Parameter: | Voltage | Formula |
|---|---|---|
| Channel 0 | 5.0V Analog DAC | 2 * ADC0 |
| Channel 1 | 3.3V Digital/Clock | 2 * ADC1 |
| Channel 2 | 1.8V Analog/Digital | 2 * ADC2 |
| Channel 3 | 4.0V RF | 2 * ADC3 |
| Channel 4 | 5.0V Analog | 2 * ADC4 |
| Channel 5 | 3.3V Analog | 2 * ADC5 |
| Channel 6 | 3.3V TCXO | 2 * ADC6 |
| Channel 7 | VADJ | 2 * ADC7 |
| Temperature (Ch 8) | | |

**Table 5: Temperature and voltage parameters**

## 8.3 Cooling

Two different types of cooling will be available for the FMC30RF.

### 8.3.1 Convection cooling

The air flow provided by the chassis fans the FMC30RF is enclosed in will dissipate the heat generated by the on board components. A minimum airflow of 300 LFM is recommended.

For stand alone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC and ensure that the temperature of the devices is within the allowed range. 4DSP's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

### 8.3.2 Conduction cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions the junction temperature of power consuming devices will exceed the operating conditions recommended by the devices manufacturers (mostly +85˚C).

The FMC30RF is designed for maximum heat transfer to conduction cooled ribs. A customized cooling frame that connects directly to the surface of the devices is allowed (contact 4DSP for detailed mechanical information).

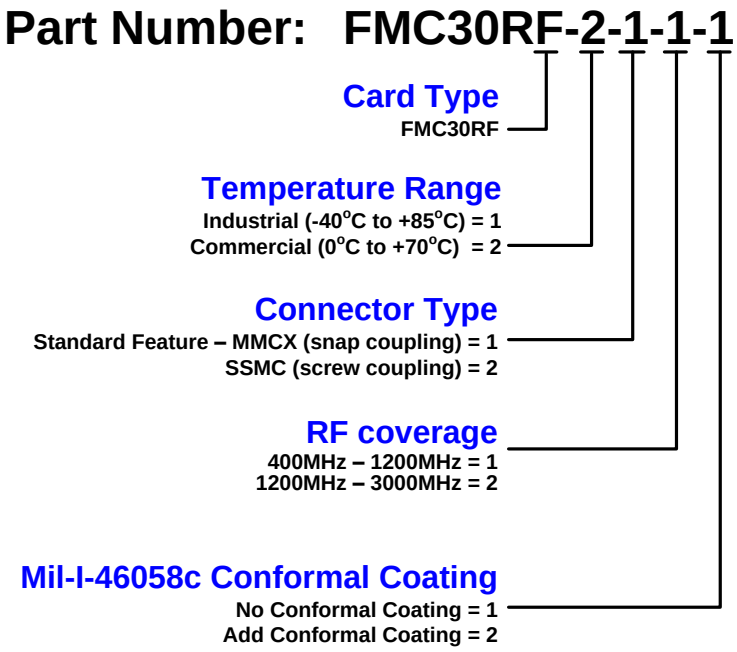
# 9 Safety

This module presents no hazard to the user.

# 10 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

# 11 Ordering information




# 12 Warranty

| | *Hardware* | *Software/Firmware* |
|---|---|---|
| Basic Warranty (included) | 1 Year from Date of Shipment | 90 Days from Date of Shipment |
| Extended Warranty (optional) | 2 Years from Date of Shipment | 1 Year from Date of Shipment |

# Appendix A LPC pin-out FMC30RF

| FMC label | FMC30RF Signal | Description |
|---|---|---|
| CLK0_M2C_N | CLK_TO_FPGA_N | Output from CDCE62005 |
| CLK0_M2C_P | CLK_TO_FPGA_P | Output from CDCE62005 |
| LA00_N_CC | ADC_DCLKOUT_N | Connects to AFE7225 |
| LA00_P_CC | ADC_DCLKOUT_P | Connects to AFE7225 |
| LA01_N_CC | ADC_FCLKOUT_N | Connects to AFE7225 |
| LA01_P_CC | ADC_FCLKOUT_P | Connects to AFE7225 |
| LA02_N | ADCB_DATA1_N | Connects to AFE7225 |
| LA02_P | ADCB_DATA1_P | Connects to AFE7225 |
| LA03_N | ADCB_DATA0_N | Connects to AFE7225 |
| LA03_P | ADCB_DATA0_P | Connects to AFE7225 |
| LA04_N | ADCA_DATA1_N | Connects to AFE7225 |
| LA04_P | ADCA_DATA1_P | Connects to AFE7225 |
| LA05_N | ADCA_DATA0_N | Connects to AFE7225 |
| LA05_P | ADCA_DATA0_P | Connects to AFE7225 |
| LA06_N | DAC_FCLKIN_N | Connects to AFE7225 |
| LA06_P | DAC_FCLKIN_P | Connects to AFE7225 |
| LA07_N | DACA_DATA1_N | Connects to AFE7225 |
| LA07_P | DACA_DATA1_P | Connects to AFE7225 |
| LA08_N | DACA_DATA0_N | Connects to AFE7225 |
| LA08_P | DACA_DATA0_P | Connects to AFE7225 |
| LA09_N | DACB_DATA0_N | Connects to AFE7225 |
| LA09_P | DACB_DATA0_P | Connects to AFE7225 |
| LA10_N | DAC_DCLKIN_N | Connects to AFE7225 |
| LA10_P | DAC_DCLKIN_P | Connects to AFE7225 |
| LA11_N | DAC_SYNCIN_N | Connects to AFE7225 |
| LA11_P | DAC_SYNCIN_P | Connects to AFE7225 |
| LA12_N | DACB_DATA1_N | Connects to AFE7225 |
| LA12_P | DACB_DATA1_P | Connects to AFE7225 |
| LA13_N | LNA_BYPASS_CTRL | '0' = 2nd LNA is excluded from the RX path<br>'1' = 2nd LNA is included in the RX path |
| LA13_P | TRX_SWITCH_CTRL | Behavior on RF I/O connector;<br>'0' = RF I/O connector is receiving (RX)<br>'1' = RF I/O connector is transmitting (TX)<br>Behavior on RF IN connector;<br>'0' = RF IN connector is disconnected<br>'1' = RF IN connector is receiving (RX) |
| LA14_N | RF_ATT_V1 | Connects to SKY12329-350LF V1 |
| LA14_P | RF_ATT_V2 | Connects to SKY12329-350LF V2 |
| LA15_N | TRF3765_CS# | Connects to TRF3765 STROBE |

| | | |
|---|---|---|
| LA15_P | AFE7225_RESET | Connects to AFE7225 RESET |
| LA16_N | AFE7225_CS# | Connects to AFE7225 SEN |
| LA16_P | AFE7225_PD | Connects to AFE7225 PDN |
| LA17_N_CC | RF_ATT_V4 | Connects to SKY12329-350LF V4 |
| LA17_P_CC | RF_ATT_V3 | Connects to SKY12329-350LF V3 |
| LA18_N_CC | AMC7823_CS# | Connects to AMC7823 SS |
| LA18_P_CC | AMC7823_RESET# | Connects to AMC7823 RESET |
| LA19_N | CDCE62005_LOCK | Connects to CDCE62005 PLL_LOCK |
| LA19_P | TRF3765_LOCK | Connects to TRF3765 LD |
| LA20_N | RF_ATT_V5 | Connects to SKY12329-350LF V5 |
| LA20_P | TRF3720_LOCK | Connects to TRF3720 LD |
| LA21_N | SCLK | Connects to:<br>- CDCE62005 SPI_CLK<br>- TRF3765 CLOCK<br>- TRF3720 CLK<br>- TRF3711 CLOCK<br>- AFE7225 SCLK<br>- AMC7823 SCLK |
| LA21_P | TRF3720_CS# | Connects to TRF3720 LE |
| LA22_N | RX_VCO_CTRL | Behavior on RX CLK connector;<br>‘0’ = RX CLK connector is VCO output from TRF3765 LO4_OUT<br>‘1’ = RX CLK connector is VCO input to TRF3765 EXTVCO_IN |
| LA22_P | TRF3720_PS | Connects to TRF3720 PS |
| LA23_N | TX_VCO_CTRL | Behavior on TX CLK connector;<br>‘0’ = TX CLK connector is VCO output from TRF3720 LO_OUT<br>‘1’ = TX CLK connector is VCO input to TRF3720 EXT_VCO |
| LA23_P | TRF3711_PD# | Connects to TRF3711 CHIP_EN |
| LA24_N | TRF3711_CS# | Connects to TRF3711 STROBE |
| LA24_P | SDATA | Connects to<br>- CDCE62005 MOSI<br>- TRF3765 DATA<br>- TRF3720 DATA<br>- TRF3711 DATA<br>- AFE7225 SDATA<br>- AMC7823 MOSI |
| LA25_N | TRF3711_GAIN_B0 | Connects to TRF3711 GAIN_B0 |
| LA25_P | TRF3711_GAIN_B1 | Connects to TRF3711 GAIN_B1 |
| LA26_N | CDCE62005_REFEN | Behavior on on-board reference clock;<br>‘0’ = the on-board reference clock is powered down<br>‘1’ = the on-board reference clock is enabled |
| LA26_P | TRF3711_GAIN_B2 | Connects to TRF3711 GAIN_B2 |
| LA27_N | CDCE62005_SDOUT | Connects to CDCE62005 MISO |
| LA27_P | AFE7225_SDOUT | Connects to AFE7225 SDOUT |
| LA28_N | CDCE62005_PD# | Connects to CDCE62005 POWER_DOWN |
| LA28_P | CDCE62005_SYNC# | Connects to CDCE62005 SYNC |
| LA29_N | TRF3720_SDOUT | Connects to TRF3720 RDBK |

| | | |
|---|---|---|
| LA29_P | TRF3711_SDOUT | Connects to TRF3711 READBACK |
| LA30_N | AMC7823_SDOUT | Connects to AMC7823 MISO |
| LA30_P | CDCE62005_CS# | Connects to CDCE62005 SPI_LE |
| LA31_N | AMC7823_GALR# | Connects to AMC7823 GALR# |
| LA31_P | TRF3765_SDOUT | Connects to TRF3765 READBACK |
| LA32_N | | Not connected |
| LA32_P | | Not connected |
| LA33_N | | Not connected |
| LA33_P | | Not connected |
| PRSNT_M2C_L | PRSNT_M2C_L | Connects to GND |
| PG_C2M | PG_C2M | Connects to PS_EN |