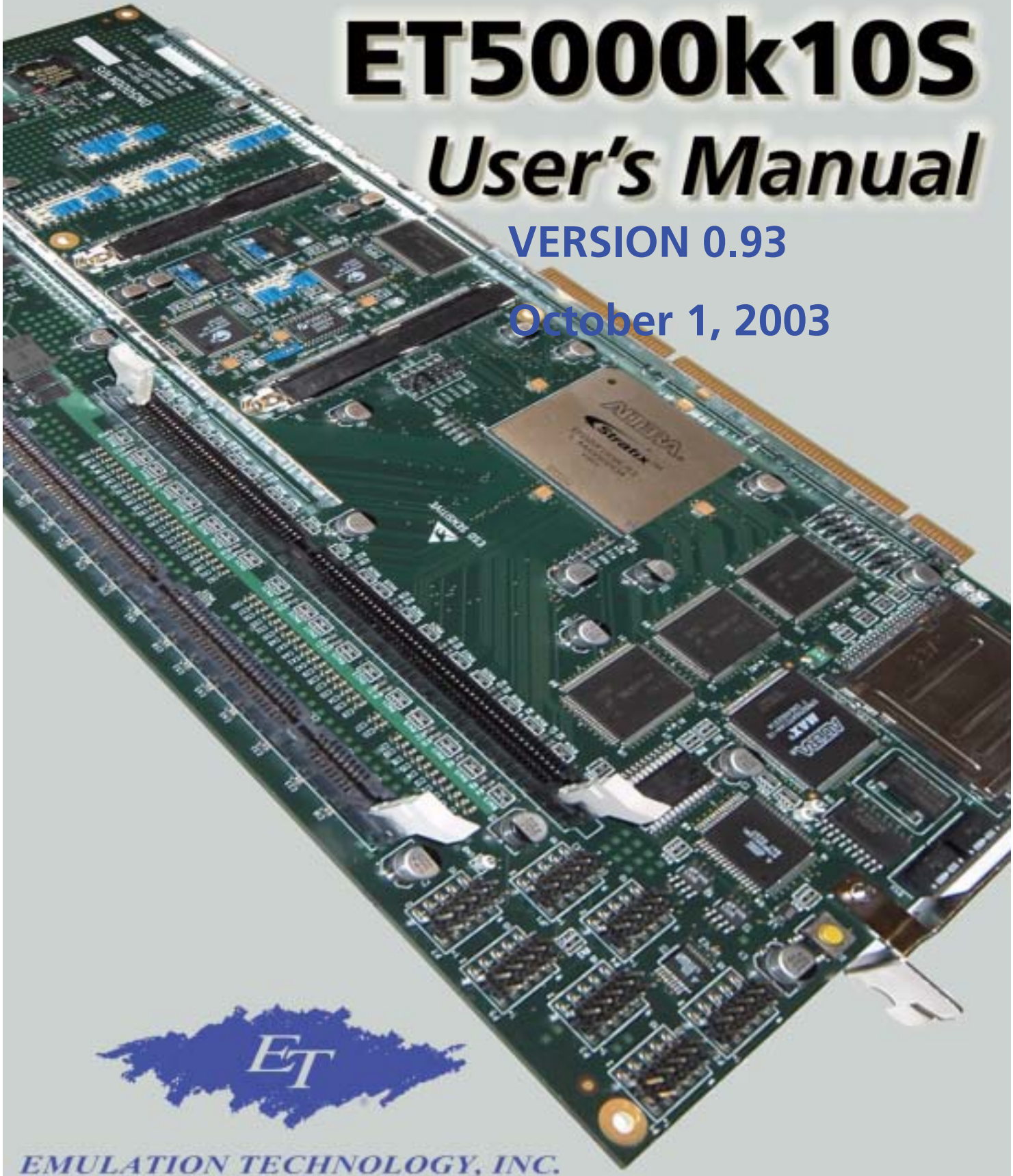
ET5000k10S

User's Manual

VERSION 0.93

October 1, 2003



EMULATION TECHNOLOGY, INC.

World Leader in Adapters, Clips, and Test Accessories

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Chapter 1

Getting Started

The ET5000k10S is sensitive to static electricity, so treat the PWB accordingly. The target market for this product is engineers that are familiar with FPGAs and circuit boards, so a lecture in ESD really isn't appropriate (and wouldn't be read anyway). However, we have sold some of these units to people who are not as familiar with this issue. The following web page has an excellent tutorial on the Fundamentals of ESD for those of you who are new to ESD-sensitive products:

http://www.esda.org/basics/part1.cfm.

Emulation Technology, Inc. Technical Support

The following means of technical support are available:

1. **The ET5000k10S User's Manual.** This is the main source of technical information. We strive to produce excellent documentation, and this manual should contain most of the answers to your questions.
2. The Emulation Technology Web Page. The web page will contain the latest manual, application notes, faq, articles, and any device errata and manual addenda. Please visit and bookmark: http://www.emulation.com.
3. E-Mail to support@emulation.com. You may direct questions and feedback to Emulation Technology using this e-mail address.
4. Phone Support. We are happy to help. Call us at 1-800-ADAPTER during the hours of 8:00 A.M. to 5:00 P.M. Pacific Time. Some of us get in early and stay late, so you might try us outside of these hours also.
5. Frequently Asked Questions. In the downloads section of our web page you can find a document called ET5000k10/S Frequently Asked Questions (FAQ). We will update this document occasionally with information that may not be in the User's Manual.

Relevant Information

Information about PCI can be obtained from the following sources:

The PCI Special Interest Group has a web page that has lots of good stuff. Copies of the latest PCI specification may be ordered here.

http://www.pcisig.com/
PCI Special Interest Group
2575 NE Kathryn St. #17
Hillsboro, OR 97124
FAX: (503) 693-8344

As of June 2003, the most current versions of the PCI Specifications are:

PCI Local Bus Specification, Revision 3.0
PCI Hot-Plug Specification, Revision 2.0
PCI Power Management Interface Specification, Revision 1.1
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a

Other recommended specifications include:

PCIMG 2.0 Compact PCI Specification, Revision 2.1 (or greater)
PCI Industrial Computer Manufacturers Group (PICMG)
401 Edgewater Place, Suite 500
Wakefield, MA 01880, USA
TEL: 781-224-1100
FAX: 781-224-1239
http://www.picmg.org

The best book to get if you need an introduction to PCI is:

PCI System Architecture
Fourth Edition
MindShare, Inc.
Tom Shanley and Don Anderson

Ignore some of the ignorant statements made in the Customer Review section at **http://www.amazon.com/**. This is an excellent book for PCI and well worth the money.

The best book to get if you need an introduction to PCI-X is:

PCI-X System Architecture
MindShare, Inc.
Tom Shanely and Karen Gettman

You are going to need to know Verilog or VHDL to use the Stratix FPGA. If you need a reference, we recommend the following book for Verilog:

Verilog HDL: A Guide to Digital Design and Synthesis
Samir Palnitkar
ISBN: 0-13-451675-3

If you are one of those people that actually like VHDL, we feel sorry for you. The following books may be helpful:

Essential VHDL: RTL Synthesis Done Right
Sundar Rajan

The IQ Booster: Improve Your IQ Performance Dramatically
Edwin Breecher

Conventions

This manual uses the following conventions. An example illustrates each convention.

- The term PCI-X will be used generically unless there is a specific instance where PCI applies.
- This design guide generically refers to PCI-X protocol.

- `Courier font` denotes the following items:
  - Signals on PCI Bus side of the PCI-X Interface

    `FRAME_IO` (PCI-X Interface signal name)

    `FRAME#` (PCI-X Bus signal name)
  - Signals within the user application

    `BACK_UP, START`
  - Command line input and output

    `setenv XIL_MAP_LOC_CLOSED`
  - HDL pseudocode

    ```
    assign question = to_be | !to_be;

    assign cannot = have_cake & eat_it;
    ```
  - Design file names

    `pcim_top.v, pcim_top.vhd`
- **`Courier bold`** denotes the following items:
  - Signals on the user side of the LogiCORE PCI-X Interface

    `ADDR_VLD`
  - Menu selections or button presses

    `FILE -> OPEN`
- Italic font denotes the following items:
  - Variables in statements which require user-supplied values

    ngdbuild *design_name*
  - References to other manuals

    See the *Libraries Guide* for more information.
  - Emphasis in text

    It is not a bug, it is a *feature*.
- Dark shading indicates items that are not supported or reserved:

SDONE_I	in/out	Snoop Done signal. Not Supported.

- Square brackets "[ ]" indicate an optional entry or a bus index:

  ngdbuild [*option_name*] *design_name*

DATA[31:0]

- A vertical or horizontal ellipsis indicates repetitive material that has been omitted.

  A B C... X Y Z

- The use of "`fn(SIG1. . . SIGn)`" in an HDL pseudocode fragment should be interpreted as "combinational function of signals SIG1 through SIGn.

  SUM = fn(A, B, Cin);

- The prefix "`0x`" or the suffix "`h`" indicate hexadecimal notation.

  A read of address `0x00110373` returned `45524943h`.

- A "#" an "_n" , an "n" or a "–" means the signal is active low

  `INT#` is active low.

  `fpga_inta_n` is active low.

  `SRAMCS–` is active low.

  `FPGA_GRSTn` is active low.

Chapter 2

ET5000k10S Features, Overview and General Description

ET5000k10S Features

The ET5000k10S features include:

- 32/64-bit, +3.3V, PCI/PCI-X-based PWB with a single Altera Stratix™ FPGA (FBGA1508).
  - Device availability: EP1S80, EP1S60 and EP1S40
  - ~450,000 ASIC gates (with EP1S80 — LSI standard)

Device	I/O	Flip-Flops	18 x 18 Multipliers	Embedded Memory		
				M512 RAM	M4K RAM	M-RAM
EP1S40	822	41,250	56	384	183	4
EP1S60	1022	57,120	72	574	292	6
EP1S80	1203	79,040	88	767	364	9

- Fast/Easy FPGA configuration via standard SmartMedia FLASH card
  - Microprocessor controlled (ATmega128L)
  - RS232 port for configuration/operation status and control
  - Fastest possible configuration speed (via Passive Parallel method)
- 10A on-board linear regulator for +3.3V and +1.5V
  - Standalone operation via separate power connector
  - +3.3V not needed on backplane
- 6 low skew clocks distributed to the FPGA and test connectors:
  - 2 CY7B993/4 RoboclockII PLLs
  - 2 socketed oscillators
  - PCI Clock
  - 1 dividable clock via CPLD
- Robust observation/debug with 242 connections for logic analyzer observability or for pattern generator stimulus.
- Status LEDs.
- User-designed daughter PWB for custom circuitry and interfaces.

- SignalTap and Identify (from Synplicity) fully supported via JTAG interface.

Figure 2-1 shows a block diagram of the ET5000k10S.

ET5000k10S Description

The ET5000k10S is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The ET5000k10S can be hosted in a 32/64-bit PCI/PCI-X slot, or can be used as a stand-alone device. A single ET5000k10S stuffed with a single EP1S80 can emulate up to 450,000 gates of logic as measured by LSI. A high I/O-count, 1508-pin, flip-chip BGA package is employed. The F1508 package has 1203 I/Os, which allows for abundant connections to daughter connectors and external memories. A total of 242 test pins are provided on the top of the PWB via high-density connectors for logic analyzer-based debugging, or for pattern generator stimulus. Custom daughter cards such as the ET3k10SD can be mounted to these connectors as a means of interfacing the ET5000k10S to application-specific circuits. A reference 32-bit PCI target design and test bench is provided in Verilog and VHDL at no additional cost.

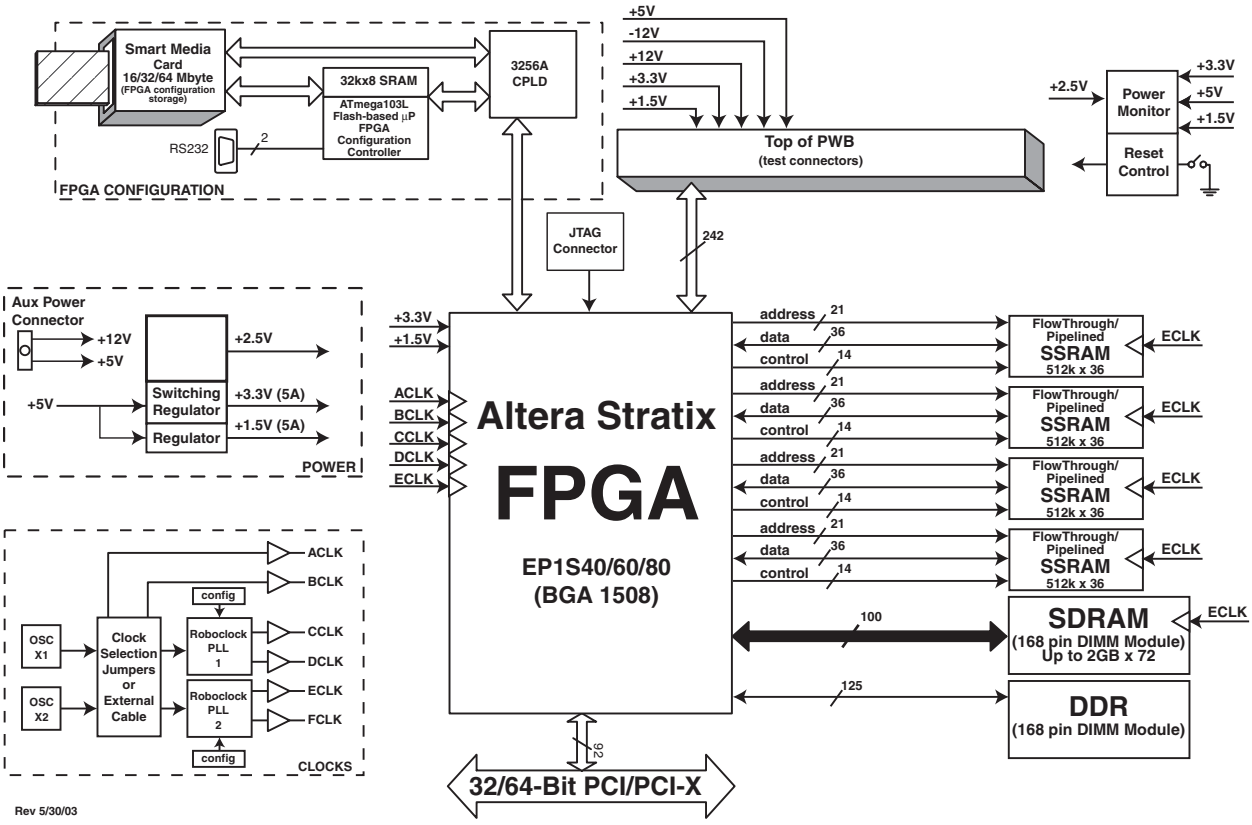


Figure 2-1 ET5000k10S Block Diagram

Easy Configuration via SmartMedia

The configuration bit files for the FPGA are copied onto a 32-megabyte SmartMedia FLASH card (provided) and an on-board microprocessor controls the FPGA configuration process. Visibility into the configuration process is enhanced with an RS232 port. FPGA configuration runs quickly at 48 MHz. Eight LEDs provide instant status and operational feedback. Four of these LEDs are connected to the CPLD and can be user-configured.

FPGA — Stratix (U11, F)

The ET5000k10S contains one Stratix™ FPGA. The package is a flip chip fine-pitch BGA with 1508 pins (F1508). The pitch on the pins is 1 mm. This isn't important, but this pin density makes the PWB a bitch to layout. Keep that in mind if you try to make one of these at home. Most of the 1203 I/O pins are utilized on the F1508 package. The standard speed grade we stuff is –7. We can use the –6 speed grade, but don't fall out of your chair when you get the price. Note that Altera seems to have cancelled plans for the EP1S120. Although this part appears in some Altera literature, we haven't seen any scheduled release date or other documentation for it. Don't expect to see anything larger than the EP1S80 until at least the 2004 time frame. Table 2-1 shows the stuffing options for the ET5000k10S.

Table 2-1 ET5000k10S Stuffing Option Comparison

Stuffed FPGA	SSRAMs	SDRAM	DDR SDRAM	Total Header Connections
EP1S40_1508	3	1	1	77
EP1S60_1508	3	1	1	180
EP1S80_1508	4	1	1	242

The following is a very brief overview of the Stratix family. More information can be gleaned from the Stratix Datasheet (`ds_stx.pdf`). This file is on the CD-ROM supplied with the ET5000k10S, but you are better off getting the latest version from the Altera Web page (**http://www.altera.com/**). Make sure to get the latest errata sheet also.

Flip-Flops and LUTs

Figure 2-2 shows what Altera calls a Logic Element, or LE. Each LE contains a flip-flop and a 4x1 look-up table (LUT). LEs are arranged in groups of 10, called Logic Array Blocks (LAB). The EP1S80 is an array of LABs with 91 rows and 101 columns, but there are 9 RAM blocks which appear in place of 13-row by 11-column sections of the grid, leaving a total of 7904 LABs and 19040 LEs. (Other blocks, such as DSP/multiplier blocks and smaller RAM, are arranged in entire columns squeezed between two LAB columns.)

Each LUT can implement any Boolean function of four inputs. An LUT can also be configured as a two-input adder/subtractor with a carry chain coming from the adjacent LE and going to the next LE. In order to reduce delays caused by long carry chains, each set of 5 LEs computes two adder

results simultaneously, then uses the carry result from the previous set of 5 to select which result is correct.

The flip-flop in each LE includes a clock enable input, an asynchronous preset and reset, synchronous set and reset logic, and an asynchronous load function. Data input can come from the LUT in the same LE to register addition or boolean outputs, or the LUT and flip-flop can be used independently of each other. For more information, check **www.altera.com** for the Stratix datasheet.

Embedded Memory

Stratix has boatloads of embedded memory. The EP1S80 contains 767 blocks of 576 bits, 364 blocks of 4.5 Kbits, and 9 blocks of 576 Kbits. The smallest memory blocks (called M512 RAM) can be configured for data widths ranging from 32 x 18 bits to 512 x 1 bit; medium-sized blocks (M4K RAM) can be configured ranging from 128 x 36 bits to 4K x 1 bit; and the largest blocks (M-RAM) can be configured anywhere from 4K x 144 bits to 64K x 9 bits. The embedded memory is dual-ported, and can be used to construct almost any type of memory - FIFOs, dual-port RAMs, single-port RAMs, etc.

The two largest blocks, M-RAM and M4K RAM, are fully dual-ported memory, with read and write functions available on two separately clocked ports. M512 RAM is a "simple dual-port" memory, meaning that

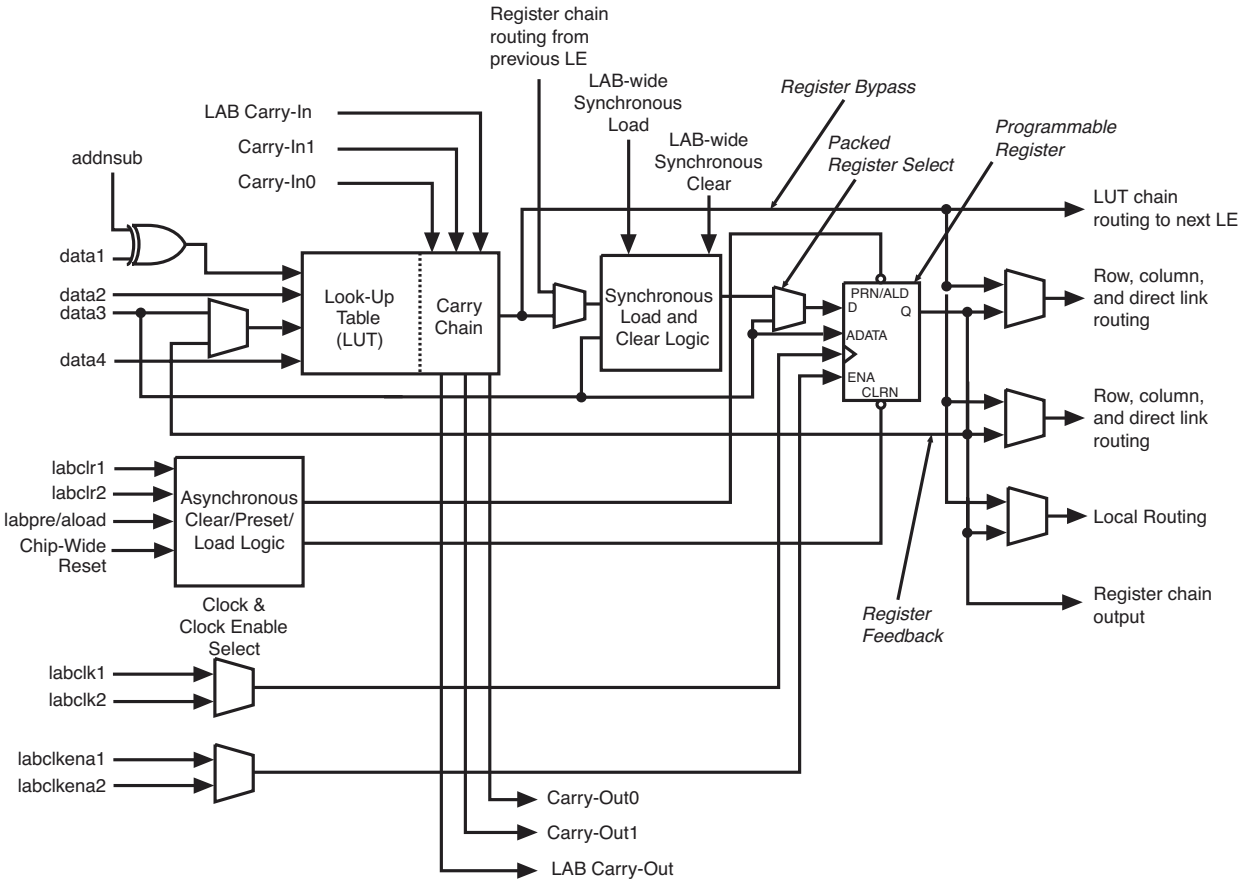


Figure 2-2 General LE Diagram

one port is write-only and the other is read-only. Any of the memory blocks can be configured as simple dual-port or single-port memory. See Figure 2-3 for a diagram of the memory.

Multipliers

Stratix devices feature a large number of multipliers grouped into what Altera calls DSP blocks (see Figure 2-4). The EP1S80 contains 22 DSP blocks, each of which can provide one 36x36 bit multiplier, four 18x18 bit multipliers, or eight 9x9 bit multipliers. Each block also contains adder/subtractor/accumulator registers which can be configured to provide many common DSP functions, such as FIR or IIR filters, FFT, or DCT, without the use of LAB resources. The Stratix datasheet (available at **www.altera.com**) has more detailed information on how the multipliers and adders are configured for some common functions.

Figure 2-4 shows a DSP block configured for four 18x18 bit multipliers. A DSP block can be configured as two parallel systems of 9x9 bit multipliers, each of which is also described by Figure 2-4. The adder blocks can be used to add or subtract two or four multipliers, such as in complex multiplication, or to add a new result each clock cycle to an accumulated sum. They are also used to configure the DSP block as a 36x36 bit multiplier, with or without an accumulator.

All registers in Figure 2-4 are optional, as shown by Figure 2-5, which is a detailed view of a single 18x18 bit or 9x9 bit multiplier. Any or all of the registers may be used to pipeline the multiplier logic and improve the clock speed, or the alternate path may be used to bypass the register.

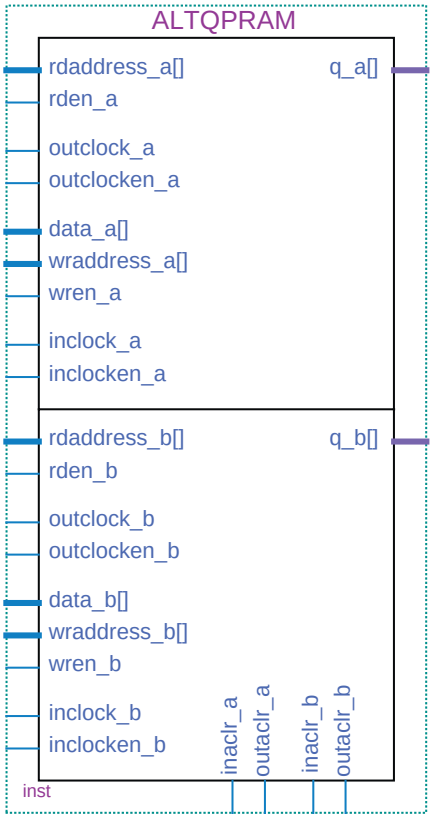


Figure 2-3 Dual-Port Data Flows

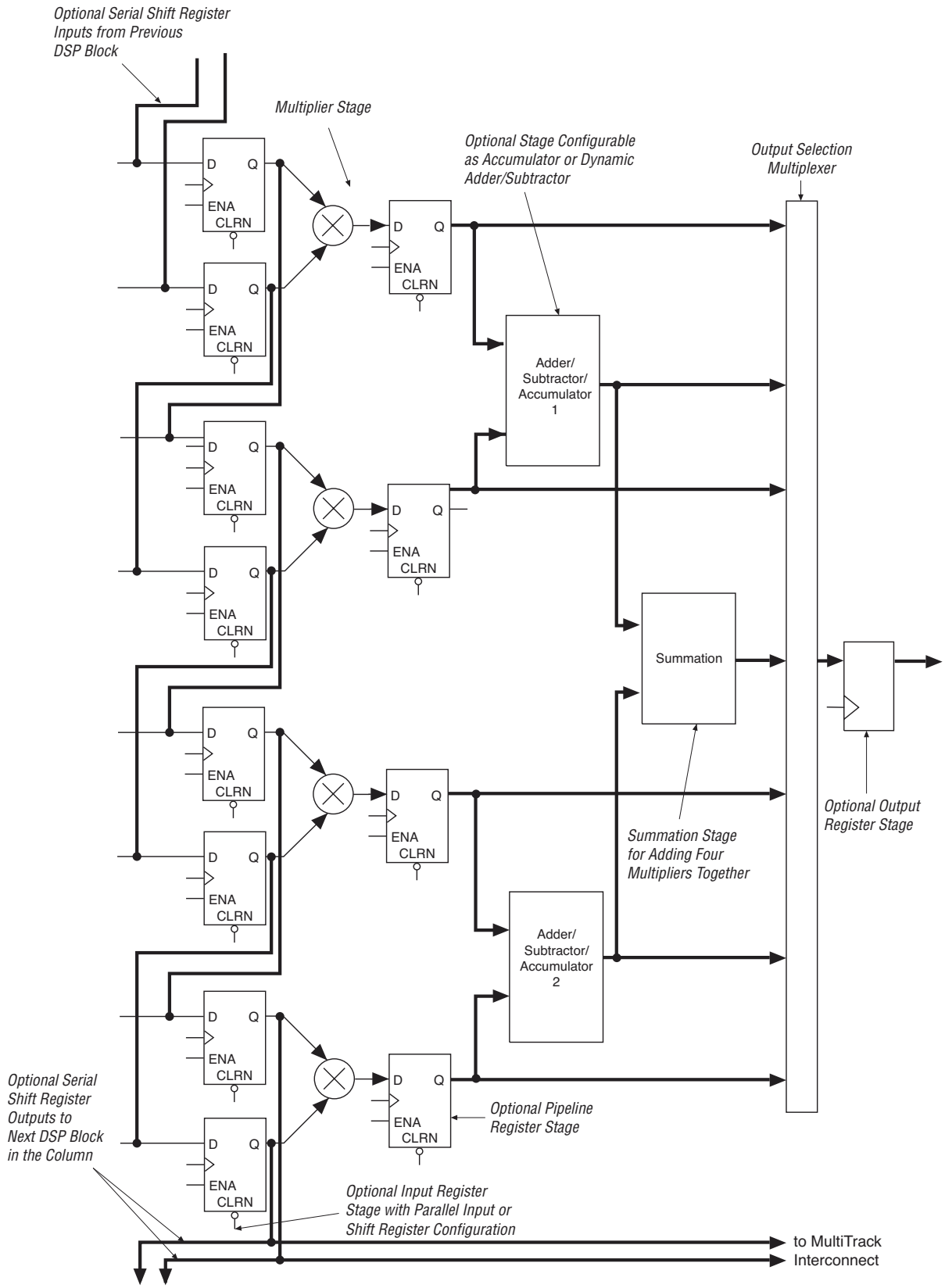


Figure 2-4 DSP Block Diagram

Figure 2-5 also shows more detail about the optional shift register path, which makes FIR or IIR filters easy to implement.

Most synthesis tools will accept Verilog or VHDL descriptions of multpliers and infer a DSP block with the appropriate configuration. For those that don't, Altera provides a megafunction generator to help with direct instantiation of the hardware resources. See "Synthesis and Emulation Issues" on page 24 for more detail.

I/O Issues

Terminator technology is supported on all pins. The resistors used for RDN and RUP should be 250 ohms for series termination or impedance matching I/O standards. Parallel termination requires 1000 ohm resistors for RDN and RUP. Terminator technology is a very nice feature and we recommend you use it on all I/O signals. The default IO_STANDARD attribute for the `.csf` file is **LVTLL**.

All VCCO pins are connected to either +3.3 V or +2.5 V. The VREF pins are connected to +1.5 V or +2.5 V, so the ET5000k10S does not support I/O standards that require other values of VREF. So the I/O standards supported are:

LVTTL — Low-Voltage TTL
The low-voltage TTL, or LVTTL, standard is a general-purpose EIA/JESDSA

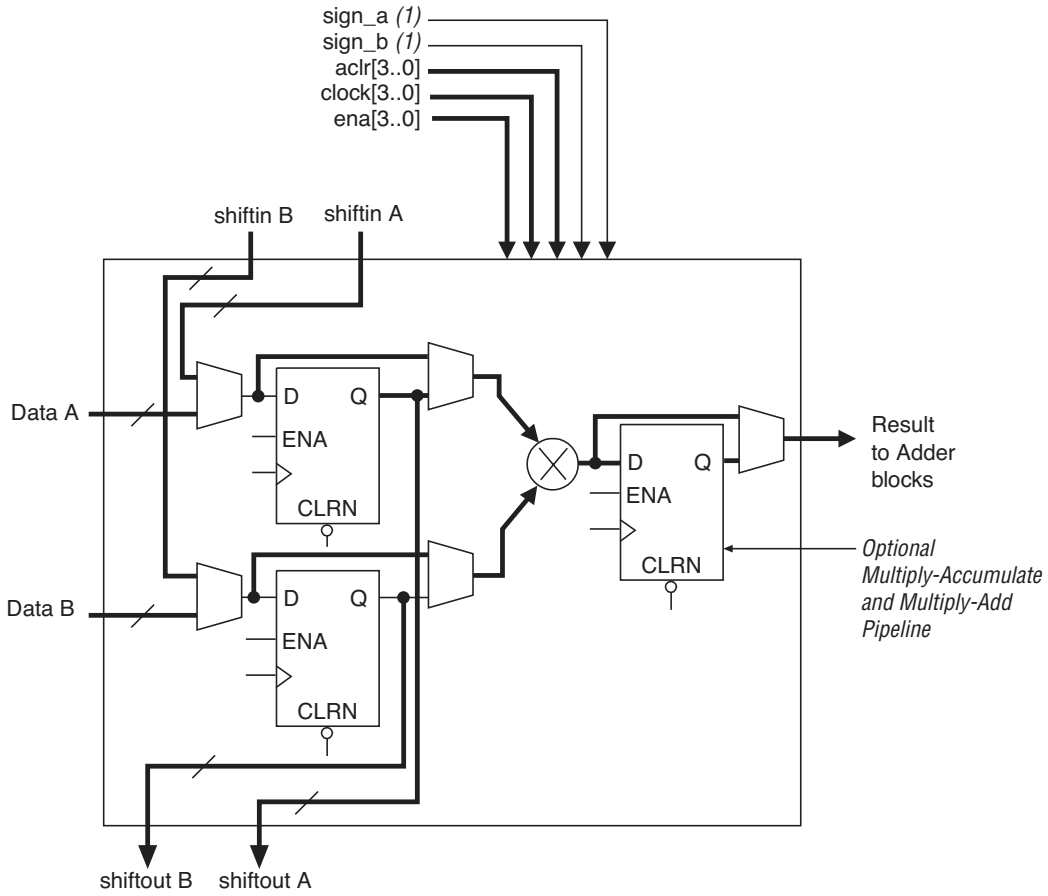


Figure 2-5 Multiplier Sub-Component Block Diagram

standard for 3.3 V applications that use the LVTTL input buffer and a Push-Pull output buffer. The standard requires a 3.3 V input and output source voltage (V_{CCO}) but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS33 — 3.3 Volt Low-Voltage CMOS
This standard is an extension of the LVCMOS standard (JESD8. –5). It is used in general-purpose 3.3 V applications. The standard requires a 3.3 V input/output source voltage (V_{CCO}) but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

PCI-X — Peripheral Component Interface
The PCI standard specifies support for 33 MHz, 66 MHz and 133 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}); however, it does require 3.3 V input output source voltage (V_{CCO}).

SSTL-3 class I and II
SSTL-3 uses a series termination resistor on output signals and a parallel termination resistor on input signals. Stratix devices use a VREF of +1.5V to enable the appropriate resistors internally. Because SSTL-3 requires parallel termination, it is only available on banks 3, 4, 7 and 8, and on clock output signals.

CTT
CTT uses a parallel termination resistor on input signals, with no termination resistors on output signals. Stratix devices use a VREF of +1.5V to enable the appropriate resistors internally. Because CTT requires parallel termination, it is only available on I/O banks 3, 4, 7 and 8, and on clock output signals.

SSTL-2 Class I & II
The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed DDR SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operation in conditions where a bus must be isolated from large stubs.

Differential SSTL-2
The differential SSTL-2 I/O standard is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard does not require an input reference voltage differential.

Bitstream Encryptions

Stratix devices have no special bitstream encryption function. Emulation Technology, Inc. may be able to assist with scrambling bitfiles to protect IP on the SmartMedia card, which would then be descrambled in the programming CPLD. Users should be aware, however, that the bitstream would be unprotected between the CPLD and FPGA, so they could still be examined and reverse-engineered. Our ET3000k10 products use Xilinx FPGAs which can be used to decrypt the bitstream inside the FPGA,

providing complete design protection. If you are interested in this feature, please be aware that there are some issues with the Xilinx encryption feature, described in the ET3000k10 FAQ on our website.

µP and FPGA Configuration

The ET5000k10S has an ATmega128L microprocessor (µP) that is used to control the configuration process (**U4**). The amount of internal SRAM (4 Kbytes) was not large enough to hold the FAT needed for SmartMedia, so an external 32 k x 8 SRAM was added. The address latching function is done via an LVT373 (**U1**).

The microprocessor has the following responsibilities:

- Reading the SmartMedia card
- Configuring the Stratix FPGA
- Executing ET5000k10S self tests.

Other than FPGA configuration, the µP has no responsibilities. Less than 25% of the 128 Kbytes of FLASH is used for FPGA configuration and utilities, so you are welcome to use the rest of the resources of the µP for your own purposes. Instructions for customizing the µP are contained in the file `Custom_ATmega128L.pdf`. This file is on the cd-rom, or it can be downloaded from the Emulation Technology, Inc. web page.

REMEMBER: You can use the microprocessor for your own purposes!

We ship a programming cable for the ATmega128L with the ET5000k10S. Updates to the code will be posted on our web site. If you wish to do your own development you will need the compiler, which we do not ship with the product. The compiler is available from IAR (**http://www.iar.com/**). The part number is EWA90PCUBLV150.

Note that if you are willing to program the FPGA with the JTAG or serial cable, the CLPD and the µP have **no** function. In this case you can use all of the resources of the µP for your own purposes.

The µP: Some Details

The ATmega128L is gross overkill for the FPGA configuration function. The datasheet and user's manual are on the CD-ROM that was shipped with the ET5000k10S. The file names are `ATmega128_UM.pdf` and `ATmega128_DS.pdf`. But if you intend to use the µP for your own purposes, you should check the Atmel web page to get a copy of the latest user's manual, datasheet, and erratas. The Atmel web page is **http://www.eu.atmel.com/atmel/**. The ATmega128L is under the section called "Flash Microcontroller, AVR 8-Bit RISC." Most of the features are unused. A variety of test headers allow for possible use of these features. Each header and the various possible functions are described in the sections that follow. Figure 2-6 is a block diagram of the ATmega128L and its various interfaces on the ET5000k10S.

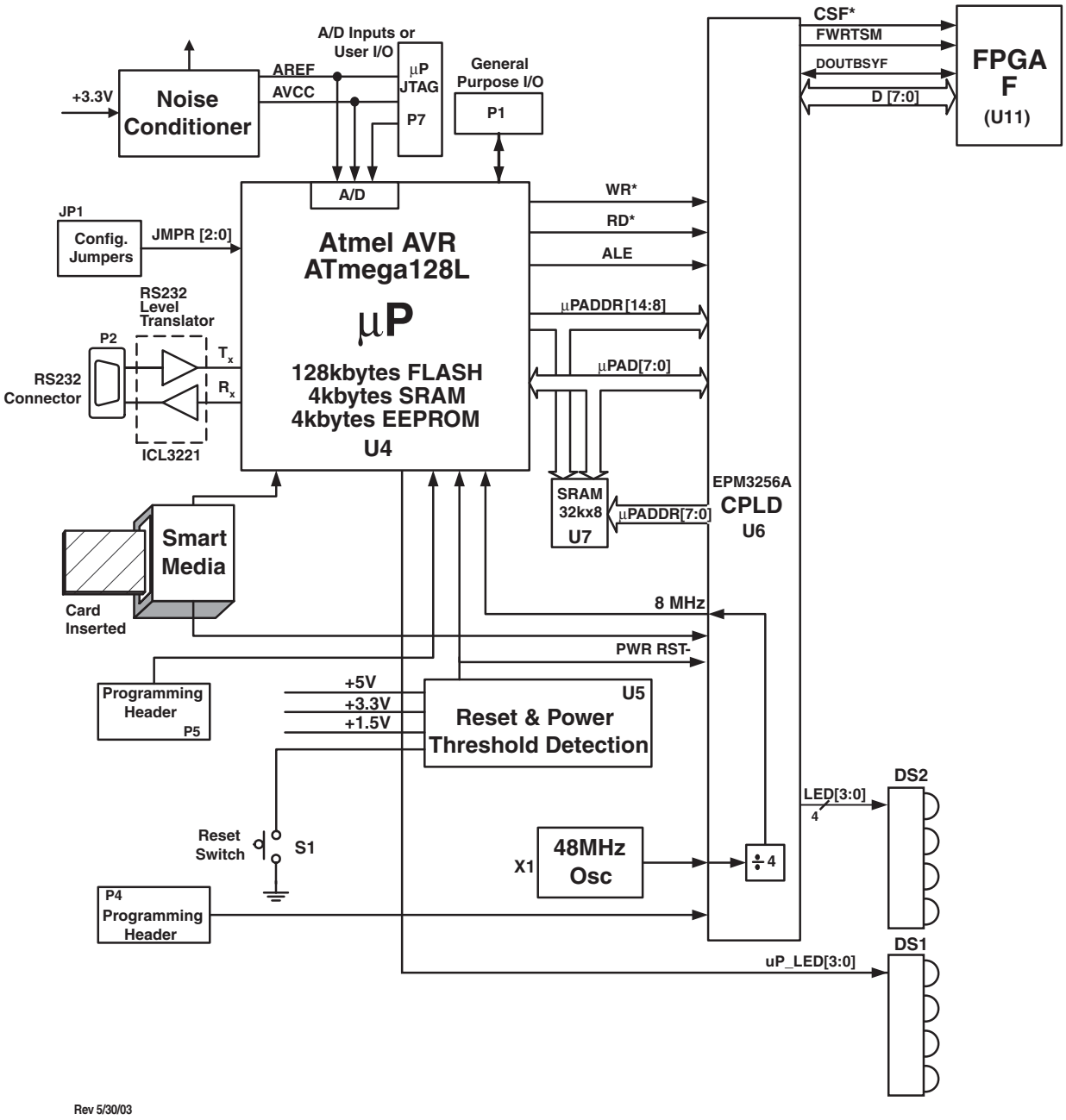


Figure 2-6 ET5000k10SBlock Diagram of ATmega128L and ET5000k10S Interfaces

P1: Unused µP Connections

P1 contains connections to the ATmega128L that were not used elsewhere. These ten connections can be used for external TTL connections to the µP, externally generated interrupts, or any other function that the ATmega128L supports on these pins. Remember that the ATmega128L is not +5 V tolerant, so if you attach external TTL signals to these pins, the voltage level of these signals must not exceed +3.3 V.

The **P1** schematic is shown in Figure 2-7.

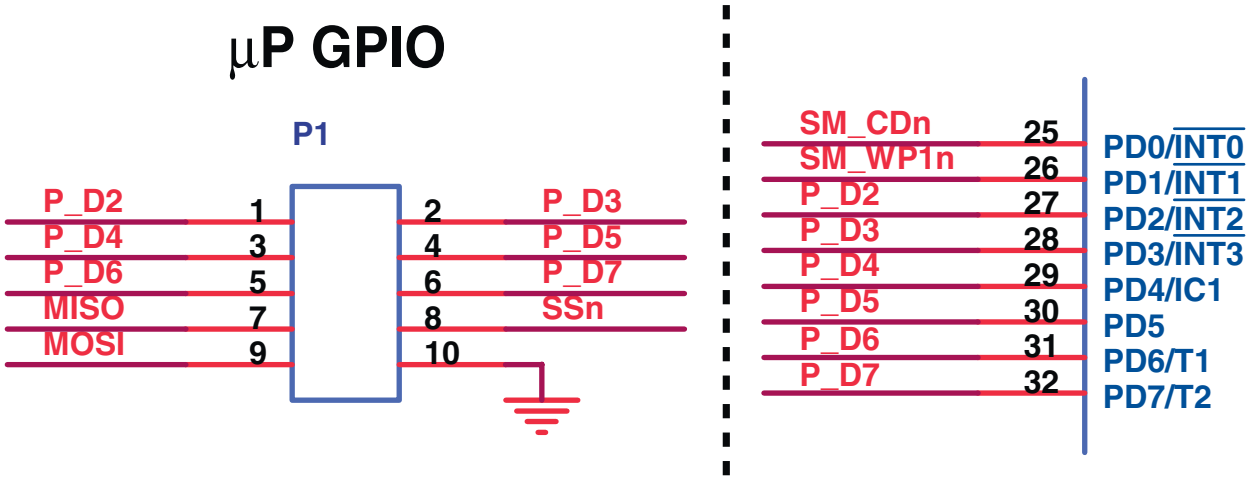


Figure 2-7 P1: Unused µP Connections

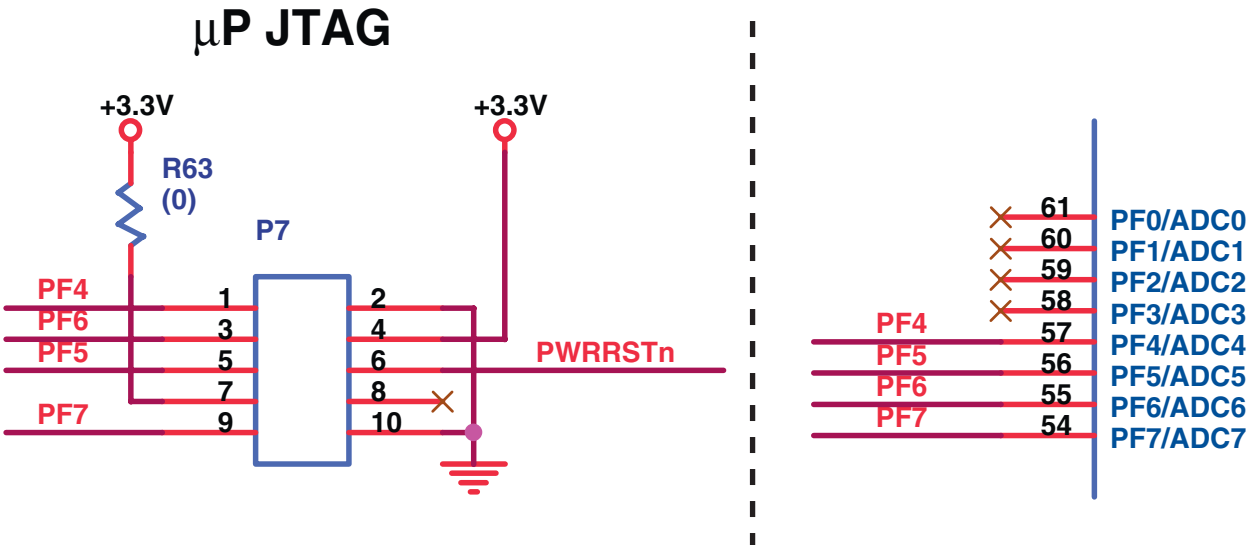


Figure 2-8 P7 JTAG Interface

ATmega128L JTAG Interface

The ATmega128L processor has a JTAG interface that can be used for on-chip debugging, real-time emulation, and programming of FLASH, EEPROM, fuses, and Lock Bits. In order to take advantage of the JTAG interface, you must have the Atmel AVR JTAG ICE kit (part number ATAVR-JTAGICE) and AVR studio software that Atmel provides free at

www.atmel.com. The JTAG interface for the ATmega128L can be accessed through header **P7** of the ET5000k10S (see Figure 2-8).

Programming the ATmega128L (U8)

A cable used to reprogram the ATmega128L is shipped with the ET5000k10S. You will need to reprogram the ATmega128L if we update the code or you intend to use the processor for your own application. **P5** is used for this purpose.

Figure 2-9 illustrates **P5**.

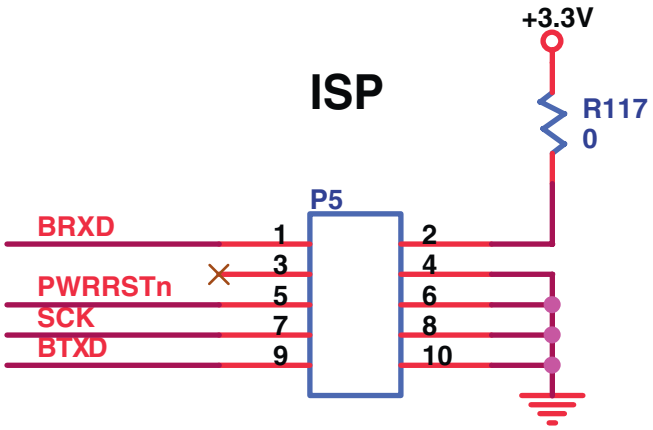


Figure 2-9 P5 Schematic

Detailed Instructions

1. Download the latest update for the processor and CPLD at **www.emulation.com** (file `uP_CPLD.zip`).
2. You will first need to reprogram the CPLD. Please see "CPLD—EPM3256A" on page 14 for instructions (use the file `*.jed` that can be found in the downloaded zip file.
3. Next, you will program the processor (ATmetga128L). Connect the AVR cable that was shipped with the ET5000k10S to header **P5** with the red/purple wire on the cable connected to pin 1 and connect the other end to the serial port of your PC.
4. In order to program the processor, you will need to install AVR Studio that is included on the CD that was shipped with the ET5000k10S. This software can also be downloaded at **www.atmel.com**.
5. From the Windows **START** menu, choose **PROGRAMS–>Atmel AVR Studio x.xx** (where x.xx is the version number).
6. Once AVR Studio is open, select **TOOLS–>STK500/AVRISP/JTAG ICE** and a new window should appear with the title **STK500**. At the bottom of the **STK500** window, if you see:

   ```
   Detecting…FAILED!
   ```

   that means either there is no power on the ET5000k10S, there is another program open that is using the serial port, or the serial cable connecting the AVR tool is not connected properly. If this happens,

you should close down the window titled **STK500**, correct the situation, and then select **TOOLS–>STK500/AVRISP/JTAG ICE** again. You will not be able to continue unless you see something very similar to the following at the bottom of the **STK500** window:

```
Detecting…AVRISP found on COM1:
Getting revisions…HW: 0x01, SW Major: 0x01, SW
Minor: 0x07…OK
```

7. On the **PROGRAM** tab, select the **ATmega128** under the **DEVICE** drop down menu, and in the **FLASH** section where it says **INPUT HEX FILE**, browse and select the file `ET5000k10S_128.a90` that can be found in the downloaded zip file (`uP_CPLD.zip`) from the Emulation Technology, Inc. website. To program the device all you need to do is hit the **PROGRAM** button in the **FLASH** section. When the programming is complete (it takes about 45 seconds) you should see a message at the bottom of the window that looks something like this:

```
Detecting…AVRISP found on COM1:
Getting revisions…HW: 0x01, SW Major 0x01, SW
Minor: 0x07…OK
Reading FLASH input file…OK
Setting device parameters, serial programming
mode…OK
Entering programming mode…OK
Erasing device…OK
Programming FLASH using block mode…100% OK
Leaving programming mode…OK
```

8. After programming the processor, close all AVR Studio windows and setup the serial port according to the section titled “Setting up the Serial Port (P2 — RS232 Port)” on page 17. Please note that in this situation, connecting the serial port is mandatory and the FPGA cannot be configured via the SmartMedia card until you have completed all the instructions in this section.

9. Reset the ET5000k10S by pressing **S1**. After about 5 seconds, you should see the following in the HyperTerminal window:

```
Please select the FPGA on the board:
```

Enter one of the FPGA locations on your board that contains an FPGA, and you should see the following menu:

```
1) Virtex II 1000 (FG456)
2) Virtex II 6000 (FF1152)
3) Virtex II 4000 (FF1152)
4) Virtex II 3000 (FG676)
5) Virtex II 8000 (FF1152)
6) Altera Apex II (2A40)
7) Altera Apex II (2A70)
8) Altera Stratix (EP1S80F1508C7)

  Please enter selection (1-6): for FPGA D:
```

Enter option 8 for Stratix FPGAs.

10. The processor and the CPLD are now ready to configure the FPGA(s). Please see the section titled "Starting Fast Passive Parallel Configuration" on page 21 for further instructions.

CPLD—EPM3256A

Some non-volatile logic is needed to handle the counters and state machines associated with the high-speed interface to the SmartMedia card. We used an EPM3256A CPLD from Altera for this function. The datasheet is on the CD-ROM and is titled `epm3256a.pdf`. Approximately 90% of the resources of this device are utilized, so 10% are available for your own purposes. The Verilog source for the CPLD is provided on the CD–ROM. The file name is `CPLD.V`.

The CPLD performs the following functions:

- Interface to ATmega128L µP and SRAM
  - Clock Output to µP: `BUP_CLK`
  - Data/Lower Address: `UPAD[7:0]`
  - Upper Address:`UPPADDR[15:8]`
  - Control Signals: `UP_ALE, UP_RDn, UP_WRn`
  - SRAM Select: `SRAM_CSn`
- Data Retrieval from SmartMedia Card
  - Data Bus: `SM_D[7:0]`
  - Control: `SM_CLE, SM_ALE, SM_WEn, SM_WPn, SM_CEn, SM_REn, SM_RDYBUSYn`
- Configuration and Clock Status Reporting:
  - `CPLD_LED[3:0], ROBO_LOCK1, ROBO_LOCK2`
- Control of FPGA Parallel Configuration
  - Clock: `FPGA_DCLK`
  - Chip Select: `FPGA_CSnF, FPGA_CEnF`
  - Control: `FPGA_nCONFF, FPGA_CDONEF, FPGA_IODONEF, FPGA_RDYnBUSYF`
  - Data Bus: {`FPGA_D[7:1], FPGA_D0F`}
  - Mode Selector Switches: `FPGA_MSEL[2:0], DIP1_0`
- Pass-Through of Serial/JTAG Cable Signals
  - Cable: `DCLK/TCK, CONF_DONE/TDO, nCONFIG/TMS, nSTATUS, DATA0/TDI`
  - FPGA Chain: `CPLD_TMS, CPLD_TDO, CPLD_TDI, CPLD_TCK, CPLD_TRST`
- Support for Clocking Schemes:
  - CPLD Clock Input: `CLK[48]`
  - Inputs from Clock Buffers: `CPLD_CLK[1:0]`
  - Output to Clock Grid: `PCPLD_CLKOUT`
- Interface to Reset Schemes:
  - `FPGA_GRSTn, PWR_RSTn`

We may periodically update the CPLD. The connections are on header **P4**. The relevant signals and the connections to **P4** are listed in Table 2-2. Figure 2-10 shows the location of **P4**.

Table 2-2 Signals and Connections to P4

JTAG Cable	P4 Signal Name	P4 Pin
VCC	+3.3 V	4, 6
GND	GND	2, 10
TCK	JTAG_CPLD_TCK	1
TDO	JTAG_CPLD_TDO	3
TDI	JTAG_CPLD_TDI	9
TMS	JTAG_CPLD_TMS	5

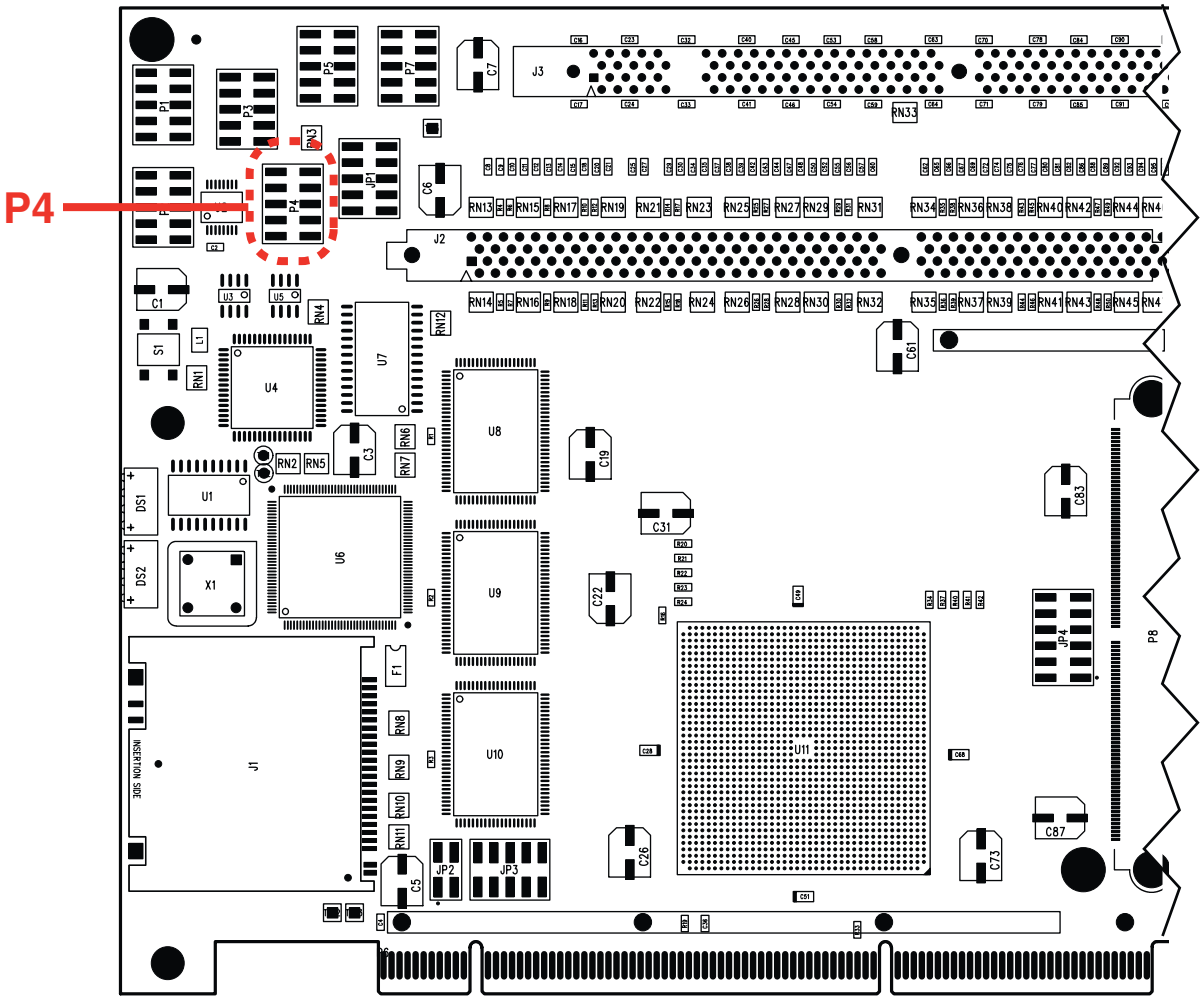


Figure 2-10 Location of P4 on the ET5000k10S

Some Miscellaneous Notes on the CPLD

X1 is a 48 MHz oscillator. This part is soldered down to the PWB and is not intended to be user-configurable. The 48 MHz is divided down to 8 MHz in the CPLD to provide the clock for the ATmega128L µP. The processor clock signal is labeled CPUCLK (and BCPUCLK) on the schematic.

Serial and JTAG configuration of the Stratix FPGA are back off positions only—that is why those signals are connected to the CPLD. Fast Passive Parallel is the quickest configuration method, but we wanted to provide the user as many options as possible.

If you want to use 100% of the CPLD and µP for your own purposes, you can configure the FPGA using the JTAG cable.

The 48 MHz clock can be divided down in the CPLD and used to drive the PWB clock network. See Chapter 4 for a more detailed description of this option.

Notes on Header P3

Fast Passive Parallel using the SmartMedia card is the best way to configure the FPGA. Two other options exists if, for some reason, the SmartMedia card method is not applicable.

1. Serial Programming Using the Cable. Header **P3** has the 5 serial connections that are used to configure the FPGA using the serial method. Table 2-3 has the pinouts. Note that this is a back-off position to SmartMedia and JTAG and should only be used in dire circumstances. Note also that the switches on **P5** will need to change to reflect "slave-serial" configuration.

2. JTAG Programming.
   The JTAG connection can be used to configure the FPGA and can also be used to connect the SignalTap Logic Analyzer (See Application Note 175 at **www.altera.com/literature/lit-qts.html**) or other solutions such as the Bridges2Silicon system, which was recently acquired by Synplicity (see **www.bridges2silicon.com**). The JTAG method of configuration should be used if the SmartMedia method isn't working. Remember that programming a Stratix part through JTAG uses a `.sof` file, not a `.rbf` file. Table 2-3 has the pinouts.

Table 2-3 FPGA Serial/JTAG Configuration Header

Name on Schematic	Name on Cable		Header Pin (P3)
	Serial Mode	JTAG Mode	
DCLK/TCK	DCLK	TCK	1
CONF_DONE/TDO	CONF_DONE	TDO	3
DATA0/TDI	DATA0	TDI	9
nCONFIG/TMS	nCONFIG	TMS	5
nSTATUS	nSTATUS	(none)	7

Table 2-3 FPGA Serial/JTAG Configuration Header

Name on Schematic	Name on Cable		Header Pin (P3)
	Serial Mode	JTAG Mode	
GND	GND	GND	2, 10
VCC	VCC	VCC	4, 6

Fast Passive Parallel Configuration Instructions

The FPGA on the ET5000k10S can be configured in Fast Passive Parallel mode using a Smart Media card. Fast Passive Parallel configuration is the easiest and quickest way to configure the FPGA. The ET5000k10S is shipped with two 32 MB Smart Media cards. One of these Smart Media cards contains reference design bit files produced for Fast Passive Parallel configuration, and files `main.txt` that sets options for the configuration process (for description of options, see "Creating Main Configuration File main.txt" on page 19). This Smart Media card has been labeled with a sticker marked "reference design." The other Smart Media card is empty and is for use with your own designs. To configure the FPGA with the reference design, please skip to "Starting Fast Passive Parallel Configuration" on page 21.

Creating RBF Files for Fast Passive Parallel

To create an RBF file with QuartusII software:

Go to Assignments menu and drag down to Settings. Click on Device under Compiler Settings on the left, then click the Device & Pin Options button on the right. Go to the Configuration tab, select Configuration Scheme = Fast Passive Parallel, and disable the option to Use Configuration Device. Go to the Programming Files tab, turn on Raw Binary File (`.rbf`), and turn off all other options. (Note: the `.sof` file for JTAG programming will also be created.)

The easy way to assign pins is to create your project, then open the `.csf` file created in a text editor. If your pinlist is formatted correctly, you can copy it and paste it into the `.csf` file in the section labeled "CHIP (design_name)". Sample files on the software CD provided, found in the folder labeled Verilog, show how to format the information and provide the correct pinlist for the signal names used on the board.

Setting up the Serial Port (P2 — RS232 Port)

P2 is for an RS232 connection to a terminal. An ICL3221 (**U2**) provides voltage translation to RS232 levels. A cable that converts the 10-pin header to a DB9 is shipped with the ET5000k10S. This cable comes packaged with a bracket attached. Remove the bracket to eliminate the possibility of it falling on the ET5000k10S, which could short signals and damage the board. After you have removed the bracket, plug the cable into **P2**. **P2** is not keyed—so make sure you get the orientation correct. Pin 1 is identified with the number 1 and a dot. Figure 2-11 is a cutout from the assembly drawing, and shows the location of **P2** and Pin 1.

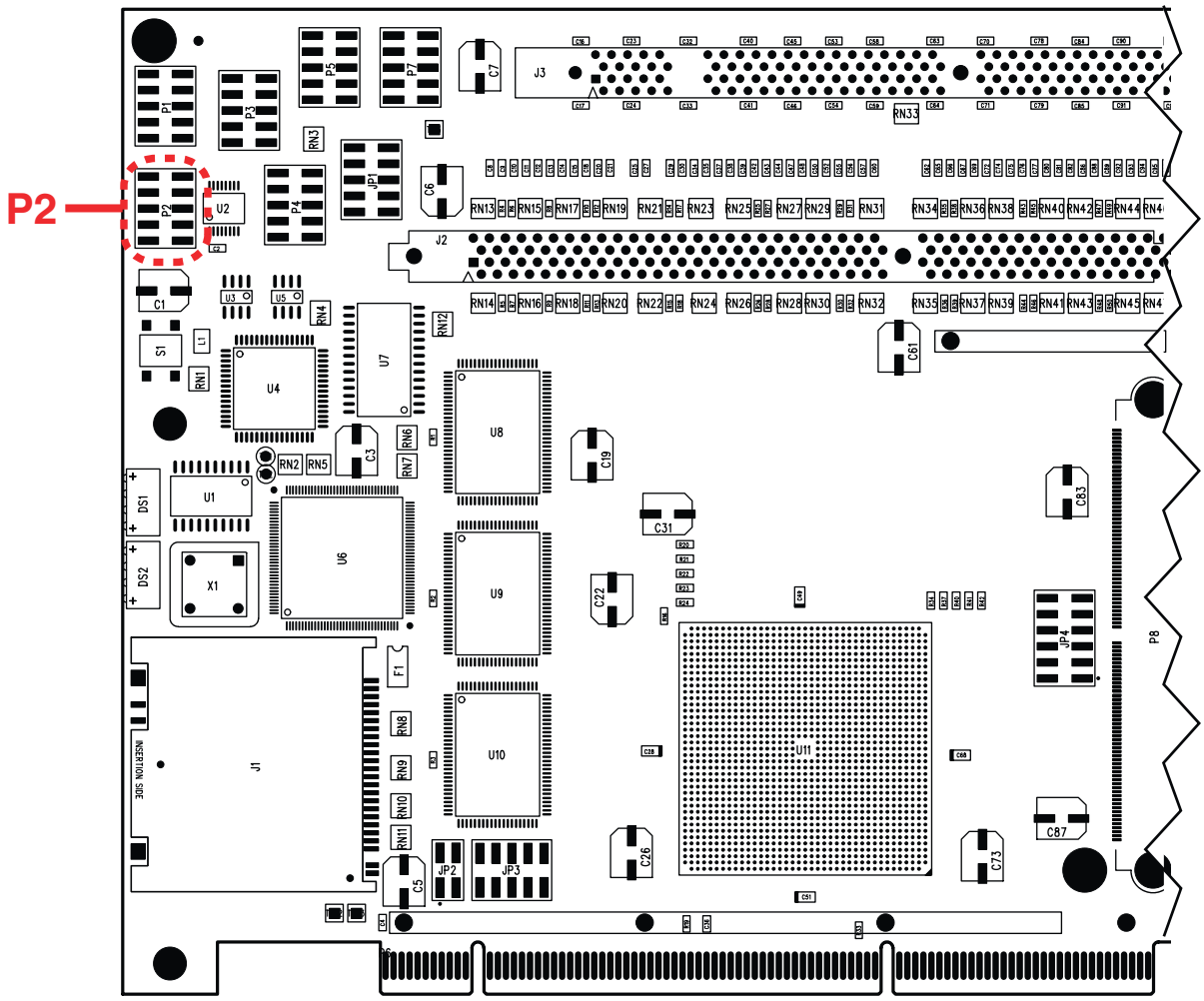


Figure 2-11 P2 Serial Port Locations

A female-to-female RS232 cable is provided with the ET5000k10S. This cable will attach directly to the RS232 port of a PC. We get our cables from Jameco (**http://www.jameco.com**).The part number is 132345. Male-to-female extension cables are part number 25700.

The RS232 port is configured with the following parameters:

Bits per second:9600
Data bits:8
Parity:None
Stop Bits:1
FLow control:None
Terminal Emulation:VT100

We use the Windows-based program HyperTerminal (`Hypertrm.exe`). The configuration file `ET5000k10S.ht` is supplied on the CD-ROM or can be downloaded from our web page.

Users have the option of connecting the serial port if they wish to see any messages during the configuration process.

NOTE: It is NOT mandatory to have the serial port connection in order to configure the FPGA in SelectMAP mode. However, if an error occurs during the configuration, then without a serial port connection the user will not be able to see any error messages. In addition, without a serial port connection, a user cannot select any Main Menu options after the configuration process is complete.

Creating Main Configuration File main.txt

To control which bit file on the Smart Media card is used to configure the FPGA in SelectMAP mode a file named `main.txt` must be created and copied to the root directory of the Smart Media card. The configuration process cannot be performed without this file. Below is a description of the options that can be set in the file, a description of the format this file needs to follow, and an example of a `main.txt` file.

Options:

Verbose Level — During the configuration process, there are three different verbose levels that can be selected for the serial port messages:

- Level 0:
  - Fatal error messages
  - Sanity Check errors (e.g., RBF file was created for the wrong part, RBF file was created with wrong version of Altera tools, or Quartus options are set incorrectly)
  - Initializing message will appear before configuration
  - A single message will appear once the FPGA is configured
- Level 1:
  - All messages that Level 0 displays
  - Displays configuration type (should be Fast Passive Parallel
  - Displays current FPGA being configured if the configuration type is set to Fast Passive Parallel
  - Displays a message at the completion of configuration for each FPGA configured.
- Level 2:
  - All messages that Level 1 displays
  - Options that are found in `main.txt`
  - RBF file names for each FPGA as entered in `main.txt`
  - Maker ID, Device ID, and size of Smart Media card
  - All files found on Smart Media card
  - If sanity check is chosen, the RBF file attributes will be displayed (part, package, date, and time of the RBF file)
  - During configuration, a "." will be printed out after each block (16 KB) has successfully been transferred from the Smart Media to the current FPGA.

Sanity Check — The Sanity Check if enabled, verifies that the RBF file was created for the right part, the right version of Altera was used, and the Quartus options were set correctly. If any of the settings found in the RBF file are not compatible with the FPGA, a message will appear from the serial port, and the user will be asked whether or not they want to continue with the RBF file. Please see the section "Creating RBF Files for

Fast Passive Parallel" on page 17 for details on which Quartus options need to be changed from the default settings.

Format:

The format of the `main.txt` file is as follows:

- The first nonempty/uncommented line in `main.txt` should be:

  ```
  Verbose level: X
  ```

  where "X" can be 0, 1 or 2. If this line is missing or X is an invalid level, then the default verbose level will be 2.

- The second nonempty/uncommented line in `main.txt` tells whether or not to perform a sanity check on the bit files before configuring an FPGA:

  ```
  Sanity check: y
  ```

  where "y" stands for yes, "n" for no. If the line is missing or the character after the ":" is not "y" or "n" then the sanity check will be enabled.

- For each FPGA that the user wants to configure, there should be exactly one entry in the `main.txt` file with the following format:

  ```
  FPGA F: example.rbf
  ```

  In the above format, the "F" following FPGA is to signal that this entry is for FPGA F, and FPGA F would then be configured with the bit file `example.rbf`. The ET5000k10S has one to five FPGAs, which are FPGA A, B, D, E and F. The example has only one FPGA, which is FPGA F. There can be any number of spaces between the ":" and the configuration file name, but they need to be on the same line.

- Comments are allowed with the following rules:
  1. All comments must start at the beginning of the line.
  2. All comments must begin with //
  3. If a comment spans multiple lines, then each line must start with //

  Commented lines will be ignored during configuration, and are only for the user's purpose.

- The file `main.txt` is **NOT** case sensitive.

IMPORTANT: All configuration file names have a maximum length of eight (8) characters, with an additional three (3) for the extension. Do not name your configuration files with long file names. In addition, all file names should be located in the root directory of the Smart Media card—no subdirectories or folders are allowed. Since the `main.txt` file controls which file is used to configure the FPGA, the Smart Media card can contain other files.

Example of `main.txt`:

```
//start of file “main.txt”
Verbose level: 2
Sanity check: y

FPGA F: fpgaF.rbf
//the line above configures FPGA F a file “fpgaF.rbf”

//end of main.txt
```

Given the above example file:

- Verbose level is set to 2
- A sanity check on the bit files will be performed
- FPGA F will be configured with file `fpgaF.rbf`.

Starting Fast Passive Parallel Configuration

If using the reference design SmartMedia card that came with the ET5000k10S then no files need to be copied to the card. Otherwise, copy your RBF file and `main.txt` to the root directory of the SmartMedia card using the FlashPath floppy adapter. Make sure the jumpers on **JP1** are set for Fast Passive Parallel as shown in Table 2-4.

Table 2-4 JP1 Configuration Jumper Settings

Pins 9–10 MSEL[2]	Pins 7–8 MSEL[1]	Pins 5–6 MSEL[0]	Configuration Mode
off	off	off	Fast Passive Parallel
off	on	off	Passive Serial

Set up the serial port connection as described above in “Setting up the Serial Port (P2 — RS232 Port)” on page 17. Next, place the SmartMedia card in the SmartMedia socket on the ET5000k10S and turn on the power (NOTE: the card can only go in one way). The SmartMedia card is hot-swappable and can be taken out or put into the socket even when the power is on. Once the power has been turned on, the configuration process will begin as long as there is a valid SmartMedia card inserted properly in the socket. If there is not a valid SmartMedia card in the socket, then UP_LED[3:0] will flash (see Figure 8-2 on page 8-3 for LED descriptions) and the Main Menu will appear from the serial port. A SmartMedia card is determined to be invalid if either the format of the card does not follow the SSFDC specifications, or if it does not contain a file named `main.txt` in the root directory. If the configuration was successful, a message stating so will appear and the **Main Menu** will come up. Otherwise, an error message will appear.

The LEDs on **DS1** and **DS2** give feedback during and after the configuration process; see “LEDs” on page 3 for further details.

After the FPGA has been configured, the following **Main Menu** will appear on the serial port:

1. `Configure FPGA(s) using main.txt`

2. Interactive FPGA configuration menu
3. Check Configuration status
4. Select file to use in place of main.txt
5. List files on SmartMedia
6. Select FPGA to program via JTAG

Description of Main Menu Options.

1. **Configure FPGAS Using "main.txt" as the Configuration File**— By selecting this option, the FPGA will configure in Fast Passive Parallel mode. You can also press the reset button (**S1**) to reconfigure the FPGA in Fast Passive Parallel mode.
2. **Interactive FPGA configuration menu** — This option takes you to a menu titled "**Interactive Configuration Menu**" and allows the FPGA to be configured through a set of menu options instead of using the main.txt file. The menu options are described below.

   Description of **Interactive Configuration Menu** options:

   1. **Select a bit file to configure FPGA(s)** — This menu option allows the user to select a file from a list of files found on the SmartMedia card to use to configure the FPGA.
   2. **Set verbose level (current level = 2)** — This menu option allows the user to change the verbose level from the current setting. Please note: if the user goes back to the main menu and configures the FPGA(s) using main.txt, the verbose level will be set to whatever setting is specified in main.txt.
   3. **Disable/Enable sanity check for bit files** — This menu option either allows the user to disable or enable the sanity check, depending on what the current setting is. Please note: if the user goes back to the main menu and configures the FPGA(s) using main.txt, the sanity check will be set to whatever setting is specified in main.txt.

   M)**Main menu** — This menu option takes the user back to the Main Menu described above.
3. **Check Configuration status** — This option checks the status of the **DONE** pin and prints out whether or not the FPGA(s) have been configured along with the file name that was used for configuration.
4. **Select file to use in place of** main.txt — By default, the processor uses the file main.txt to get the names of the files to be used for configuration as well as options for the configuration process. However, a user can put several files that follow the format for main.txt on the SmartMedia card that contain different options for the configuration process. By selecting the main menu option 4, the user can select a .txt file from a list of files that should be used in place of main.txt. After selecting a new file to use in place of main.txt, the user should select Main Menu option 1 to configure the FPGA(s) according to this new file. If the power is turned off or the reset but-

ton (**S1**) is pressed, the configuration file is changed back to the default, `main.txt`.

5. **List files on SmartMedia** — This option prints out a list of all the files found on the SmartMedia card.
6. **Select FPGA to Program with JTAG** — This option must be set to enable an FPGA before it can be programmed through JTAG.

SmartMedia

The configuration file for the FPGA is copied to a SmartMedia card using the SmartDisk FlashPath Floppy Disk Adapter. The approximate file size for each possible Stratix FPGA is shown below in Table 2-5. Note that several files can be put on a 32-megabyte card. We supply two 32-megabyte SmartMedia cards with the ET5000k10S. SmartMedia is a standard, so you can get more SmartMedia cards if you want. The ET5000k10S requires a +3.3 V card. Card sizes of 16, 32, 64, and 128 megabytes have been tested on the ET5000k10S. We have not seen 256 MB or larger cards for sale yet, but when we do there will probably be an update to the CPLD and processor on our website to support them.

Table 2-5 Stratix FPGA Approximate File Sizes

Stratix FPGA	Number of Configuration Bytes
SOF for EP1S80	2,954,672
RBF for EP1S80	2,992,071

We get our SmartMedia cards from **http://www.computers4sure.com/**. A Delkin Devices 16-megabyte card (part number DDSMFLS2-16) sells for about $15. A 32-megabyte card (part number DDSMFLS2-32) will set you back about $20 (see Figure 2-12). New SmartMedia cards do not require formatting before use.

NOTE: SmartMedia cards do not need to be formatted before they are used. The Windows format command DOES NOT WORK— it is necessary to use the FlashPath utility to format a SmartMedia card.

Do not press down on the top of the SmartMedia Connector **J1** if a SmartMedia card is not installed. The metal case shorts to the +3.3 V power supply and the case gets hot enough to burn your finger. We suggest that you leave a SmartMedia card in the connector to prevent this from occurring. A polyswitch fuse (**F1**) has been added so that the PWB and the SmartMedia connector are protected if you do accidently press on the top of the connector.

NOTE: Do NOT press on the SmartMedia Connector P58 if a card is not installed!

Figure 2-12 Delkin 32 MB 3.3 V Smart Media Card

WARNING:

Do NOT format a SmartMedia card using the default Windows format program. All Smart Media cards come preformatted from the factory, and files can be deleted from the card when they are no longer needed. If for some reason you absolutely need to format a SmartMedia card, you must use the format program that is included in the FlashPath (SmartMedia floppy adapter) software.

Synthesis and Emulation Issues

The QuartusII™ software from Altera is able to synthesize directly from Verilog or VHDL code. However, third-party synthesis tools provide an advantage: to create a memory block or multiplier, all you need to do is describe them functionally, and the tool will infer the appropriate DSP and RAM megafunctions for Quartus to place and route. On the other hand, if you are using Quartus to synthesize, and you try to infer an M-RAM block using a functional description, Quartus will attempt to route 200,000 LEs as a memory array. So, if you don't have any other synthesis tool, you will need to become familiar with Quartus megafunctions.

We have tried the following tools for synthesis:

Synplicity Synplify (http://www.synplicity.com/)

Synopsys FPGA Express (http://www.synopsys.com/)

Synopsys FPGA Compiler II

Exemplar LeonardoSpectrum (http://www.exemplar.com/products/leonardospectrum.html)

Of the four listed here, we find that Synplicity offers the best performance, followed by Exemplar. The Synopsys products are not the easiest

products to use, and probably should be avoided until Synopsys decides that they want to be in this market. It is generally not worth your time to preserve your Synopsys ASIC compiler directives and scripts by using the FPGA synthesis products from Synopsys. The time you save using Snopsys products is offset by other hassles.

Synthesis Notes

1. The FPGA used on your ET5000k10S is an EP1S80s in an F1508 package (EP1S60s available on request). Unless you paid for a faster speed grade, the –6 is what you will be getting.
2. Assuming you have a synthesis tool other than QuartusII, memories are best implemented by describing them behaviorally in your RTL. All four synthesis products are sophisticated enough to map your behavioral descriptions into the memory blocks. It is **NOT** necessary to instantiate memories manually, unless you are synthesizing with Quartus. Make sure, however, to check the report files to make sure that your memories were implemented in memory blocks (if this is possible). If input and output registers in your RTL don't match the behavior of the embedded memory blocks, the synthesis program may not recognize what you intended, and give you arrays of LEs instead.
3. Much to our surprise, the synthesis programs recognized RTL multiplier code and used the embedded multipliers without any trouble. So, like the memories, RTL description of your multipliers is all that is necessary unless you are synthesizing with Quartus. Make sure to check the report files—multipliers that are implemented using logic blocks (as opposed to the embedded memory blocks) take huge amounts of FPGA resources.
4. Clocks are the biggest problem when converting ASIC code to FPGA code. FPGAs only have a limited number of clock arrays. This is far too complicated to describe here, so get the *Stratix Data Sheet* and read about the clocks.

Chapter 3

PCI

Overview

The ET5000k10S can be hosted in a 32-bit, or 64-bit PCI slot. PCI-X is also supported. Stand-alone operation is described in "Stand-Alone Operation" on page 3. An EP1580-7, with care, should be able to support a 64-bit, 66 MHz PCI or PCI-X controller. We have not tested the PWB at PCI-X speeds of 100 MHz and 133 MHz. We suspect, but won't guarantee, that the ET5000k10S can support these high frequencies, provided the speed grade of the FPGA is adequate. Figure 3-1 shows the FPGA pin connections for the PCI signals. This data is provided on the CD-ROM in a `.csf` file titled `pins_F.csf`, for your convenience.

The PCI/PCI-X edge connector is shown in Figure 3-2.

Stratix parts cannot tolerate +5 V ttl signaling, so the ET5000k10S must be plugged into a +3.3 V PCI slot. PCI-X, by definition, is +3.3 V signaling. The PWB is keyed so that it is not possible to mistakenly plug the board into a +5 V pci slot. Do NOT grind out the key in the PCI host slot, and Do NOT modify the ET5000k10S to get it to fit into the slot. If you need a +3.3 V PCI slot, the ETPCIEXT-S3 Extender card can do this function. This extender also has the capability to slow the clock frequency of the PCI bus by a factor of two—a function that is very useful when prototyping ASICS.

NOTE: +5 V Signaling on Stratix parts causes them to smoke! This is quite BAD! Do NOT Modify the ET5000k10S board to fit into your pci slot.

PCI Mechanical Specifications

The ET5000k10S is **not** a standard sized PCI card—it is too tall and slightly too long. This is sometimes an issue in servers that have a bracket installed over the top of the PCI cards. If you need to close the case on a ET5000k10S, some tower configurations may work. Figure 3-3 shows the exact dimensions of the ET5000k10S.

Some Notes on the ET5000k10S and PCI/PCI-X

+3.3 V power is not needed on the host PCI connector. +3.3 V power is derived from +5 V using an on-board 10 A switching regulator. Power distribution for the ET5000k10S is described in "Power Supplies and Power Distribution" on page 1.

LOCK# has a pull-up. This is technically a violation of the PCI specification, but we have seen systems (from SUN!) that have the LOCK# pin floating. Remember that the function of this pin was deleted in the 2.2 version of

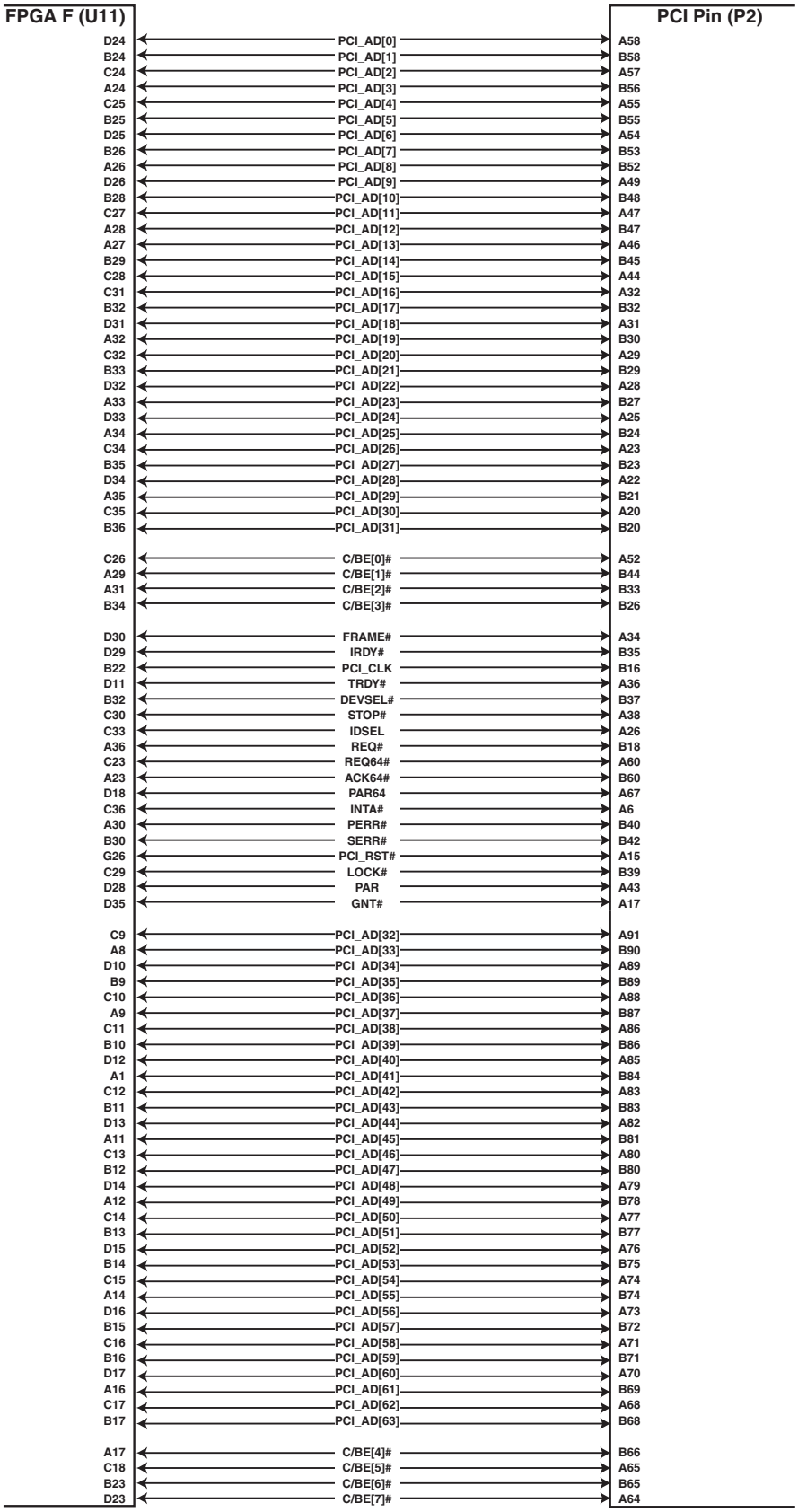
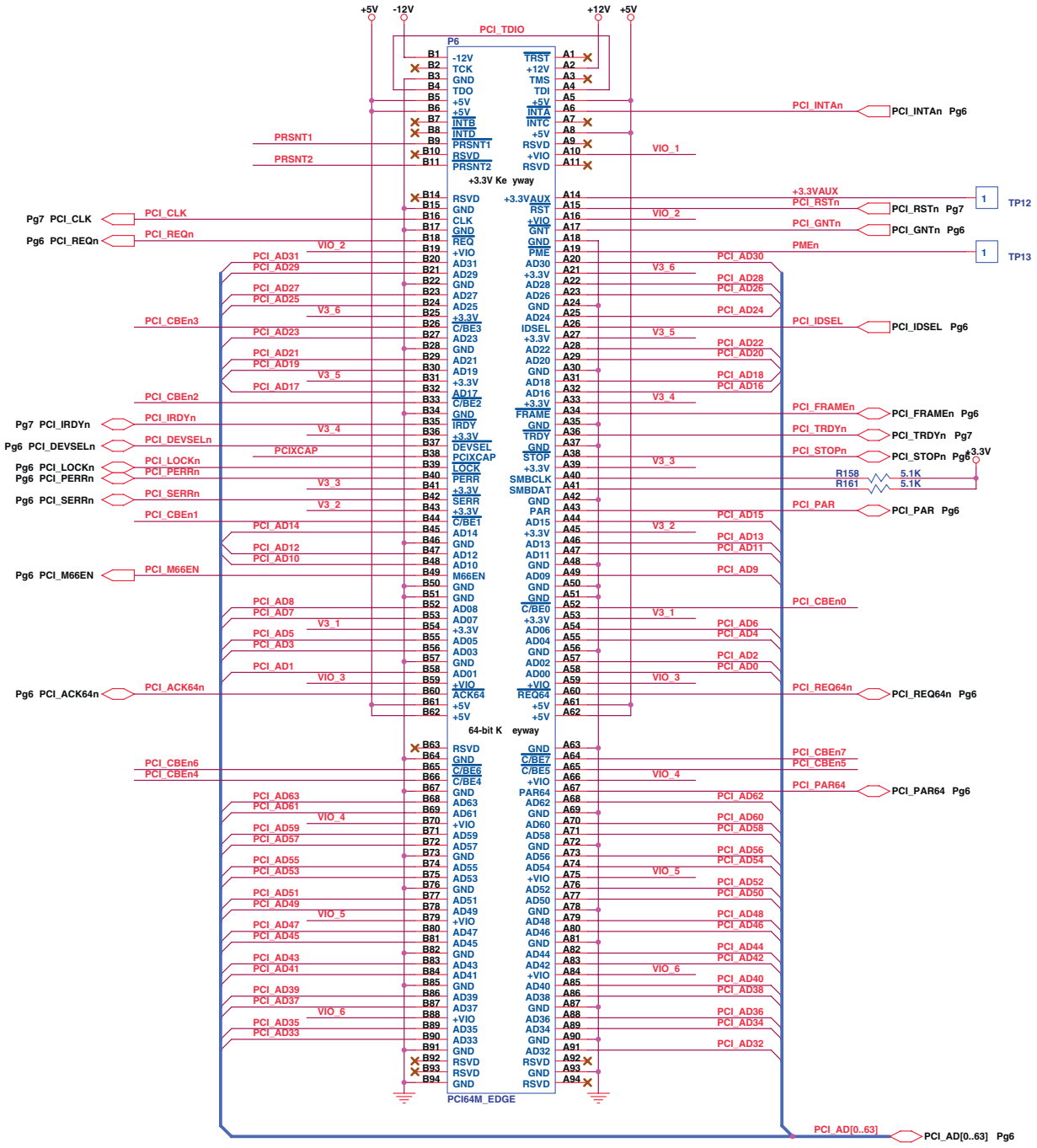


Figure 3-1 FPGA Pin Connections for PCI Signals



Note: The B side of the connector must be on the components side of the PCB.

Figure 3-2 PCI/PCI-X Edge Connector

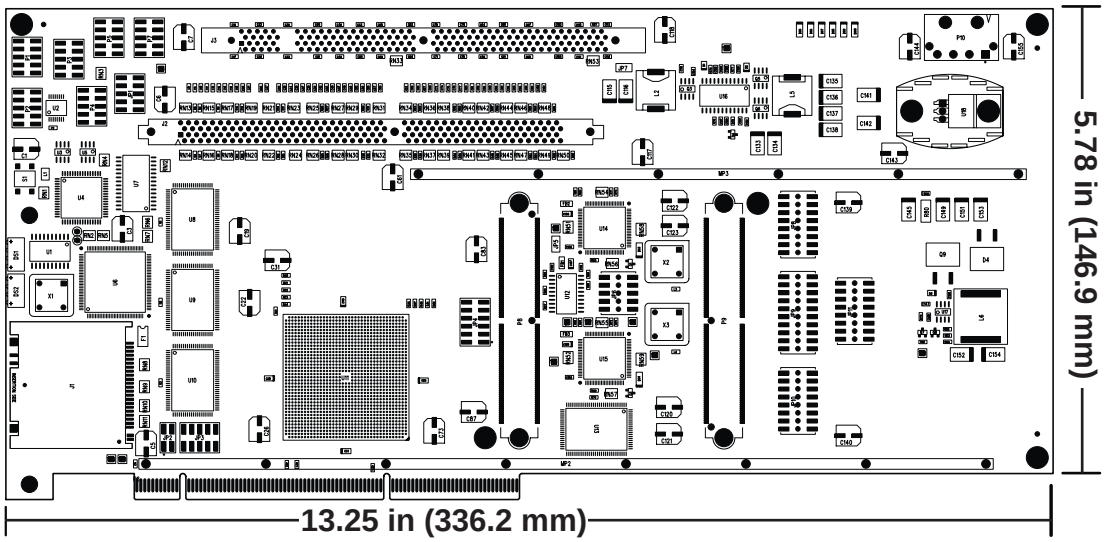


Figure 3-3 ET5000k10S Dimensions

the PCI Specification. The pull-up is 1M, which should not adversely impact PCI functionality in any way.

The PCI JTAG signals TDI, TDO, TCK, TMS, TRST#, are not used. TDI and TDO are connected together per the PCI Specification to maintain JTAG chain integrity on the motherboard. The signals TMS, TCK, and TRST# are left unconnected.

The FPGA is volatile, meaning it loses its brains when power is off. The SmartMedia method takes about 1 second to configure an EP1580 after power is stable. It is likely that FPGA F will finish the configuration process before RST# is deasserted. If your system has an unusually fast RST#, it is possible that the FPGA will not be configured when RST# deasserts. A RST# that deasserts before the FPGA has finished cannot properly configure the PCI/PCI-X mode latch.

The signal 3.3Vaux is not connected.

The signals INTB#, INTC#, and INTD# are not connected.

JP2: Present Signals for PCI/PCI-X

The present signals indicate to the system board whether an add-in card is physically present in the slot and, if one is present, the total power requirements of the add-in card.

The **JP2** PCI-X Present Header is shown in Figure 3-4.

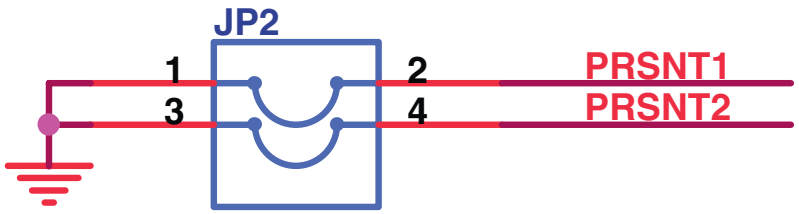


Figure 3-4 JP2 PCI-X Present Header

Table 3-1 shows the Present Signal Definitions for PCI/PCI-X.

Table 3-1 Present Signal Definitions

PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25W maximum
Open	Ground	Expansion board present, 15W maximum
Ground	Ground	Expansion board present, 7.5W maximum.

We have never seen the present signals used anywhere, but we have heard of systems that will not PNP (Plug-and-Play) configure a PCI board if both the present pins are left open. We recommend installing a jumper in location 1-2 (for PRSNT1-), or 3–4(for PRSNT2-), or both.

JP3: M66EN—66MHz Enable

The 66MHZ_ENABLE pin (**M66EN**) indicates to the host whether the device can operate at 66 MHz or 33 MHz. Section 7.5.1 in the *PCI Specification 2.2* provides the gory details. For 33 MHz only FPGA designs, install a jumper between pins 9 and 10 of **JP3**. For 66 MHz capable designs, install a jumper between pins 7and 8 instead. Table 3-2 shows the jumper descriptions for M66EN.

Table 3-2 M66EN Jumper Descriptions

	Jumper JP3	Description
M66EN	Pins 9-10	33 MHz
	Pins 7-8	66 MHz

TP13: PME–, Power Management Enable

This board does not have built-in support for **PME–** (power management enable). Connecting **PME–** to an FPGA that is not powered is a bad idea—the system powers up as the board is installed. **PME–** is connected to **TP13**. This test pin allows the user to connect external circuitry to **PME–** if this functionality is desired.

JP3: PCI/PCI-X Capability

Figure 3-5 shows the PCI-X/M66EN Capabilities Header. Add in PCI-X boards tell the system what speed they are capable of running by the correct setting of this header.

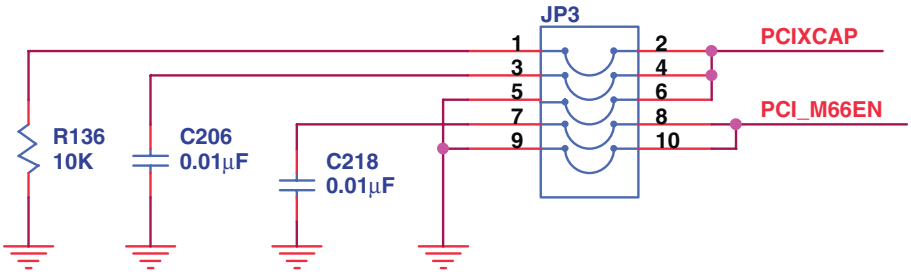


Figure 3-5 PCI-X/M66EN Capability Header

Add-in cards indicate at which frequency they support PCI-X, using a pin called **PCIXCAP**. If the card's maximum frequency is 133 MHz, this pin is left unconnected (except for a decoupling capacitor **C206**). If the card's maximum frequency is 66 MHz, it connects **PCIXCAP** to ground through a resistor **R93** (and decoupling capacitor **C206**). Conventional PCI cards connect this pin to ground.

JP3—PCIXCAP

For PCI only (not PCI-X capable), jumper between pins 5 and 6.

For PCI-X 133 MHz capable, jumper between pins 3 and 4.

For PCI-X 66 MHz capable, jumper between pins 1 and 2 and pins 3 and 4.

The **PCIXCAP** jumpers are detailed in Table 3-3.

Table 3-3 PCIXCAP Jumpers

PCIXCAP	Jumper(s) Installed
PCI Only	5–6
PCI-X 133 MHz	3–4
PCI-X 66 MHz	1-2, 3–4

The M66EN and PCIXCAP Encodings are shown in Table 3-4.

Table 3-4 M66EN and PCIXCAP Encoding

M66EN	PCIXCAP	Conventional Device Frequency Capability	PCI-X Device Frequency Capability
Ground	Ground	33 MHz	Not Capable
Not Connected	Ground	66 MHz	Not Capable
Ground	Pull-down	33 MHz	PCI-X 66 MHz
Not Connected	Pull-down	66 MHz	PCI-X 66 MHz
Ground	Not Connected	33 MHz	PCI-X 133 MHz
Not Connected	Not Connected	66 MHz	PCI-X 133 MHz

Chapter 4

Clocks and Clock Distribution

Functional Overview

The ET5000k10S ASIC emulation board has a flexible and configurable clock scheme. Figure 4-1 is a block diagram showing the clocking resources and connections.

The clocking structures for the ET5000k10S include the following features:

- 2 user-selectable socketed oscillators (**X2**, **X3**)
- 1 48 MHz oscillator (**X1**)
- 2 CY7B993 (or CY7B994) RoboclockII™ Multi-Phase PLL Clock Buffers
- 2 FCT3807 Low-Skew Clock Buffers

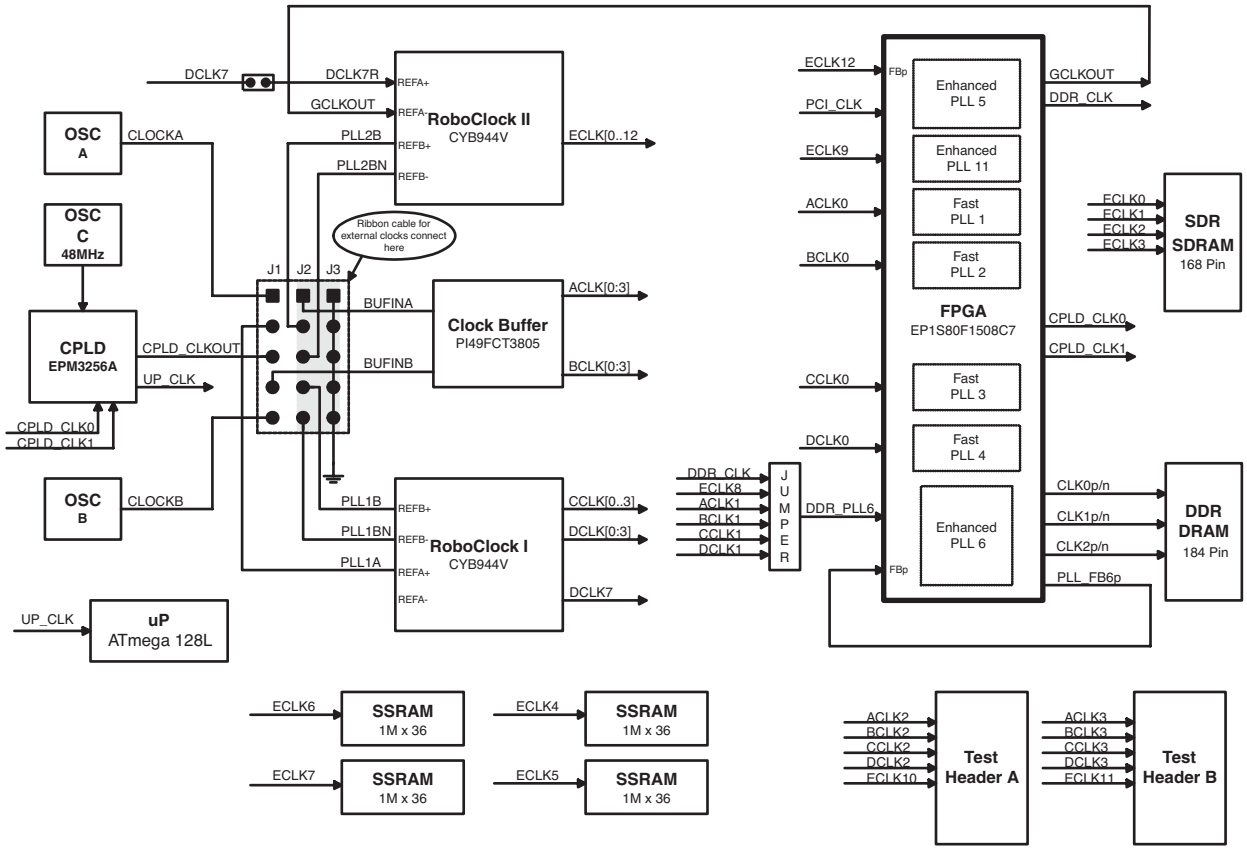


Figure 4-1 Clock Distribution Block Diagram

The Clock Grid, **JP6:** a 5X3 0.1 in. header distributes clock signals to two FCT3807 clock buffers and two RoboclockII™ PLL clock buffers (CY7B993 or CY7B994). The clock outputs from the buffers are dispersed throughout the board.

Two 3.3 V half-can oscillator sockets (**X2** and **X3**) and the signal CLKOUT from the CPLD provide on-board input clock solutions. The ET5000k10S is shipped with both a 14.318 MHz (**X2**) and a 33 MHz (**X3**) oscillator. Neither **X2** nor **X3** are used by the configuration circuitry, so the user is free to stuff any standard 3.3 V half-can oscillator in the **X2** and **X3** positions (more detail later in "Customizing the Oscillators" on page 12). The Clock Grid can also accept a 5X2 ribbon cable. This cable can provide input clocks to both of the RoboclockII's and one of the 3807 buffers.

The FCT3807 clock buffer provides a high speed 1-to-10 buffer with low skew (0.35 ns) allowing clocks A (ACLK[9:0]) and B (BCLK[9:0]) to be distributed point-to-point. The two RoboclockII PLL clock buffers (**U14** and **U15**) offer functional control of clock frequency and skew, among other things. They are configured via header arrays (**J8, JP10, JP9** and **JP11)**. The ET5000k10S comes from the factory stuffed with CY7B994V, which can operate at frequencies from 24 MHz to 200 MHz. They can also be stuffed with CY7B993V which operate from 12 MHz to 100 MHz. (Note: Output frequency can be as low as 1 MHz, depending on the operating frequency—see below for details.) Each chip has 16 output clocks along with 2 feedback output clocks. Two sets of eight output clocks are jumper selectable for each chip. The feedback clocks are controlled separately.

The PLL clock buffers can accept either 3.3 V LVTTL or LV Differential (LVPECL) reference inputs. The devices can operate at up to 12x the input frequency while the output clocks can be divided up to 12x the operating frequency. Phase adjustments can be made in 625 ps or 1300 ps steps up to ±10.4 ns. All adjustments are jumper selectable.

Clock Grid

Orientation and Description

The clock grid, **JP6**, gives the user the ability to customize the clock scheme on the ET5000k10S. A brief description of each pin is given in Table 4-1. The physical orientation of the pins is diagrammed in Figure 4-2.

.

Table 4-1 Clock Grid Signal Descriptions

Signal	Description
CLKOUT	**Clock signal from CPLD. Typically 12 MHz.**
PLL1A	**Input to RoboclockII #1**
CLOCKA	**Clock signal of oscillator #1 (X1)**
BUFINB	**Clock input to 3807 #2**
CLOCKB	**Clock signal of oscillator #2 (X2)**

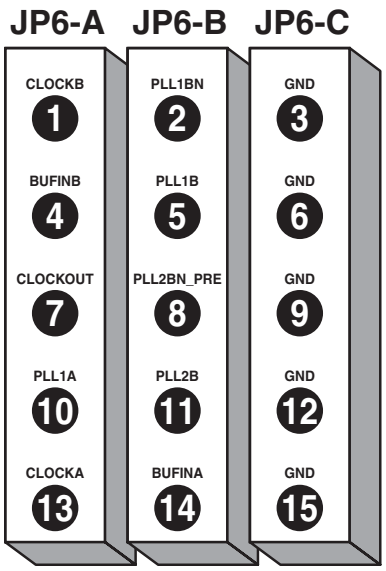


Figure 4-2 Clock Grid

Table 4-1 Clock Grid Signal Descriptions

Signal	Description
PLL2B_PRE	**Secondary clock input to RoboclockII #2. Differential pair with PLL2BN_PRE.**
PLL2BN_PRE	**Secondary clock input to RoboclockII #2. Differential pair with PLL2B_PRE.**
BUFINA	**Clock input to 3807 #1**
PLL1BN_PRE	**Secondary clock input to RoboclockII #1. Differential pair with PLL1B_PRE.**
PLL1B_PRE	**Secondary clock input to RoboclockII #1. Differential pair with PLL1BN_PRE.**
GND	**Ground signals to provide signal integrity for ribbon cables.**

Jumper Control for the Most Common Applications

Three main configurations are the most common.

First, the grid may be jumpered as follows:

> **Configuration #1**: CLKOUT <–>PLL1A, CLOCKA <–>BUFINA and CLOCKB <–> BUFINB

Both 3807s receive their inputs from the oscillators. RoboclockII #1 receives a clock input from the CPLD. Also, RoboclockII #2 can use DCLK[7] from RoboclockII #1 as an input. This is explained in “Roboclock PLL Clock Buffers” on page 5. Second, the input clock distribution can be configured as:

> **Configuration #2**: CLKOUT <–>PLL2BN_PRE, CLOCKA <–>PLL1A and CLOCKB <–> BUFINB

In this configuration, a 3807 #2 receives an oscillator input. RoboclockII #1 receives an oscillator input while RoboclockII #2 receives the CPLD output clock signal. 3807 #1 is unused.

Finally, the grid may be configured as:

> **Configuration #3**: CLKOUT <–>BUFINB, CLOCKA <–>BUFINA, and CLOCKB <–> PLL1BN_PRE

The 3807 #1 receives an oscillator input, and the 3807 #2 receives a CPLD input. Meanwhile, RoboclockII #1 receives the other oscillator input. The user can wire-wrap a clock to the unused driver(s) as needed. This enables full use of the timing devices on the ET5000k10S.

Also, the destination of the output clocks might dictate some other configuration. This manual and other documentation should provide more than enough information to satisfy the user's needs (See Figure 4-3).

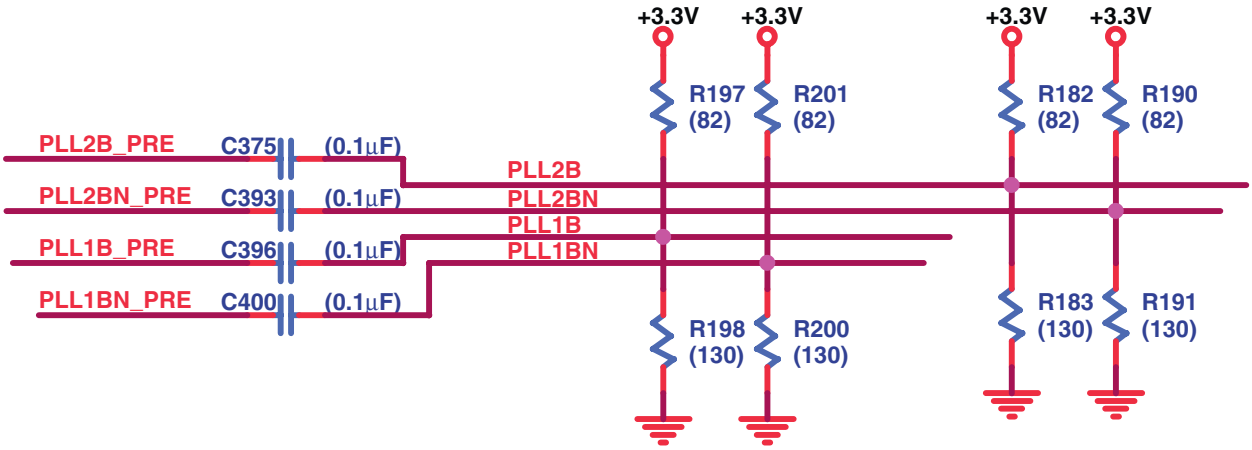


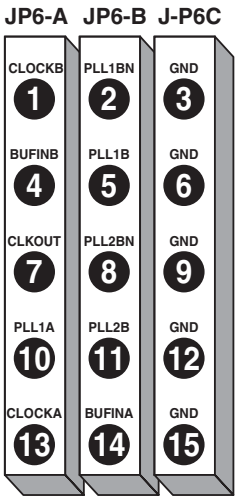
Figure 4-3 PECL Clock Input and Termination

NOTE: C380, C381, C382 and C383 are stuffed with 0-ohm resistors!

Note that the schematic shows capacitors in positions **C380**, **C381**, **C382** and **C383**. The ET5000k10S has 0-ohm resistors in these capacitor positions. The termination resistors **R206-R211, R207–R212, R209–R198** and **R214–R210** are not stuffed.

Ribbon Cable: Providing an Off-Board Clock to the ET5000k10S

The ET5000k10S gives the user a simple means to bring off-board clocks onto the board. The user can attach 10-pin ribbon cable to rows B and C of the Clock Grid. **JP6-B** consists of an input to 3807 #1 and differential pair inputs to both RoboclockII's. **JP6-C** consists of ground pins for signal integrity. These signals are described in Table 4-1 on page 2. BUFINA is a standard 3.3 V TTL input.



WITHOUT 10-PIN RIBBON CABLE				
Option	CLKOUT (JP6.7) goes to:	CLOCKA (JP6.13) goes to:	CLOCKB (JP6.1) goes to:	Notes
1	PLL1A (JP6.10)	BUFINA (JP6.14)	BUFINB (JP6.4)	Roboclock 2 may be driven by Roboclock 1
2	BUFINB (JP6.4)	BUFINA (JP6.14)	PLL1BN (JP6.2)	Roboclock 2 may be driven by Roboclock 1
3	PLL2BN (JP6.8)	BUFINA (JP6.14)	PLL1BN (JP6.2)	Buffer B is undriven
		PLL1A (JP6.10)	BUFINB (JP6.4)	
4	BUFINB (JP6.4)	PLL2B (JP6.11) (requires wire wrap)	PLL1BN (JP6.2)	Buffer A is undriven

BUFINA → Buffer A → ACLK
BUFFINB → Buffer B → BCLK
PLL1A → Roboclock1 → CCLK, DCLK (PLLSEL1 low)
PLL1B → Roboclock1 → CCLK, DCLK (PLLSEL1 high)
PLL2B → Roboclock2 → ECLK (PLLSEL2 high)
Roboclock1 → Roboclock2 with PLLSEL2 low, J27 installed, and FCKLOUT unused.

WITH 10-PIN RIBBON CABLE	
Option	(Connected to J21 and J22)
3 external clocks	PLL1B, PLL2B and BUFINA are driven from cable. BUFINB can be jumpered to CLKOUT or CLOCKB, or left undriven.
2 external clocks	PLL2B and BUFINA are driven from cable, with PLL1A jumpered to CLKOUT or CLOCKA. Same options as above for BUFINB.
PECL clocks	The board can be set up for PECL inputs in PLL1B and PLL1BN, and in PLL2B and PLL2BN. PECL-ready boards cannot function without the cable except as in options 3 and 4 above.

Figure 4-4 External Ribbon Cable Connections

Both differential pairs provide some flexibility. The user can provide a single 3.3 V TTL input. It can be attached to either input. However, the other input must be left open. The user can provide a differential clock input to the pair. The differential clock inputs must obey the electrical specifications listed in Table 4-8 on page 11.

While attaching a ribbon cable, the user can jumper oscillator signal CLOCKB to BUFINB (3807 #2) on **P54**. This results in full use of all of the timing devices on the ET5000k10S (See Figure 4-4).

Roboclock PLL Clock Buffers

Figure 4-5 is a functional diagram of Roboclock 1 and Roboclock 2.

Jumper Descriptions

Headers **J8, JP10, JP9** and **JP11** are used to control the PLLs. Each header consists of GND pins in row A, various PLL inputs in row B, and +3.3 V pins in row C. The layout of the headers is shown in Figure 4-6.

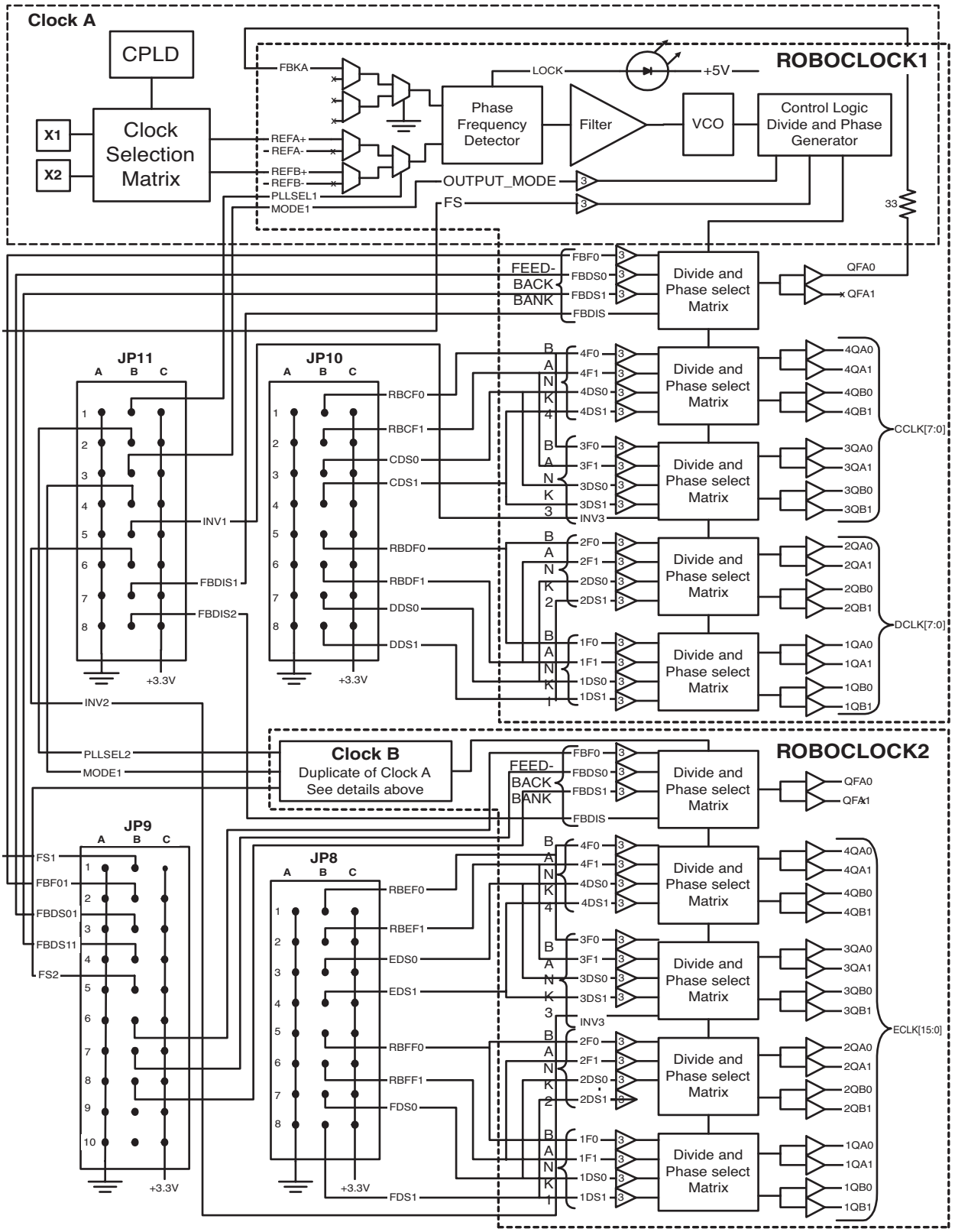


Figure 4-5 Functional Diagram of Roboclock 1 and Roboclock 2

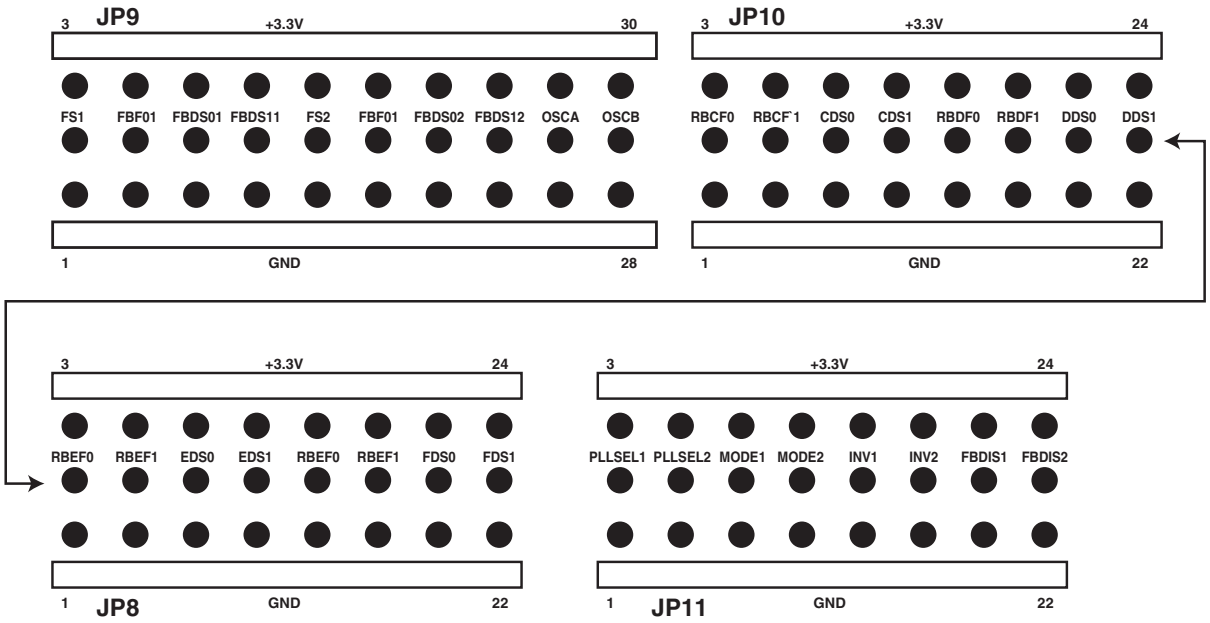


Figure 4-6 Header Layout

The Header Classifications are shown in Table 4-2.

Table 4-2 Header Classification

Controls	Header
Group I: General Control	JP11
Group 2: PLL1 Divider Control	JP10
Group 3: PLL2 Divider Control	JP8
Group 4: Feedback and f_{NOM} Control	JP9

The input pins are either LVTTL or 3-level input pins. The LVTTL pins need to be jumpered HIGH or LOW, which is achieved by connecting the input pin to the neighboring +3.3 V or GND pin, using a jumper. The 3-level input pins can be in a HIGH, MID, or LOW state. The HIGH and LOW states are achieved in the same way as the LVTTL pins. The MID state is reached by leaving the input pin unjumpered. The RoboclockII's have internal circuitry

to bring the pin to 1.5 V when left open. The Jumper Definitions are shown in Table 4-3.

Table 4-3 Jumper Definitions

Name	Type	Default	Description
PLLSEL2[1]	LVTTL	LOW	Input Clock Select: If LOW, U15:DCLK[7] or FCLKOUT (U14:PLL1A or HDR_CLKOUT) is selected as the input clock. If HIGH, the U15:PLL2BN (U14:PLL1BN) pair is selected as the input clock.
MODE[2:1]	3-Level	HIGH	Output Mode: If HIGH, clock outputs disable to high-Z state. If LOW, clock outputs disable to "HOLD-OFF' mode. If MID, clock outputs disable to factory test mode.
INV2[1]	3-Level	MID	Invert Mode: When HIGH, clocks CCLK[3:0] (ECLK[3:0]) are inverted. When MID, these clock outputs are non-inverting. When LOW, the pairs CCLK[1:0] and CCLK[3:2] (ECLK[1:0] and ECLK[3:2]) will be complementary.
FBDIS[2:1]	LVTTL	LOW	Feedback Disable: When HIGH, feedback is disabled. When LOW, feedback is enabled.
RB[C-F]F[1:0]	3-Level	MID	Output Phase Function: Each pair controls the phase function of the respective group of outputs. See "Clock Skew" on page 10 for more information.
[C-F]DS[1:0]	3-Level	LOW	Output Divider Function: Each pair controls the divider function of the respective group of outputs. See "Clock Division" on page 9 for more information.
FS[2:1]	3-Level	LOW	Frequency Select: The input specifies the operating range of the nominal frequency (f_{NOM}). See "General Control" on page 8 for more information.
FBF0[2:1]	3-Level	LOW	Feedback Output Phase Function: The input controls the phase function of the feedback outputs. See "Feedback and Clock Multiplication" on page 9 for more information.
FBDS[1:0][2:1]	3-Level	MID	Feedback Output Divider Function: Each pair controls the divider function of the feedback outputs. See "Feedback and Clock Multiplication" on page 9 for more information.

General Control

FS[2:1] is a 3-Level input which determines the allowable range for the operating frequency f_{NOM} of the device. Depending on the chip grade, the PLL can operate between 12–100 MHz or 24–200 MHz. The actual f_{NOM}

frequency can be determined by setting all jumpers to their defaults. Thus, f_{NOM} will be seen on all of the "divide-by-one" clock outputs. The user can set FS accordingly. The Frequency Range Settings are shown in Table 4-4.

Table 4-4 Frequency Range Settings

FS[2:1]	CY7B993V		CY7B994V	
	f_{NOM} (MHz)		f_{NOM} (MHz)	
	MIN	MAX	MIN	MAX
LOW	12	26	24	52
MID	24	52	48	100
HIGH	48	100	96	200

Feedback and Clock Multiplication

First of all, FBDIS[2:1] must be set LOW, enabling feedback. The feedback output is looped back to the feedback input. When a divided output is applied to the feedback input, the VCO (voltage controlled oscillator) of the PLL aligns the feedback input with the original input clock. Thus, with a 10 MHz input clock and the feedback outputs set to divide by 2, f_{NOM} must be 20 MHz. Consequently, 10 MHz is seen on the feedback output clocks and can be aligned with the input clocks. The feedback clock divider function actually serves as a clock multiplication mechanism for the operating frequency f_{NOM}. The divider function and the clock skew function are set in the same manner for the feedback and the normal clock outputs. See "Clock Division" on page 9 and "Clock Skew" on page 10, respectively.

Clock Division

The three pairs of DS inputs per chip are used to control the two groups of clock outputs and the feedback outputs of each PLL. The user can simply follow the Divider Function Table to acquire the desired output frequency. There are two things to remember. First, FS[2:1] must be set properly according to fNOM. Second, the FBDS feedback inputs act as operating clock frequency multipliers. The Output Divider Settings are shown in Table 4-5.

Table 4-5 Output Divider Settings

Input Signals		Output Divider Function	
[C-fF]DS1 and FBDS1[2:1]	[C-F]DS0 and FBDS0[2:1]	Output Signals	Feedback Output Signals
LOW	LOW	/1	/1
LOW	MID	/2	/2
LOW	HIGH	/3	/3
MID	LOW	/4	/4

Table 4-5 Output Divider Settings

Input Signals		Output Divider Function	
[C-fF]DS1 and FBDS1[2:1]	[C-F]DS0 and FBDS0[2:1]	Output Signals	Feedback Output Signals
MID	MID	/5	/5
MID	HIGH	/6	/6
HIGH	LOW	/8	/8
HIGH	MID	/10	/10
HIGH	HIGH	/12	/12

Clock Skew

Clock skew is controlled by the "F" inputs. The clock skew may be any integer value from 0 to ±8 times the RoboclockII time unit t_U. The time unit value is derived from the operating frequency f_{NOM} and the FS[2:1] setting. The following equation yields the time unit t_U.

$$t_U = \frac{1}{f_{NOM} \cdot N}$$

The possible values for N are given in Table 4-6. The available skew for each RoboclockII derived clock is given in Table 4-7. Based on the following information, the user will be able to adjust the skew for any of the RoboclockII outputs.

Table 4-6 Time Unit N-factor

FS	CY7B993V		CY7B994V	
	N	f_{NOM} (MHz) at which t_U = 1 ns	N	f_{NOM} (MHz) at which t_U = 1 ns
LOW	64	15.625	32	31.25
MID	32	31.25	16	62.5
HIGH	16	62.5	8	125

Table 4-7 Clock Skew Settings

Input Signals		Output Skew Function				
RB[C-F]F1	RB[C-F]F0 and FBF0[2:1]	DCLK[3:0] or ECLK[11:8]	DCLK[7:4] or ECLK[15:12]	CCLK[3:0] or ECLK[3:0]	CCLK[7:4] or ECLK[7:4]	Feedback Output Signals
LOW	LOW	$-4t_U$	$-4t_U$	$-8t_U$	$-8t_U$	$-4t_U$
LOW	MID	$-3t_U$	$-3t_U$	$-7t_U$	$-7t_U$	N/A
LOW	HIGH	$-2t_U$	$-2t_U$	$-6t_U$	$-6t_U$	N/A
MID	LOW	$-1t_U$	$-1t_U$	COL1*	COL1*	N/A
MID	MID	$0t_U$	$0t_U$	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+1t_U$	COL2**	COL2**	N/A
HIGH	LOW	$+2t_U$	$+2t_U$	$+6t_U$	$+6t_U$	N/A
HIGH	MID	$+3t_U$	$+3t_U$	$+7t_U$	$+7t_U$	N/A
HIGH	HIGH	$+4t_U$	$+4t_U$	$+8t_U$	$+8t_U$	$+4t_U$
*The clock skew is equivalent to the skew on DCLK[3:0] or ECLK[11:8] **The clock skew is equivalent to the skew on DCLK[7:4] or ECLK[15:12]						

Differential Clocks

In addition to LVTTL clock signals, the RoboclockII clock buffers can handle LV Differential (LVPECL) clocks. The user can cable in an acceptable differential signal to PLL1B and PLL1BN, or PLL2B and PLL2BN through the clock grid **JP6**. The signals must obey the specifications given in Table 4-8. Onboard circuitry is available to center the signals about the proper voltage, if needed.

Table 4-8 LVPECL Input Specifications

Description	Min	Max
Differential Voltage	0.4	3.3
Highest HIGH Voltage	1.0	3.3
Lowest LOW Voltage	GND	2.9
Common Mode range (crossing voltage)	0.8	3.3

The clock input of the RoboclockII can accept a superset of PECL. PECL involves a 1 V swing about $V_{CC}/2$. The RoboclockII clock input can accept a swing of up to 3.3 V about $V_{CC}/2$, which gives the user another dimension of flexibility.

The CY7B993V/4V can output LVTTL complementary (differential) signals, too. Setting INV1 (INV2) LOW will result in clocks CCLK[1:0] and CCLK[3:2] (ECLK[1:0] and ECLK[3:2]) becoming complementary pairs. A network of series and parallel resistors could be used to reduce the nominal swing of the clock signals.

Useful Notes and Hints

The CYB993V consistently outputs ~32.5 MHz signals in cases of improper settings or unacceptable clock inputs. This was observed when:

- The CY7B993V part was operating at a nominal frequency f_{NOM} of 36.4 MHz with FS set LOW.
- Identical clocks were sent to PLL2B and PLL2BN.

For the CY7B994V part, the operating frequency can reach up to 200 MHz. However, the maximum output frequency is 185 MHz. This means when 185 MHz ≤ f_{NOM} ≤ 200 MHz, the output divider must be set to at least 2. Otherwise, the RoboclockII's will output garbage.

Customizing the Oscillators

The user can customize the frequency of the clock networks by stuffing oscillators in **X2** and **X3**. The ET5000k10S is shipped with a 14.318 MHz oscillator in location **X2** and a 100 MHz oscillator in **X2**. The RoboclockII's are **not** +5 V tolerant, so +3.3 V oscillators are necessary.

NOTE: If you stuff your own oscillators, +3.3 V CMOS outputs are necessary since the RoboclockII's are not +5 V signalling tolerant!

We get our oscillators from Digi-Key (**http://www.digikey.com/**). Of note is an Epson line of oscillators called the **SG-8002 Programmable Oscillators**. Any frequency between 1.00 MHz–106.25 MHz can be procured in the normal Digi-Key shipping time of 24 hours. A half-can, +3.3 V CMOS version is needed with a tolerance of 50 ppm. The part number for an acceptable oscillator from this family would be:

SG-8002DC-PCB-ND
- package SG-531
- output enable
- 3.3 V CMOS
- 50 ppm

If the order is placed via the web page, the requested frequency to two decimal places is placed in the Web Order Notes. The datasheet is on the CD-ROM for this oscillator. The file name is SG8002DC.pdf.

Any polarity of output enable for each oscillator (on pin 1) is acceptable. Make sure that you have the proper jumper settings at positions 9 and10 of **JP9A**, **JP9B** and **JP9C**. See Figure 4-7 and Table 4-9 for a description.

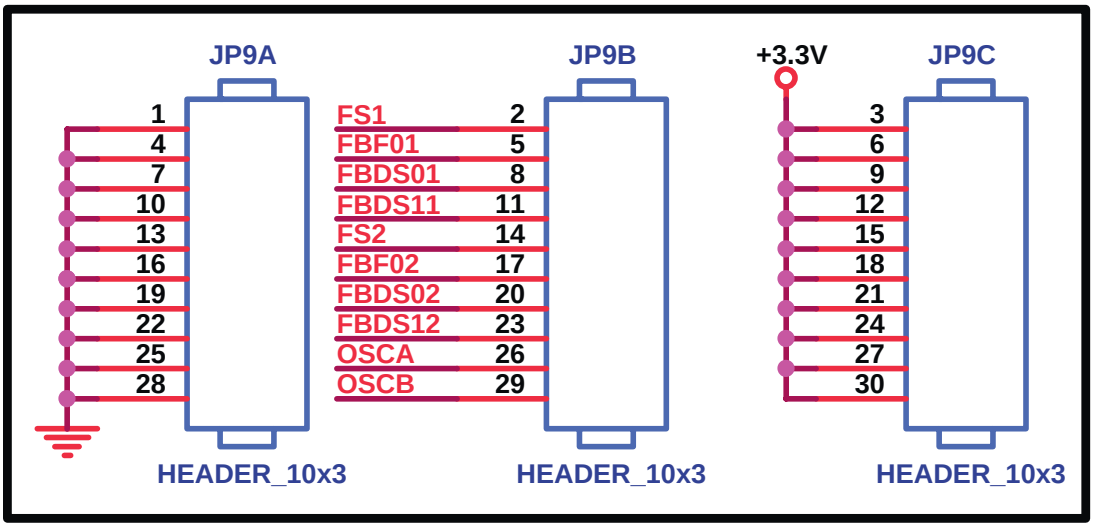


Figure 4-7 Clock OE Pin Jumper Settings

Table 4-9 Clock OE Pin Jumper Settings

Clock OE	Jumper Settings
Active High OE for X2	Jumper JP9.26 to JP9.27
Active Low OE for X2	Jumper JP9.26 to JP9.25
Active High OE for X3	Jumper JP9.29 to JP9.30
Active Low OE for X3	Jumper JP9.29 to JP9.28

ET5000k10S PCI_CLK Operation

The ET5000k10S ASIC emulation board has the ability to run the FPGA, all SSRAMs, SDRAM, and DDR SDRAM off of PCI_CLK. PCI_CLK is a single destination clock which is routed to FPGA F(**U11**) from the PCI connector. The user can input PCI_CLK to the Stratix Enhanced PLL5. The resulting PLL output can be sent to RoboclockII (**U14**) via the signal GCLKOUT. All of the memories on the ET5000k10S run off one of the ECLK clock outputs from RoboclockII.

PCI_CLK Details

PCI_CLK is connected to the Stratix Enhanced PLL5 input (pin **B22**). To run all memories off of PCI_CLK, a PLL must be instantiated in the FPGA code. The PLL will require a minimum of three connections (input clk, output clk, and external feedback input). For further information on Stratix PLL operation, see the Altera website at **http://www.altera.com.** The Stratix Datasheet (ds_stx.pdf) which can be found on the ET5000k10S CD-ROM, also provides useful information on PLLs.

The GCLKOUT signal is connected to one of the four input pins on RoboclockII. GCLKOUT's complementary input is DCLK[7](R). FCLKOUT and DCLK[7](R) are both single ended TTL inputs. When either of them is being used, the other one must be left open. For complete PCI_CLK operation, jumper **JP5** must not be stuffed leaving DCLK[7](R) open.

If set to the default configuration, RoboclockII will drive a one-to-one PCI_CLK derived clock on its outputs. See "Roboclock PLL Clock Buffers" on page 5 for more information. RoboclockII has 12 clock outputs (ECLK[12:0]). The FPGA (ECLK[9], ECLK[12]), SSRAMs (ECLK[7:4]), DDR SDRAM (ECLK[3:0]), and DDR SDRAM (PLL outputs – **JP4** must have jumper connecting pins 9 & 10 to send ECLK[8] to DDR SDRAM) receive ECLK signals.

To complete this setup, a feedback signal must be connected to the PLL in FPGA. RoboclockII sends ECLK[12] to the feedback input of the FPGA. ECLK[12] needs to be connected to the "fbin" input signal of the PLL. Using ECLK[12] as feedback allows the PLL to properly synchronize the ET5000k10S PCI_CLK network which completes the setup (see Figure 4-8 for a diagram of the PCI_CLK PLL circuit).

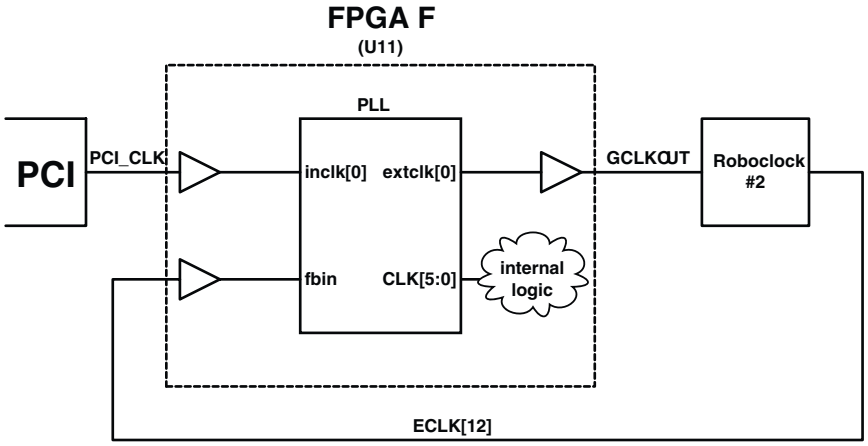


Figure 4-8 PCI_CLK PLL Circuit

The ET5000k10S can be run off any single-ended TTL clock signal which is sent to the Roboclocks. The ECK distribution provides the ET5000k10S this flexibility. PCI_CLK has special implications for the ET5000k10 PCI operation.

GCLKOUT

GCLKOUT is assigned to a dedicated clock output pin in the Stratix architecture, and can be used to drive Roboclock 2 (see the section "ET5000k10S PCI_CLK Operation" on page 13 for details). The ET5000k10S differs from previous emulator boards because the Stratix architecture assigns each PLL to specific clock pins. In the case of GCLKOUT, the only possible source is from PLL5, which has only one possible input, PCI_CLK. So, the sole purpose of GCLKOUT is to provide the means to run the whole board with PCI_CLK.

Header Clocks

Each of the two 200-pin header (**P8** and **P9**) receives a clock signal from each of the five clock groups (ACLK, BCLK, CCLK, DCLK, and ECLK).

DCLK[7](R)

The signal DCLK[7](R) is routed from one of the Roboclock I outputs to one of the RoboclockII inputs. Jumper **JP5** lies along this connection route. **JP5** must be installed in order to utilize DCLK[7](R). DCLK[7](R)and GCLKOUT are complementary input on Roboclock 2, and are both single-ended TTL inputs. When either of them is being used, the other one must be left open. Thus, GCLKOUT must be undriven on FPGA F for DCLK[7](R) to operate.

DCLK[7](R) provides two useful results. First, any clock signal or some derivation sent to Roboclock 1 can be driven onto RoboclockII for full distribution.

Second, running a clock through Roboclock I to RoboclockII gives the user more divide and multiply options for the clock frequencies. Here is an example. If you have a 40MHz input clock, the user cannot output a 30MHz clock with a single RoboclockII's multiply and divide options. However, the user can input a 40MHz to RoboclockII #1 and divide it by 4. By installing the **JP5** jumper, a 10MHz clock will be driven onto RoboclockII #2. Setting RoboclockII #2's feedback outputs to divide by 3, the operating frequency will become 30MHz. Thus, a 30MHz could be driven onto the RoboclockII #2 output signals.

NOTE: The signal GCLKOUT must be left open in order to utilize DCLK[7](R)

Chapter 5

Memories

The ET5000k10S has six external memories: four 36-bit SSRAMs, one 72-bit SDRAM DIMM, and one 72-bit DDR SDRAM DIMM. The four SSRAMS are referred to as SSRAM 1 (**U9)**, SSRAM 2 (**U6**), SSRAM 3 (**U8**), and SSRAM 4 (**U13**).

SSRAMs

The SSRAMs can be stuffed with ZBT, non-ZBT, pipeline, or flowthrough parts. We believe we have anticipated the additional address lines for the 1 M x 36 and 2 M x 36 parts when they are available. The ET5000k10S is stuffed at the factory with 512 K x 36-bit Synchronous Pipeline Burst SRAM. Samsung K7A163600M-QC1400 are probably the parts you will have stuffed into your ET5000k10S. The datasheet is on the CD-ROM in the file DS_K7A1636(18)00M.pdf. The SSRAMs are tested at 133 MHz.

SSRAM Notes

All SSRAMs use ECLK for their clock.

The signal connections for SSRAM 1 are shown in Figure 5-1.

The signal connections for SSRAM 2 are shown in Figure 5-2.

The signal connections for SSRAM 3 are shown in Figure 5-3.

The signal connections for SSRAM 4 are shown in Figure 5-4.

Flowthrough SSRAMs are functionally the closest to ASIC-style memories. Pipeline SSRAMs can be clocked at faster frequencies. ZBT SSRAMs are typically one generation behind in density. The subtle differences between the styles of memories are described in the next section.

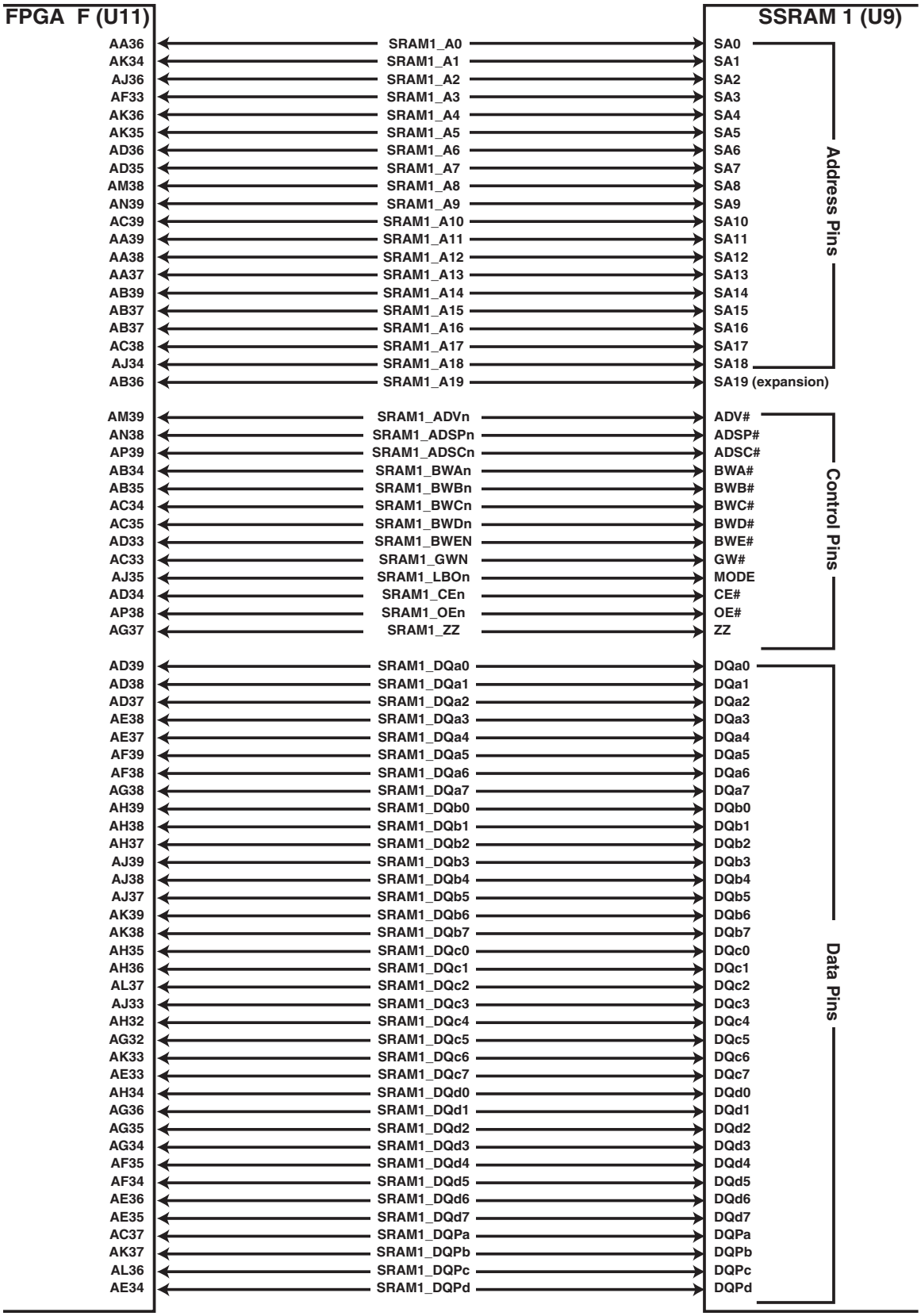


Figure 5-1 SSRAM 1 (U9) Bus Signals

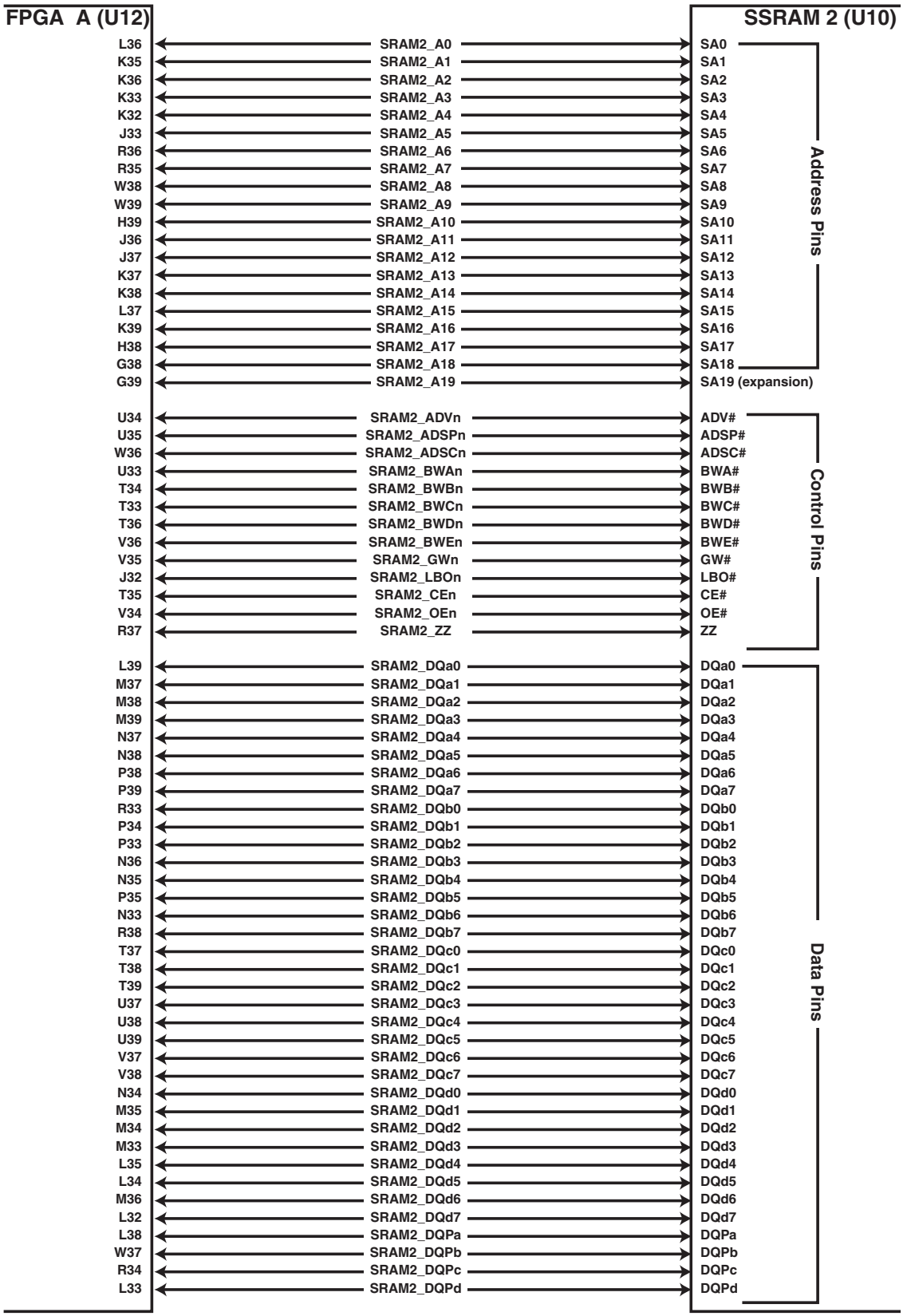


Figure 5-2 SSRAM 2 (U10) Bus Signals

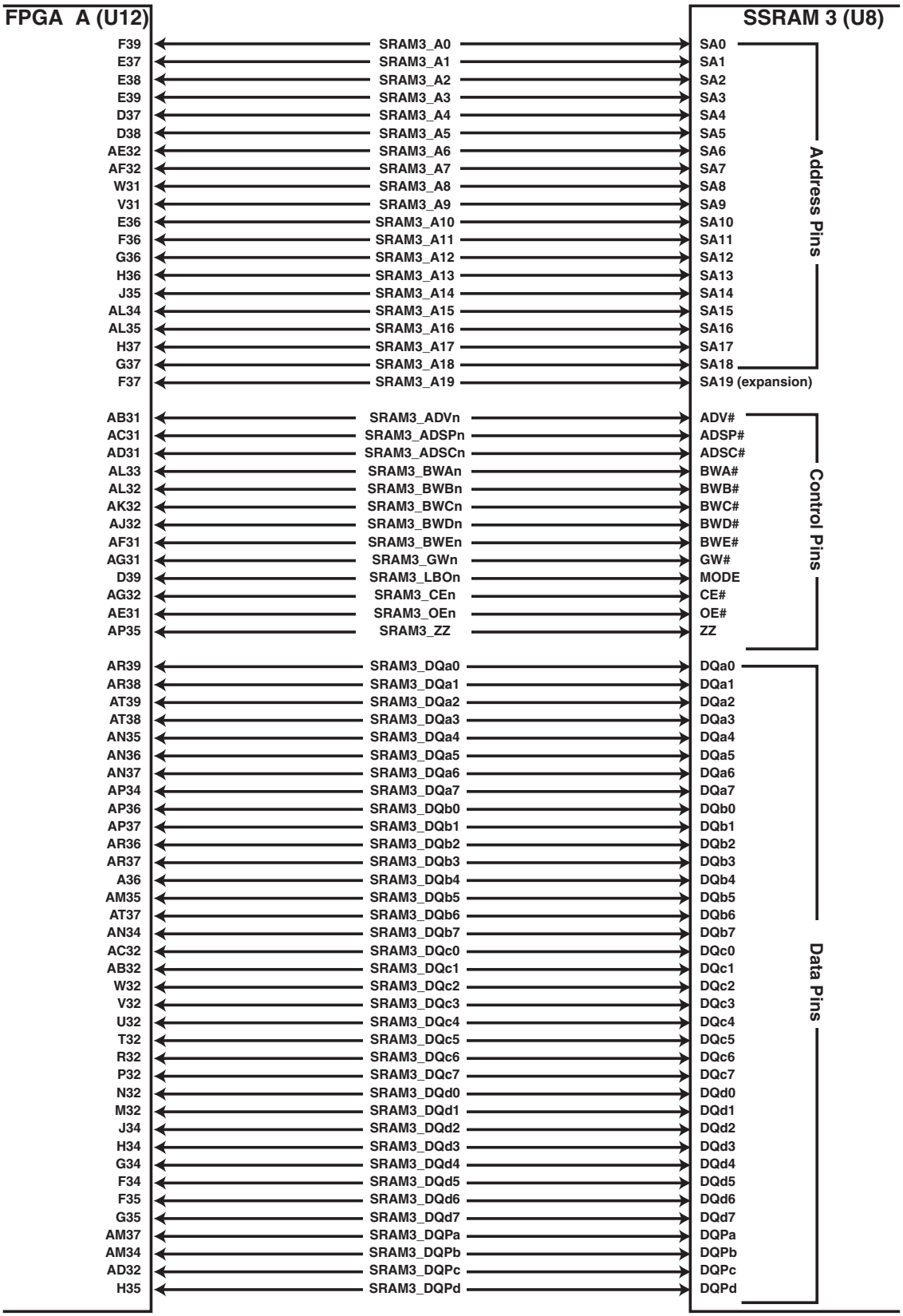


Figure 5-3 SSRAM 3 (U8) Bus Signals

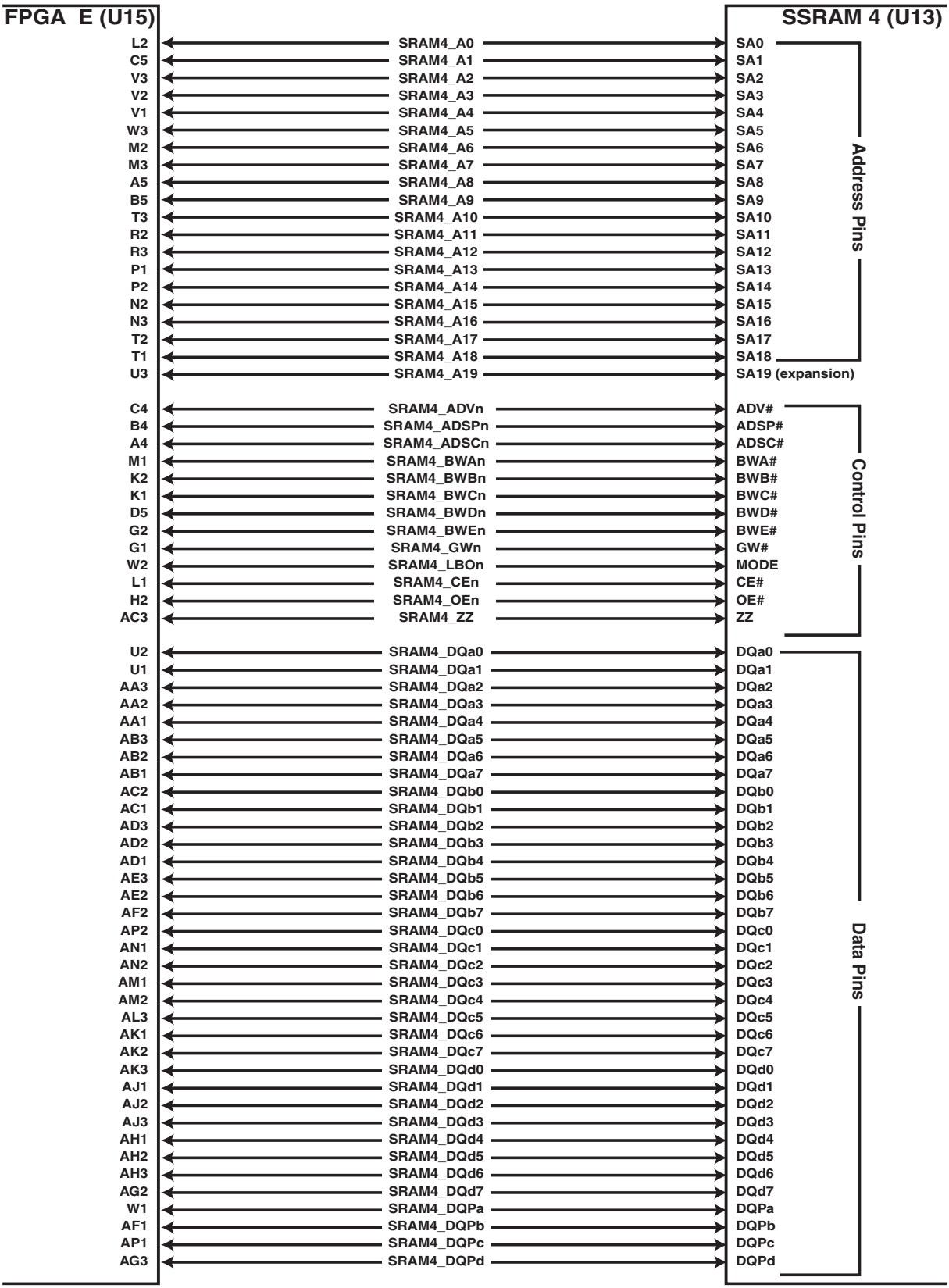


Figure 5-4 SSRAM 4 (U13) Bus Signals

Pin 14 of each SSRAM may be pulled high, pulled low, or left unconnected. Table 5-1describes which 0-ohm resistors must be used for each type of SSRAM to function correctly.

Table 5-1 Requirements for Non-Standard SSRAMs

	FB	AD	AB	ED
ZBT Pipeline	**Install R129 R2**	**Install R130 R3**	**Install R128 R1**	**Install R215 R70**
ZBT Flowthrough	**Install R129 R140**	**Install R130 R142**	**Install R128 R138**	**Install R215 R216**
Syncburst Flowthrough or Pipeline	**No Extra Resistors**			

Pipeline, Flowthrough, ZBT

Syncburst FT (Flowthrough) (Figure 5-5) is the most straightforward type of SSRAM available for the ET5000k10S. Write data may be accepted on the same clock cycle as the activation signal and address, and read data is returned one clock cycle after it is requested. Syncburst is designed to allow two controllers to access the same SSRAM, using two activation signals, ADSC# and ADSP#; an activation with ADSP# requires data and byte enables one clock cycle after the address and activation. Syncburst PL (Pipelined) (Figure 5-6) is identical except for registered outputs, which delay read data an additional clock cycle but may be necessary for high-speed designs.

Zero-Bus-Turnaround (ZBT) SSRAMs are designed to eliminate wait states between reads and writes by synchronizing data. Thus, ZBT FT SSRAMs (Figure 5-7) accept and return data one clock cycle after the address phase, and ZBT PL SSRAMs (Figure 5-8) accept and return data two clock cycles after the address phase. This allows the user to begin a write burst immediately after the last word of a read burst, because read data will be returned before the first write data is required. The timing is illustrated in Figure 5-9 and Table 5-2.

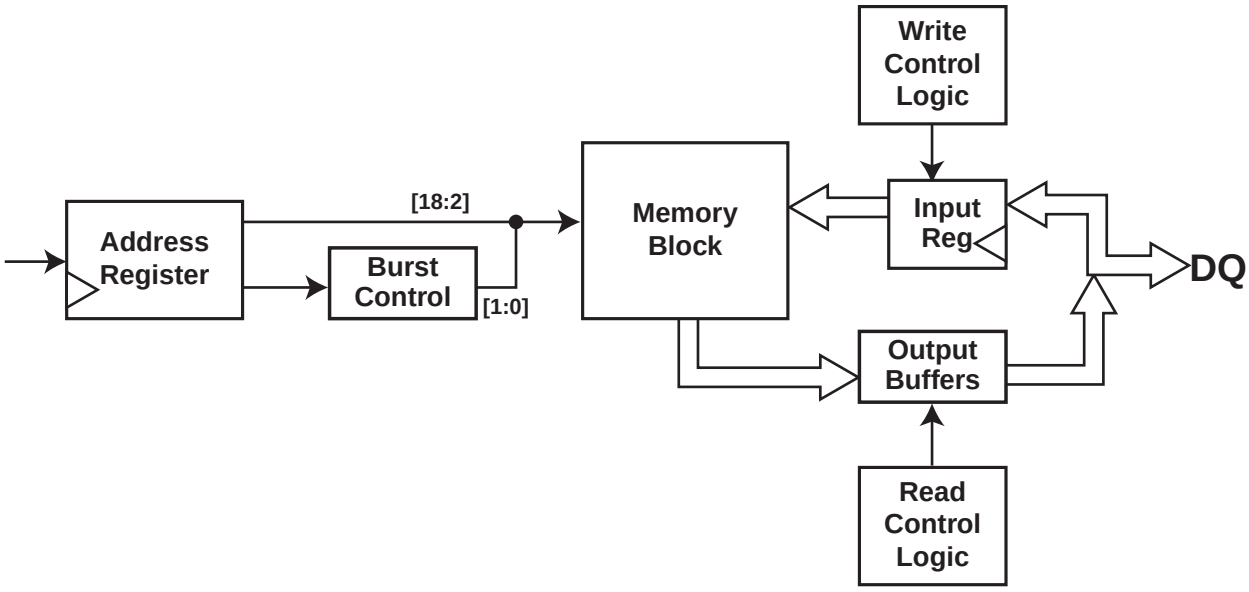


Figure 5-5 Syncburst FT

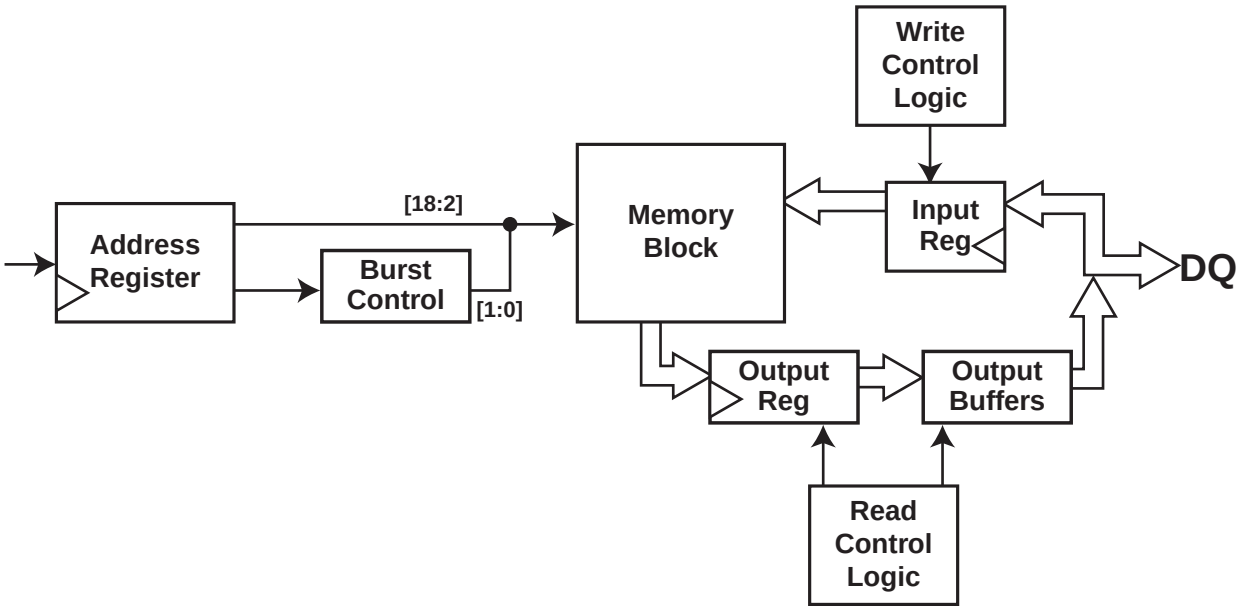


Figure 5-6 Syncburst PL

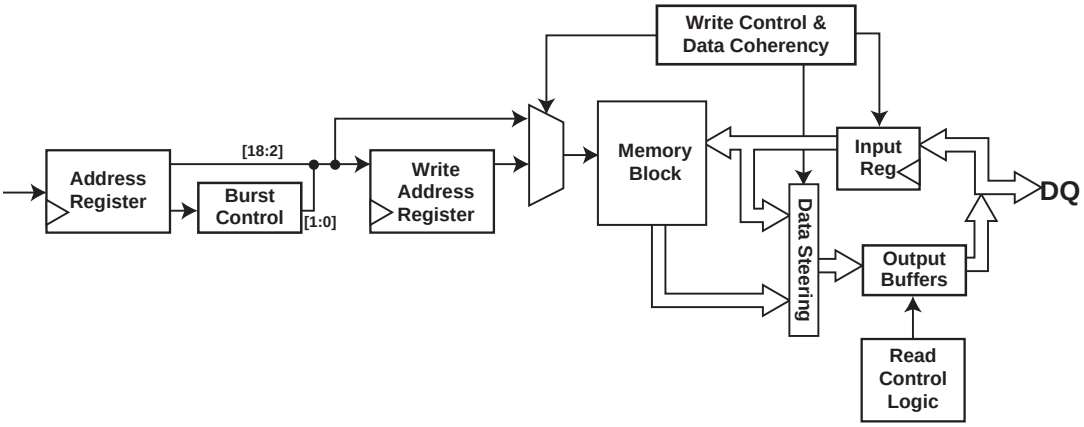


Figure 5-7 Syncburst ZBT FT

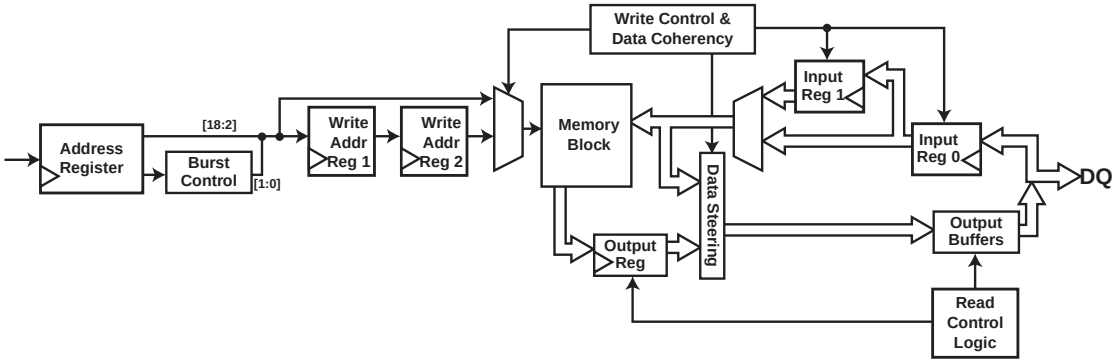


Figure 5-8 Syncburst ZBT PL

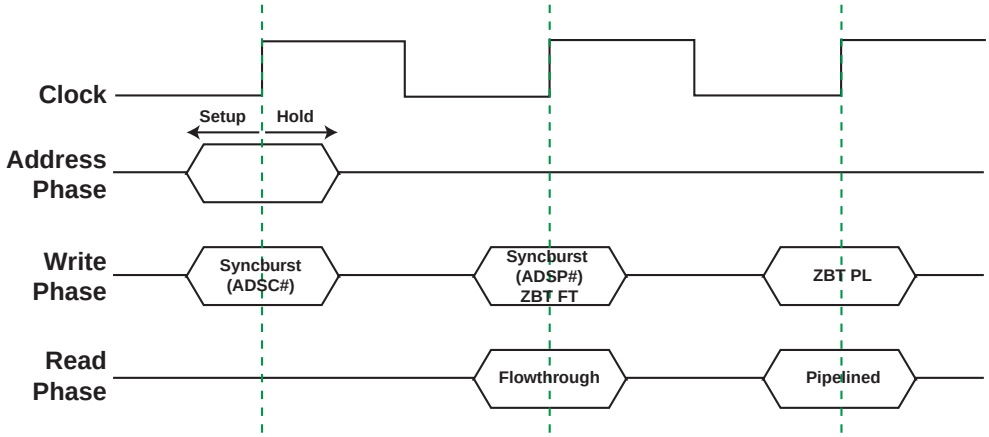


Figure 5-9 Syncburst and ZBT SSRAM Timing

Table 5-2 Syncburst and ZBT SSRAM Timing

	Syncburst	ZBT
Address Phase	CE#, CE2#, CE ADSC#, **or** ADSP# **address** **or** ADV#[1]	CE#, CE2#, CE R/W#, LD#[2], BWx# **address** **or** ADV[2], BWx#[3]
Write Phase	BWE#, BWx#, **or** GW#[4] **data**	**data**
Read Phase	**Valid Data**	**Valid Data**
[1]**To continue a burst.** [2]ADV/LD# **is low to load a new address, high to continue bust.** [3]**For write access only.** [4]**Writes to all four bytes.**		

SDRAM

- The ET5000k10S has a socket for a +3.3 V 168-pin SDRAM DIMM. Either registered or unbuffered modules fit in the socket (**J3**). The same PC100/PC133 SDRAM modules that you put into your PC are used here. Your ET5000k10S will be stuffed and tested with a 1 Gbyte PC133 SDRAM DIMM, unless otherwise requested.

All DIMM pins are connected to the FPGA and the pins are shown in Figure 5-10 and Figure 5-11. We aren't quite sure what the largest size SDRAM DIMM is that will work in the ET5000k10S, but here is the math as best we understand it:

14 Address lines A[13:0]
(multiplexed between RAS* and CAS*, address 10 not used for CAS*)27
2 bank address BA[1:0] 2
4 chip selects (S[3:0]*) used in pairs1

So, we think that there are 29 address bits (27 + 2) and 2 possible chips selects, which add one more address bit. This totals 30 address bits — 1 G of 72-bit long words, which is 8 Gbytes. Please tell us if this math is wrong.

SDRAM modules require 4 clocks — CK[3:0]. These clocks are driven by the RoboclockII 2 and the signal names are ECLK.

The CD-ROM has a datasheet of an acceptable 1 Gbyte SDRAM module from Micron. The file name is SDF36C64_127x72G_B.pdf.

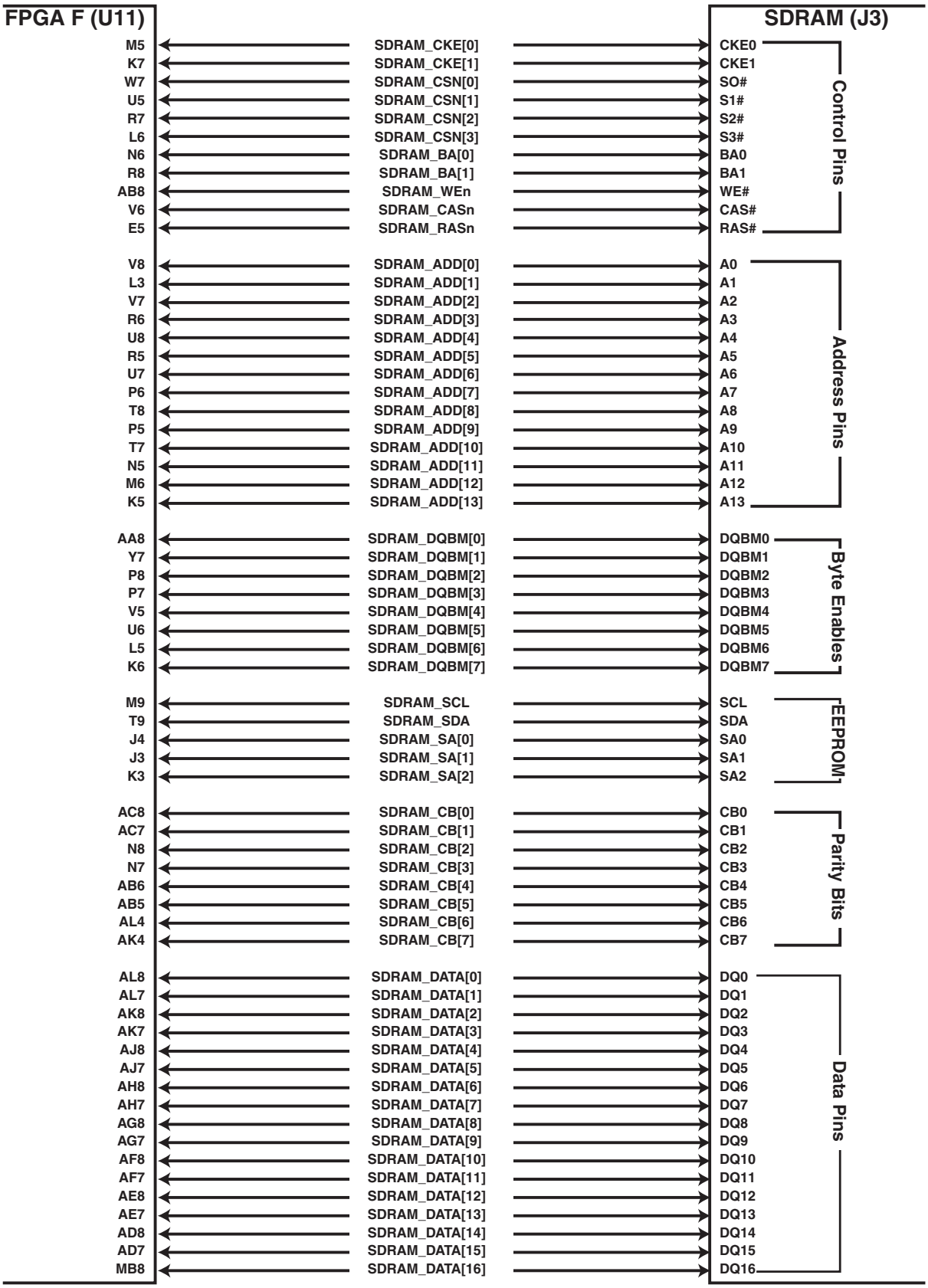


Figure 5-10 SDRAM (J19) Bus Signals (Page 1 of 2)

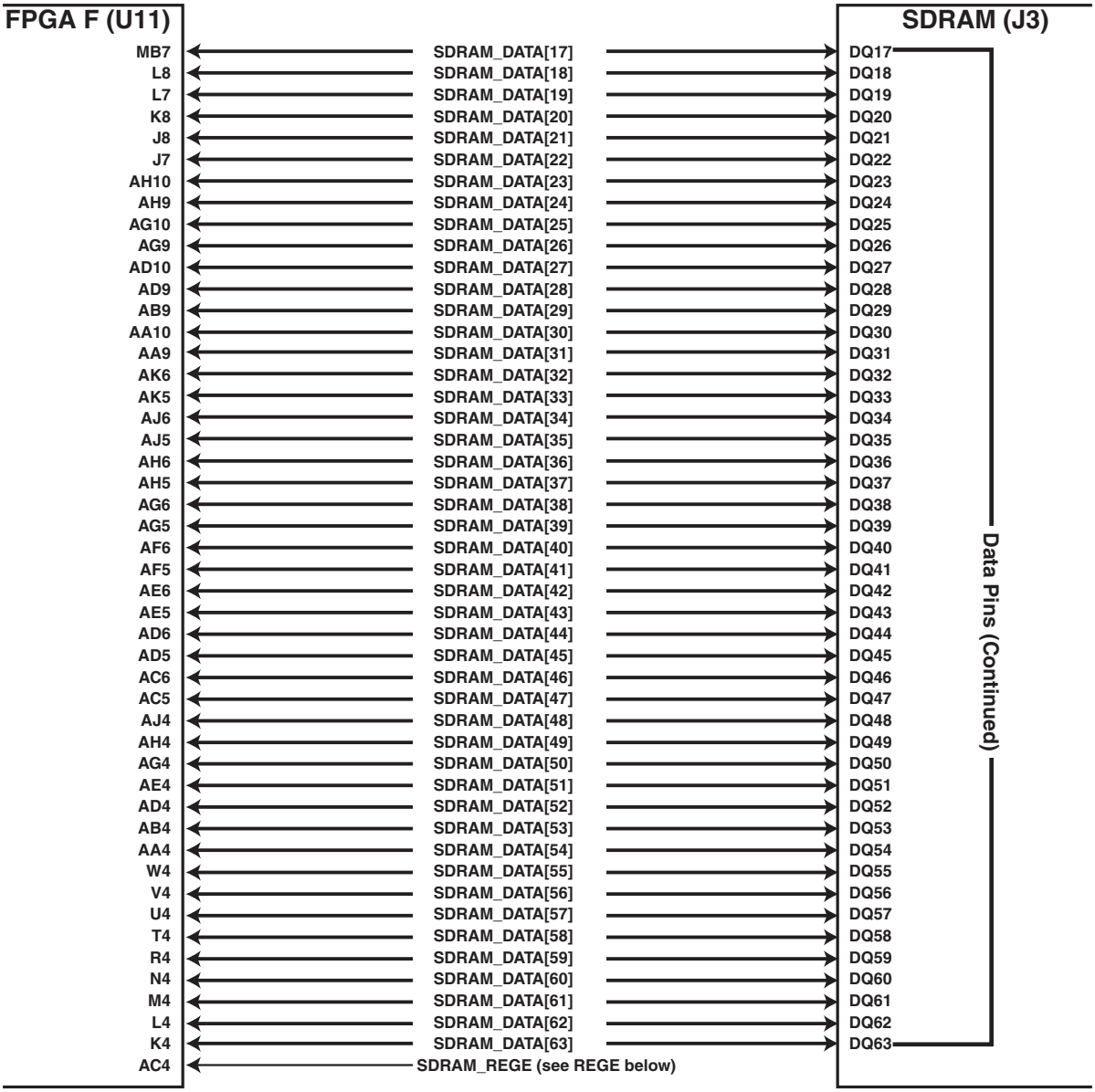


Figure 5-11 SDRAM (J19) Bus Signals (Page 2 of 2)

SDRAM On-Board Options

R218 and **R217** are connected to the WP (Write Protect) input of the SDRAM EEPROM. Stuffing a 0-ohm resistor in **R217** will keep the WP signal high, whereas stuffing it in **R218** drives the signal low. The default configuration is **R217** stuffed. **NEVER** stuff both resistors at the same time.

The EEPROM holds data describing the size, configuration, and timing characteristics of the SDRAM. The data is write-protected when the WP signal is high. There should be little or no reason to want to overwrite the EEPROM data. Some SDRAM manufacturers simply connect the WP pin of the EEPROM chip to the power supply of the SDRAM, in which case the WP resistors have no effect whatsoever.

Header **JP7** is connected to the REGE (Register Enable) input of the SDRAM and to ground. A pull-up resistor keeps the REGE signal high when the header is unconnected; adding a jumper between the two pins drives the signal low. The default configuration is no jumper. REGE is also connected to the FPGA, intended as an input so that the design can check the status of REGE. Do **NOT** drive this signal high when **JP7** is jumpered.

On some SDRAMs, the REGE input may be used to select Registered or Non-Registered behavior. If REGE is high, the control signals will go through registers before being sent to the individual DRAMs, delaying access by one clock cycle but improving fanout; if it is low, the signals will be passed directly to the DRAMs.

DDR SDRAM

The ET5000k10S has a socket for a 184-pin DDR SDRAM DIMM. Either a registered or unbuffered module fits in the socket (**J2**). The same PC266/PC2100 modules that you put into your PC are used here. Your ET5000k10S will be stuffed and tested with a 512 MB PC2100 DDR SDRAM DIMM unless otherwise specified.

All DIMM pins are connected to the FPGA and the pins are shown in Figure 5-12 and Figure 5-13. The largest DDR SDRAM that the ET5000k10S can be stuffed with is 1 GB x 72 (8 GB).

DDR SDRAM modules require three (3) differential clocks: CK[2:0] and CK#[2:0]. these clocks are driven by the FPGA's enhanced PLL6 outputs and the signal names are DDR_CLK[2:0] and DDR_CLKn[2:0]. For further information on Stratix PLL operation, see the Altera website at **www.altera.com**. The Stratx Datasheet (ds_stx.pdf), which can be found on the ET5000k10S CD-ROM, also provides useful information on PLLs.

DDR SDRAM On-Board Options

R59 is connected to the WP (Write Protect) input of the DDR SDRAM EEPROM. Stuffing a 10 K-Ohm resistor in **R59** will keep the WP signal low (inactive). The default configuration is **R59** stuffed.

The EEPROM holds data describing size, configuration, and timing characteristics of the DDR SDRAM. The data is write-protected when the WP signal is high. There should be little or no reason to want to overwrite the EEPROM data. Some manufacturers simply connect the WP pin of the EEPROM chip to the power supply, in which case the WP resistor has no effect whatsoever.

Header **JP4** allows the user to select which clock the DDR SDRAM runs off of. Figure 5-14 shows the DDR Clock Select Jumper **JP4**. The signal DDR_PLL6, which is connected to pin 2 of **JP4** connects to the input of the FPGA's Enhance PLL6. A PLL must be instantiated in the FPGA HDL code to setup the DDR clock signal. This PLL will need to have three (3) output positive differential clocks: one board level clock output used for feedback, one clock input and one feedback input (see Figure 5-14 for a diagram of the DDR PLL circuit).

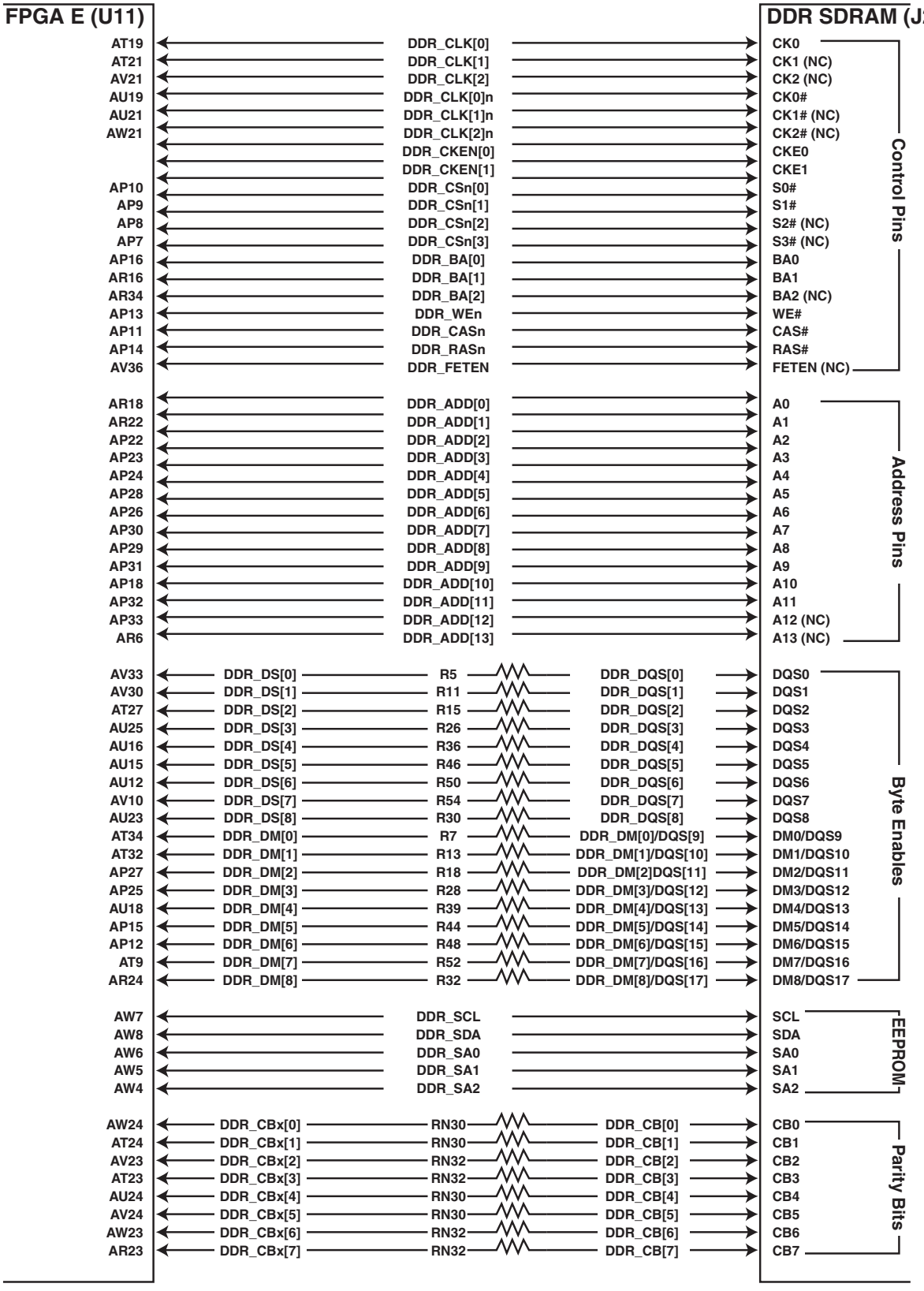


Figure 5-12 DDR SDRAM (J2) Bus Signals (Page 1 of 2)

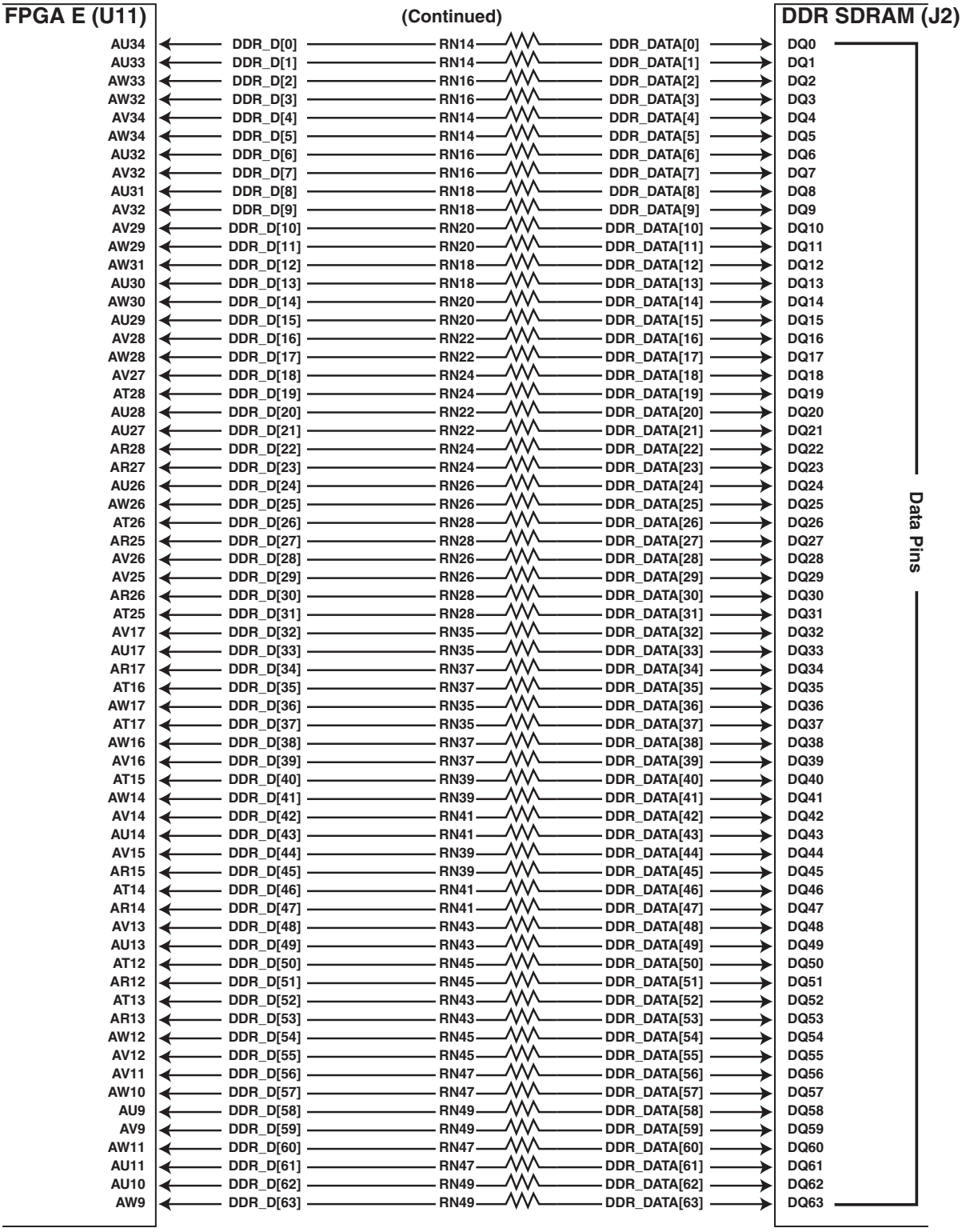


Figure 5-13 DDR SDRAM (J2) Bus Signals (Page 2 of 2)

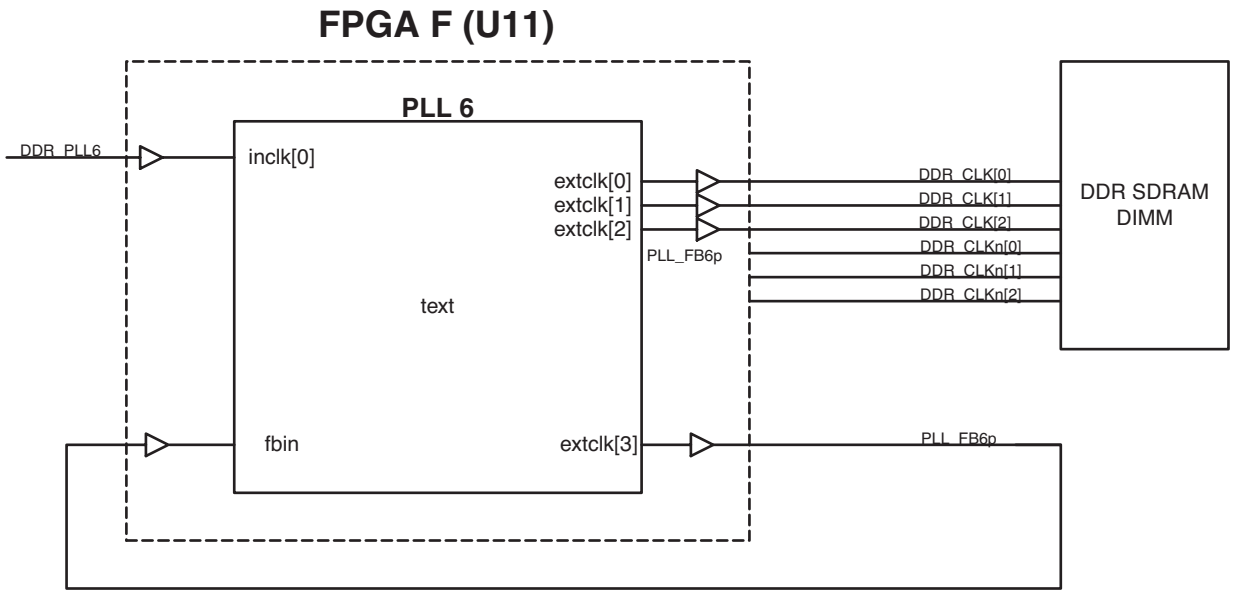


Figure 5-14 DDR PLL Circuit Block Diagram

To make the three positive differential output clocks differential, the IO_STANDARD for all three clock signals needs to be set to DIFFERENTIAL SSTL-2. The Board level PLL clock output is used for the feedback, and needs to have IO_STANDARD set to SSTL-2 CLASS I. The input clock to the PLL must have its IO_STANDARD set to SSTL-2 CLASS II. For information on how to set the IO_STANDARD property, please see the Quantus help files. If the IO_STANDARD properties are set up correctly, then the three negative differential clock signals (DDR_CLKn[2:0]) will automatically be output from the FPGA. You do not need to include these negative clock signals in your FPGA HDL code or pin assignment file.

To change which clock goes to the DDR, the user just needs to change the position of the jumper on **JP4**. Please note there should only be one jumper on **JP4**. The DDR Clock Select Jumper is illustrated in Figure 5-15.

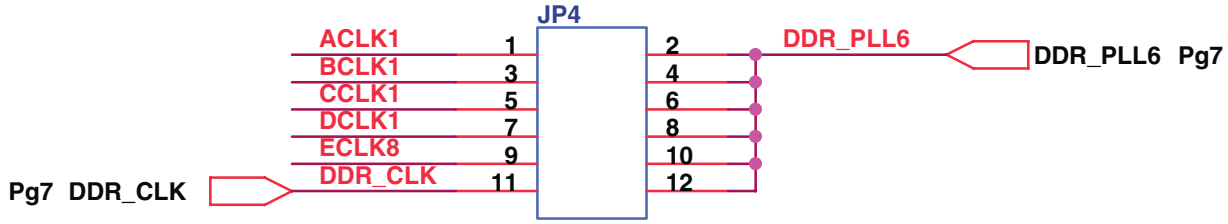


Figure 5-15 DDR Clock Select Jumper (JP4)

Chapter 6

Power Supplies and Power Distribution

The ET5000k10S can be hosted in a +3.3 V PCI slot, or it can be used stand-alone. Figure 6-1 shows the various supplies used on the ET5000k10S and the connections of these supplies on the circuit board. The supply, +5 V, from the PCI connector (or **P1**) supplies the basic power to the ET5000k10S. The +3.3 V power from the PCI connector is ***not*** used, nor is it connected to any circuitry on the ET5000k10S.

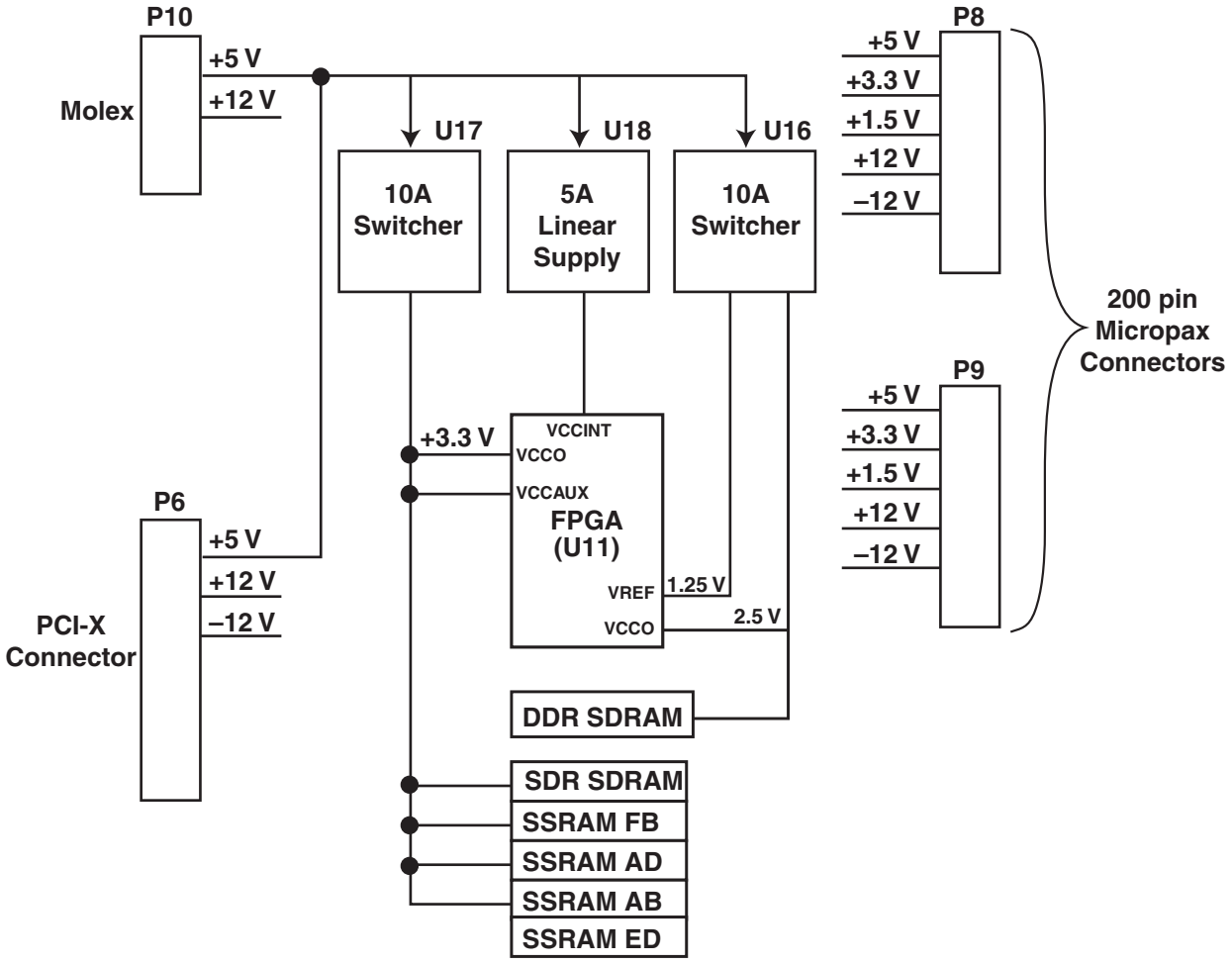


Figure 6-1 ET5000k10S Power Distribution

The ET5000k10S, when plugged into a PCI slot, has the following different power rails:

- +5 V
- +3.3 V

- +2.5 V
- +1.25 V (tracks to +2.5 V)
- +1.5 V
- –12 V
- +12 V

The power rails +3.3 V, +2.5 V, and +1.25 V and +1.5 V are created using switching regulators with +5 V as the input, while +1.5 V is created with a linear regulator. +3.3 V from the PCI fingers is ***not*** used. **U17** is for +3.3 V, **U16** is for +2.5 V and +1.25 V, and **U18** is for +1.5 V. Heat is not an issue with this style of switching regulator. Each regulator should be able to supply the minimum 10 A of current without strain. The most demanding application of the ET5000k10S should fit within the 10 A budget on these two power rails. A heat sink is used to keep the linear regulator within its specification.

+3.3 V Power

The specification for the +3.3 V power is shown in Table 6-1. The +3.3 V supply is used by the following components on the ET5000k10S:

- Stratix FPGA I/O (**U11,** banks 1–6)
- Roboclocks **U14, U15**
- Clock buffer **(U12)**
- CPLD (**U6**)
- Microprocessor (**U4**)
- Microprocessor SRAM (**U7**)
- 4 SSRAMs (**U8, U9, U10, U13**)
- DDR SDRAM DIMM (**J3**)
- 3 Oscillators **X1**, **X2**, **X3**

We do run +3.3 V a little hot. At worst case for all components, the +3.3 V power supply should never fall below +3.30 V.

Table 6-1 Specification for +3.3 V Power

	Minimum	Typical	Maximum
Voltage	**+3.35 V**	**+3.39 V**	**+3.44 V**
Current	**N/A**	**N/A**	**12 A**

+2.5 V Power

The specification for the +2.5 V power is shown in Table 6-2. The +2.5 V supply is used by the following components on the ET5000k10S:

- Stratix FPGA I/O (**U11**, banks 7–8)
- DDR SDRAM DIMM (**J2**)

In addition, the +2.5 V supply outputs a +1.25 V power rail, used by the Stratix FPGA as a reference voltage. The reference voltage tracks to the supply voltage, within 1%.

Table 6-2 Specification for +2.5 V Power and +1.25 V Reference

	Min	Typical	Max
Supply Voltage	+2.45	+2.50	+2.55
Supply Current	N/A	N/A	10 A
Reference Voltage	49.5% of Supply	50% of Supply	50.5% of Supply
Reference Current	N/A	N/A	5 A

+1.5 V Power

The specification for the +1.5 V power is shown in Table 6-3. The +1.5 V supply is used by the following component on the ET5000k10S:

- Stratix FPGA V_{cc}INT (**U11**)

We also run +1.5 V a little hot. At worst case for all components, the +1.5 V power supply should never fall below +1.50 V.

Table 6-3 Specification for +1.5 V Power

	Minimum	Typical	Maximum
Voltage	+1.55 V	+1.56 V	+1.58 V
Current	N/A	N/A	12 A

If you use the ET5000k10S in a lab environment, the Stratix FPGA will never see worst case power and temperature—so you can use typical, commercial timing.

NOTE: In a lab environment, the FPGA never sees the worst-case temperature and power. You can use typical, commercial timing!

Stand-Alone Operation

The ET5000k10S can be used stand-alone, meaning it doesn't have to be plugged into a PCI slot. Connector **P1** is used to provide power to the ET5000k10S in this configuration. **P1** is a Molex drive power connector and will connect to any standard ATX power supply (see Figure 6-2). The power supply that we used is shown in Figure 6-3, but any ATX or AT style power supply will work. We use a 250-watt ATX supply. Since the ET5000k10S does not draw enough current to meet the minimums required by the supply, we plug an old disk drive into another one of the Molex connectors. The current drawn by the disk drive sinks enough current to make the switchers in the power supply happy.

Figure 6-3 Example ATX Power Supply

The **P1** connector is rated to 13 A, far more current than the ET5000k10S can use.

The ET5000k10S, when used stand-alone, has the following different power rails:

- +5 V

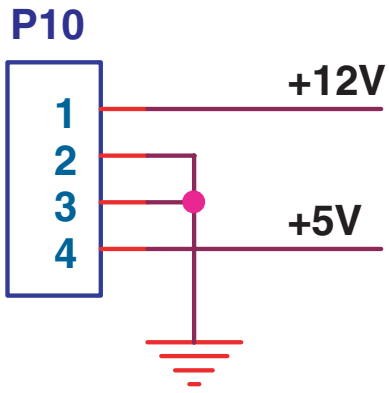


Figure 6-2 Molex Connector P1—Auxiliary Power

- +3.3 V
- +2.5 V
- +1.25 V (tracks to 2.5 V)
- +1.5 V
- +12 V

NOTE: If you use the ET5000k10S stand-alone with an ATX power supply, the ET5000k10S may not draw enough current to meet the minimum current required by the switchers in the supply. Connecting a disk drive to another connector will solve this problem!

By specification, a PCI board may consume a maximum of 25 watts from the fingers of the PCI connector. This power limit is below that the ET5000k10S is capable of consuming, even if daughter cards and/or large SDRAM banks are installed. The **P1** connector can be used to augment the power obtained from the PCI fingers. **P1** can be used provided that the +5 V and +12 V power rails on the connector are supplied by the same power source as the PCI fingers.

NOTE: P1 and PCI may provide power at the same time, but ONLY if the same power source used to supply P1 is also supplying power to PCI.

Chapter 7

Daughter Connections to ET3k10SD—Observation Daughter Card for 200-pin Connectors

The traditional approach to experiment with new devices involving wiring together some ICs on a breadboard is fast becoming impractical and ineffective. Instead, designers using new high-density devices need custom PC boards representing a substantial investment of time and money.

Prototype boards from manufacturers can meet this demand for experimentation while eliminating the expense and time involved with custom PC boards. Additionally, such prototype boards facilitate the understanding and advantages of new device features.

Purpose

The ET3k10SD daughter card allows external connection to the signals present on the ET5000k10S series ASIC prototyping boards. The ET5000k10S allows logic emulation with Stratix™ devices prior to committing to using them for specific applications. It allows designers to try Stratix features such as BlockRAM, DLLs, and SelectI/O™ resource, with an off-the-shelf resource.

Features

The ET3k10SD Daughter Card has the following features:

- Buffered I/O, Passive and Active Bus Drivers
- Unbuffered I/O
- Differential LVDS pairs (Note: Not available on ET5000k10S ASIC prototyping board)
- Headers for Test Points

The daughter card contains headers that may be useful with certain types of oscilloscope probes, or when wiring pins to prototype areas.

Figure 7-1 is a block diagram of the ET3k10SD Daughter Card.

The ET3k10SD Daughter Card is pictured in Figure 7-2.

Figure 7-3 shows the assembly drawing of the ET3k10SD Daughter Card.

The ET3k10SD Daughter Card provides 16 differential pairs, 48 buffered (passive/active) I/O, and 66 unbuffered I/O signals. The IDT74FST163245 chips are used as bus switches in the passive mode, and the

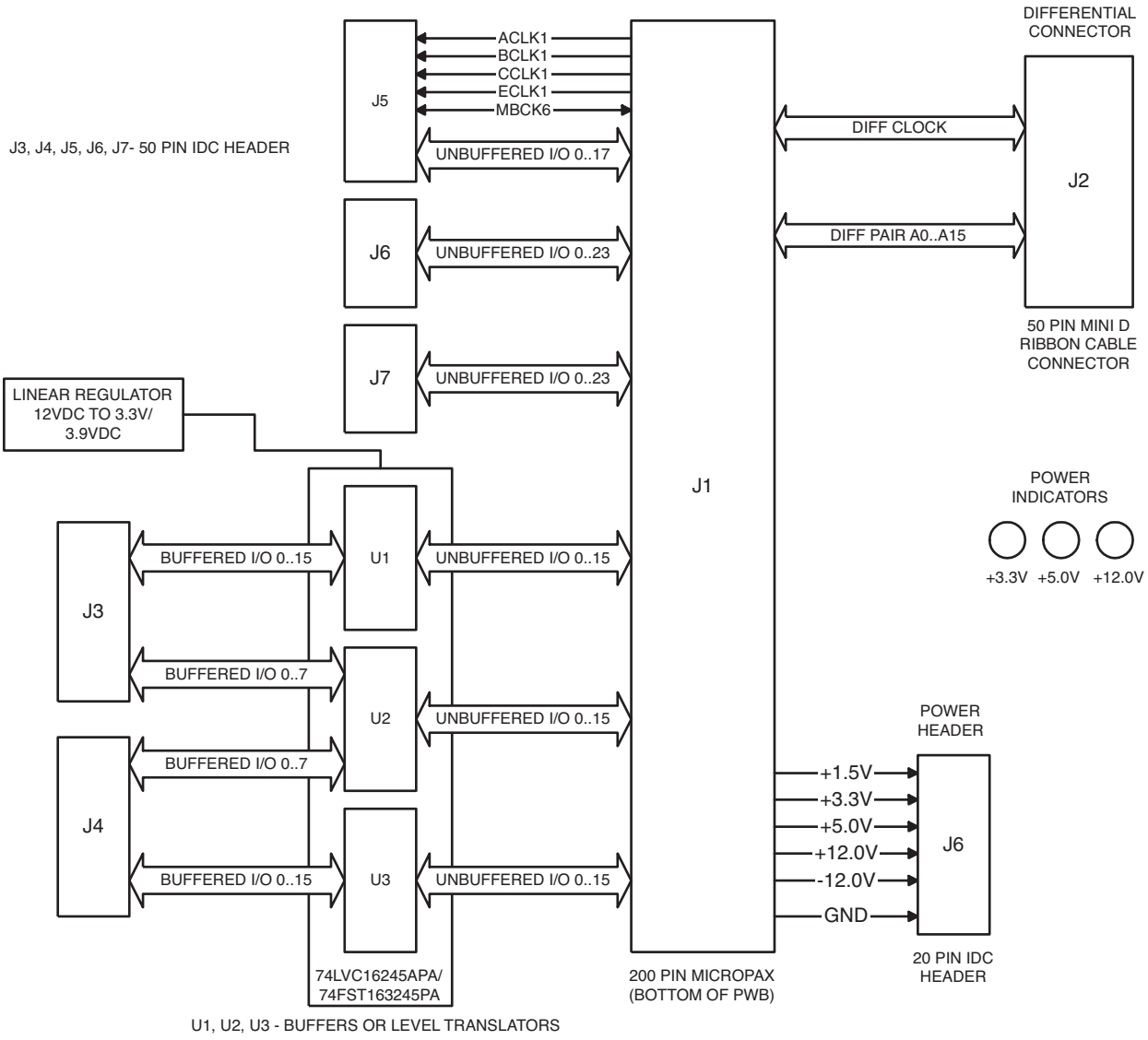
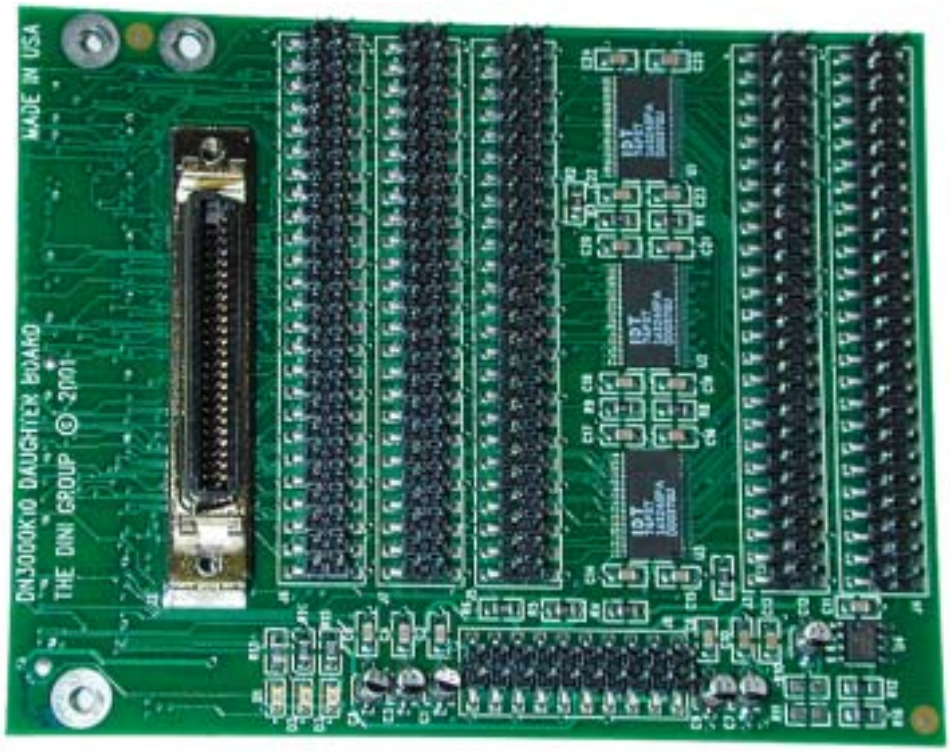
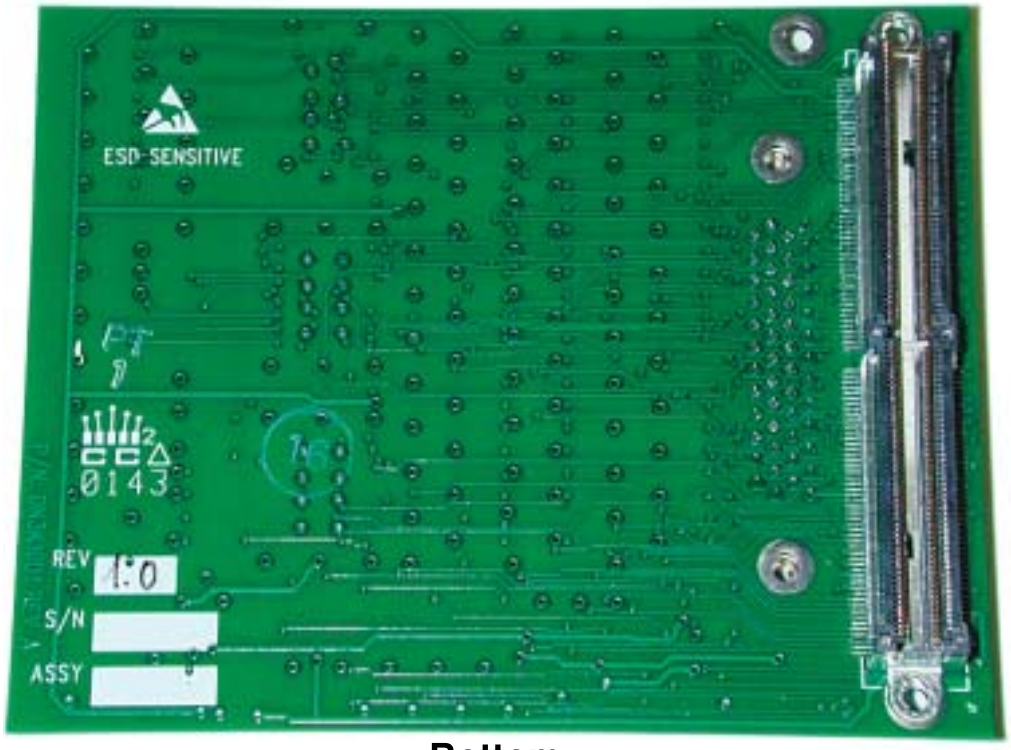


Figure 7-1 ET3k10SD Daughter Card Block Diagram



Top



Bottom

Figure 7-2 ET3k10SD Daughter Card

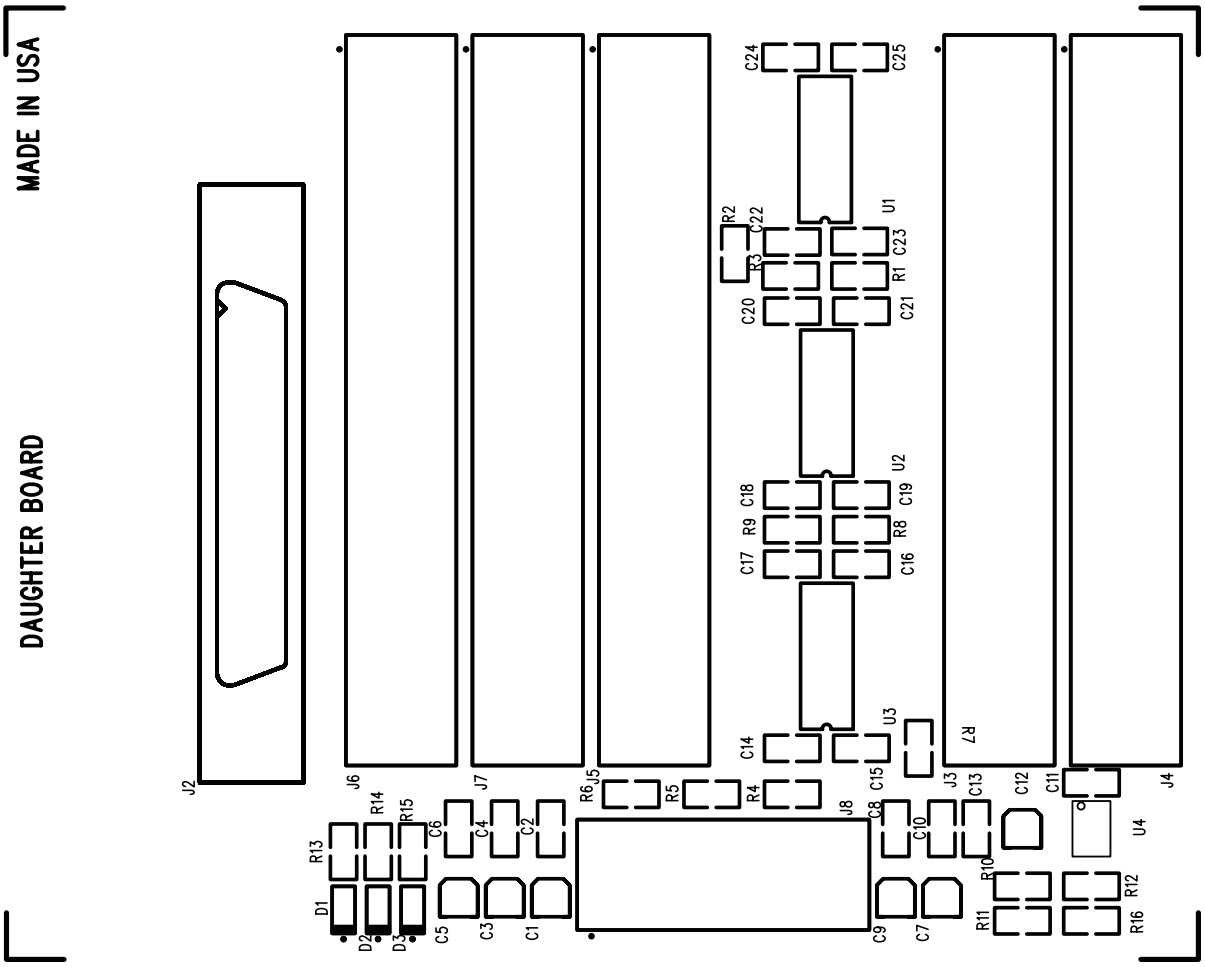


Figure 7-3 ET3k10SD Daughter Card Assembly Drawing

IDT74LVC16245A chips are used as bus transceivers in the active mode. The ET3k10SD has separate enable/direction signals for each driver.

NOTE: Availability of these I/O signals depends on the location of the daughter card with respect to the development board.

Daughter Card LEDs

The LEDs act as visual indicators, representing the active power sources.

- **D1** — LED indicating +3.3 V present
- **D2** — LED indicating +5.0 V present
- **D3** — LED indicating +12 V present

Under normal operating conditions, all LEDs should be on.

Power Supply

A linear power supply (**U4**) is present to provide level shift/translation functions when the board is populated with bus switches.

Options

Resistors **R10** and **R11** can be used to select different voltage sources, +5 V or +3.3 V, respectively. When used, **U4** must be removed in order to prevent contention.

NOTE: Never populate R10/R11 simultaneously: this will result in a shorted power supply.

Power Rating

- +5 V power supply is rated for 1 A.
- +3.3 V power supply is rated for 1 A.
- +1.5 V power supply is rated for 1 A.
- +12 V power supply is rated for 0.5 A.
- –12 V power supply is rated for 0.5 A.

Connector J8

Table 7-1 shows the connections of **J8**.

Table 7-1 Connector J8 Pins External Power

Pin	Function	Pin	Function
1	GND	11	GND
2	+5 V	12	+1.5 V
3	GND	13	GND
4	+5 V	14	+12 V
5	GND	15	GND
6	+3.3 V	16	+12 V
7	GND	17	GND
8	+3.3 V	18	–12 V
9	GND	19	GND
10	+1.5 V	20	–12 V

LVDS

Low-voltage differential signaling (LVDS) is a signaling method used for high-speed transmission of binary data over copper. It is well recognized that the benefits of balanced data transmission begin to outweigh the costs over single-ended techniques when the signal transmission times approach 10 ns. This represents signaling rates of about 30 Mbps or clock rates of 60 MHz (in single-edge clocking systems) and above. LVDS is defined in the TIA/EIA-644 standards.

NOTE: Not available on the ET5000k10S ASIC prototyping board.

Connector P5

This is a Mini D Ribbon (MDR) connector (50 pin) manufactured by 3M, used specifically for high speed LVDS signaling. The connector mates with a standard off-the-shelf 3M-cable assembly:

P/N 14150-EZBB-XXX-0LC

where XXX is:050 = 0.5 m
150 = 1.5 m
300 = 3.0 m
500 = 5.0 m

Please contact 3M for further details: **http://www1.3m.com/**.

Unbuffered I/O

The ET3k10SD Daughter Card provides 66 unbuffered I/O signals, including 5 single ended clock signals. The function of these signals is position dependent.

NOTE: SIgnals P4NX7 and P4NX6 are also used for direction select and output enable on U2 and U3 respectively.

Connectors P2, P4

P2, **P4**— Buffered Interface header

IDC headers (50 pin) providing 48 buffered I/O signals.

See Table 7-2 on page 7.

Connector P7, P1, P3

P7, P1, P3 — Unbuffered Interface Header

IDC headers (50 pin) providing 66 buffered I/O signals.

See Table 7-2 on page 7.

Buffered I/O

The ET3k10SD Daughter Card provides 48 buffered I/O signals. The function of these signals is position dependent. **U1**, **U2**, and **U3** allow for different populating options, and devices can be active or passive.

Active

The LCV162245A is used for asynchronous communication between data buses. It allows data transmission from the A to the B or from the B to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE#) input can be used to disable the device so that the busses are effectively isolated.

Passive

The FST163245 bus switches are used to connect or isolate two ports without providing any current sink or source capabilities. Thus, they generate little or no noise of their own while providing a low resistance

path for an external driver. The output-enable (0E#) input can be used to disable the device so that the busses are effectively isolated.

Test Interface

The ET3k10SD Daughter Card provides a 200-pin connector to interface to one of three test connectors on the ET5000k10S ASIC prototyping board: **J9**, **J10** and **J16**.

Connector J1

J1—Test Interface Connector

Micropax connector (200 pin) used as a standard interface to all the Emulation Technology, Inc. development boards. This connector has a specified current rating of 0.5 amps per contact. See Table 7-2 on page 7.

Daughter Card I/O Connections

Table 7-2 shows the ET3k10SD Daughter Card I/O Interconnects to connectors **P55, P56** and **P58**.

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
1	+12 V		P8.001	+12 V		P9.001	+12 V	
2	GND	J1.184	P8.002	GND	K20	P9.002	GND	K20
3	ACLK[1]	J5.1	P8.003	ACLK[2]		P9.003	ACLK[3]	
4	+5 V	J1.006	P8.004	+5 V		P9.004	+5 V	
5	BCLK[1]	J5.3	P8.005	BCLK[2]		P9.005	BCLK[3]	
6	+5 V		P8.006	+5 V		P9.006	+5 V	
7	CCLK[1]	J5.5	P8.007	CCLK[2]		P9.007	CCLK[3]	
8	GND	J1.204	P8.008	GND	K20	P9.008	GND	K20
9	+3.3 V		P8.009	+3.3 V	H20	P9.009	+3.3 V	H20
10	P2N[3]	U1.26 J3.1	P8.010	ECLK[10]		P9.010	ECLK[11]	
11	GND	J4.26 J7.38	P8.011	GND	K20	P9.011	GND	K20
12	P2N[2]	U1.27 J3.3	P8.012	TST_HDRA[0]	AU2	P9.012	TST_HDRB[0]	G33
13	P2N[1]	J2.8	P8.013	TST_HDRA[1]	AT1	P9.013	TST_HDRB[1]	F33
14	P2N[0]	J2.9	P8.014	TST_HDRA[2]	AT2	P9.014	TST_HDRB[2]	G32
15	P2NX[7]	U1.29 J3.5	P8.015	TST_HDRA[3]	AT3	P9.015	TST_HDRB[3]	F32
16	P2NX[6]	U1.30 J3.7	P8.016	TST_HDRA[4]	AR1	P9.016	TST_HDRB[4]	F31
17	P2NX[5]	U1.32 J3.9	P8.017	TST_HDRA[5]	AR2	P9.017	TST_HDRB[5]	G31

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
18	P2NX[4]	U1.33 J3.11	P8.018	TST_HDRA[6]	AR3	P9.018	TST_HDRB[6]	H31
19	P2NX[1]	J2.10	P8.019	TST_HDRA[7]	AP3	P9.019	TST_HDRB[7]	M31
20	P2NX[0]	J2.11	P8.020	TST_HDRA[8]	AN3	P9.020	TST_HDRB[8]	N31
21	P3NX[9]	J2.40	P8.021	TST_HDRA[9]	AM3	P9.021	TST_HDRB[9]	P31
22	GND	J1.101	P8.022	GND	K20	P9.022	GND	K20
23	P3NX[8]	J2.41	P8.023	TST_HDRA[10]	H3	P9.023	TST_HDRB[10]	R31
24	P3NX[5]	U1.35 J3.13	P8.024	TST_HDRA[11]	G3	P9.024	TST_HDRB[11]	T31
25	P3NX[4]	U1.36 J3.15	P8.025	TST_HDRA[12]	F1	P9.025	TST_HDRB[12]	U31
26	P3N[89]	U1.37 J3.17	P8.026	TST_HDRA[13]	F2	P9.026	TST_HDRB[13]	F30
27	P3N[88]	U1.38 J3.19	P8.027	TST_HDRA[14]	F3	P9.027	TST_HDRB[14]	G30
28	P3N[87]	U1.40 J3.21	P8.028	TST_HDRA[15]	E1	P9.028	TST_HDRB[15]	J30
29	P3N86	U1.41 J3.23	P8.028	TST_HDRA[16]	E2	P9.029	TST_HDRB[16]	M30
30	P3N[83]	U1.43 J3.25	P8.030	TST_HDRA[17]	E3	P9.030	TST_HDRB[17]	N30
31	P3N[82]	U1.44 J3.27	P8.031	TST_HDRA[18]	D1	P9.031	TST_HDRB[18]	P30
32	P3N[77]	U1.46 J3.29	P8.032	TST_HDRA[19]	D2	P9.032	TST_HDRB[19]	R30
33	GND	J5.20 J6.22	P8.033	GND	K20	P9.033	GND	K20
34	P3N[76]	U1.47 J3.31	P8.034	TST_HDRA[20]	D3	P9.034	TST_HDRB[20]	T30
35	P3N[75]	U2.26 J3.33	P8.035	TST_HDRA[21]	C2	P9.035	TST_HDRB[21]	U30
36	P3N[74]	U2.27 J3.35	P8.036	TST_HDRA[22]	B3	P9.036	TST_HDRB[22]	V30
37	P3N[69]	J2.42	P8.037	TST_HDRA[23]	AR4	P9.037	TST_HDRB[23]	W30
38	P3N[68]	J2.43	P8.038	TST_HDRA[24]	AP4	P9.038	TST_HDRB[25]	AC30
39	P3N[67]	U2.29 J3.37	P8.039	TST_HDRA[25]	AP5	P9.039	TST_HDRB[24]	AD30
40	P3N[66]	U2.30 J3.39	P8.040	TST_HDRA[26]	AN4	P9.040	TST_HDRB[26]	AD30
41	P3N[63]	U2.32 J3.41	P8.041	TST_HDRA[27]	AN5	P9.041	TST_HDRB[27]	AE30
42	P3N[62]	U2.33 J3.43	P8.042	TST_HDRA[28]	AM4	P9.042	TST_HDRB[28]	AF30
43	P3N[57]	U2.35 J3.45	P8.043	TST_HDRA[29]	AM5	P9.043	TST_HDRB[29]	AG30
44	GND	J3.36	P8.044	GND	K20	P9.044	GND	K20
45	P3N[56]	U2.36 J3.47	P8.045	TST_HDRA[30]	AL5	P9.045	TST_HDRB[30]	AH30
46	P3N[55]		P8.046	TST_HDRA[31]	J5	P9.046	TST_HDRB[31]	AD29

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
47	P3N[54]		P8.047	TST_HDRA[32]	H4	P9.047	TST_HDRB[32]	AC29
48	P3N[49]	U2.37 J4.1	P8.048	TST_HDRA[33]	H5	P9.048	TST_HDRB[33]	AB29
49	P3N[48]	U2.38 J4.3	P8.049	TST_HDRA[34]	G4	P9.049	TST_HDRB[34]	W29
50	P3N[47]	J2.19	P8.050	TST_HDRA[35]	G5			
51	P3N[46]	J2.20	P8.051	TST_HDRA[36]	F4	P9.051	TST_HDRB[36]	U29
52	P3N[43]	U2.40 J4.5	P8.052	TST_HDRA[37]	F5	P9.052	TST_HDRB[37]	T29
53	P3N[42]]	U2.41 J4.7	P8.053	TST_HDRA[38]	E4	P9.053	TST_HDRB[38]	K29
54	P3N[39]	U2.43 J4.9	P8.054	TST_HDRA[39]	D4	P9.054	TST_HDRB[39]	J29
55	GND	J1.044	P8.055	GND	K20	P9.055	GND	K20
56	P3N[38]	U2.44 J4.11	P8.056	TST_HDRA[40]	AP6	P9.056	TST_HDRB[40]	H29
57	P3N[35]	U2.46 J4.13	P8.057	TST_HDRA[41]	AN6	P9.057	TST_HDRB[41]	G29
58	P3N[34]	U2.47 J4.15	P8.058	TST_HDRA[42]	AM6	P9.058	TST_HDRB[42]	F29
59	P3N[29]	U3.26. J4.17	P8.059	TST_HDRA[43]	AL6	P9.059	TST_HDRB[43]	F28
60	P3N[28]	U3.27 J4.19	P8.060	TST_HDRA[44]	AA6	P9.060	TST_HDRB[44]	G28
61	P3N[27]	U3.29 J4.21	P8.061	TST_HDRA[45]	J6	P9.061	TST_HDRB[45]	H28
62	P3N[26]	U3.30 J4.23	P8.062	TST_HDRA[46]	H6	P9.062	TST_HDRB[46]	J28
63	P3N[23]	J2.21	P8.063	TST_HDRA[47]	G6	P9.063	TST_HDRB[47]	K28
64	P3N[22]	J2.22	P8.064	TST_HDRA[48]	F6	P9.064	TST_HDRB[48]	M28
65	P3N[19]	U3.32 J4.25	P8.065	TST_HDRA[49]	E6	P9.065	TST_HDRB[49]	N28
66	GND	J1.044	P8.066	GND	K20	P9.066	GND	K20
67	P3N[18]	U3.33 J4.27	P8.067	TST_HDRA[50]	D6	P9.067	TST_HDRB[50]	P28
68	P3N[15]	U3.35 J4.29	P8.068	TST_HDRA[51]	C6	P9.068	TST_HDRB[51]	R28
69	P3N[14]	U3.36 J4.31	P8.069	TST_HDRA[52]	B6	P9.069	TST_HDRB[52]	T28
70	P3N[9]	J2.23	P8.070	TST_HDRA[53]	A6	P9.070	TST_HDRB[53]	U28
71	P3N[8]	J2.24	P8.071	TST_HDRA[54]	AB7	P9.071	TST_HDRB[54]	V28
72	P3N[7]	U3.37 J4.33	P8.072	TST_HDRA[55]	G7	P9.072	TST_HDRB[55]	W28
73	P3N[6]	U3.38 J4.35	P8.073	TST_HDRA[56]	F7	P9.073	TST_HDRB[56]	AB28
74	P3N[3]	U3.40 J4.37	P8.074	TST_HDRA[57]	E7	P9.074	TST_HDRB[57]	AC28
75	P3N[2]	U3.41 J4.39	P8.075	TST_HDRA[58]	D7	P9.075	TST_HDRB[58]	AD28

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
76	P4N[27]	U3.43 J4.41	P8.076	TST_HDRA[59]	C7	P9.076	TST_HDRB[59]	AE28
77	GND	J4.42 J5.28 J6.6	P8.077	GND	K20	P9.077	GND	K20
78	P4N[26]	U3.44 J4.43	P8.078	TST_HDRA[60]	B7	P9.078	TST_HDRB[60]	AF28
79	P4N[21]	U3.46 J4.45	P8.079	TST_HDRA[61]	A7	P8.079	TST_HDRB[61]	AG28
80	P4N[20]	U3.47 J4.47	P8.080	TST_HDRA[62]	G8	P9.080	TST_HDRB[62]	AH28
81	P4N[19]		P8.081	TST_HDRA[63]	F8	P9.081	TST_HDRB[63]	M27
82	P4N[18]		P8.082	TST_HDRA[64]	D8	P9.082	TST_HDRB[64]	K27
83	P4N[13]		P8.083	TST_HDRA[65]	C8	P9.083	TST_HDRB[65]	J27
84	P4N[12]		P8.084	TST_HDRA[66]	B8	P9.084	TST_HDRB[66]	H27
85	P4N[11]		P8.085	TST_HDRA[67]	AF9	P9.085	TST_HDRA[67]	G27
86	P4N[10]		P8.086	TST_HDRA[68]	AE9	P9.086	TST_HDRB[68]	F27
87	P4N[7]		P8.087	TST_HDRA[69]	AC9	P9.087	TST_HDRB[69]	F26
88	GND	J1.184	P8.088	GND	K20	P9.088	GND	K20
89	P4N[6]	U1.1	P8.089	TST_HDRA[70]	V9	P9.089	TST_HDRB[70]	H26‘
90	P4N[3]	U1.24	P8.090	TST_HDRA[71]	U9	P9.090	TST_HDRB[71]	J26
91	P4N[2]	U1.25	P8.091	TST_HDRA[72]	R9	P9.091	TST_HDRB[72]	K26
92	P4NX[11]	U2.1	P8.092	TST_HDRA[73]	P9	P9.092	TST_HDRB[73]	K25
93	+1.5 V	J1.103	P8.093	+1.5 V	AE20	P9.093	+1.5 V	AE20
94	P4NX[10]	U2.24	P8.094	TST_HDRA[74]	N9	P9.094	TST_HDRB[74]	H25
95	P4NX[7]	J7.45 U2.25	P8.095	TST_HDRA[75]	H9	P9.095	TST_HDRB[75]	G25
96	P4NX[6]	J7.47 U3.1	P8.096	TST_HDRA[76]	G9	P9.096	TST_HDRB[76]	F25
97	P4NX[5]	U3.24	P8.097	TST_HDRA[77]	F9	P9.097	TST_HDRB[77]	F24
98	PRNX[4]	U3.25	P8.098	TST_HDRA[78]	E9	P9.098	TST_HDRB[78]	G24
99	GND	J1.203	P8.099	GND	K20	P9.099	GND	K20
100	-12 V		P8.100	-12 V		P9.100	-12 V	
101	GND	J5.26 J6.24 J7.12	P8.101	GND	K20	P9.101	GND	K20
102	MBCK[1]	J2.27	P8.102	GND	K20	P9.102	GND	K20
103	+1.5 V		P8.103	+1.5 V	AE20	P9.103	+1.5 V	AE20
104	MBCK[0]	J2.28	P8.104	GND	K20	P9.104	GND	K20

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
105	+3.3 V		P8.105	+3.3 V	H20	P9.105	+3.3 V	H20
106	MBCK[6]	J5.9	P8.106	DCLK[2]		P9.106	DCLK[3]	
107	GND	J1.203	P8.107	GND	K20	P9.107	GND	K20
108	ECLK[1]	J5.7	P8.108	GND	K20	P9.108	GND	K20
109	GND	J4.46 J5.40 J7.22	P8.109	GND	K20	P9.109	GND	K20
110	GND	J1.202	P8.110	GND	K20	P9.110	GND	K20
111	P2N[5]	J5.15	P8.111	TST_HDRA[79]	AF10	P9.111	TST_HDRB[79]	H24
112	P2N[4]	J5.17	P8.112	TST_HDRA[80]	AE10	P9.112	TST_HDRB[80]	J24
113	P2NX[11]	J2.2	P8.113	TST_HDRA[81]	AC10	P9.113	TST_HDRB[81]	K24
114	P2NX[10]	J2.1	P8.114	TST_HDRA[82]	AB10	P9.114	TST_HDRB[82]	M23
115	P2NX[9]	J5.19	P8.115	TST_HDRA[83]	V10	P9.115	TST_HDRB[83]	K23
116	P2NX[8]	J5.21	P8.116	TST_HDRA[84]	U10	P9.116	TST_HDRB[84]	H23
117	P2NX[3]	J5.23	P8.117	TST_HDRA[85]	R10	P9.117	TST_HDRB[85]	G23
118	GND	J1.033	P8.118	GND	K20	P9.118	GND	K20
119	P2NX[2]	J5.25	P8.119	TST_HDRA[86]	P10	P9.119	TST_HDRB[86]	F23
120	P3NX[11]	J2.29	P8.120	TST_HDRA[87]	N10	P9.120	TST_HDRB[87]	F22
121	P3NX[10]	J2.30	P8.121	TST_HDRA[88]	M10	P9.121	TST_HDRB[88]	G22
122	P3NX[7]	J2.31	P8.122	TST_HDRA[89]	J10	P9.122	TST_HDRB[89]	J22
123	P3NX[6]	J2.32	P8.123	TST_HDRA[90]	G10	P9.123	TST_HDRB[90]	M22
124	P3NX[3]	J5.27	P8.124	TST_HDRA[91]	F10	P9.124	TST_HDRB[91]	M18
125	P3NX[2]	J5.29	P8.125	TST_HDRA[92]	AD11	P9.125	TST_HDRB[92]	J18
126	P3NX[1]	J5.31	P8.126	TST_HDRA[93]	AC11	P9.126	TST_HDRB[93]	H18
127	P3NX[0]	J5.33	P8.127	TST_HDRA[94]	AB11	P9.127	TST_HDRB[94]	G18
128	P3N[85]	J5.35	P8.128	TST_HDRA[95]	AA11	P9.128	TST_HDRB[95]	F18
129	GND	J1.202	P8.129	GND	K20	P9.129	GND	K20
130	P3N[84]	J5.37	P8.130	TST_HDRA[96]	V11			
131	P3N[81]	J5.39	P8.131	TST_HDRA[97]	U11			
132	P3N[80]	J5.41	P8.132	TST_HDRA[98]	T11			
133	P3N[79]	J2.3	P8.133	TST_HDRA[99]	K11			

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
134	P3N[78]	J2.4	P8.134	TST_HDRA[100]	J11			
135	P3N[73]	J2.6	P8.135	TST_HDRA[101]	H11			
136	P3N[72]	J2.7	P8.136	TST_HDRA[102]	G11			
137	P3N[71]	J2.33	P8.137	TST_HDRA[103]	F11			
138	P3N[70]	J2.34	P8.138	TST_HDRA[104]	AG12			
139	P3N[65]	J5.43	P8.139	TST_HDRA[105]	AF12			
140	GND	J1.203	P8.140	GND	K20	P9.140	GND	K20
141	P3N[64]	J5.45	P8.141	TST_HDRA[106]	AE12			
142	P3N[61]	J5.47	P8.142	TST_HDRA[107]	AD12			
143	P3N[60]	J5.49	P8.143	TST_HDRA[108]	AC12			
144	P3N[59]	J6.1	P8.144	TST_HDRA[109]	AB12			
145	P3N[58]	J6.3	P8.145	TST_HDRA[110]	AA12			
146	P3N[53]	J6.5	P8.146	TST_HDRA[111]	V12			
147	P3N[52]	J6.7	P8.147	TST_HDRA[112]	U12			‘
148	P3N[51]	J2.17	P8.148	TST_HDRA[113]	T12			
149	P3N[50]	J2.18	P8.149	TST_HDRA[114]	R12			
150	P3N[45]	J6.9	P8.150	TST_HDRA[115]	P12			
151	GND	J1.011	P8.151	GND	K20	P9.151	GND	K20
152	P3N[44]	J6.11	P8.152	TST_HDRA[116]	N12			
153	P3N[41]	J6.13	P8.153	TST_HDRA[117]	M12			
154	P3N[40]	J6.15	P8.154	TST_HDRA[118]	K12			
155	P3N[37]	J6.17	P8.155	TST_HDRA[119]	J12			
156	P3N[36]	J6.19	P8.156	TST_HDRA[120]	H12			
157	P3N[33]	J6.21	P8.157	TST_HDRA[121]	G12			
158	P3N[32]	J6.23	P8.158	TST_HDRA[122]	F12			
159	P3N[31]	J2.44	P8.159	TST_HDRA[123]	M13			
160	P3N[30]	J2.45	P8.160	TST_HDRA[124]	K13			
161	P3N[25]	J6.25	P8.161	TST_HDRA[125]	J13			
162	GND	J1.011	P8.162	GND	K20	P9.162	GND	K20

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
163	P3N[24]	J6.27	P8.163	TST_HDRA[126]	H13			
164	P3N[21]	J6.29	P8.164	TST_HDRA[127]	G13			
165	P3N[20]	J6.31	P8.165	TST_HDRA[128]	F13			
166	P3N[17]	J6.33	P8.166	TST_HDRA[129]	M14			
167	P3N[16]	J6.35	P8.167	TST_HDRA[130]	K14			
168	P3N[13]	J6.37	P8.168	TST_HDRA[131]	J14			
169	P3N[12]	J6.39	P8.169	TST_HDRA[132]	H14			
170	P3N[11]	J2.47	P8.170	TST_HDRA[133]	F14			
171	P3N[10]	J2.48	P8.171	TST_HDRA[134]	M15			
172	P3N[5]	J6.41	P8.172	TST_HDRA[135]	K15			
173	GND	J1.204	P8.173	GND	K20	P9.173	GND	K20
174	P3N[4]	J6.43	P8.174	TST_HDRA[136]	J15			
175	P3N[1]	J6.45	P8.175	TST_HDRA[137]	H15			
176	P3N[0]	J6.47	P8.176	TST_HDRA[138]	G15			
177	P4N[25]	J7.1	P8.177	TST_HDRA[139]	M16			
178	P4N[24]	J7.3	P8.178	TST_HDRA[140]	K16			
179	P4N[23]	J7.5	P8.179	TST_HDRA[141]	J16			
180	P4N[22]	J7.7	P8.180	TST_HDRA[142]	H16			
181	P4N[17]	J7.9	P8.181	TST_HDRA[143]	G16			
182	P4N[16]	J7.11	P8.182	TST_HDRA[144]	K17			
183	P4N[15]	J7.13	P8.183	TST_HDRA[145]	H17			
184	GND	J5.16 J7.2	P8.184	GND	K2	P9.184	GND	K20
185	P4N[14]	J7.15	P8.185	TST_HDRA[146]	G17			
186	P4N[9]	J7.17	P8.186	TST_HDRA[147]	F17			
187	P4N[8]	J7.19						
188	P4N[5]	J7.21						
189	P4N[4]	J7.23						
190	P4N[1]	J7.25						
191	P4N[0]	J7.27						

Table 7-2 Daughter Board-Header-FPGA Pin Map

J1	Signal	Daughter Board Header	Test Header P8	P8 Signal	FPGA Pin U11	Test Header P9	P9 Signal	FPGA Pin U11
192	P4NX[13]	J7.29						
193	P4NX[12]	J7.31						
194	P4NX[9]	J7.33						
195	GND	J1.033	P8.195	GND	K20	J9.195	GND	K20
196	P4NX[8]	J7.35						
197	P4NX[3]	J7.37						
198	P4NX[2]	J7.39						
199	P4NX[1]	J7.41						
200	PRNX[0]	J7.43						
201	GND	J1.204	P8.201	GND	K20	P9.201	GND	K20
202	GND	J5.46 J7.48	P8.202	GND	K20	P9.202	GND	K20
203	GND	J5.4	P8.203	GND	K20	P9.203	GND	K20
204	GND	J5.2	P8.204	GND	K20	P9.204	GND	K20

Chapter 8

Reset Schemes, LEDs, Bus Bars and 200 Pin Connectors

Reset Schemes

A LTC1326 chip from Linear Technology controls reset functionality for the ET5000k10S. Figure 8-1 shows the distribution of the reset signal PWRRST-. In addition to controlling the reset, the power supplies rails +5 V, +3.3 V, +2.5 Vand +1.5 V are threshold detected by the LTC1326. Undervoltage conditions will case the assertion of the reset signal.

The LTC1326 has a push-button. Momentarily depressing this button causes a 200 ms reset pulse on the signal PWRRST-. If the push-button is depressed for 2 seconds and held, PWRRST- is asserted continuously. LED5, when lit, means that reset is asserted, so if you press and hold **S1**, you should see LED5 illuminate after a few seconds. If LED5 illuminates for any reason during normal operation, this indicates that PWRRST- is active and that something is wrong. Note that if you press **S1** and release it quickly, you probably won't see LED5 since the 200 ms reset pulse is not long enough for the eye to observe.

Depressing the push-button S1 causes the following sequence of events:

1. Reset of the CPLD and µP
2. FPGA configuration is cleared
3. If the switches on **S2** are set for Fast Passive Parallel and there is a valid SmartMedia card inserted into the socket, then the FPGA will be configured. A SmartMedia card is valid if it complies with the SSFDC specification and contains a file named `main.txt` in the root directory. If the card is invalid or there is no card present, then the FPGA will not be configured.
4. The Main Menu will appear.

The identical sequence of events occurs at power-up.

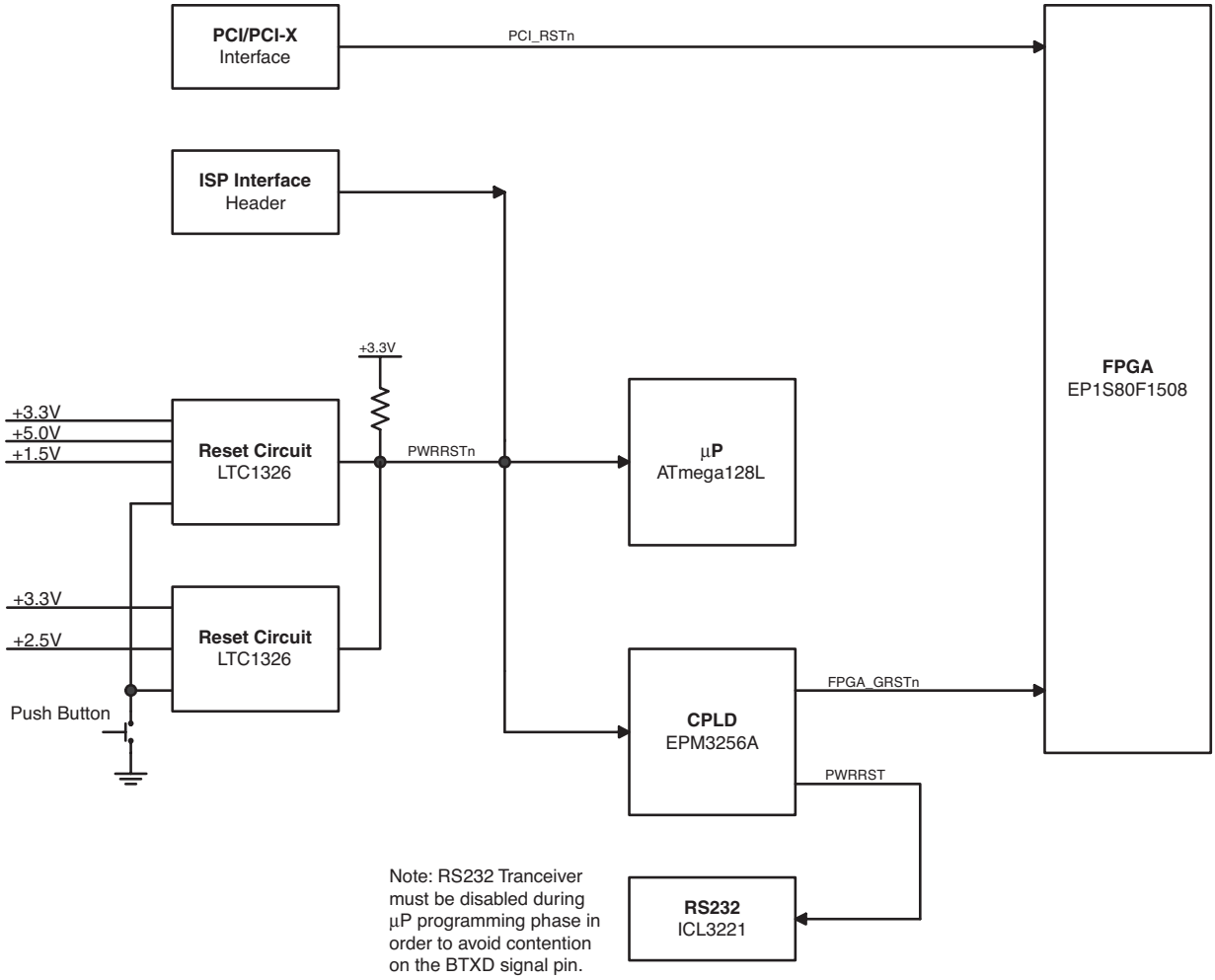


Figure 8-1 Reset Functionality

LEDs

The DN5000k10S has eight LEDs that are used to visually communicate the status of circuitry (Figure 8-2).

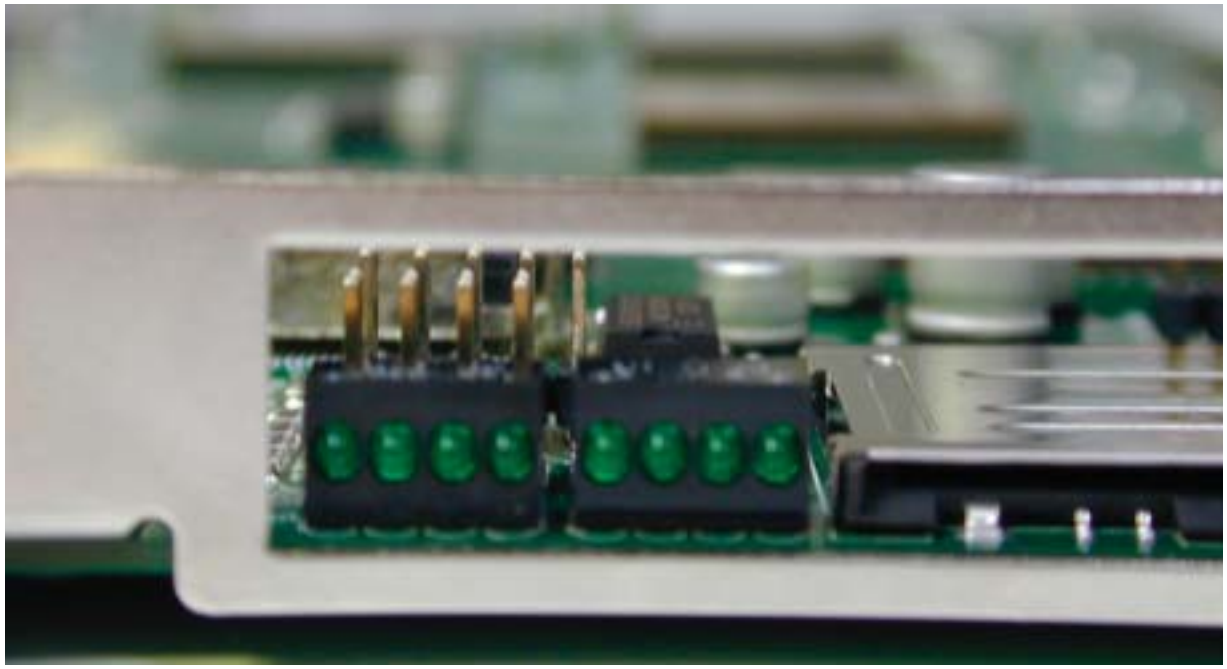


Figure 8-2 ET5000k10S LEDs

From left to right, the LEDs are labeled: CPLD_LED0, CPLD_LED1, CPLD_LED2, CPLD_LED3, UP_LED0, UP_LED1, UP_LED2, UP_LED3 (see Figure 8-3).

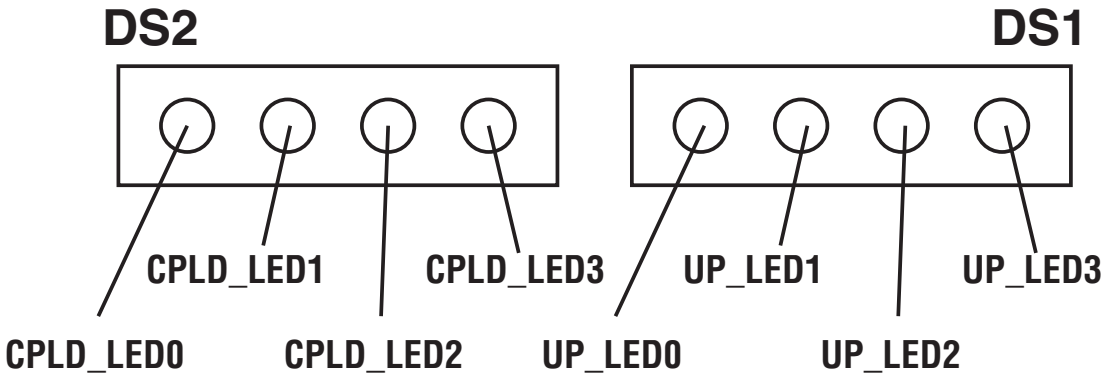


Figure 8-3 ET5000k10S LED Diagram

The LEDs have the following functions:

UP_LED3 Lights when the configuration process from the SmartMedia was successful.

UP_LED[2:0] These three LEDs have multiple meanings:

- When all 3 LEDs are blinking, then the µP has been reprogrammed and is waiting for the user to enter FPGA stuffing

information via serial port or there is not a valid SmartMedia card present and the FPGA has been configured.

- During configuration, the combination of LEDs lit tells the user which FPGA is currently being configured (UP_LED2, UP_LED1, UP_LED0):
  - off, off, on = FPGA F
  - off, on, off = FPGA A
  - off, on, on = FPGA E
  - on, off, off = FPGA B
  - on, off, on = FPGA D

CPLD_LED3 lights when the FPGA is NOT configured

CPLD_LED2 lights when reset is asserted (PWRRST-)

CPLD_LED1 lights when the PLL in Roboclock I is LOCKED

CPLD_LED0 lights when the PLL in Roboclock II is LOCKED

You are free to reprogram the CPLD and/or microprocessor to use any or all of the LEDs for your own purposes.

Bus Bars

The two bus bars, **B1** and **B2,** are installed to prevent flexing of the PWB and serve no other purpose. They are connected quite solidly into the ground plane of the DN5000k10S at every hole, and you can use the metal bars to ground-test equipment such as oscilloscopes and pattern generators. Be careful not to short any power rails or signals to these metal bars—they can carry a lot of current. The PCI bracket, **BRK1**, is also connected to the ground plane at each of the screw mounts.

The 200 Pin Connectors: P8 and P9

The DN5000k10S contains two 200-pin connectors, **P8** and **P9**. Daughter cards of any sort may be plugged into these connectors. The relative pin location of the powers, grounds, and signals is identical for each of the connectors. A hole that can be used to attach a standoff is located at the same relative position from each connector (seeFigure 8-4). This hole is grounded on the DN5000k10S, so connect this mounting hole to digital ground on your daughter card.

The mechanical position of the 200-pin connectors on the DN5000k10S is shown in Figure 8-4. The 200-pin connector used on the DN5000k10S is a Berg Electronics 91294-003 in the Micropax™ family. This link will take you to the Berg website: **http://www.berg.com/**. This Berg connector was chosen because of its high pin density, performance, and availability. The part number for the mating connector is 91403-003. We stock the mating connector at our offices in La Jolla, CA, so if you are designing a daughter card and are having trouble getting this part, call us. We would be happy to send you a few at our cost. Appendix A contains a mechanical datasheet for both the Berg 91403-003 and 91294-003 connectors.

This style of connector has four mounting holes—two screw holes at each end and two alignment holes between pins 50–51 and after pin 100 (see Figure 8-4). These mounting holes are part of the metal shell of the connector and make an important connection to the mating connector. All

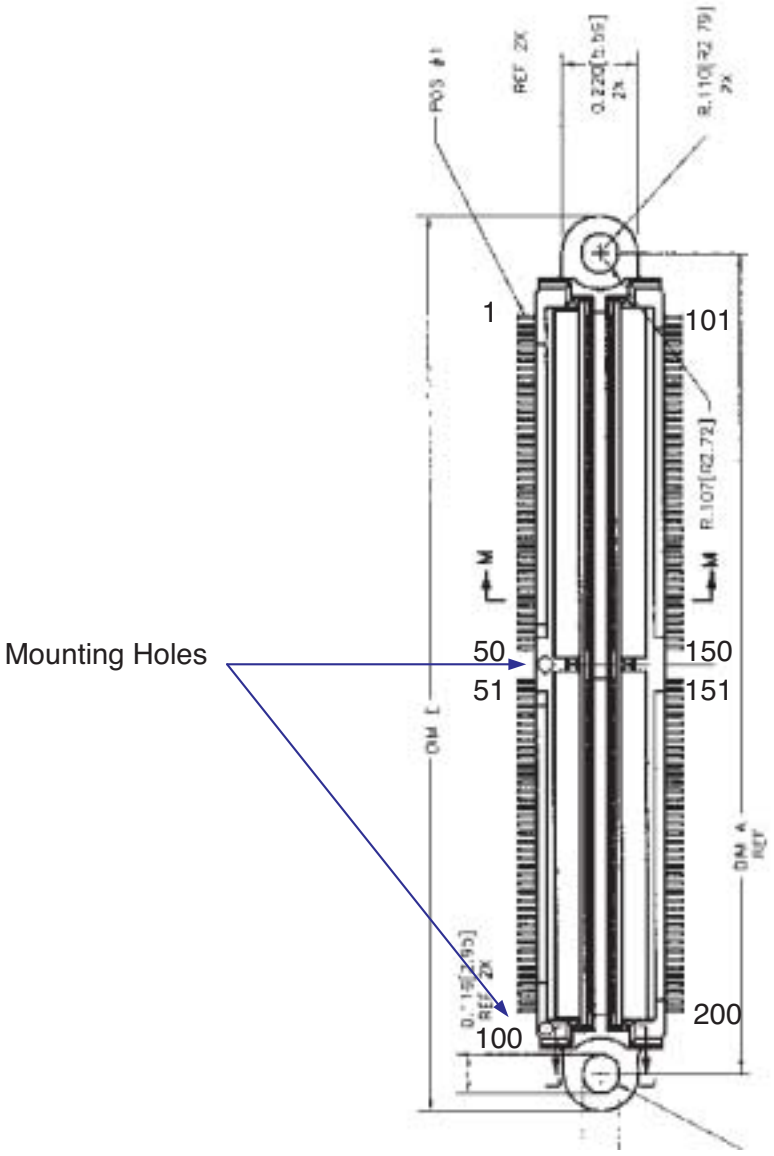


Figure 8-4 91294-003 Pin Numbering

four of these mounting holes are connected to digital ground on the DN5000k10S—therefore, the shell of the connector is grounded.

We used the pin numbering shown in Figure 8-4 for the 200-pin, 91294-003 connectors.

The Signals

Each of the two 200-pin connectors has the following:

- **P8** has 147 signals connected to the FPGA.
- **P9** has 96 signals connected to the FPGA.
- 5clocks
- The following power rails:
  - +12V(1 pin)
  - -12V(1 pin)
  - +5V(2 pins)

- +3.3V(2 pins)
- +1.5V(2 pins)
- GND(23 pins + case)

Regarding the amount of current that the power pins can carry, the following text is lifted directly from the specification for the Micropax™ family of connectors:

> *6.1 Current Rating. Current rating shall be evaluated in still air at 25°C ambient temperature. Under the following conditions, the temperature rise shall be no greater than 30°C:*
> *All contacts powered at 0.5 amp*
> *One contact powered at 3.0 amps*

Most of the signals are TTL (or some low current variation such as LVDS), so you can reasonably expect to get up to 3 amps per power pin through this connector. Remember that the +3.3V and +1.5V power supplies are limited to 5 amps total—the memories, the FPGA and the clock circuitry on the DN5000k10S consume +3.3V. The FPGA only consumes +1.5V.

If you use the DN5000k10S stand-alone (meaning that it is *not* plugged into a PCI slot), the auxiliary power connector has +5V and +12V, but does not have –12V. So unless you provide –12V to the DN5000k10S via another connection, –12V will not be available for use by a daughter card.

The 200-pin connectors are shown in Figure 8-5.

NOTE: –12V is not required by the DN5000k10S. The DN5000k10S will operate normally without a –12V power supply.

Figure 8-5 200-Pin Connectors — Signal Connections

Chapter 9

Utilities

PCI Debug—General Pontificating

Debugging of PCI-based hardware can be troublesome, so it is best to do so with a tiered approach. The following sequence of events needs to occur for a PCI-based peripheral to start working:

1. The hardware must boot itself at power-up — in the case of the ET5000k10S:
   a.The µP must boot.
   b.Recognize the SmartMedia card.
   c.Configure the FPGA. (Hopefully, all this occurs before RST# on the PCI bus is deasserted.)
2. The PCI BIOS executes the PNP routines and configures the BARs on all PCI peripherals.
3. The operating system driver initializes the card.
4. The application initiates communication with the driver and the application executes.

The steps are dependant. Each of the steps must start and execute flawlessly before the next step occurs. When you get a PCI card for the first time, it is necessary to debug each step before attempting to go to the next. We provide utilities to help with each step.

Steps 1 and 2 are best done without an operating system in place. Windows NT-based systems take minutes to reboot after a crash (the-BLUE-screen-of-death) and an NT driver won't work unless the hardware is debugged. Since crashing is a regular occurrence in a PCI hardware debug environment, we find it easiest to do our debug and manufacturing test in the old DOS environment. Virtually all PCI peripherals get configured with addresses beyond the IM boundary. On a PC, C programs cannot access memory locations beyond IM unless special programs called DOS extenders are used. Several freeware DOS extenders are available. We use a free DOS-extender called DJGPP. More information can be found at **http://www.delorie.com/DJGPP**.

PC-Based—AETEST.EXE

A utility program called AETEST is provided with the ET5000k10S. AETEST can be run under DOS, Windows 98/ME, Windows NT/2000, or LINUX. When used under DOS, you must boot your PC with a DOS disk. We ship one with the ET5000k10S in case you don't know how to make one on your own. All features work in the native mode of AETEST, which is DOS.

All source code for AETEST is provided, so you are welcome to customize the program to your own applications.

AETEST is not a stable program. We add and subtract features when we need to for debug and verification purposes, so don't be concerned if the screens that you see aren't exactly replicated here.

In a nutshell, AETEST lets you do the following:

- Determine if PCI recognizes the ET5000k10S
- Read/write/loop any memory location
- Read/write/loop configuration space
- Display all configured PCI devices
- Display memory setting from any locations
- Fill memory with various patterns
- Run various tests on the ET5000k10S
  - SSRAM Test
  - Multiplier Test
  - SDRAM Test
  - Interconnect Test
  - Daughter Card Test

AETEST Utility Installation Instructions

Installation Instructions for DOS

1. The files `aetestdj.exe` and `cwsdpmi.exe` (the DOS extender) need to be in the same directory.
2. Run `aetestdj.exe`.

Installation Instructions for Windows NT

1. Install the device driver: `install.exe` and `qldriver.sys` must be in the same directory.
2. Type "`install`"
3. After the driver is installed, start the driver by selecting **Control Panel–>Devices–>**find **"QLDriver"** –>click **"Start"**
4. Run `aetestnt.exe`.

Installation Instructions for Windows 2000

1. Install the device driver: `qldriver2000.inf` and the driver file (`qldriver.sys`) should be in the same directory.
2. Open **Control Panel**, click on "**Add/Remove Hardware**" and then go to "**Next–>**."
3. Choose **Add/Troubleshoot a device** (the default option) and click on "**Next–>**."
4. Wait until it finishes new hardware device searching; choose "**Add a new device**," and click on "**Next–>**."
5. Choose "**No, I want to select the hardware from a list**," and press "**Next–>**."
6. Choose "**Other Devices**" from **Hardware Types** list and press "Next–>"
7. Click on "**Have Disk…**"

8. In "**Copy Manufacturer's Files From:**" window, find the directory where `qldriver.sys` is located, then press "**OK**."
9. You should see "`dn2000k10 driver`" under **Models**; click on "**Next–>**."
10. Press "**Next–>**" and then "**Finish**."
11. Run `aetestnt.exe`.

Installation Instructions for LINUX

This has been tested on Red Hat Linux 7.2 (kernel version 2.4.x).

Note that all the text files, including the scripts, are DOS text format (with an extra carriage return character after every new line), so you need to convert them.

1. You must be root to start the driver and the program. "`dndev_load`" and "`dndev_unload`" are scripts that load and unload the driver; "`dndev.o`" is the driver file.
2. Load the driver; type "`sh dndev_load`"
3. Unload the driver; type "`sh dndev_unload`"
4. After driver is loaded, run the utility `aetest_linux`.
5. Note: You might need to run chmod on `aetest_linux` to make it executable: type "`chmod u+x aetest_linux`."

Installation Instructions for Solaris

The utility and driver are tested on Solaris 7.0/Sparc, with the 32-bit kernel.

Note that all the text files, including the scripts, are DOS text format (with an extra carriage return character after every new line), so you need to convert them.

1. To install the driver, go to the driver directory, make sure the driver file "`dndev`" is in the sparc sub-directory, and run "`sh dndev_uninstall.sh`"
2. To uninstall the driver, run "`sh dndev_uninstall.sh`"
3. To run the test utility, run "`aetest_solaris`" as root after the driver is loaded.

The driver is compiled with the gcc compiler.

`aetest_solaris` is compiled with "gmake." You can download it from the GNU website. The "make" from the Solaris installation does not work with our makefile format.

You may need to make `aetest_solaris` executable; run "`chmod u+x aetest_solaris`."

Installation Instructions for Windows 98/ME

There are two ways to run AETEST: You can run the DOS version "`aetestdj.exe`" directly, or you can run AETEST with a device driver.

To run AETEST with a device driver follow the steps below.

1. Choose a default PCI driver for the device. When Windows first starts with the device plugged in, it should ask for a device driver. Select "**Specify the location of the driver.**"
2. Select "**Display a list of the drivers in a specific location…**"
3. Select "**Other devices.**"
4. Under "**Manufacturers**" tab, select "**unknown device**."
5. Under "Models" select "**unsupported device**."
6. The driver file (`pcifg.vxd`) and `aetest98.exe` must be in the same directory. Run `aetest98.exe`.

NOTE: To re-compile the driver file `pcicfg.vxd`, you need the VtoolsD compiler from **www.numega.com**.

AETEST Options: Description and Definitions

Startup

When AETEST is first started, it tries to find a device that it recognizes. We have arbitrarily defined the ET5000k10S with a `DEVICE_ID` of `0x1505` and a `VENDOR_ID` of `0x17DF`. You should see the following screen if AETEST recognizes a ET5000k10S (Figure 9-1):

```
DEVICE_ID==1501
searching for "DN5000K10 Stratix Asic Emulator (PCI 64-bit test)" VENDOR_ID==17d
f, DEVICE_ID==1506
searching for "DN5000104 Stratix FPGA board" VENDOR_ID==17df, DEVICE_ID==1505

found device ---- v17df, d1505 bus=2 d&f=30, name="DN5000104 Stratix FPGA board"

Configuration space:
00: 150517df       04: 0000001f
08: ff000047       0c: 00000000
10: fd000000       14: fe400000
18: fe000000       1c: 00000000
20: 00000000       24: 00000000
28: 00000000       2c: 90ab5678
30: 00000000       34: 00000000
38: 00000000       3c: 00000000
BAR0 xfd000000, size=0x01000000
BAR1 xfe400000, size=0x00400000
BAR2 xfe000000, size=0x00400000
BAR3 x00000000, size=0x00000000
BAR4 x00000000, size=0x00000000
BAR5 x00000000, size=0x00000000
Compiled on: Jun 13 2003 at 13:38:22
press any key
```

Figure 9-1 ET5000k10SAETEST Startup Screen, ET5000k10S Recognized

Most of this initial display is debug information. The program is looking for a Vendor and Device ID that it recognizes, and finds `vendor=0x17DF` and `device=0x1505`, which is a ET5000k10S. The lines after `Configuration space:` show what is in the configuration space and how the BARs are configured.

If AETEST does **not** see a PCI peripheral it recognizes, you will see the following (Figure 9-2):

```
searching for "Quad Sharc" VENDOR_ID==5045, DEVICE_ID==1
searching for "DN2000K10 Asic Emulator" VENDOR_ID==abcd, DEVICE_ID==1234
searching for "DN2000K10 Asic Emulator (2000E)" VENDOR_ID==abcd, DEVICE_ID==1235
searching for "DN2000K10 Asic Emulator (1000E)" VENDOR_ID==abcd, DEVICE_ID==1236
searching for "DN2000K10 Asic Emulator (1600E)" VENDOR_ID==abcd, DEVICE_ID==1237
searching for "DN3000K10S Asic Emulator (6000)" VENDOR_ID==abcd, DEVICE_ID==1240
searching for "ql5064 interface test" VENDOR_ID==1234, DEVICE_ID==5678
searching for "ql5064 64MB dram+LFSR" VENDOR_ID==1234, DEVICE_ID==5679
searching for "ql5064 PowerPC bridge" VENDOR_ID==11e3, DEVICE_ID==6
searching for "ql5064 PowerPC bridge (old VID/DID)" VENDOR_ID==1010, DEVICE_ID==5064
searching for "ql5064 AntiFuse test #1" VENDOR_ID==71f3, DEVICE_ID==2454
searching for "ql5064 AntiFuse test #2" VENDOR_ID==507, DEVICE_ID==2367
searching for "ql5064 AntiFuse test #3" VENDOR_ID==bc92, DEVICE_ID==2e6c
searching for "ql5064 AntiFuse test #4" VENDOR_ID==e125, DEVICE_ID==c38c
searching for "ql5064 AntiFuse test #5" VENDOR_ID==e62c, DEVICE_ID==ca76
searching for "ql5064 AntiFuse test #6" VENDOR_ID==448b, DEVICE_ID==e6a
searching for "ql5064 Emulated with 8051" VENDOR_ID==1243, DEVICE_ID==4321
searching for "Greg's PCI Device" VENDOR_ID==5143, DEVICE_ID==2
searching for "Cohu's PCI Device (sensor board)" VENDOR_ID==dead, DEVICE_ID==beef
searching for "LYNX 9610" VENDOR_ID==10b5, DEVICE_ID==9610

Didn't find known device in the following list:
   vendor_id=5045, device_id=1
   vendor_id=abcd, device_id=1234
   vendor_id=abcd, device_id=1235
   vendor_id=abcd, device_id=1236
   vendor_id=abcd, device_id=1237
   vendor_id=abcd, device_id=1240
   vendor_id=1234, device_id=5678
   vendor_id=1234, device_id=5679
   vendor_id=11e3, device_id=6
   vendor_id=1010, device_id=5064
   vendor_id=71f3, device_id=2454
   vendor_id=507, device_id=2367
   vendor_id=bc92, device_id=2e6c
   vendor_id=e125, device_id=c38c
   vendor_id=e62c, device_id=ca76
   vendor_id=448b, device_id=e6a
   vendor_id=1243, device_id=4321
   vendor_id=5143, device_id=2
   vendor_id=dead, device_id=beef
   vendor_id=10b5, device_id=9610

Hit a key to continue
```

Figure 9-2 AETEST Startup Screen, No PCI Peripheral Recognized

AETEST will still run, but many product-specific options will not be available.

AETEST Main Screen

The AETEST Main Screen is shown in Figure 9-3.

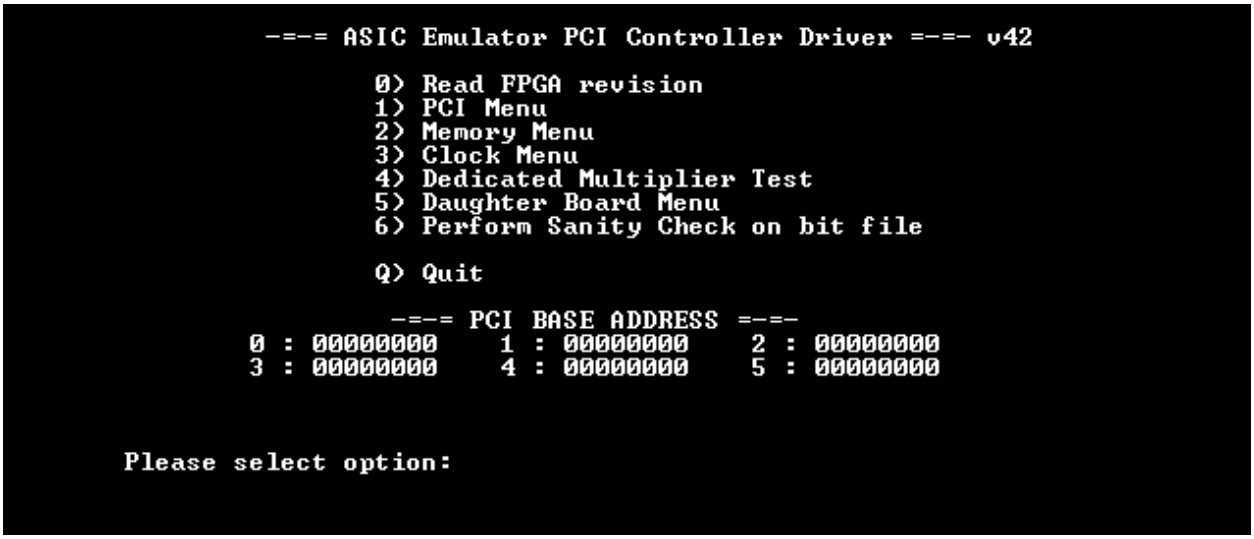


Figure 9-3 AETEST Main Screen

Options

Read FPGA Revision. Display the revision ID of the FPGA. We will update the revision ID of the FPGA every time we change the reference design.

PCI Menu. Display the PCI utilities menu.

Memory Menu. Display the Memory Menu.

Flash Menu. Display the Flash Utilities Menu (ET2000k10 series only!).

Clock Menu. Display the Clock Utilities Menu.

Dedicated Multiplier Test. Execute the multiplier test.

Q. Quit and return to the DOS prompt

The selections are sometimes case sensitive, so be aware of the status of the CAPS LOCK on your keyboard. The base addresses for each of the configured BARs is displayed on all screens. You will need these addresses if you want to manually read and write to address locations within the PCI reference design. In this example (Figure 9-3, above), BAR0 is configured to `0xFD800000` and BAR1 is configured to `0xE0000000`. BAR[5:2] are not configured so they show up as `0x0`.

PCI Menu

The AETEST PCI menu is shown in Figure 9-4.

```
          -=-= ASIC Emulator PCI Controller Driver =-=- v42
      PCI Device/Function Num: 0x01, 0x00

S) Set PCI Device Number
F) Set PCI Function Number
D) Display all Configured PCI Devices
1) Display Vendor and Device ID for PCI device-function: 1-0
2) Loop on PCI device-fun: 1-0 and Display Vendor and Device ID
3) Loop on PCI device-fun: 1-0 and Don't Display Vendor and Device ID
4) Loop on all PCI device numbers and Display Device/Vendor ID's
5) Display all PCI information for PCI device-function: 1-0
6) Write config dword
7) Read config dword
8) Display Config Registers 0x0 - 0xFC for device-function: 1-0

C) Configure BAR's from File
V) Save BAR Configuration to File
M) Main Menu
Q) Quit

                -=-= PCI BASE ADDRESS =-=-
        0 : 00000000    1 : 00000000    2 : 00000000
        3 : 00000000    4 : 00000000    5 : 00000000

Please select option:
```

Figure 9-4 AETEST PCI Menu

Set PCI Device Number. Sets a PCI device number of your choice as the "active" device (hex input). This option lists the available Device Numbers to help you match up your Device ID and Vendor ID with the device number.

Set PCI Function Number. Sets a PCI function number of your choice as the "active" function of a multi-function device (hex input). This option lists the Device ID and Vendor ID of each function within the "active" device number to help you to choose the desired function.

Display all Configured PCI Devices. Displays the PCI Device Numbers and corresponding Device ID and Vendor ID of all devices seen on the bus. This does not display device numbers with a Device ID and Vendor ID of all ones (0xFFFF).

Display Vendor and Device ID for PCI device-function. Displays the Vendor ID and Device ID of the active device and function number. In the example above, this would display the Vendor ID and Device ID of the PCI device at device number 0x7F, function number 0x00.

Loop on PCI device-fun: 7f-0 and Display Vendor and Device ID. Reads and displays the Vendor ID and Device ID of the "active" device number and function number. Repeats this action until the user hits a key to stop it.

Loop on PCI device-fun: 7f-0 and Don't Display Vendor and Device ID. Same as previous menu option, except doesn't display results. This menu option is useful when using an oscilloscope to debug configuration reads.

Loop on all PCI device numbers and Display Device/Vendor ID's. Loops on each device number, reading the Vendor ID and Device ID for each. It moves onto the next device number when you press any key. That is, it continually reads the Vendor ID and Device ID from device number 0 until you hit a key, at which point it continually reads the Vendor ID and Device ID from device number 1. It moves all the way through device number 0 to device number 0x7F (in case there are any bridges on your PCI bus).

Display all PCI information for PCI device-function: 7f-0.

Reads and displays all of the configuration space for the "active" device and function number. Use options "S" and "F" to change between the "active" device number and function number, and then use this option to view the entire configuration space.

Write config(uration) DWORD. Allows write to configuration space. The following text will appear to remind you what is in configuration space for a PCI device:

```
PCI_CS_VENDOR_ID0x00
PCI_CS_DEVICE_ID0x02
PCI_CS_COMMAND0x04
PCI_CS_STATUS0x06
PCI_CS_REVISION_ID0x08
PCI_CS_CLASS_CODE0x09
PCI_CS_CACHE_LINE_SIZE0x0c
PCI_CS_MASTER_LATENCY0x0d
PCI_CS_HEADER_TYPE0x0e
PCI_CS_BIST0x0f
PCI_CS_BASE_ADDRESS_00x10
PCI_CS_BASE_ADDRESS_10x14
PCI_CS_BASE_ADDRESS_20x18
PCI_CS_BASE_ADDRESS_30x1c
PCI_CS_BASE_ADDRESS_40x20
PCI_CS_BASE_ADDRESS_50x24
PCI_CS_EXPANSION_ROM0x30
PCI_CS_INTERRUPT_LINE0x3c
PCI_CS_INTERRUPT_PIN0x3d
PCI_CS_MIN_GNT0x3e
PCI_CS_MAX_LAT0x3f

Input config offset (hex 0x00-0xff):
word to write (in hex):

Loop indefinitely? (y or n)?
```

If looping was selected, any keypress will stop the loop.

Read config(uration) DWORD. Allows read from configuration space. Has options for single read, loop read with display, and loop read without display.

Configure BARs from File. Reloads the PCI configuration of the "active" device from a file. It writes 0x001F to the command register, and writes the 6 bars with the values from the file. This is useful for hot-swapping devices (power switch still required on extender), or reinitializing a device when its configuration has been altered.

WARNING: Because the PCI BIOS is not assigning the BARs for this device, you may induce a memory conflict by using this option. This option is for advanced users only!

Save Bar Configuration to File. Writes PCI Device ID, Vendor ID and the BARs into a file (from the "active" device). This option is for advanced users only!

Memory Menu

The memory menu (Figure 9-5) allows you to perform a variety of tests of PCI memory along with some ET5000k10S specific tasks.

```
          -=-= ASIC Emulator PCI Controller Driver =-=- v42

        1) Write Dword (Same Address)  2) Read Dword (Same Address)
        3) Write/Read Dword (Same Address)
        4) BAR Memory Fill
        5) BAR Memory Write
        8) BAR Memory Display
        c) memory test on SSRAM 1
        d) memory test on SSRAM 2
        e) memory test on SSRAM 3
        f) memory test on SDRAM
        g) full memory test (including blockram)
        n) memory test on FPGA block memory
        p) bar memory range test
        k) bar memory address/data bitwise test
        u) SRAM memory test
        M) Main Menu                    Q) Quit

                  -=-= PCI BASE ADDRESS =-=-
        0 : 00000000    1 : 00000000    2 : 00000000
        3 : 00000000    4 : 00000000    5 : 00000000

Please select option:
```

Figure 9-5 AETEST Memory Menu

Write to Memory Test. Write a selected number of long words to a specific PCI memory location (Figure 9-6).

```
                        --------

        Bar Number (0-5) -- 1
        Address (hex) -- fb000000
Numbers of long words to write (in decimal) ?  2
long word to write (in hex) :aaaaaaaa
long word to write (in hex) :55555555

Loop indefinitely? (y or n)?



Hit a key to continue....
```

Figure 9-6 AETEST Write to Memory Test

You will be prompted for the memory location (in hex). The physical address is needed. All 4 gigabytes of PCI memory can be accessed. A minimum of 1 to a maximum of 1024 long words can be written, in sequential order, to the same address. A looping option is available if you want to use an oscilloscope. If you are in a scope loop, any keypress will terminate the loop and return you to the main menu.

Read Memory Test. Read a single long word from a specific PCI memory location (Figure 9-7).

```
            --------
        Bar Number (0-5) -- 0
        Address (hex) -- fb000000

        1.Display result
        2.Display result and loop indefinitely
        3.Don't display result and loop indefinitely
Please select:
```

Figure 9-7 AETEST Read Memory Test

You will be prompted for the memory location (in hex). The physical address is needed. All 4 gigabytes of PCI memory can be read. Three options are available:

1. Read once and display.
2. Read indefinitely and display.
3. Read indefinitely and don't display.

Write/Read Test. Write a long word to a specific PCI memory location and immediately read what was written. Repeat for a selected number of long words (Figure 9-8).

```
        Bar Number (0-5) -- 0
        Address (hex) -- fb000000
Numbers of long words to write (in decimal) ?  2
long word to write (in hex) :000
long word to write (in hex) :aaa

        1.Display result
        2.Display result and loop indefinitely
        3.Don't display result and loop indefinitely
Please select: _
```

Figure 9-8 AETEST Write/Read Test

You will be prompted for the memory location (in hex). The physical address is needed. All 4 gigabytes of PCI memory can be read. The program will prompt for the number of long words you with to write (1 to 1024). Three options are available:

1. Read once and display.
2. Read indefinitely and display.
3. Read indefinitely and don't display.

Option 3 is a very useful scope loop.

Memory Fill. Fill memory with a selected pattern (Figure 9-9).

```
Input bar number (0-5): 0

Input starting address (hex and 32 bit aligned): fb000000

Input number of bytes (hex and divisible by 4): 1000

1 -- Fill with 0
2 -- address=data
3 -- 0x55555555, 0xaaaaaaaa
4 -- 0xffffffff
5 -- data=~address_
```

Figure 9-9 AETEST Memory Fill

You will be prompted for the memory location (in hex). The physical address is needed. All 4 gigabytes of PCI memory can be written. The program will prompt for the number of bytes (in hex) you wish to fill (`4` to `0xfffffffc`). The following fill options are available:

1. **fill with 0** — fill all the locations with `0x00000000` (clear the memory)
2. **address=data** — fill each long word with its address
3. alternating `0x55555555`, `0xAAAAAAAA`

4. `0xffffffff` — set all of memory
5. **data=~address** — fill each long word with the address (each bit inverted).

Memory Display. Display 160 long words of memory. You are prompted for the starting address (in hex):

```
Input starting address (hex and 32 bit aligned):
```

The following screen is displayed (Figure 9-10):

```
        0       4       8       c       10      14      18      1c
000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000020 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000040 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000060 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000080 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000a0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000c0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000e0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000100 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000120 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000140 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000160 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000180 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0001a0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0001c0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0001e0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000200 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000220 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000240 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000260 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
 (f)orward  (b)ack  (j)ump  goto(0)  (q)uit
```

Figure 9-10 AETEST Memory Display

(f) forward — pages the screen forward in memory.
(b) back — pages the screen backwards in memory.
(j) jump — jump to a specific location (in hex).
(0) goto — jump back to the original address location specified at the beginning.
(d) delay and display loop — display, wait for a second, and display again. Loop until a key is struck.

You will be prompted for the memory location (in hex). The physical address is needed. All 4 gigabytes of PCI memory can be read. Three options are available:

1. Read once and display.
2. Read indefinitely and display.
3. Read indefinitely and don't display.

Write/Read Memory Byte. Write and read a single DWORD from a specific PCI memory location. After entering a memory address (hex, 32 bits), you specify how many DWORDS you want written and read back, and

the data. Then, you choose from the 3 options as above. The menu option does not perform any data checking. (Figure 9-11)

```
Numbers of long words to write (in decimal) ?  2

byte to write (in hex) :88888888
byte to write (in hex) :99999999

        1.Display result
        2.Display result and loop indefinitely
        3.Don't display result and loop indefinitely
Please select:
```

Figure 9-11 AETEST Write/Read Memory Byte

Memory test on SSRAM1. Tests one of the SSRAM chips on the ET5000k10S.

Memory test on SSRAM2. Tests one of the SSRAM chips on the ET5000k10S.

Memory test on SSRAM3. Tests one of the SSRAM chips on the ET5000k10S.

Memory test on SDRAM. Tests the SDRAM chip on the ET5000k10S.

Full Memory Test (Including BlockRAM). Tests all of the memories. This includes the SSRAM chips, the SDRAM, and the BlockRAM internal to the FPGA.

Memory test on FPGA block memory. Tests the BlockRAM inside the FPGA. On the ET2000k10, the BlockRAM is only in FPGA F.

BAR memory range test. Generic memory test that prompts the user for BAR number, starting address offset, DWORD count, and number of iterations. The user is also prompted if the program should stop if error occurs, or if the program should display any errors that occur. This allows for maximum flexibility when debugging a design with an oscilloscope, or debugging any memories or memory locations on your PCI bus. The memory test is very complete, performing a write then a read to every location, a read from every location, and then a read/write/read test to every location. All other memory test options listed in the memory menu are based on this generic memory test function.

Appendix A

Berg Connector Datasheets

Figure A-1 and Figure A-2 contain the schematics for the Berg 91403-003 Connector.

Figure A-3 through Figure A-5 contain the schematics for the Berg 91294-003 connector.

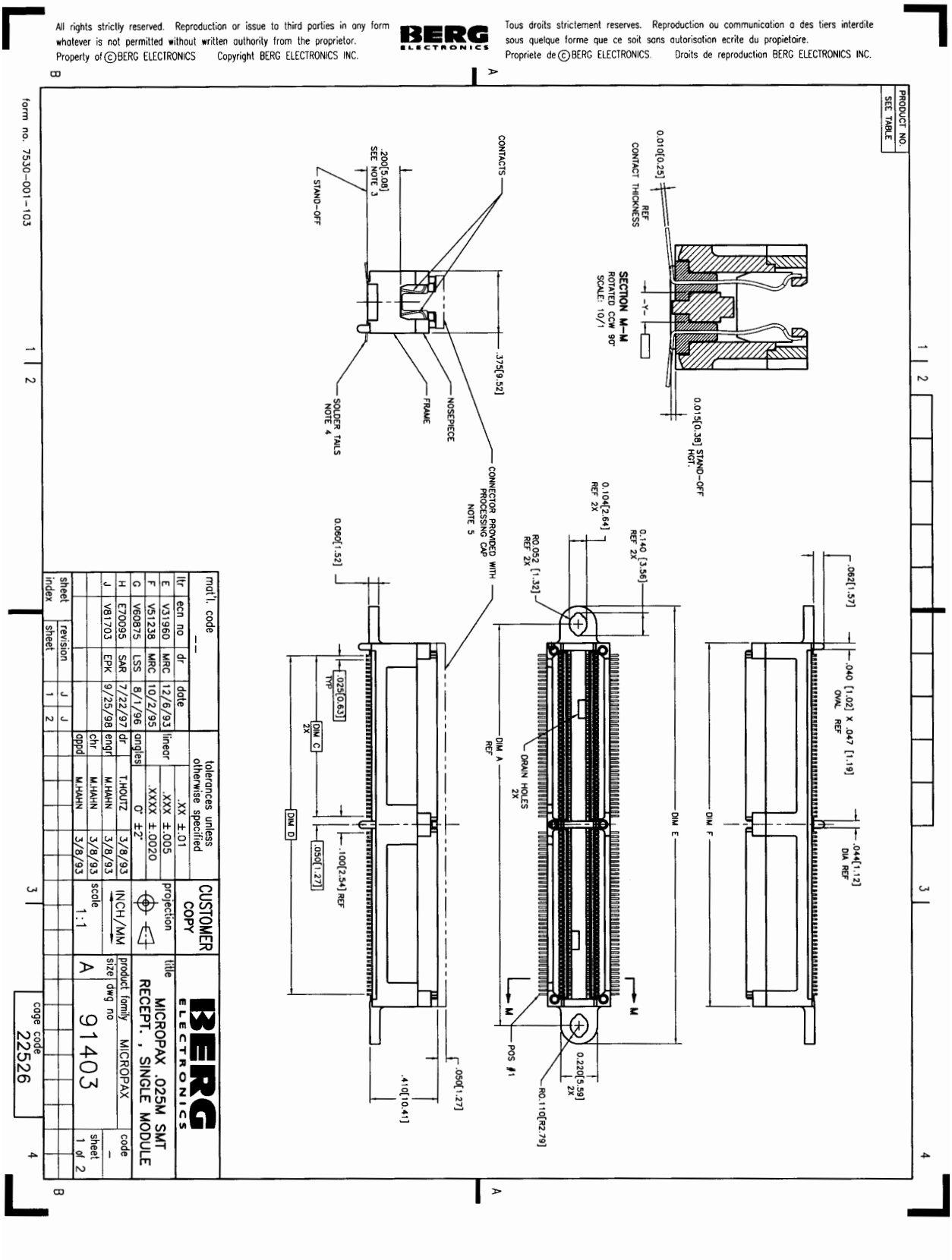
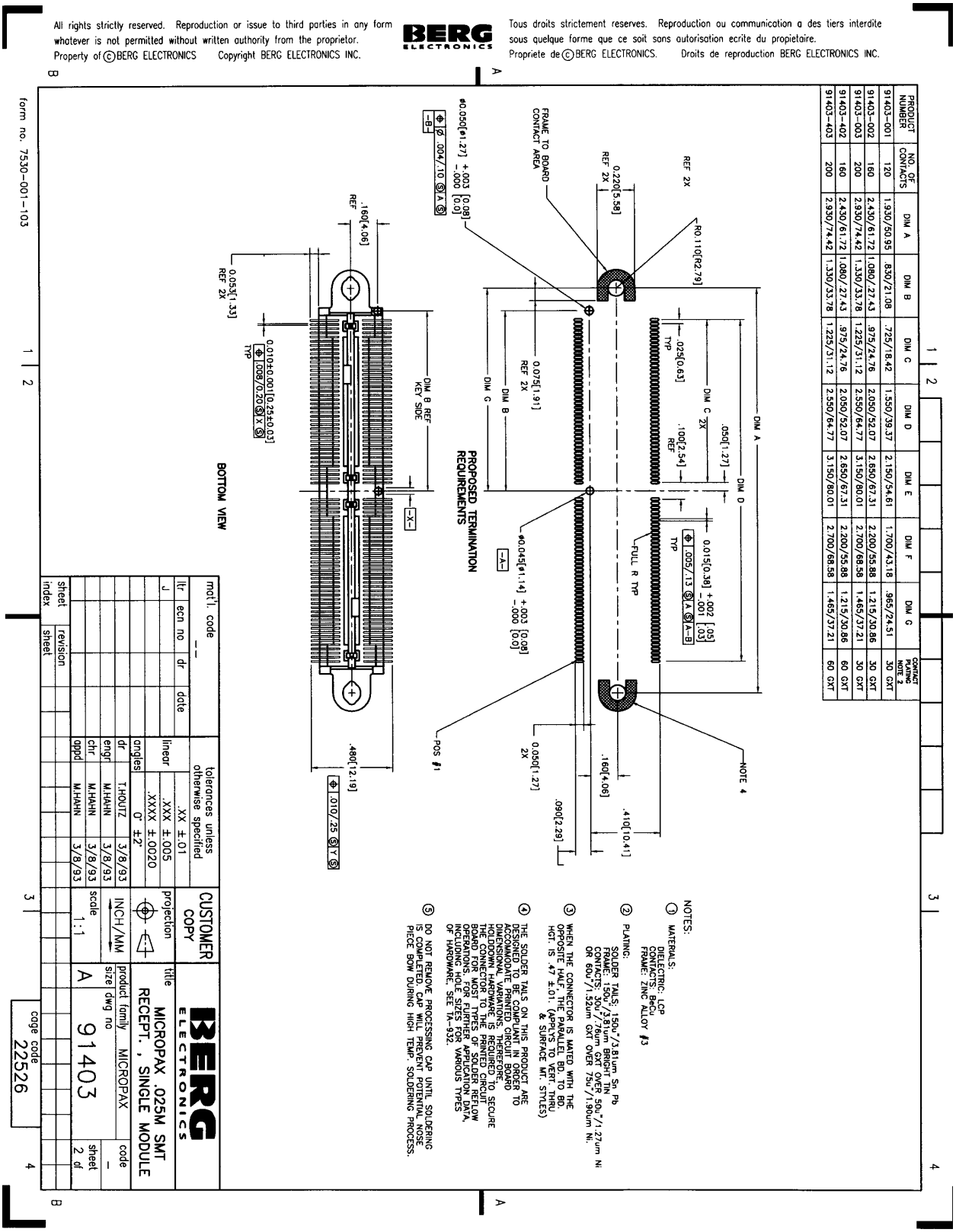


Figure A-1 Berg 91403-003 Datasheet Page 1 of 2



PRODUCT NUMBER	NO. OF CONTACTS	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	CONTACT PLATING NOTE 2
91403-001	120	1.930/50.95	.830/21.08	.725/18.42	1.550/39.37	2.150/54.61	1.700/43.18	.965/24.51	30 GXT
91403-002	160	2.430/61.72	1.080/27.43	.975/24.76	2.050/52.07	2.850/67.31	2.200/55.88	1.215/30.86	30 GXT
91403-003	200	2.930/74.42	1.330/33.78	1.225/31.12	2.550/64.77	3.150/80.01	2.700/68.58	1.465/37.21	30 GXT
91403-402	160	2.430/61.72	1.080/27.43	.975/24.76	2.050/52.07	2.850/67.31	2.200/55.88	1.215/30.86	60 GXT
91403-403	200	2.930/74.42	1.330/33.78	1.225/31.12	2.550/64.77	3.150/80.01	2.700/68.58	1.465/37.21	60 GXT

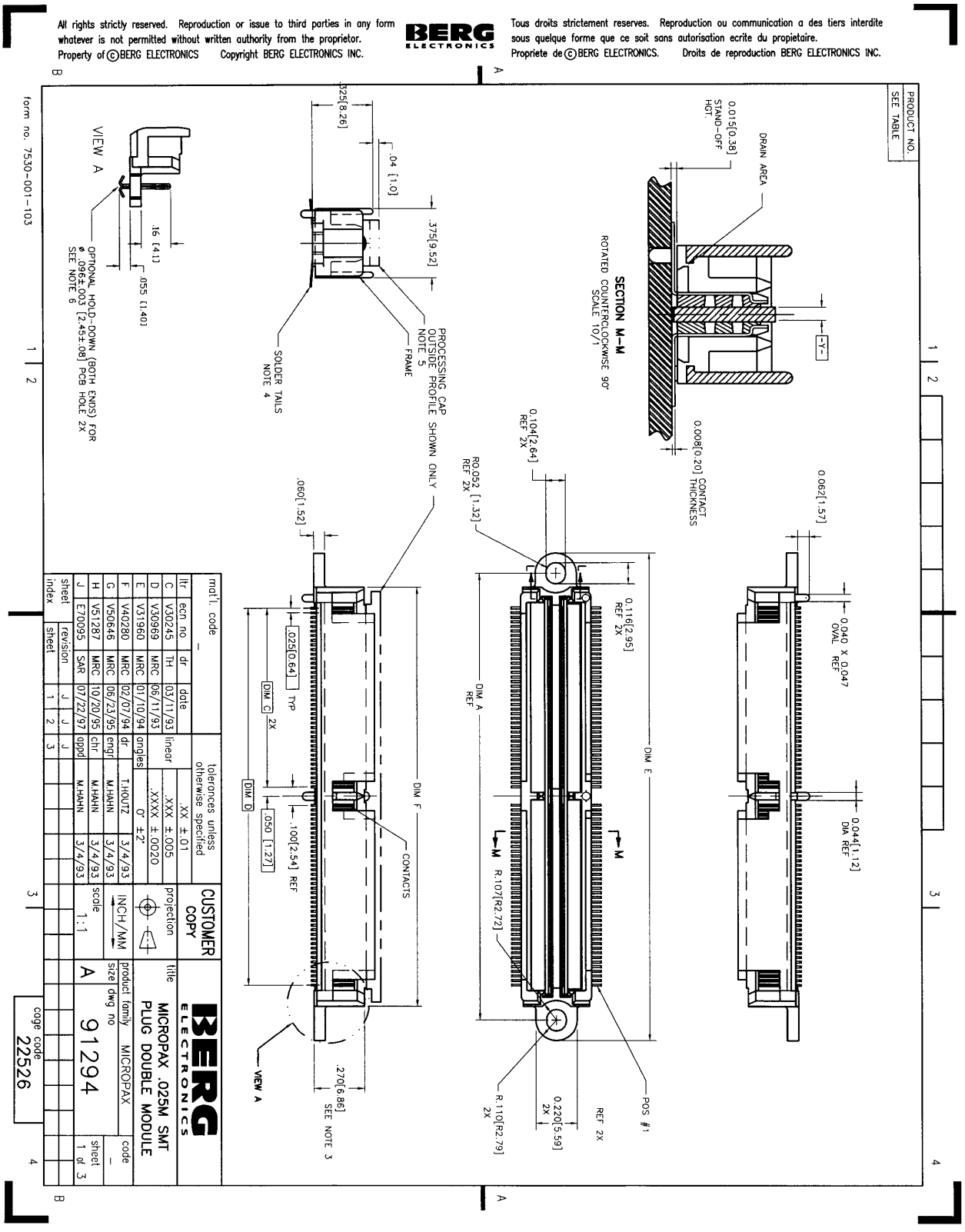


Figure A-3 Berg 91294-003 Datasheet Page 1 of 3

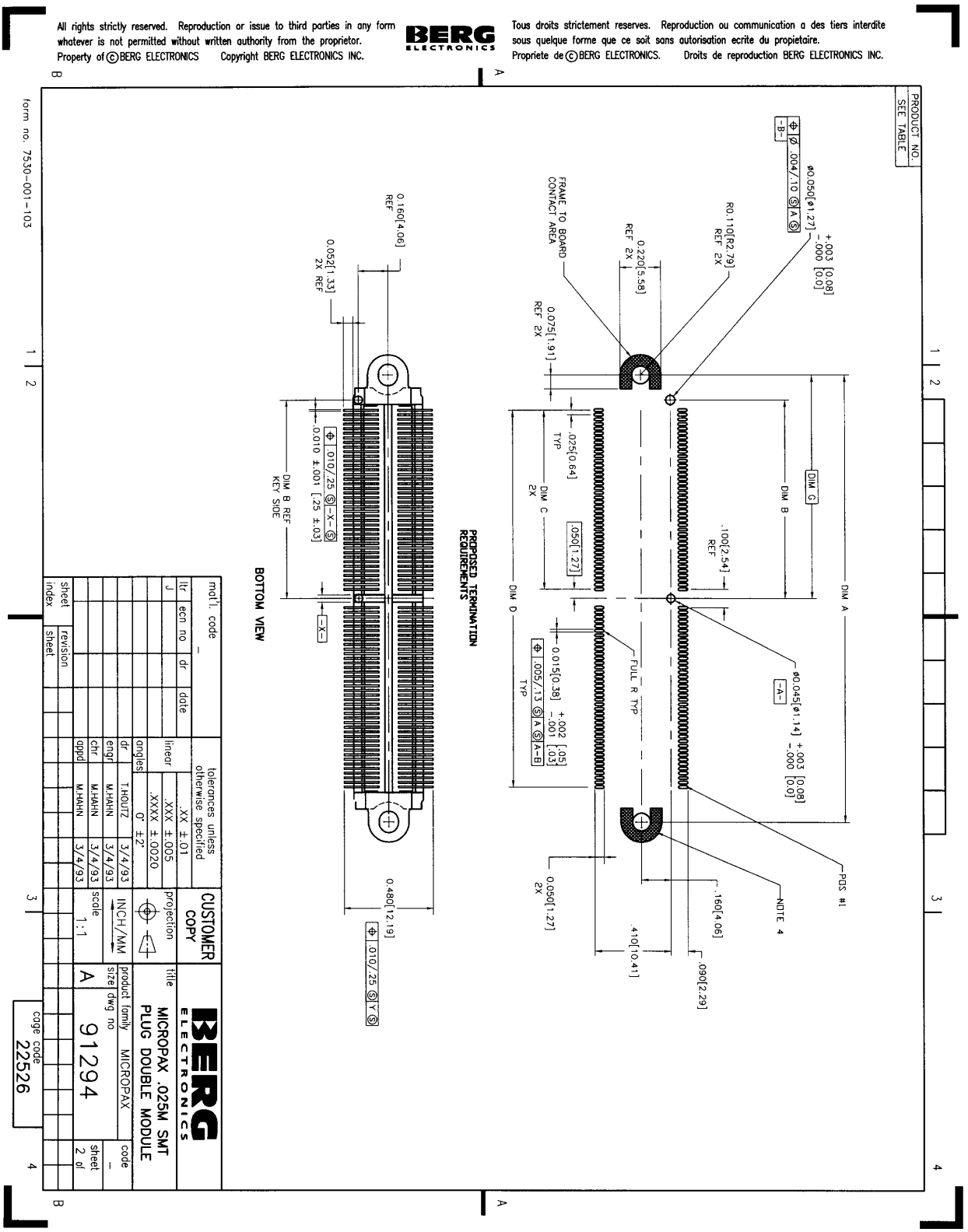
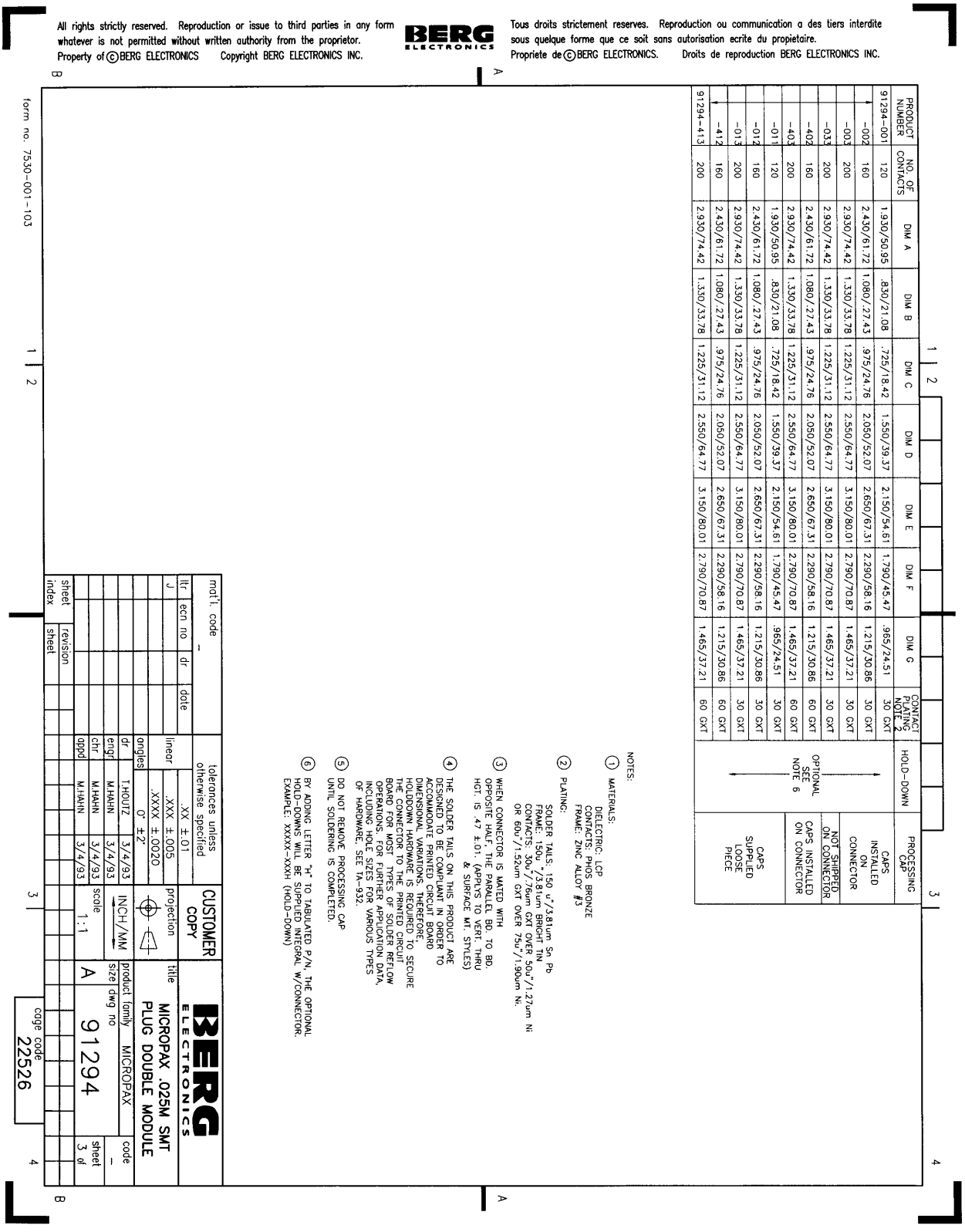


Figure A-4 Berg 91294-003 Datasheet Page 2 of 3



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Propriete de ©BERG ELECTRONICS. Droits de reproduction BERG ELECTRONICS INC.

PRODUCT NUMBER	NO. OF CONTACTS	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	CONTACT PLATING NOTE 2	HOLD-DOWN	PROCESSING CAP
91294-001	120	1.930/50.95	.830/21.08	.725/18.42	1.550/39.37	2.150/54.61	1.790/45.47	.965/24.51	30 GXT	OPTIONAL SEE NOTE 6	CAPS INSTALLED ON CONNECTOR
-002	160	2.430/61.72	1.080/27.43	.975/24.76	2.050/52.07	2.650/67.31	2.290/58.16	1.215/30.86	30 GXT		
-003	200	2.930/74.42	1.330/33.78	1.225/31.12	2.550/64.77	3.150/80.01	2.790/70.87	1.465/37.21	30 GXT		
-033	200	2.930/74.42	1.330/33.78	1.225/31.12	2.550/64.77	3.150/80.01	2.790/70.87	1.465/37.21	30 GXT		NOT SHIPPED ON CONNECTOR
-402	160	2.430/61.72	1.080/27.43	.975/24.76	2.050/52.07	2.650/67.31	2.290/58.16	1.215/30.86	60 GXT		CAPS INSTALLED ON CONNECTOR
-403	200	2.930/74.42	1.330/33.78	1.225/31.12	2.550/64.77	3.150/80.01	2.790/70.87	1.465/37.21	60 GXT		
-011	120	1.930/50.95	.830/21.08	.725/18.42	1.550/39.37	2.150/54.61	1.790/45.47	.965/24.51	30 GXT		
-012	160	2.430/61.72	1.080/27.43	.975/24.76	2.050/52.07	2.650/67.31	2.290/58.16	1.215/30.86	30 GXT		CAPS SUPPLIED LOOSE PIECE
-013	200	2.930/74.42	1.330/33.78	1.225/31.12	2.550/64.77	3.150/80.01	2.790/70.87	1.465/37.21	30 GXT		
-412	160	2.430/61.72	1.080/27.43	.975/24.76	2.050/52.07	2.650/67.31	2.290/58.16	1.215/30.86	60 GXT		
91294-413	200	2.930/74.42	1.330/33.78	1.225/31.12	2.550/64.77	3.150/80.01	2.790/70.87	1.465/37.21	60 GXT		

NOTES:

1. MATERIALS:
   DIELECTRIC: LCP
   CONTACTS: PHOS BRONZE
   FRAME: ZINC ALLOY #3
2. PLATING:
   SOLDER TAILS: 150 u"/3.81um Sn Pb
   FRAME: 150u"/3.81um BRIGHT TIN
   CONTACTS: 30u"/.76um GXT OVER 50u"/1.27um Ni
   OR 60u"/1.52um GXT OVER 75u"/1.90um Ni.
3. WHEN CONNECTOR IS MATED WITH OPPOSITE HALF, THE PARALLEL BD. TO BD. HGT. IS .47 ±.01. (APPLYS TO VERT. THRU & SURFACE MT. STYLES)
4. THE SOLDER TAILS ON THIS PRODUCT ARE DESIGNED TO BE COMPLIANT IN ORDER TO ACCOMMODATE PRINTED CIRCUIT BOARD DIMENSIONAL VARIATIONS. THEREFORE, HOLDDOWN HARDWARE IS REQUIRED TO SECURE THE CONNECTOR TO THE PRINTED CIRCUIT BOARD FOR MOST TYPES OF SOLDER REFLOW OPERATIONS. FOR FURTHER APPLICATION DATA, INCLUDING HOLE SIZES FOR VARIOUS TYPES OF HARDWARE, SEE TA-932.
5. DO NOT REMOVE PROCESSING CAP UNTIL SOLDERING IS COMPLETED.
6. BY ADDING LETTER "H" TO TABULATED P/N, THE OPTIONAL HOLD-DOWNS WILL BE SUPPLIED INTEGRAL W/CONNECTOR.
   EXAMPLE: XXXXX-XXXH (HOLD-DOWN)

ltr	ecn no	dr	date
J			

mat'l code –

tolerances unless otherwise specified
linear .XX ±.01 .XXX ±.005 .XXXX ±.0020
angles 0° ±2°

	dr	engr	chr	appd
	T.HOLTZ	M.HAHN	M.HAHN	M.HAHN
	3/4/93	3/4/93	3/4/93	3/4/93

CUSTOMER COPY

projection

scale 1:1

BERG ELECTRONICS

title MICROPAX .025M SMT PLUG DOUBLE MODULE

product family MICROPAX

code –

size A dwg no 91294

sheet 3 of 3

cage code 22526

INCH/MM

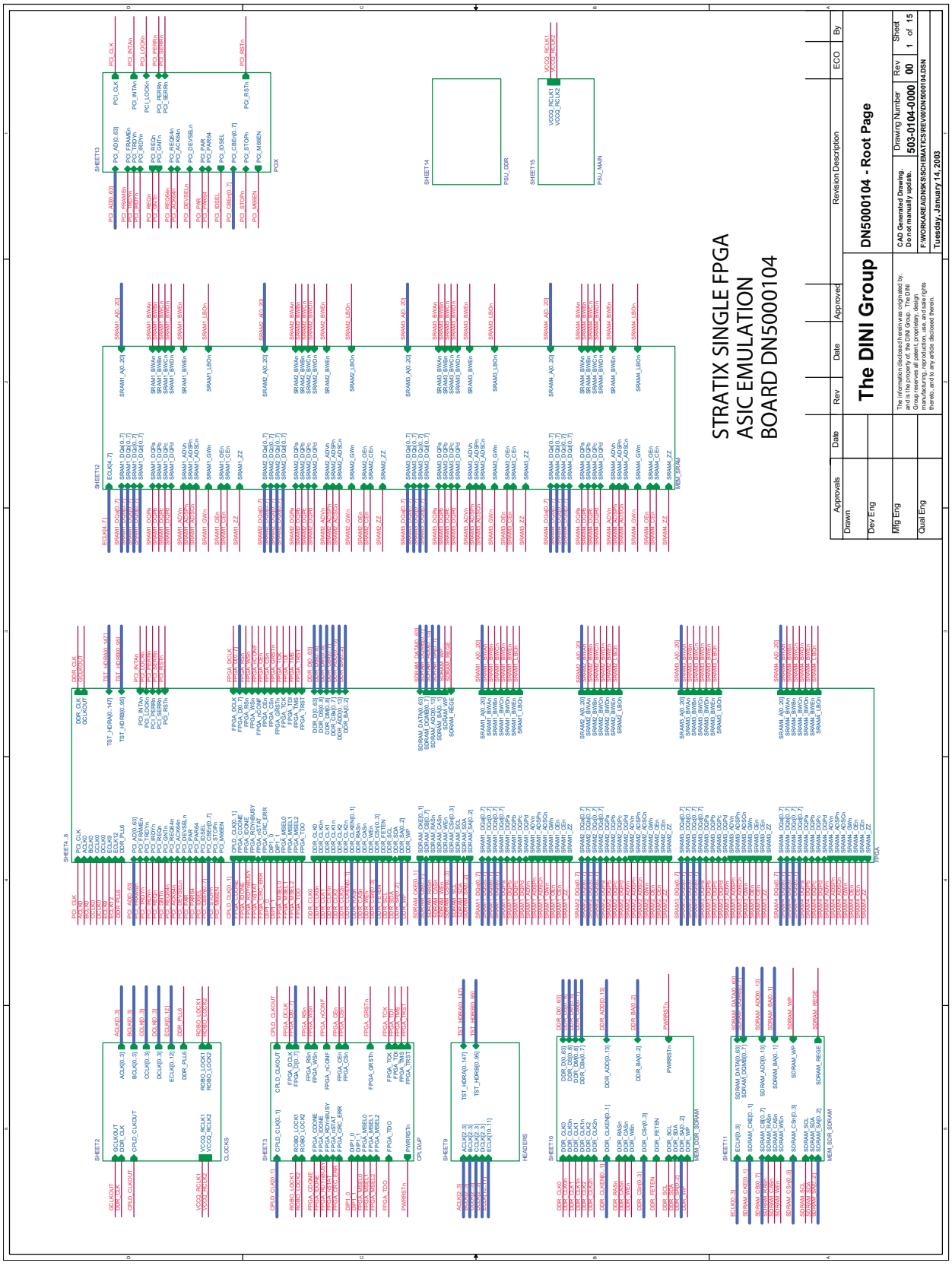
sheet index	revision	sheet

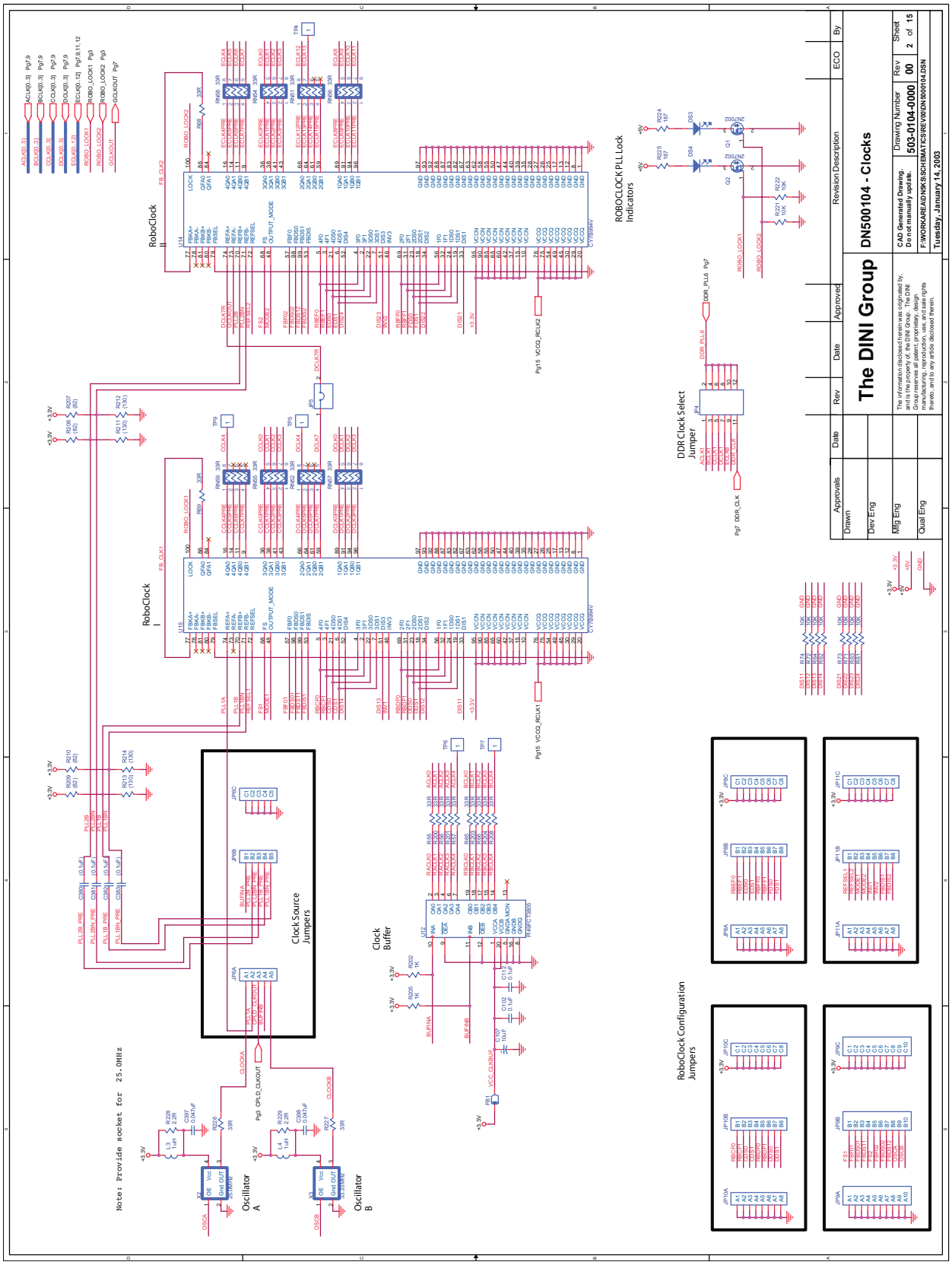
form no. 7530-001-103

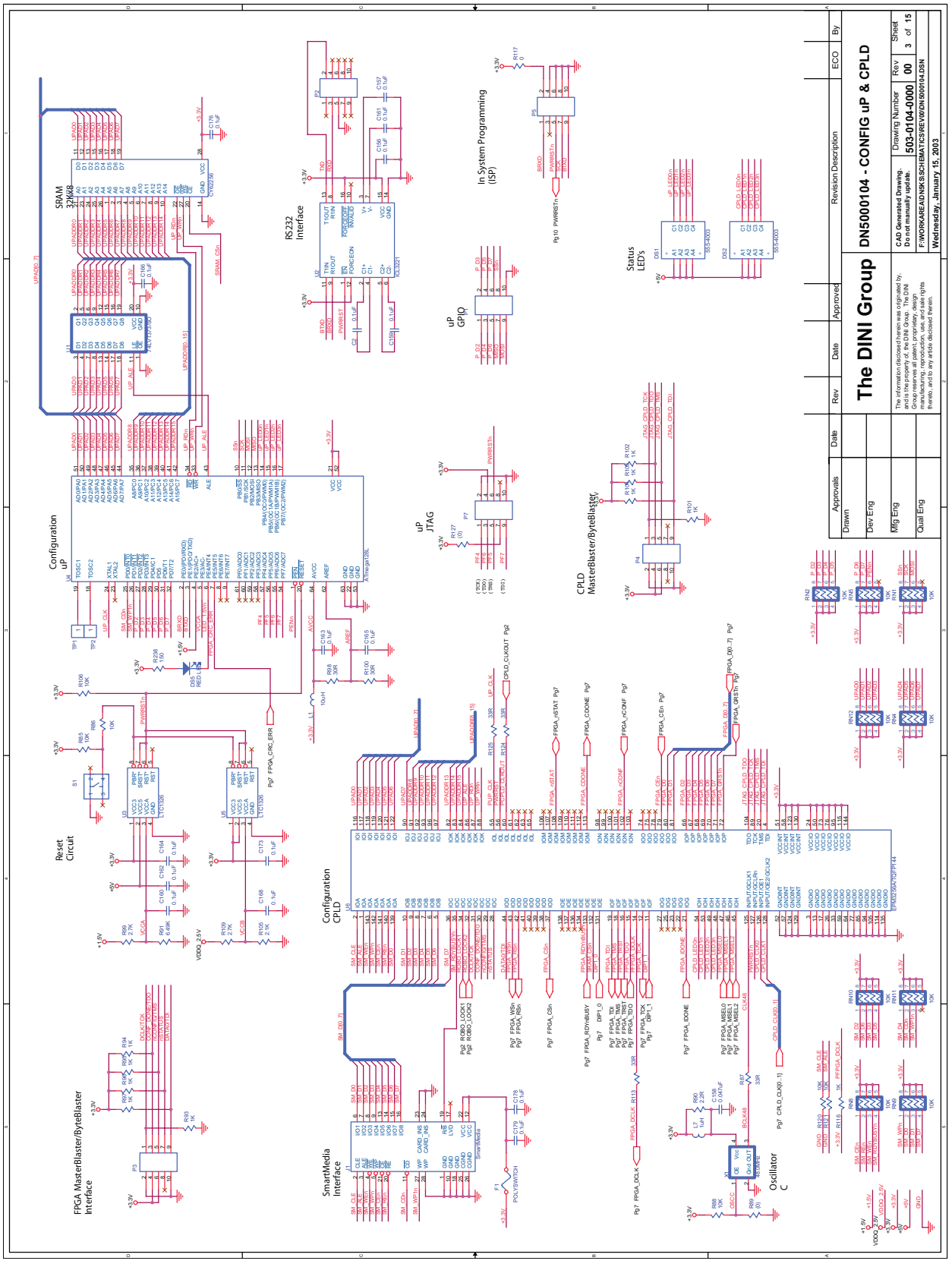
Appendix B

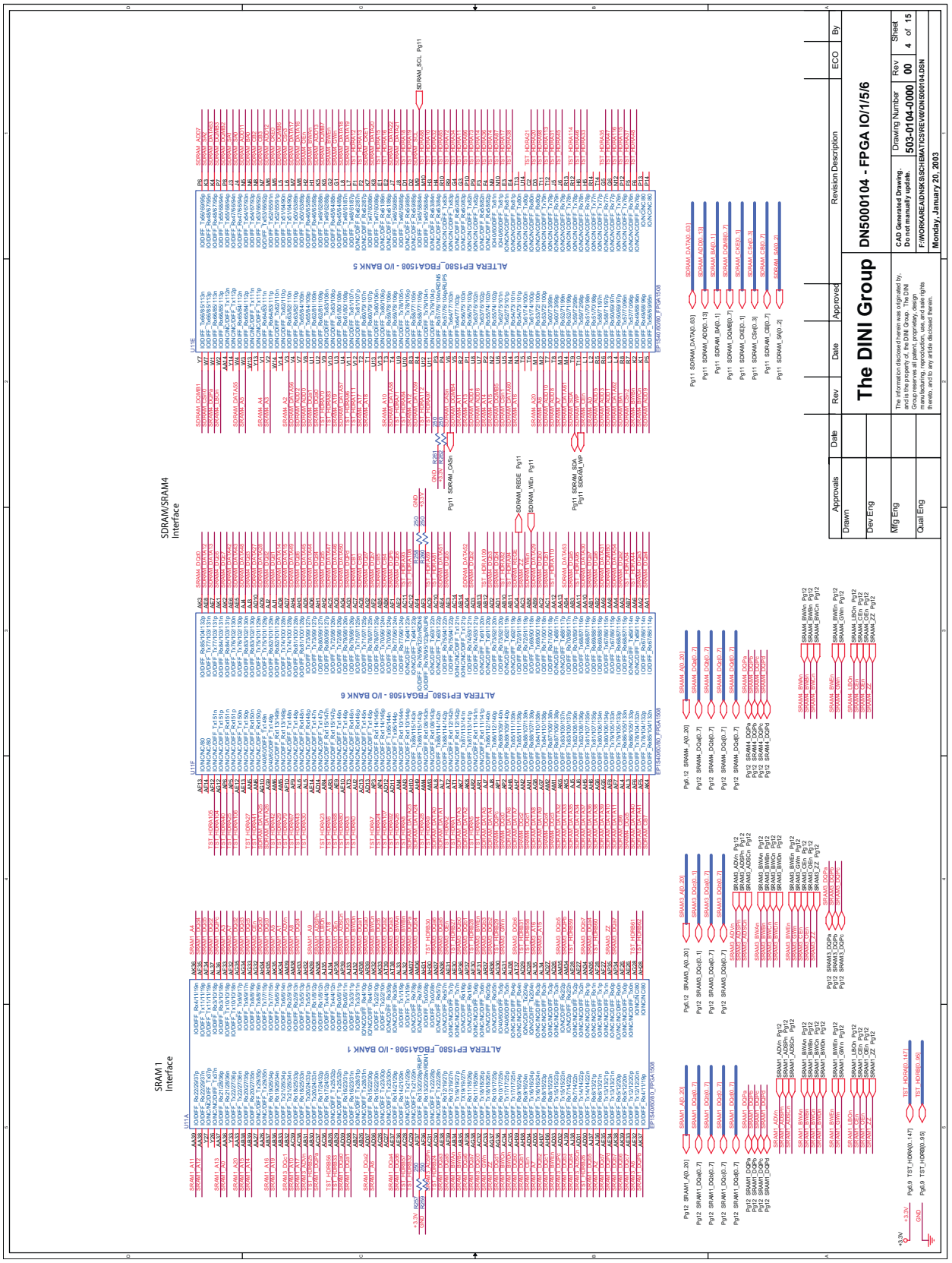
ET5000k10S Schematic

The ET5000k10S Schematic is presented on the following pages.


STRATIX SINGLE FPGA
ASIC EMULATION
BOARD DN5000104
The DINI Group
DN5000104 - Root Page
Drawing Number
503-0104-0000
Rev
00
Sheet
1 of 15
Tuesday, January 14, 2003


The DINI Group
DN500104 - Clocks
Drawing Number: 503-0104-0000
Rev: 00
Sheet: 2 of 15
Tuesday, January 14, 2003
RoboClock I
RoboClock II
Clock Source Jumpers
Clock Buffer
Oscillator A
Oscillator B
DDR Clock Select Jumper
ROBOCLOCK PLL Lock Indicators
RoboClock Configuration Jumpers
Note: Provide socket for 25.0MHz


The DINI Group
DN5000104 - CONFIG uP & CPLD
Drawing Number: 503-0104-0000
Rev: 00
Sheet: 3 of 15
Wednesday, January 15, 2003
Configuration uP
Reset Circuit
FPGA MasterBlaster/ByteBlaster Interface
SmartMedia Interface
Configuration CPLD
Oscillator
RS232 Interface
In System Programming (ISP)
uP GPIO
uP JTAG
CPLD MasterBlaster/ByteBlaster
Status LED's
SRAM 32K8


SRAM1 Interface
SDRAM/SRAM4 Interface
ALTERA EP1S80_FBGA1508 - I/O BANK 1
ALTERA EP1S80_FBGA1508 - I/O BANK 6
ALTERA EP1S80_FBGA1508 - I/O BANK 5
The DINI Group
DN5000104 - FPGA IO/1/5/6
Approvals
Drawn
Dev'Eng
Mfg Eng
Qual Eng
Date
Rev
Approved
Revision Description
ECO
By
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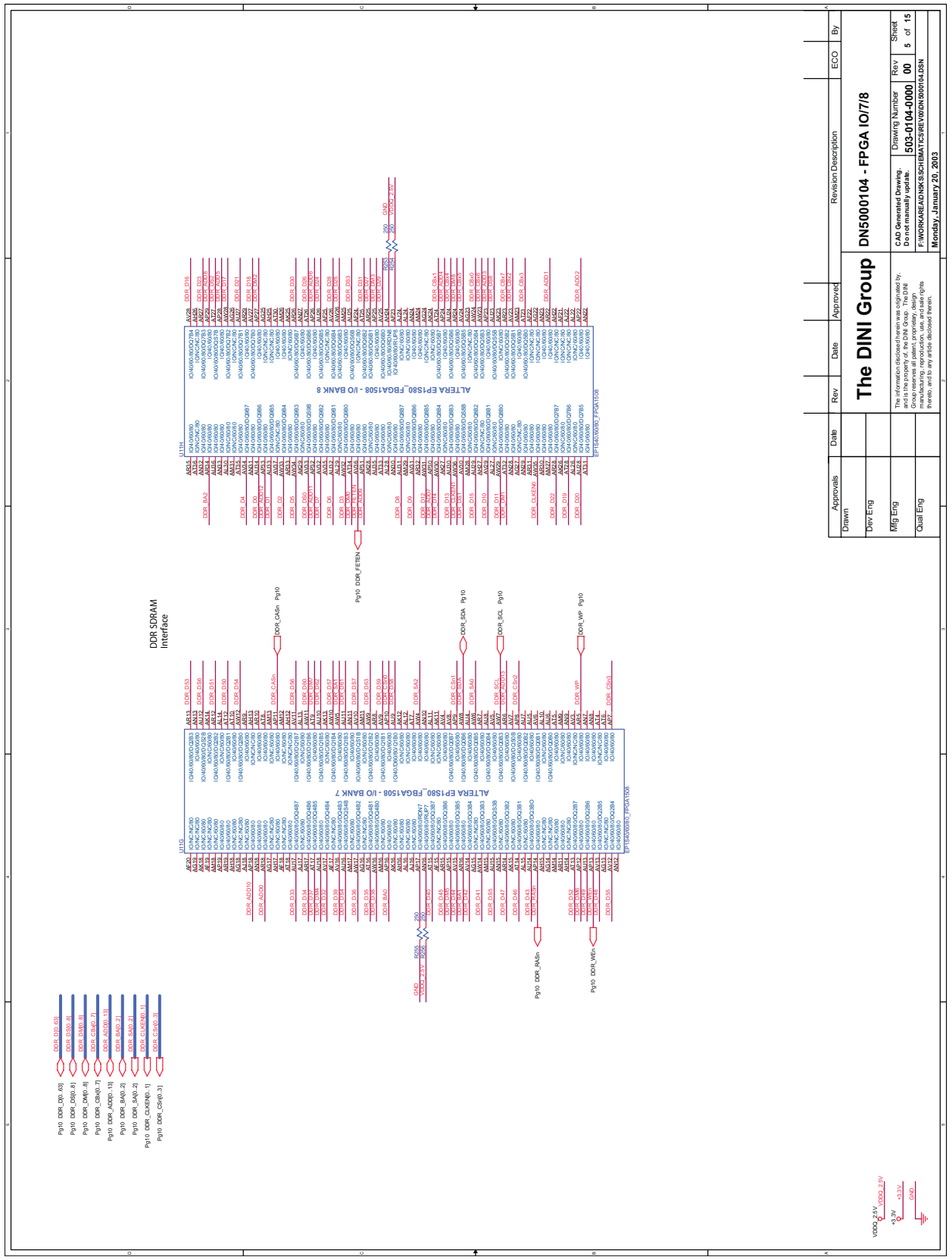
Monday, January 20, 2003


DDR SDRAM Interface
ALTERA EP1S80_FBGA1508 - I/O BANK 7
ALTERA EP1S80 _FBGA1508 - I/O BANK 8
The DINI Group
DN5000104 - FPGA IO/7/8
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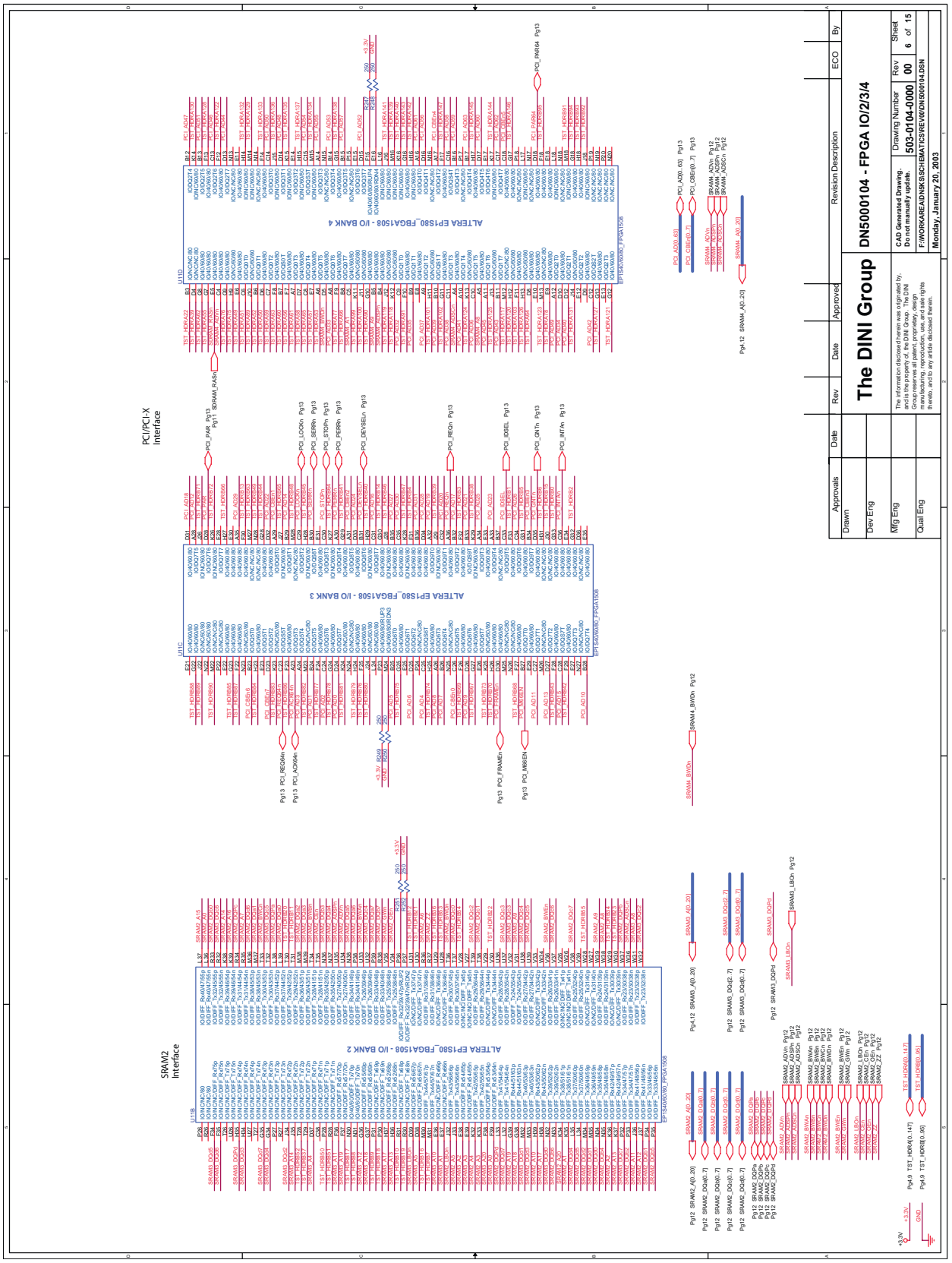
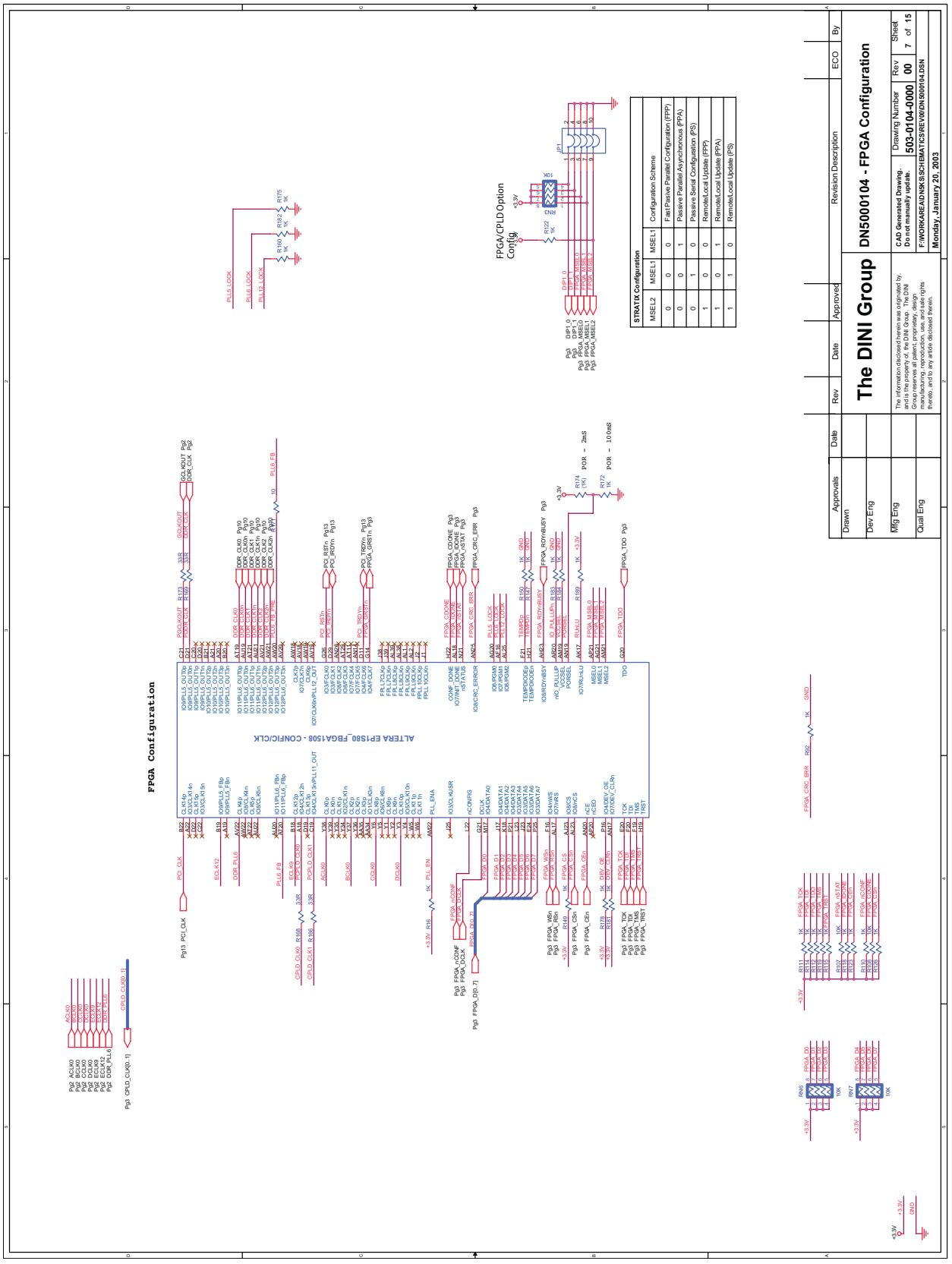

PCI/PCI-X Interface
SRAM2 Interface
ALTERA EP1S80_FBGA1508 - I/O BANK 2
ALTERA EP1S80_FBGA1508 - I/O BANK 3
ALTERA EP1S80_FBGA1508 - I/O BANK 4
The DINI Group
DN5000104 - FPGA IO/2/3/4
Revision Description
Approvals
Drawn
Dev'Eng
Mfg Eng
Qual Eng
Monday, January 20, 2003


FPGA Configuration
ALTERA EP1S80_FBGA1508 - CONFIG/CLK
The DINI Group
DN5000104 - FPGA Configuration
Revision Description
Approvals
Drawn
Dev Eng
Mfg Eng
Qual Eng
FPGA/CPLD Option Config
STRATIX Configuration
MSEL2 MSEL1 Configuration Scheme
0 0 Fast Passive Parallel Configuration (FPP)
0 0 1 Passive Parallel Asynchronous (PPA)
0 1 0 Passive Serial Configuration (PS)
1 0 0 Remote/Local Update (FPP)
1 0 1 Remote/Local Update (PPA)
1 1 0 Remote/Local Update (PS)
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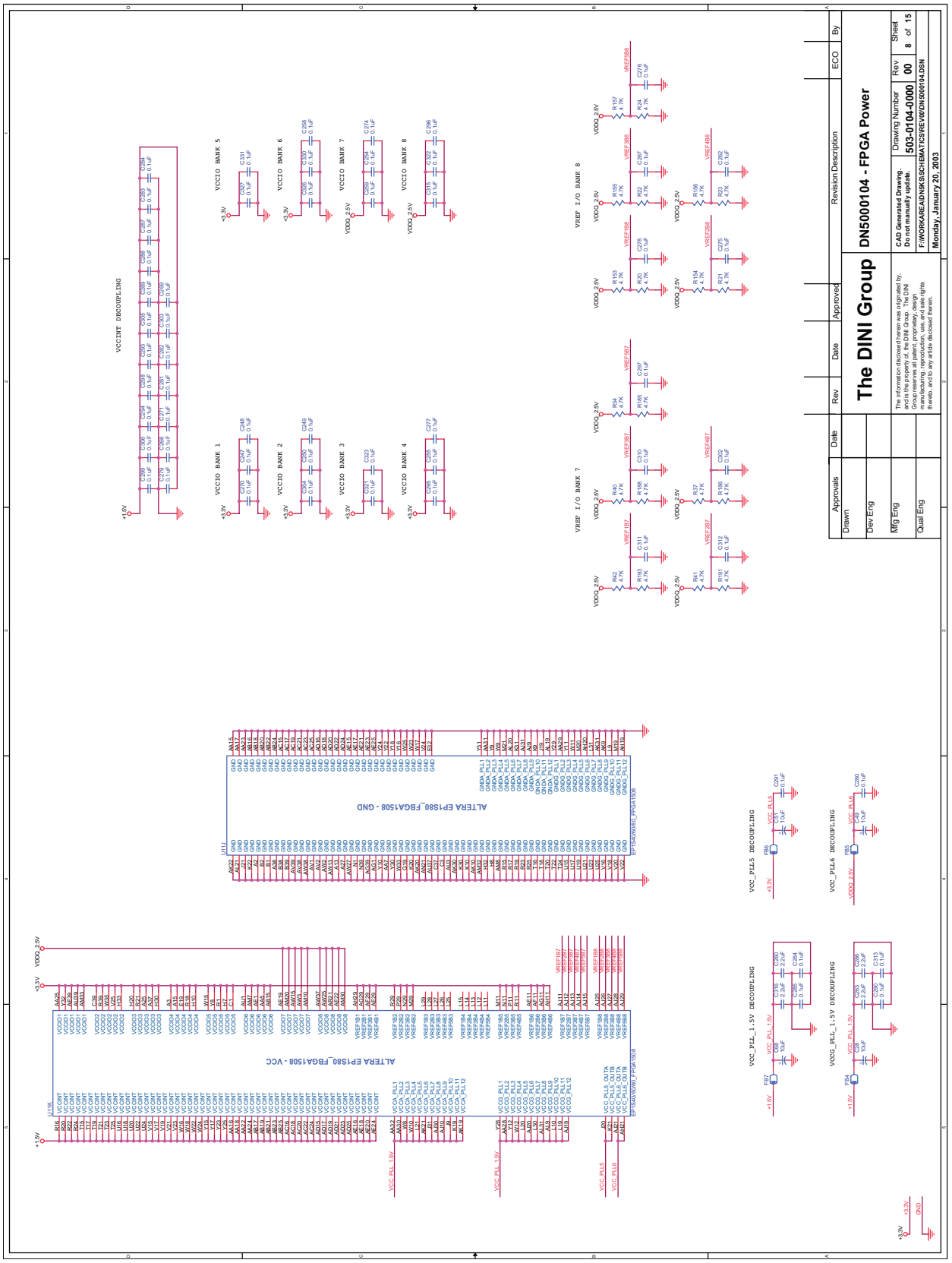
The DINI Group
DN5000104 - FPGA Power
Drawing Number: 503-0104-0000
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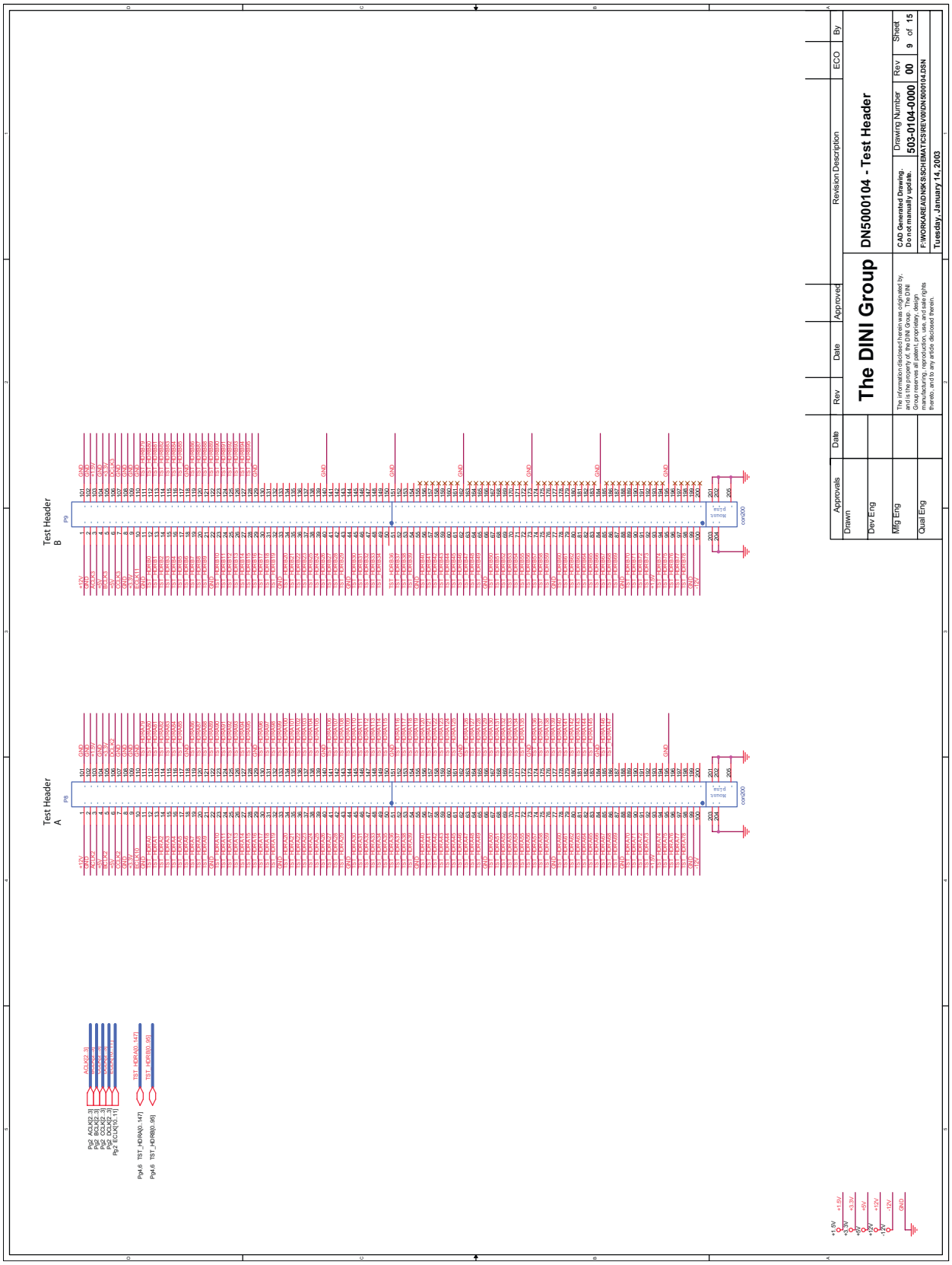
VCCINT DECOUPLING
VCCIO BANK 1
VCCIO BANK 2
VCCIO BANK 3
VCCIO BANK 4
VCCIO BANK 5
VCCIO BANK 6
VCCIO BANK 7
VCCIO BANK 8
VREF I/O BANK 7
VREF I/O BANK 8
ALTERA EP1S80_FBGA1508 - GND
ALTERA EP1S80_FBGA1508 - VCC
VCC_PLL5 DECOUPLING
VCC_PLL6 DECOUPLING
VCCG_PLL_1.5V DECOUPLING


Test Header A
Test Header B
P8
P9
Approvals
Drawn
Dev Eng
Mfg Eng
Qual Eng
Date
Rev
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Revision Description
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The DINI Group
DN5000104 - Test Header
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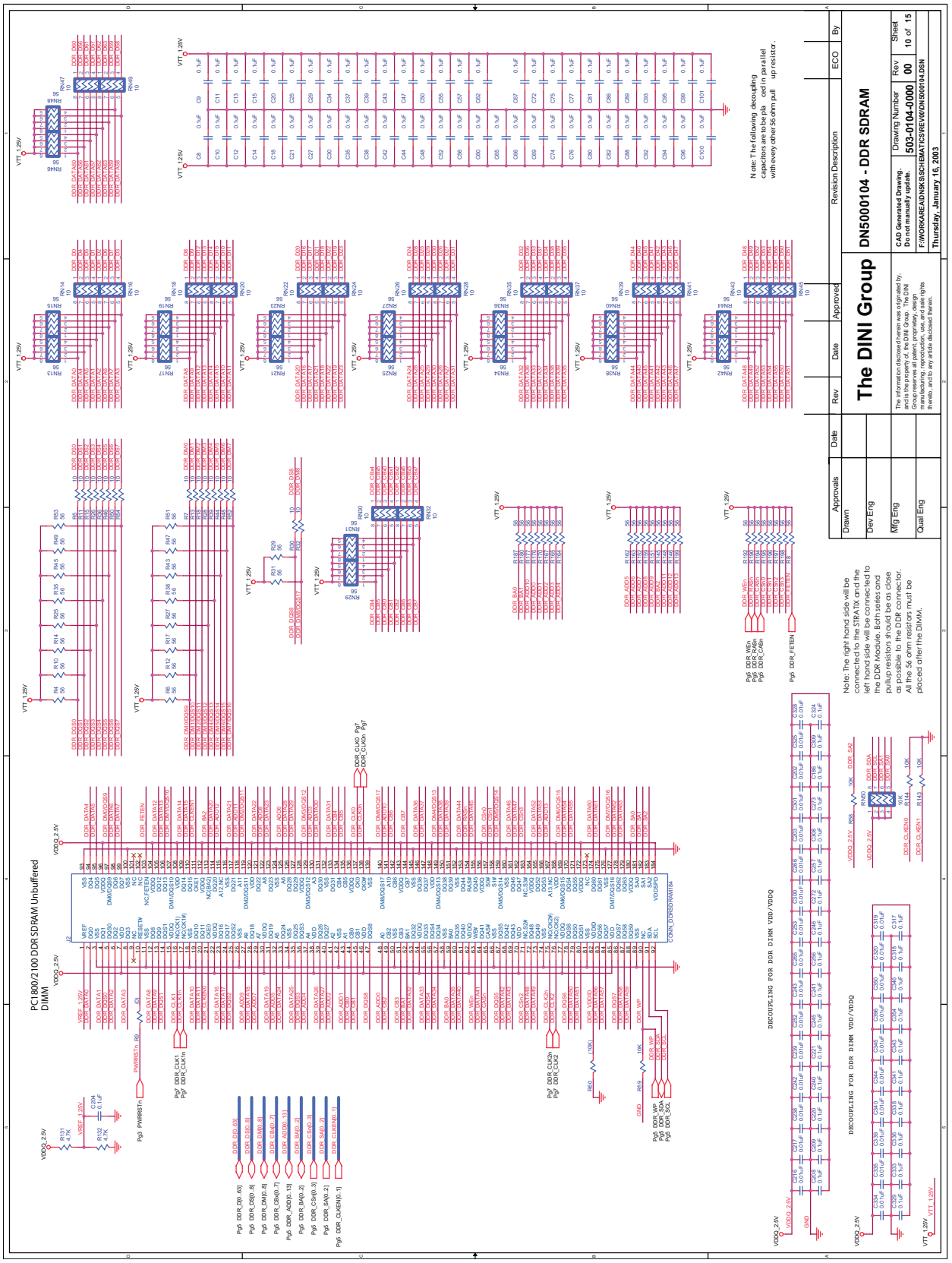
PCI 800/2100 DDR SDRAM Unbuffered DIMM
The DINI Group
DN5000104 - DDR SDRAM
Revision Description
Approvals
Drawn
Dev Eng
Mfg Eng
Qual Eng
Drawing Number 503-0104-00000
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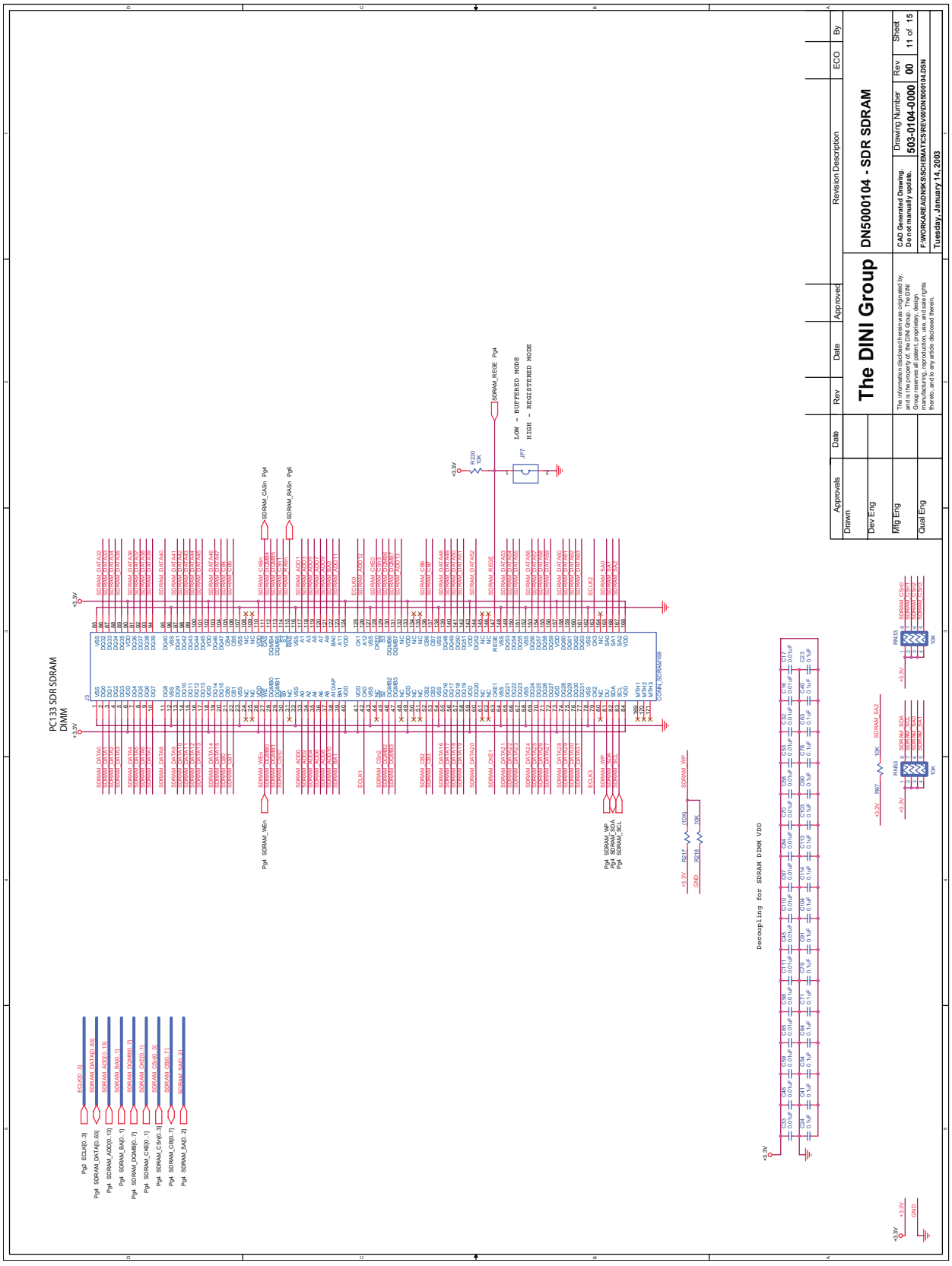
Thursday, January 16, 2003
Note: The following decoupling capacitors are to be placed in parallel with every other 56 ohm pull up resistor.
Note: The right hand side will be connected to the STRATIX and the left hand side will be connected to the DDR Module. Both series and pullup resistors should be as close as possible to the DDR connector. All the 56 ohm resistors must be placed after the DIMM.
DECOUPLING FOR DDR DIMM VDD/VDDQ


PC133 SDR SDRAM DIMM
LOW = BUFFERED MODE
HIGH = REGISTERED MODE
Decoupling for SDRAM DIMM VDD
The DINI Group
DN5000104 - SDR SDRAM
Drawing Number 503-0104-0000
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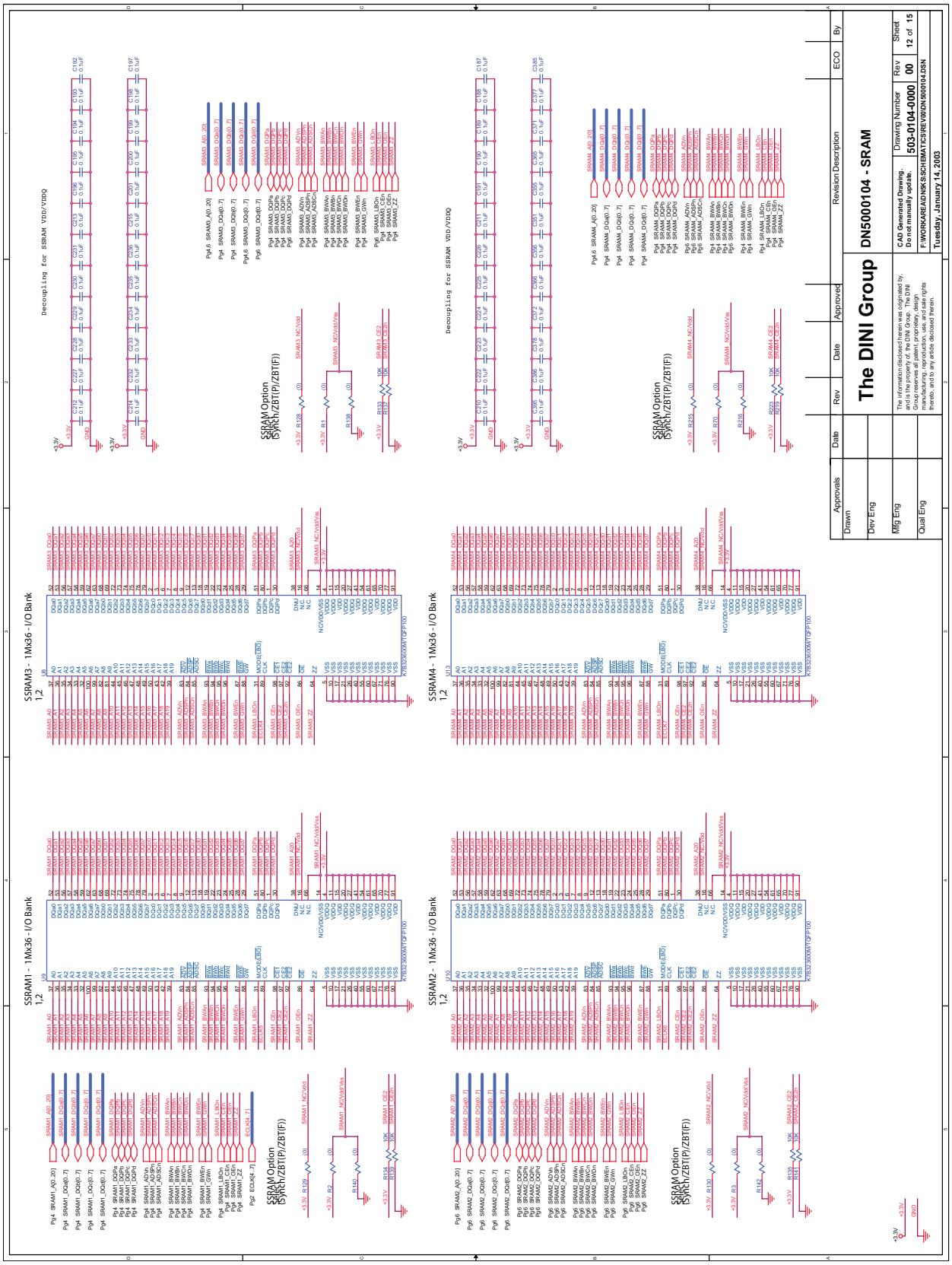
SSRAM1 - 1Mx36 - I/O Bank
SSRAM2 - 1Mx36 - I/O Bank
SSRAM3 - 1Mx36 - I/O Bank
SSRAM4 - 1Mx36 - I/O Bank
Decoupling for SSRAM VDD/VDDQ
SRAM Option
(SYNCH/ZBT(P)/ZBT(F))
Approvals
Drawn
Dev Eng
Mfg Eng
Qual Eng
Date
Rev
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Revision Description
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DN5000104 - SRAM
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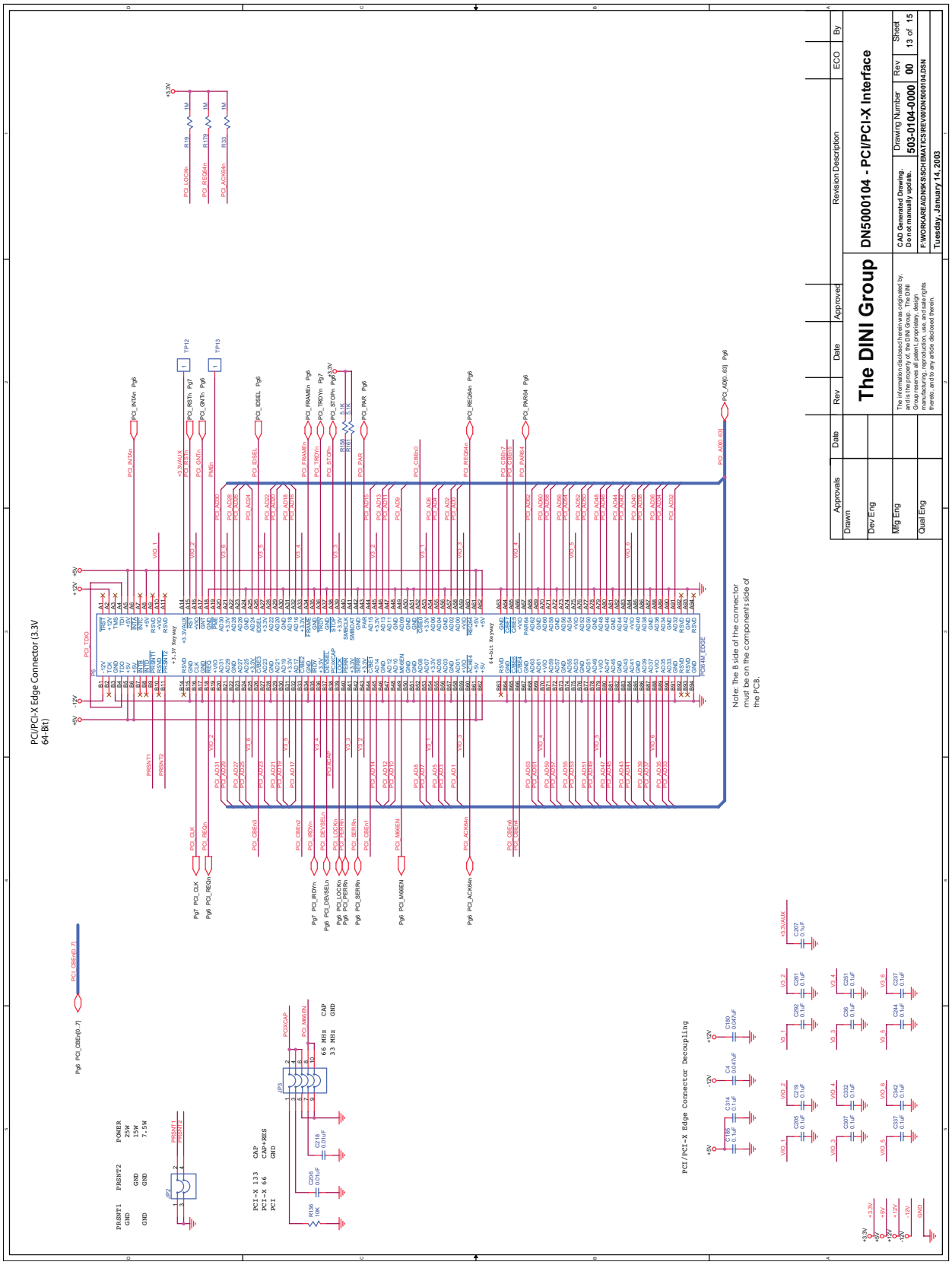
PCI/PCI-X Edge Connector (3.3V 64-Bit)
Note: The B side of the connector must be on the component's side of the PCB.
PCI/PCI-X Edge Connector Decoupling
The DINI Group
DN5000104 - PCI/PCI-X Interface
CAD Generated Drawing. Do not manually update.
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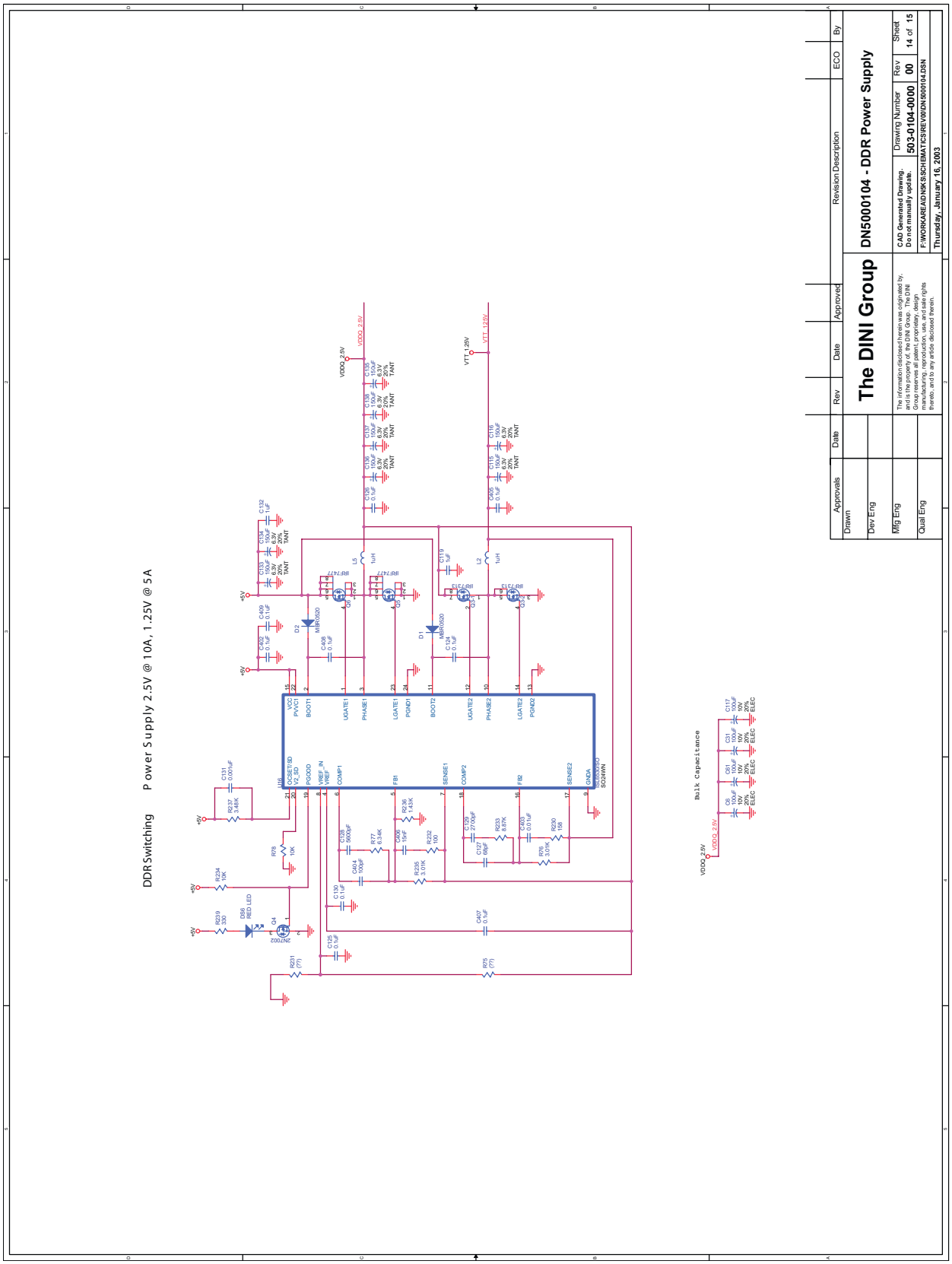
Approved


DDR Switching Power Supply 2.5V @ 10A, 1.25V @ 5A
The DINI Group
DN5000104 - DDR Power Supply
Drawing Number: 503-0104-00000
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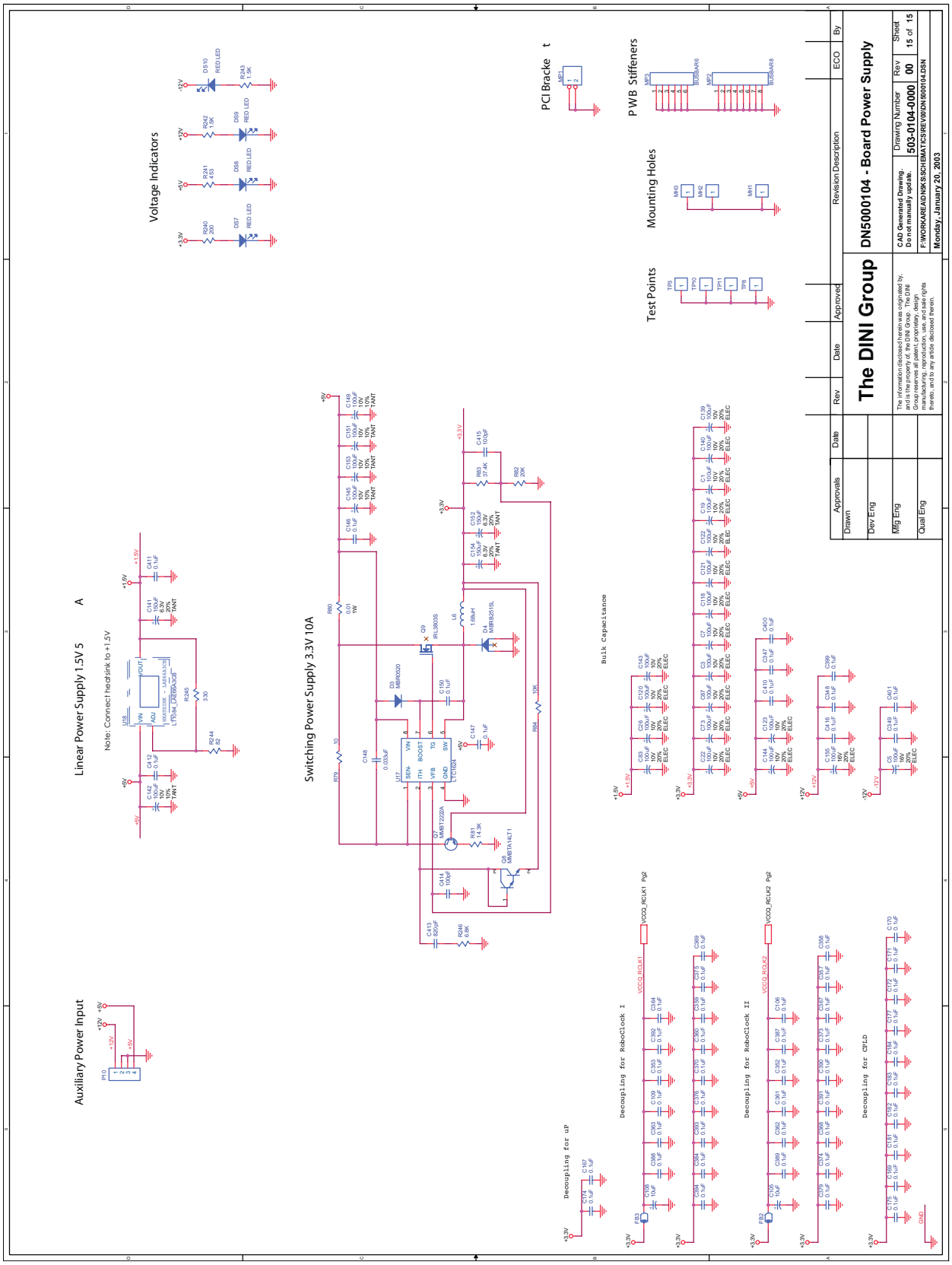
Auxiliary Power Input
Linear Power Supply 1.5V 5 A
Note: Connect heatsink to +1.5V
Switching Power Supply 3.3V 10A
Voltage Indicators
PCI Bracket
PWB Stiffeners
Test Points
Mounting Holes
Bulk Capacitance
Decoupling for uP
Decoupling for RoboClock I
Decoupling for RoboClock II
Decoupling for CPLD
The DINI Group
DN5000104 - Board Power Supply
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Glossary and Acronyms

µP	microprocessor
BAR	Base Address Register
BGA	ball grid array
BIOS	Basic Input/Output Services
CMOS	complementary metal-oxide semiconductor
CPLD	Complex Programmable Logic Device
CSF	Configuration Settings File
DSP	digital signal processing
EEPROM	Electrically Erasable PROM
EIA	Electronic Industries Association
ESD	Electro-Static Discharge
FAQ	frequently asked questions
FAT	file allocation table
FPGA	field programmable gate array
FT	flowthrough
HDL	Hardware Description Language
I/O	input/output
IP	intellectual property
LAB	Logic Array Blocks
LE	logic element
LSI	large scale integration
LUT	look-up table
LVCMOS	low voltage complementary metal-oxide semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	low voltage transistor-transistor logic
MDR	Mini D Ribbon
PCI	peripheral component interconnect
PCI-X	peripheral component interconnect (extended)
PL	pipelined
PLL	phase lock loop
PNP	plug-and-play
PWB	printed wire board
RAM	random access memory
RBF	Raw Binary File
REGE	register enable
RISC	reduced instruction set computer
SDRAM	synchronous dynamic random access memory
SRAM	shadow random access memory
SSRAM	synchronous static random access memory
TTL	transistor-transistor logic
VCO	voltage controlled oscillator
VHDL	VHSIC Hardware Description Language
VREF	reference voltage
ZBT	zero-bus-turnaround

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Symbols

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