SIS8900
µTCA FOR PHYSICS RTM

User Manual

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Revision Table:

Revision	Date	Modification
1.00	25.11.11	Initial release
1.01	21.12.11	Photograph and extensions
1.02	01.03.12	J310, J320 connector contact layout added
1.03	24.01.13	Current consumption 12V, SMD LED's positions added
1.04	28.06.13	Page 4 and 13 – SIS8300-L added Page 5 "(SIS8300 only)" added Page 9, 11 and 12 "0Ohm 0603" changed to "0Ohm 0402" Page 11 note (×) in table and below added Page 11 in Table, "J101" to "J102" changed Page 17 in note below "SIS8300-L" added Page 15 two new zone 3 identifier records added Page 20 note about Data 0,1,2,9,10,11 to SIS8300-L added

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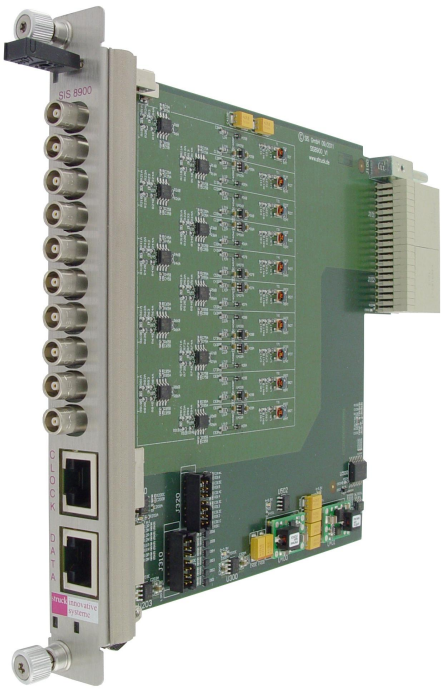
1 Introduction

The SIS8900 is a 10 channel single ended input RTM according to the MTCA.4 standard. The card as developed to be used in combination with the SIS8300/SIS8300-L 125 MS/s 16-bit MTCA.4 digitizer.



SIS8900

As we are aware, that no manual is perfect, we appreciate your feedback and will incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.html .

2 Design

The SIS8900 card is a signal conditioning input card for the SIS8300 digitizer.

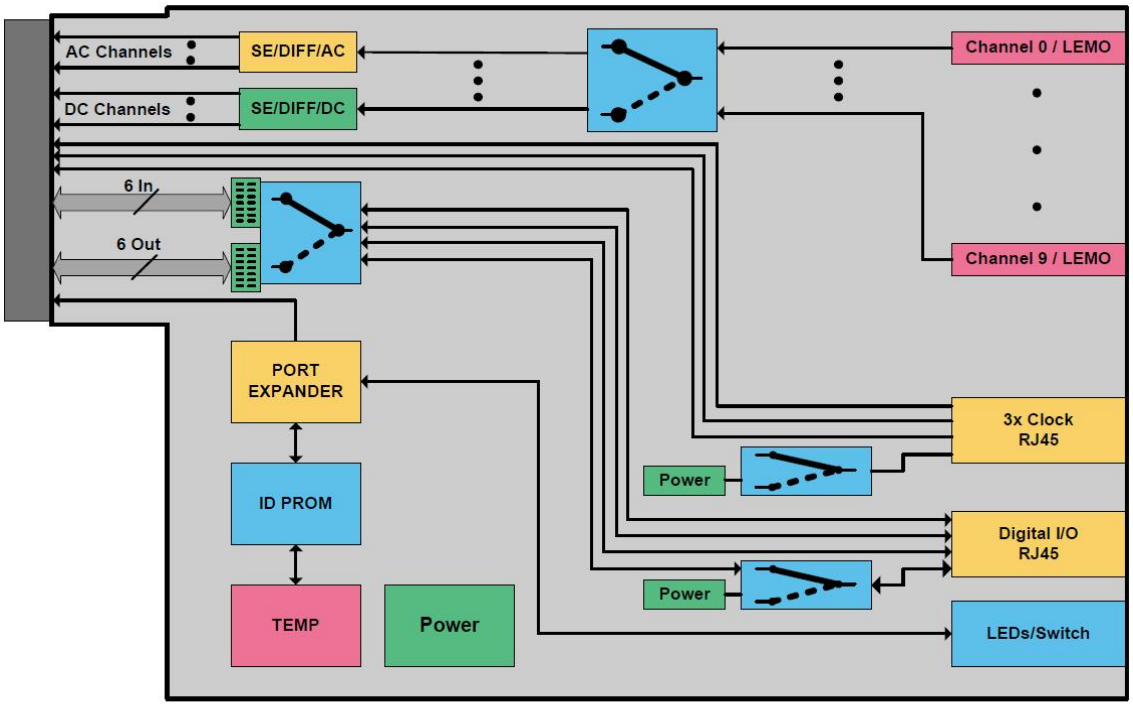
2.1 Functionality

The key properties of the SIS8900 card are listed below.

- MTCA.4 µRTM board
- IPMI port expander (µRTM management)
- 10 channel analog signal input with coaxial connectors
- coaxial connectors LEMO (optional FBM)
- channels alternatively AC or DC stage via solder bridges (assembly option)
- inputs to SIS8300 DC stage with single ended to differential conversion via operational amplifier or inputs to SIS8300 AC stage with single ended to differential conversion via transformer
- 3 differential clock inputs with RJ45 connectors
- 3 or 4 (assembly option) buffered differential I/O with RJ45 connector
- Access to 6 digital inputs and 6 digital outputs via two pin headers (with 8300 only)

2.2 Block Diagram

A simplified block diagram of the SIS8900 is shown below.



SIS8900 µRTM Transition Board

3 LEDs

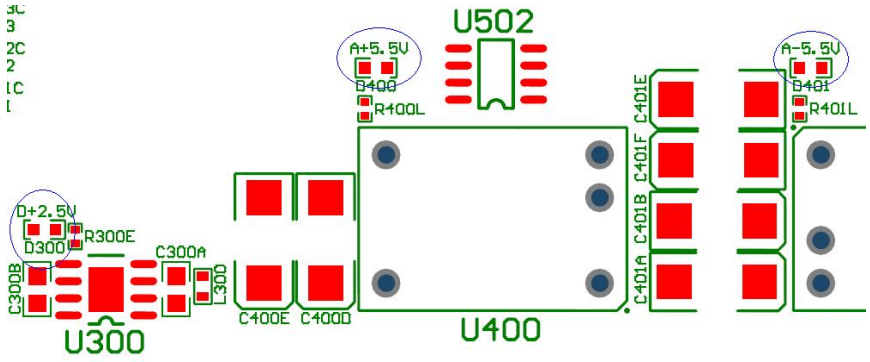
3.1 µRTM LEDs

The µRTM LEDs are implemented according to the standard.

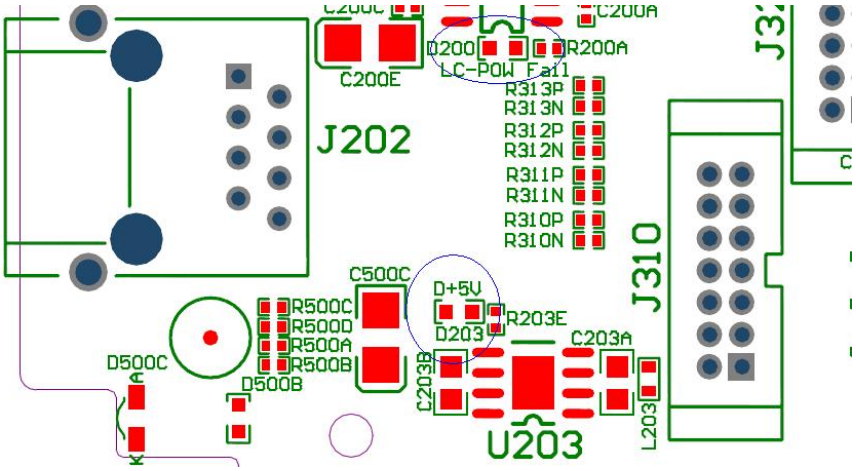
3.2 SMD LEDs

A number of surface mount red LEDs are on the SIS8900 to visualize part of the board status.

LED designator	LED comment	Function
D200	LC-POW Fail	RJ45 current limiter power fail
D203	D+5V	D+5V present
D300	D+2.5V	D+2.5V present
D400	A+5.5V	A+5.5V present
D401	A-5.5V	A-5.5V present



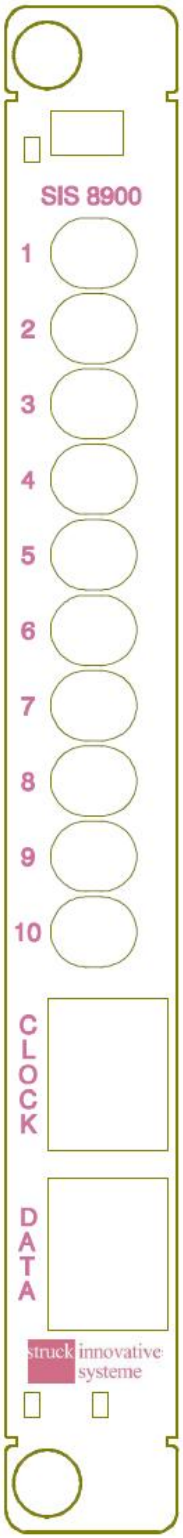
Positions of SMD LEDs D300, D400 and D401



Positions of SMD LEDs D200 and D203

4 Front panel

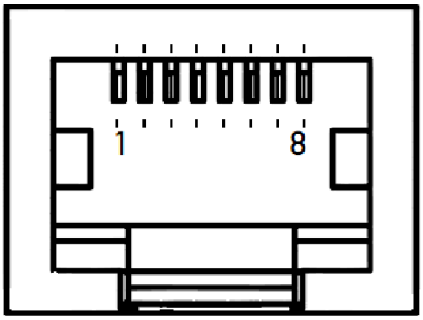
A sketch of the SIS8900 front panel is shown below.



Note: channel indexing for AC configuration (swapped for DC case in conjunction with SIS8300 V2)

4.1 RJ45 Connectors

Two RJ45 connectors are present for differential clock and digital I/O signals. Optionally +5V power can be supplied to both connectors as stuffing option. A current limiter guarantees a short circuit protected power and the current is limited to 250mA per connector.
The drawing with the pin count and the orientation of both connectors is shown below.



Front view

4.1.1 J201 RJ45 Clock Connector

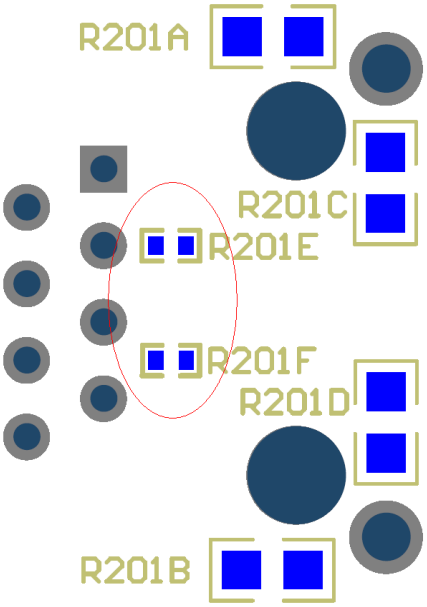
The clock input signals are fed from the RJ45 connector directly to the Zone3 connector without any signal conditioning. Pin assignment and function are shown in table below

Pin	Signal Name	Function
1	CLK0-	Clock 0, negative signal of differential pair
2	CLK0+	Clock 0, positive signal of differential pair
3	CLK_POW	+5V power supply, positive line (assembly option)
4	CLK1-	Clock 1, negative signal of differential pair
5	CLK1+	Clock 1, positive signal of differential pair
6	CLK_GND	+5V power supply, ground line (assembly option)
7	CLK2-	Clock 2, negative signal of differential pair
8	CLK2+	Clock 2, positive signal of differential pair

Pin 3 and 6 are connected to the +5V power supply by default

Note: The CLK0, CLK1 and CLK2 signals are referred to as RTM_CLK0, RTM_CLK1 and RTM_CLK2 in the SIS8300/8300-L manual's clock distribution diagram.

To configure optionally +5V power at J201 Pin 3 and 6 there are two solder bridges at bottom side below the RJ45 Clock Connector designated as R201E and R201F.



Settings of both solder bridges are shown below. To establish state closed a solder bridge (0 Ohm 0402 resistors) must be installed.

Designator	Setting/State	Function
R201E	open	J201 Pin 3 unconnected
R201F	open	J201 Pin 6 unconnected
R201E	closed	J201 Pin 3 connected to positive line of +5V power supply
R201F	closed	J201 Pin 6 connected to negative line of +5V power supply (Ground)

R201E and R201F are in state closed by default

don’t connect +5V power supply option to J201 pins if you are unsure that the opposite part of RJ45 Connection is compatible, otherwise may result in serious damage of the SIS8900 and connected cards

4.1.2 J202 RJ45 Data Connector

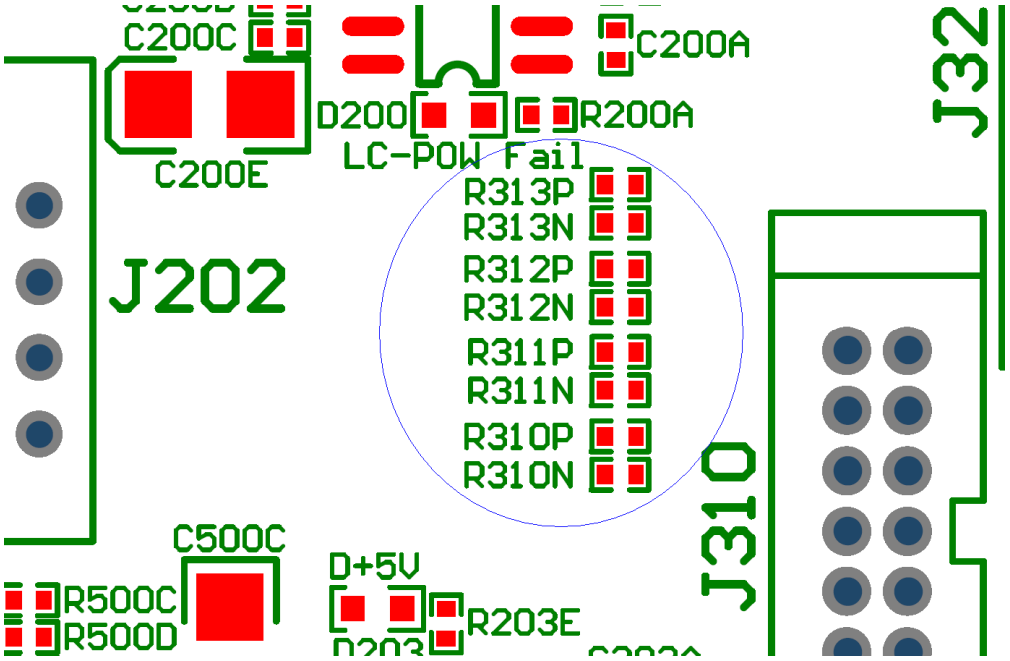
The RJ45 data I/Os are buffered LVDS signals linked to the Zone3 connector.
Pin assignment and function are shown in the table below.

Pin	Signal	Function
1	DATA3+	Data 3, positive signal of differential pair
2	DATA3-	Data 3, negative signal of differential pair
3	DATA2+ (or) DATA_POW	Data 2, positive signal of differential pair or +5V power supply, positive line (assembly option)
4	DATA1+	Data 1, positive signal of differential pair
5	DATA1-	Data 1, negative signal of differential pair
6	DATA2- (or) DATA_GND	Data 2, negative signal of differential pair or +5V power supply, ground line (assembly option)
7	DATA0+	Data 0, positive signal of differential pair
8	DATA0-	Data 0, negative signal of differential pair

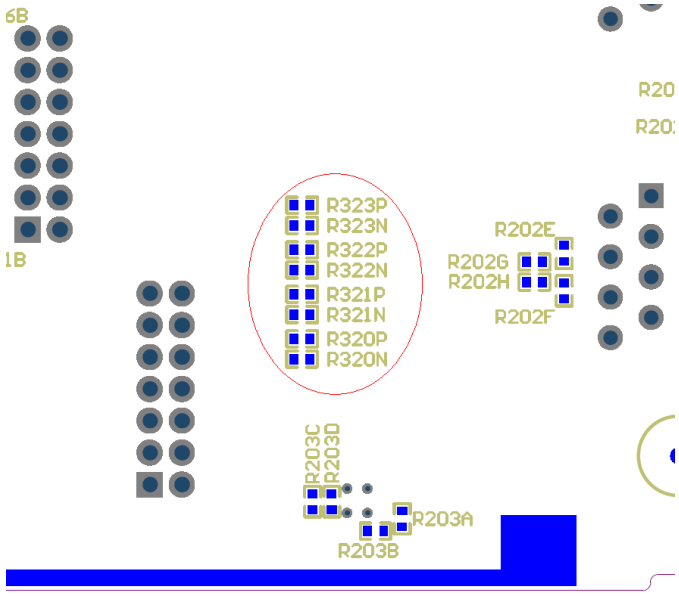
Pin 3 and 6 are connected to the +5V power supply by default

All data signals can be routed either to input or output signals of the Zone3 connector.
The connections are established with solder bridges.

The solder bridges R310(P,N) to R313(P,N) are located next to the RJ45 data connector J202 on the top side and connecting to the data outputs of the Zone3 connector.



The solder bridges R320(P,N) to R323(P,N) are located next to the RJ45 data connector J202 on the bottom side and connecting to the data inputs of the Zone3 connector.



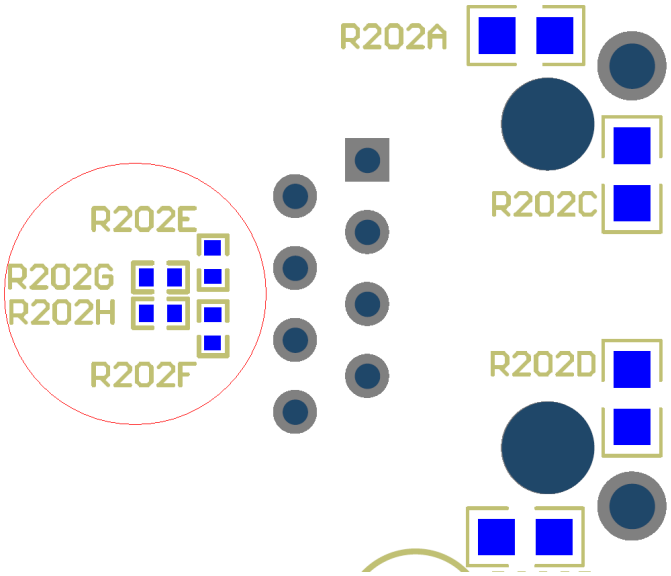
Routing table and settings of solder bridges are shown below. To establish connections to appropriate I/Os of Zone3 connector the corresponding solder bridges (0Ohm 0402 resistors) must be installed.
Installation of the solder bridges for both in- and output of one signal at the same time may result in serious damage of the SIS8900 and connected cards.

Signals on RJ45 / J202, both (+ & -)	Connection as	Solder bridges, install both (P & N)	Signals on Zone3 connector J102, both (+ & -)
DATA0	Input	R310	D0 (×)
DATA0	Output	R320	D6
DATA1	Input	R311	D1 (×)
DATA1	Output	R321	D7
DATA2	Input	R312	D2 (*) (×)
DATA2	Output	R322	D8 (*)
DATA3	Input	R313	D3
DATA3	Output	R323	D9 (×)

For use with SIS8300, DATA0, DATA1 are configured as inputs and DATA3 as output by default.
For use with SIS8300-L, DATA0, DATA1 are configured as outputs and DATA3 as input by default.

(*) this DATA bit can be used for digital I/O only if the J202 Pin 3 and 6 are not configured for +5V power supply option (see following section)
(×) this DATA bit can't be used in conjunction of SIS8300-L, this limitation don't exist at SIS8300

To configure J202 Pin 3 and 6 for optionally +5V power supply or use for digital I/O there are four solder bridges located at bottom side near the RJ45 Data Connector designated as R202E, R202F, R202G, R202H.



Settings of solder bridges are shown below. To establish state closed solder bridges (0 Ohm 0402 resistors) must be installed.

Solder bridges R202E, R202F	Solder bridges R202G, R202H	Function
closed	open	J202 Pin 3 and 6 connected to +5V power supply option
open	closed	J202 Pin 3 and 6 connected to digital I/O logic as DATA2
open	open	J202 Pin 3 and 6 unconnected

R202E, R202F are in state closed and R202G, R202H are in state open by default

only one of these three configurations shown in table above is allowed

don’t connect +5V power supply option to J202 pins if you are unsure that the opposite part of RJ45 Connection is compatible, otherwise may result in serious damage of the SIS8900 and connected cards

4.2 Coaxial Analog Input Signal Connectors

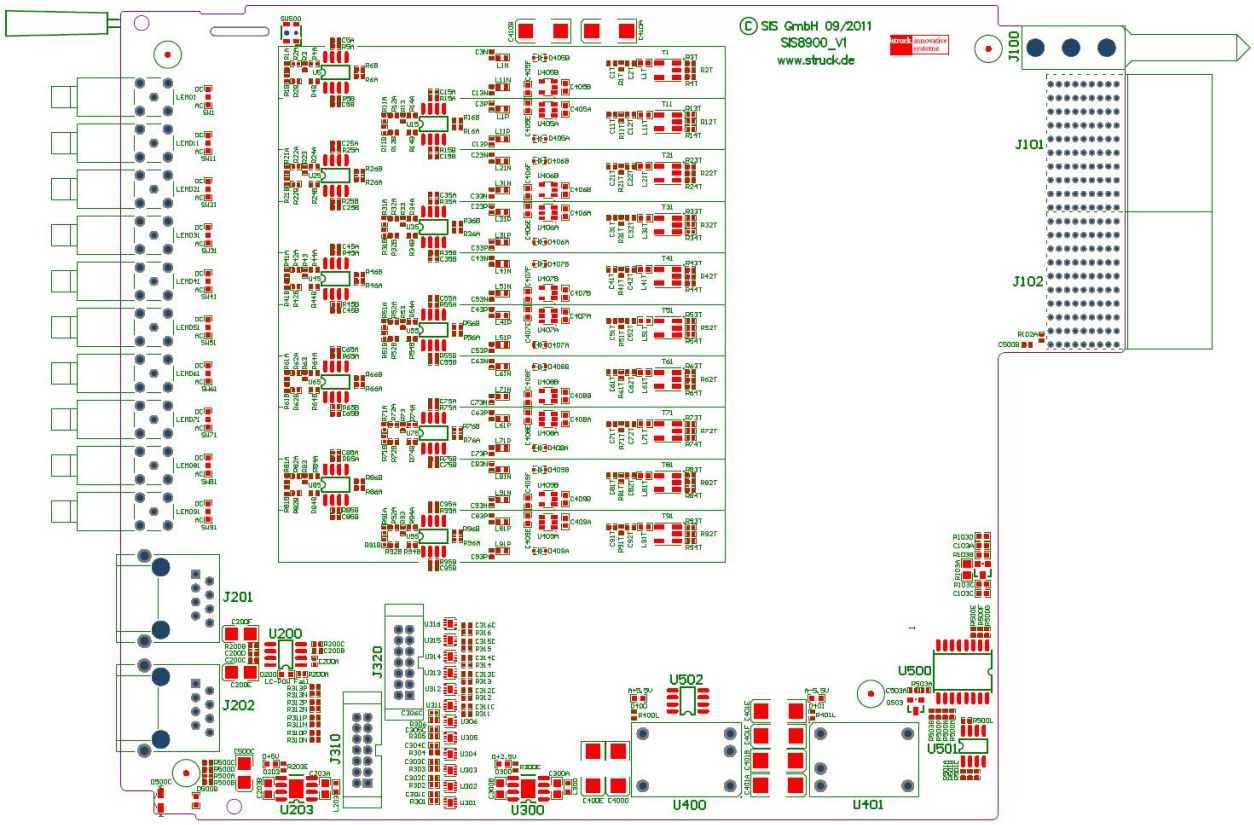
The front panel analog input connector can be stuffed with two different connector types. Designators of the connectors for channel 1..10 are LEMO1, LEMO11, LEMO21 through LEMO91.

Manufacturer	Part Number	Description
LEMO	EPL.00.250.NTN	Elbow female print socket, brass nickel-plated
FCT	FBM001P154MR	Female print socket, gold over nickel-plated

Analog Input for both, DC or AC configuration, is designed to accept a maximum peak to peak signal level of +1V…-1V into 50 Ohms in combination with the SIS8300/SIS8300-L digitizer (in default configuration). In AC configuration the analog input signal is AC coupled to the internal logic.

5 Board Layout

A print of the silk screen of the component side is shown below.



Connector types
The used connectors are listed in the table below.

Designator	Function	Manufacturer	Part Number
LEMO1 …	Coaxial Analog Input	LEMO or FCT	(See chapter 4.2)
J201, J202	RJ45, Clock, Digital I/O	ERNI	133268
J310, J320	LVDS-Bus Test Loop	MOLEX	87831-1420
J101, J102	Zone3 Conn. to AMC	ERNI	204781
J100	Male key guide µTCA	TYCO	1469265-3 (*)

Note (*): The used Key may depend on the hardware configuration of the SIS8900

6 RTM management

The SIS8900 RTM is compliant to the PICMG MTCA.4 specification. It has an on board I²C EEProm (on address 0x50) and a NXP PCF8574-compatible port expander (on address 0x7C).

The table below lists the port expander connection map for normal operation:

Port pin	Function
P0	HotSwap Switch (low active)
P1	LED Blue (low active)
P2	LED Red (low active)
P3	LED Green (low active)
P4	PowerGood (low active)
P5	Reset (low active) (but not used)
P6	PowerEnable (low active)
P7	EEprom Write Protect

The EEprom contains any relevant device information (FRU records) about the RTM (refer to PICMG AMC.0). Additionally the EEprom contains the new record types defined in PICMG MTCA.4.

RTM record contains Zone 3 Identifier record listed in the table below.

Supported Zone 3 Identifier Records (Interface Identifier OEM):

IANA PEN (Private enterprise number)	Zone 3 OEM record	Description
0x0092BD (37565)	0x83000001	SIS8300 Zone3 - v1 compatibility
0x0092BD (37565)	0x83000002	SIS8300-L Zone3 - v1 compatibility
0x0092BD (37565)	0x89000001	SIS8900 Zone3 - v1 compatibility

7 Appendix

7.1 Power Consumption

The currents drawn by the SIS8900 are listed in the table below.

Voltage	Current
3,3 V	< 30 mA
12 V	< 1.2 A

These currents are typical values during normal operation.

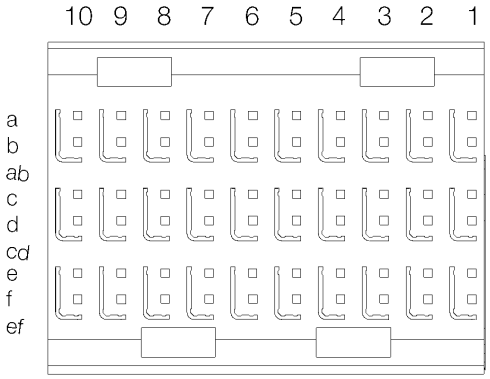
7.2 Ordering options

The SIS8900 is available with two types of coaxial connectors as listed below.

Struck part number	Coaxial Connectors	Manufacturer
00031	EPL.00.250.NTN	LEMO
04290	FBM001P154MR	FCT

7.3 AMC / Zone 3 connectors J101 and J102

J101 and J102 are 90 pin right angle male connectors providing 30 contact pairs each (60 signal contacts and 30 ground contacts). Every contact pair is surrounded by a “L” shaped male shield blade. The shielding contact is designated with the names of the corresponding signal pair (signal pin a and b is affiliated with shielding contact ab e.g.). The scheme below shows the connector contact layout as seen from the rear side of the board.



Front view

7.3.1 J101 connector pin assignments

The J101 connector routes the 10 channels differential analog output signals of the single ended to differential conversion stages and ground to the AMC. The shorthand “TF” in the signal names stands for signals from the AC coupled transformer stages. In the same fashion “PA” stands for the DC coupled operational amplifier stage.

Col → Row ↓	ef	f	e	cd	d	c	ab	b	a
10	GND	CH1_PA-	CH1_PA+	GND	GND	GND	GND	CH1_TF-	CH1_TF+
9	GND	CH2_TF-	CH2_TF+	GND	GND	GND	GND	CH2_PA-	CH2_PA+
8	GND	CH3_PA-	CH3_PA+	GND	GND	GND	GND	CH3_TF-	CH3_TF+
7	GND	CH4_TF-	CH4_TF+	GND	GND	GND	GND	CH4_PA-	CH4_PA+
6	GND	CH5_PA-	CH5_PA+	GND	GND	GND	GND	CH5_TF-	CH5_TF+
5	GND	CH6_TF-	CH6_TF+	GND	GND	GND	GND	CH6_PA-	CH6_PA+
4	GND	CH7_PA-	CH7_PA+	GND	GND	GND	GND	CH7_TF-	CH7_TF+
3	GND	CH8_TF-	CH8_TF+	GND	GND	GND	GND	CH8_PA-	CH8_PA+
2	GND	CH9_PA-	CH9_PA+	GND	GND	GND	GND	CH9_TF-	CH9_TF+
1	GND	CH10_TF-	CH10_TF+	GND	GND	GND	GND	CH10_PA-	CH10_PA+

Note: The front panel print PA channel assignment is correct for SIS8300_V1 and SIS8300-L_V1. The SIS8300_V2 PA channel assignment was optimized for better routing and is in reverse order. PA Channel 1 has changed to PA Channel 10 and so on.

7.3.2 J102 connector pin assignments

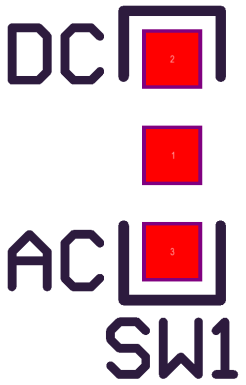
The J102 connector is used to route power, data and system management pins to the AMC board.

Col → Row ↓	ef	f	e	cd	d	c	ab	b	a
10	GND	GND	GND	GND	GND	GND	GND	GND	GND
9	GND	CLK1-	CLK1+	GND	GND	GND	GND	CLK0-	CLK0+
8	GND	GND	GND	GND	CLK2-	CLK2+	GND	GND	GND
7	GND	GND	GND	GND	GND	GND	GND	GND	GND
6	GND	D11-	D11+	GND	D10-	D10+	GND	D9-	D9+
5	GND	D8-	D8+	GND	D7-	D7+	GND	D6-	D6+
4	GND	D5-	D5+	GND	D4-	D4+	GND	D3-	D3+
3	GND	D2-	D2+	GND	D1-	D1+	GND	D0-	D0+
2	GND	nc	nc	GND	SCL	MP+3.3V	GND	PWR+12V	PWR+12V
1	GND	nc	nc	GND	SDA	PS#	GND	PWR+12V	PWR+12V

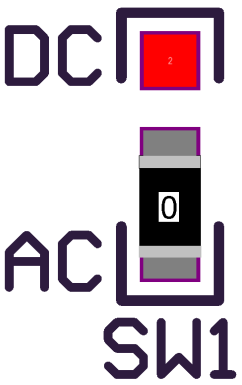
Note: The CLK0, CLK1 and CLK2 signals are referred to as RTM_CLK0, RTM_CLK1 and RTM_CLK2 in the SIS8300/SIS8300-L manual's clock distribution diagram.

7.3.3 AC/DC input stage selection

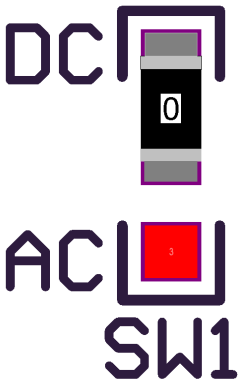
The AC (transformer) or DC (operational amplifier) input path is selected on the SIS8900 card via 0603 solder bridges as illustrated for channel 1 on the screenshots below. Solder bridges are located right beside the analog input coaxial connector on top side of the board.



not configured



AC configured



DC configured

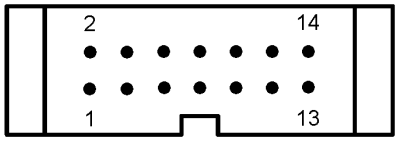
all channels are DC configured by default

The designators of solder bridges for all channels can be found in the table below.

Analog input channel	Designator
1	SW1
2	SW11
3	SW21
4	SW31
5	SW41
6	SW51
7	SW61
8	SW71
9	SW81
10	SW91

7.3.4 J310, J320 connector pin assignments

The connectors J310 and J320 can be used to access buffered LVDS signals of the Zone3 connector. The scheme below shows the contact layout of both connectors.



Top side view

J310 data signals are all inputs (onboard terminated) and buffered towards Zone3 connector. The pin assignment is shown in table below

Pin	Signal
1	DATA0+
2	DATA0-
3	DATA1+
4	DATA1-
5	DATA2+
6	DATA2-
7	GND
8	GND
9	DATA3+
10	DATA3-
11	DATA4+
12	DATA4-
13	DATA5+
14	DATA5-

J320 data signals are all outputs and buffered from the Zone3 connector towards J320. The pin assignment is shown in the table below

Pin	Signal
1	DATA6+
2	DATA6-
3	DATA7+
4	DATA7-
5	DATA8+
6	DATA8-
7	GND
8	GND
9	DATA9+
10	DATA9-
11	DATA10+
12	DATA10-
13	DATA11+
14	DATA11-

J310 and J320 can be connected via flat cable connection to establish a test loop between the lower and upper six data lines. Note, that those data lines are the same lines connected to front panel RJ45 connector J202 via solder bridges. Don't use signals of both connectors at the same time, otherwise serious damage to the SIS8900 and connected cards may result.

Data bits 0,1,2 of J310 can't be used in conjunction of SIS8300-L since there is no connection.
Data bits 9,10,11 of J320 can't be used in conjunction of SIS8300-L. They have connection to signals which aren't under free user control and have other meanings. (See SIS8300-L manual)

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