# SYS7360V3EA

5.25" LITTLE BOARD Single Board Computer For Intel<sup>®</sup> Ultra-Low Voltage Intel<sup>®</sup> Celeron<sup>®</sup> 400MHz

With VGA / Three LANs / Audio

# **User's Manual**

Ver. 0.91

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GRANTECH Industrial CPU card is warranted by GRANTECH Co., Ltd. to be free from defects in material and workmanship for up to one year from the date of purchase by the original purchaser.

Repair will be free of charge only when this device is returned freight prepaid with a copy of the original invoice and a Return Merchandise Authorization to the distributor or the GRANTECH group office from which it was purchased.

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For replacement or repair, return the device freight prepaid, with a copy of the original invoice. Please obtain a Return Merchandise Authorization Number (RMA) from our Sales Administration Department before returning any product.

\* No product will be accepted by GRANTECH group without an RMA number.

# **Caution about Battery**

Danger of explosion if battery is incorrectly replaced.

Replace only with the same or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

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# Chapter 1 Introduction

# 1.1 Specification

• Processor:

SYS7360V3EA: Ultra-Low Voltage Intel<sup>®</sup> Celeron<sup>®</sup> Processor (0.13u) in the Micro FC-BGA package 400MHz, FSB 100MHz at CPU core voltage 0.95V.

- Form Factor: 5.25" little board single card.
- Chipset: VIA CLE266 Chipset (VT8623) + (VT8235).
- Cache Size: On-die primary 16-Kbyte instruction cache and 16-Kbyte write –back data cache and on-die second level cache (256-Kbyte for the ULV Celeron<sup>®</sup> Processor 400MHz) with advanced transfer cache architecture.
- Memory: Up to 512MB DDR SDRAM (PC-100) DIMM.
- **Memory Sockets:** One 184-pin DDR SDRAM socket for SDRAM in 64MB, 128MB, 256MB and 512MB configurations.
- BIOS: Award BIOS, PnP support
  - Flash EEPROM (256KB) for BIOS update
  - Power management
- LPC Super I/O: Winbond W83697UF.
- **Parallel port:** One high-speed parallel port, SPP/EPP/ECP mode
- Series Port: Four 16550 UART ports, COM2 is RS-232/422/485 configurable.
- Enhanced IDE: One EIDE port, up to 2 IDE devices, supports Ultra DMA 33/66/100/133.
- Compact Flash: One CF port support memory card.
- **FDD Interface:** One floppy drives (360KB, 720KB, 1.2MB, 1.44MB, 2.88MB, LS-120)
- USB Interface: One box-header support 2 USB v2.0 ports
- Watchdog Timer: Supper I/O integrate WDT timer and Software programmable active to Reset.

- Hardware Monitor:.
- **Keyboard connector:** One PS/2<sup>®</sup> keyboard connector on bracket and share with mouse and one 6-pins box-header for external keyboard.
- Mouse connector: On bracket PS/2<sup>®</sup> Mouse connector share with keyboard.
- VGA Controller: Integrate VT8623 frame buffer share with system memory.
- VGA Connector: On board 15-pin D-type VGA connector.
- LCD: 40 pin TFT LCD panel digital signal connector.
- LAN: Three Realtek RT8139D controllers, three RJ-45 connector on board.
  - Wake On LAN support, Remote Boot-up
- **RTC:** battery backup by Lithium Battery (CR2032/BR2032)
  - The coin type Lithium battery specification is shown in table

Specification	CR2032	BR2032
Nominal Voltage	3V	3V
Nominal Capacity	220mAh	195mAh
Nominal Weight	3.1g	2.4g

\* The maximum using duration of CR2032/BR2032 Battery is about 3 years at  $20^{\circ}$ C.

# 1.2 Mechanical & Environmental

- POWER CONSUMPTION (Intel ULV Celeron 400 MHz) :
  - ◆ +5VDC @ 5.372A max.
  - ◆ +12VDC @ 0.50A max.
  - ◆ +5VSB @ 1.924A max.

- OPTERATING TEMPERATURE: 0 ~ 55 .
- STORAGE TEMPPERATURE: 40 ~ 80 .
- HUMIDITY: 20% to 90% RH (no condensation)
- Board dimension: 203mm(L) X 146mm(W) / 8"inch X 5.75" inch.

• BOARD WEIGHT: 300 g.

# 1.3 Check List

Please check that your package is complete and contains the items below. If you discover damaged or missing items, please contact your dealer.

- The SYS7360V3EA Industrial PCI CPU board
- This User's Manual & Registration Card
- 1 IDE 80pin Ribbon Cables
- 1 Floppy Ribbon Cable
- Driver disks utilities
- One mounting bracket attached with 1 serial ports & 1 parallel port ribbon cable
- Jumper Short Pin: 15 pcs of pitch 2.0 mm, and 2 pcs of pitch 2.54 mm.
- 6 pin mini-DIN cable (2 in 1 cable for PS/2<sup>®</sup> Mouse & Keyboard function)

# 1.4 Description

The SYS7360V3EA is a PCI compatible Industrial CPU card based on VIA VT8623/VT8235 chipset and is fully designed for harsh industrial environment. It features Intel<sup>®</sup> ULV  $\mu$  FC-BGA series compatible processor. This card accommodates up to 512MB of DDR SDRAM memory.

The SYS7360V3EA comes with CPU integrate temperature sensor to protect your processor from overheating; and wired for Management (WFM) 2.0 specifications compliance.

The SYS7360V3EA has three LAN connectors that use Realtek's RT8139D PCI LAN controller.

The SYS7360V3EA has a LCD connector that uses VT8623 integrate graphic accelerator.

# **1.5 Power Management Features**

### Overview

- Support both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
- ACPI v1.0 compliant
- APM v1.2 compliant
- CPU clock throttling and clock stop control for complete ACPI C0 to C1.
- PCI bus clock run, Power Management Enable (PME) control, all with hardware automatic wake-up
- Multiple suspend power plane controls and suspend status indicators
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Normal, doze, sleep, suspend and conserve modes
- Global and local device power control
- System event monitoring with two event classes
- Primary interrupt differentiation for individual channels

# 1.6 Power Requirements

Your system requires a clean, steady power source for reliable performance of the high frequency CPU on the SYS7360V3EA Industrial CPU card, the quality of the power supply is even more important. For the best performance makes sure your power supply provides a range of 4.75 volts minimum to 5.25 volts maximum DC power source.

### **Power Consumption**

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For typical configurations, the CPU card is designed to operate with at least a 200 W power supply. A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must meet the following requirements:

- Rise time for power supply: 2 ms to 20 ms
- Minimum delay for reset to Power Good: 100 ms
- Minimum Power down warning: 1 ms
- 3.3 V output must reach its minimum regulation level within 20ms of the +5V output reaching its minimum regulation level

The following table lists the power supply's tolerances for DC voltages:

DC Voltage	Acceptable Tolerance
+3.3 V	±5%
+5 V	±5%
+5 VSB (standby)	±5%
+12 V	±5%

1.7 Connector & Jumper Location



# **1.8 Board layout and dimensions**



# **Chapter 2 Hardware Installations**

This chapter provides information on how to use the jumpers and connectors on the SYS7360V3EA in order to set up a workable system.

# 2.1 Installation procedure

- 2.1.1 Insert the DDR DRAM module with correct orientation.
- 2.1.2 Insert all external cables except for flat panel. (Hard disk, floppy, keyboard, Mouse, LAN, etc.)
- 2.1.3 Prepare a CRT monitor for CMOS setup.
- 2.1.4 Confirm CPU card into to PCI back plane.
- 2.1.5 Turn on the power.
- 2.1.6 Enter the BIOS setup mode by pressing 'Del' key during boot up.
- 2.1.7 Use the "Load BIOS Optimal Defaults" feature.
- 2.1.8 Configure the *Peripheral Setup* and the *Standard Setup* correctly.
- Note: The CMOS memory may be in an undefined state at power-on after a period of no battery backup.

# 2.2 Main Memory Installation: DIMM1

The SYS7360V3EA PCI Industrial CPU Card supports one dual inline memory module (DDR SDRAM DIMM 184-pin) socket for a maximum total memory of 512MB on PC100. Using the serial presence detect (SPD) data structure, programmed into an  $E^2$ PROM on the module, the BIOS can determine the size of SDRAM and speed. Minimum memory size is 64MB; maximum memory size is 512MB. Memory size and speed can vary between sockets.

The CPU card supports the following memory features:

- 184-pin DDR SDRAM DIMM with gold-plated contacts
- 100 or 133 MHz DDR SDRAM.
- Non-ECC function support.
- 2.5V memory only.
- Un-buffer single or double-sided DIMM in the following sizes:

### **SDRAM**

SYNCHRONOUS DRAM (SDRAM) improves memory performance through memory access that is synchronous with the memory clock. Burst transfer rates at x-1-1-1 timing can be achieved using SDRAM, while asynchronous memory subsystems are typically limited at x-2-2-2 transfer rates.

The CPU card supports single or double-sided DIMM in the following sizes:

DIMM size	Non-ECC configuration
64MB	8Mbit x 64
128MB	16Mbit x 64
256MB	32Mbit x 64
512MB	64Mbit x 64

### **CHAPTER 2** – Hardware Installations

**Note:** All memory components and DIMM used with the SYS7360V3EA PCI CPU card must comply with the PC SDRAM Specification. These include: the PC SDRAM Specification \*memory component specific), the PC Un-buffered DIMM Specification, and the PC Serial Presence Detect Specification.

# 2.3 Serial Port connector: CN34 (COM1~COM4)

COM1~COM4 (CN34) is a 40-pins box-header; cable with D-sub connector . The following table shows the pin assignments of these connectors.

\*\* 4 serial ports on board supports with-out ISA bridge(  $\mathrm{PC}/\mathrm{104})$  model only

### The CN34 pin assignment:

CN34	PIN	PIN	PIN	PIN	RS-232
	1	11	21	31	DCD
1 2	2	12	22	32	DSR
	3	13	23	33	SIN
	4	14	24	34	RTS
	5	15	25	35	SOUT
	6	16	26	36	CTS
	7	17	27	37	DTR
39 8 8 40	8	18	28	38	RIN
	9	19	29	39	GND
	10	20	30	40	N.C

		JP15 JP16
	СОМ1	
	COM2	JP19 JP17
Ring-in	СОМЗ	JP23 JP20
	COM4	JP24 JP21
	СОМІ	JP15 JP16
+5V	СОМ2	JP19 JP17
	СОМЗ	JP23 JP20 JP23 JP20 JP23 JP20 JP23 JP20 JP23 JP20 JP23 JP20 JP23 JP20
	СОМ4	JP24 JP21
	СОМІ	JP15 JP16 JP15 JP16 JP15 JP16 JP15 JP16 JP15 JP16
+12V	СОМ2	JP19 JP17
	СОМЗ	
	СОМ4	JP24 JP21

#### Pin 8,18,28.38 ring-in signal & power option

#### RS422/485 assigned for COM2 connector only

	PIN	RS-232	RS422	RS485
	1	DCD	TX-	TX-
COM2 D-SUB	2	RXD	TX+	TX+
	3	TSD	RX+	RX+
123(5	4	DTR	RX-	RX-
000000	5	GND	GND	GND
6789	6	DST	RTS-	N.C
	7	RTS	RTS+	N.C
	8	CTS	CTS+	N.C
	9	RI	CTS-	N.C
	10	N.C	N.C	N.C

Note:

- For RS-485, TX+(pin 2) and RX+ (pin 3) must jumper together inside the D type connector.
- *TX- (pin 1) and RX- (pin 4) is the same.*

### 2.3.1 RS-422 / RS-485 specifications

- Transmission system: Asynchronous, half-/full-duplex serial transmission conforming to RS-422/RS-485
- Baud rate: 19200 to 50bpx (programmable)
- Signal extensible distance: 1.2km Max.

*Note:* The mouse and keyboard can be plugged into either PS/2 connector. Power to should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains code which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del>, software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power On Self Test (POST).

## 2.4 TV\_OUT :CN26

The Video port function by RCA Video or S/SPDIF The pin assignments are as follows

CN26		Function
2	1	TV_OUT
	2	TV_GND

# 2.5 VGA Connector: CN2

It is a VGA CRT connector (DB-15). The pin assignments are as follows:

	PIN No.	Function	PIN No.	Function
CN2	1	RED	9	N.C
	2	GREEN	10	GND
	3	BLUE	11	D-DATE
	4	N.C	12	N.C
	5	GND	13	H-SYNC
	6	GND	14	V-SYNC
	7	GND	15	D-DCLK
	8	GND		

# 2.6 RJ-45 LAN connector: CN4,CN6,CN7

These connectors are for the 10/100Mbps Ethernet capability of the CPU card. The follow table shows the pin assignments of these connectors.

• The category-5 cable is required for transmission at 100Mbps.



# 2.7 PS/2 Keyboard/Mouse Connector: CN12

The CPU board provides a 6pins box-header connector for attaching the PS/2<sup>®</sup> mouse or keyboard. The Connector pin definition is shown below:

	PIN No.	Function
	1	+5VSB
0	2	MS Clock
	3	MS Data
	4	KB Clock
6	5	KB Data
	6	GND

When used with an ATX-compliant power supply that supports remote power on/off, the CPU card can turn off the system power through software control.

To enable soft-off control in software, advanced power management must be enabled in the Setup program and in the operation system. When the system BIOS receives the correct APM command from the operating system, the

BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

# 2.8 USB Connector: CN32,CN33.CN5

The Universal Serial Bus (USB) that allows plug and play computer peripherals such as legacy keyboard, PS/2 mouse, scanner, printer, modem/ISDN, and floppy disk drive to be automatically detected when they are attached physically without having to install drivers or reboot.

The USB connectors allow any of several USB devices to be attached to the computer. Typically, the device driver for USB devices is managed by the operating system. However, because keyboard and mouse support may be needed in the Setup program before the operating system boots, the BIOS support USB keyboards

The CPU card has three USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back panel connectors. The CPU card fully supports the universal host controller interface (UHCI) v1.1 compatible and uses enhanced host controller interface (EHCI) v1.0 compatible software drivers and USBv2.0.

USB features includes:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for synchronous and asynchronous transfer types over the same set of wires
- Support three root hubs and six function ports.

### **CHAPTER 2** – Hardware Installations

- Guaranteed bandwidth and low latencies appropriate for telephony, audio and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

**Note:** Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class A requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

		CN5		CN33
	Fin No.	Function	FIN NO.	Function
	1	5VSB	1	5VSB
6	2	USBD2-	2	USBD4-
	3	USBD2+	3	USBD4+
	4	USBD3-	4	USBD5-
	5	USBD3+	5	USBD5+
	6	GND	6	GND

		CN32		CN32
	PIN NO.	Function	PIN NO.	Function
5 8	1	5VSB	5	5VSB
	2	USBD0-	6	USBD1-
	3	USBD0+	7	USBD1+
	4	GND -	8	GND -

# 2.9 Parallel Port Connector: CN15

The parallel port bracket can used to add an additional parallel port for additional parallel devices. There are four options for parallel port operation:

- Compatible (Standard mode)
- Bi-Directional (PS/2 compatible)
- Bi-Directional EPP. A driver from the peripheral manufacturer is required for operation.
- Bi-Directional High-speed ECP

	CN4	F	PIN No.	Function	PIN No.	Function
CN15		1	STROBE	2	ALF	
1		2	3	PD0	4	ERROR
	00		5	PD1	6	INIT
	00		7	PD2	8	SLCT IN
			9	PD3	10	GND
	00		11	PD4	12	GND
	00		13	PD5	14	GND
			15	PD6	16	GND
	00		17	PD7	18	GND
	00		19	ACK	20	GND
25		26	21	BUSY	22	GND
20	ĽŬ	20	23	PE	24	GND
			25	SLCT	26	N.C

# 2.10 Floppy Disk Connector: CN14

The floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

This connector supports the provided floppy drive ribbon cable. After connecting the single and to the board, connect the two plugs on the other end to the floppy drives.

	PIN No.	Function	PIN No.	Function
CN14	1	GND	2	RWC
	3	GND	4	N.C
	5	GND	6	N.C
	7	GND	8	INDEX
0 0	9	GND	10	DS0
00	11	GND	12	DS1
	13	GND	14	DS2
000	15	GND	16	MOT ON
00	17	GND	18	DIR
00	19	GND	20	STEP
	21	GND	22	WD
00	23	GND	24	WG
00	25	GND	26	TRCK 0
0 0	27	GND	28	WP
	29	GND	30	RD
	31	GND	32	SIDE 1
33 34	33	GND	34	DSK CHG

# 2.11 LCD Connector: CN19

CN10 is a 40-pin connector (Panel link) for flat panel LCD display. The following shows the pin assignment of this connector.

	0000000000	000000000			
L L					
	2 40				
PIN NO.	Function	PIN NO.	Function		
1	DP20	2	GND		
3	DP16	4	VCC		
5	DP21	6	DP0		
7	DP17	8	DP8		
9	DP22	10	DP1		
11	DP18	12	DP9		
13	DP23	14	DP2		
15	DP19	16	DP10		
17	VCC	18	DP3		
19	FLM	20	DP11		
21	MX	22	DP4		
23	LP	24	DP12		
25	GND	26	DP5		
27	SHFCLK	28	DP13		
29	3.3V	30	DP6		
31	3.3V	32	DP14		
33	ENABLK	34	DP7		
35	LCDVDD	36	DP15		
37	ENVEE	38	+12V		
39	GND	40	+12V		

# 2.12 External Battery Connector: CN1

It is a 2 Pin connector used for external battery. An external battery power for used of real-time clock and CMOS memory.

CN11	PIN No.	Function
	1	GND
	2	External battery (3V)

# 2.13 Audio Signal connector: CN23

	CN23		PIN No.	Function	PIN No.	Function
1		2	1	LINE-OUT	2	LINE-OUT
	00			-R	2	-L
	00		3	GND	4	GND
			5	NC	6	MICIN
9		10	7	GND	8	GND
			9	LINE-IN-R	10	LINE-IN-L

# 2.14 CD Audio connector: CN24

This connector is used to connect CD Audio cable from CD-ROM or

DVD drive to onboard sound.

	PIN No.	Function
CN24	1	Audio-L
	2	GND
1234	3	GND
	4	Audio-R

# 2.15 Primary /Seconadry IDE port Connector: CN22 (2x40 2.54mm Box Header)/ CN11(2x22 2.0mm Box Header)

The CPU card SYS7360V3EA has two independent bus-mastering PCI IDE interfaces. Transfer rate up to 133MB/sec to cover PIO mode 4, multi-word DMA mode 2 drivers, and UltraDMA133 interface, and increased reliability using Ultra DMA-133/100/66 transfer protocols. The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

Programmed I/O operations usually require a substantial amount of processor bandwidth. However, in multitasking operating systems, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

These connectors support the provided IDE hard disk ribbon cable. After connecting the single end to the board, connect the two plugs at the other end to your hard disk(s). If you install two hard disks, you must configure the second drive to Slave mode by setting its jumper accordingly. Please refer to your hard disk documentation for the jumper setting. **CHAPTER 2** – Hardware Installations

	PIN No.	Function	PIN No.	Function
CN22	1	RESET	2	GND
	3	D7	4	D8
1 0 2	5	D6	6	D9
	7	D5	8	D10
00	9	D4	10	D11
00	11	D3	12	D12
00	13	D2	14	D13
	15	D1	16	D14
00	17	D0	18	D15
00	19	GND	20	N.C
00	21	DREQ	22	GND
	23	IOW	24	GND
00	25	IOR	26	GND
0 0	27		28	ALE
00	29	DACK	30	GND
0 0	31	IRO	32	100.516
	33	Δ1	34	PDIAG
39 0 0 40	35	<u> </u>	36	1 DIAG
	37		38	CS1
	30		40	GND
		Function		Lunction
CN11	PIN NO.	Function	PIN NO.	GND
CN11	1 3	Function RESET D7	2 4	GND D8
CN11 1 0 2	PIN NO. 1 3 5	Function RESET D7 D6	PIN NO. 2 4 6	GND D8 D9
CN11 1 0 2	1 3 5 7	Function RESET D7 D6 D5	PIN NO. 2 4 6 8	GND D8 D9 D10
CN11 1 0 2 0 0 0 0 0 0	PIN NO. 1 3 5 7 9	Function RESET D7 D6 D5 D4	PIN No. 2 4 6 8 10	GND D8 D9 D10 D11
CN11 1 0 2 000 000 000	PIN NO. 1 3 5 7 9 11	Function RESET D7 D6 D5 D5 D4 D3	PIN No.           2           4           6           8           10           12	Function           GND           D8           D9           D10           D11           D12
CN11 1 0 2 0 0 0 0 0 0 0 0 0	1 3 5 7 9 11 13	Function           RESET           D7           D6           D5           D4           D3           D2	PIN No.           2           4           6           8           10           12           14	Function           GND           D8           D9           D10           D11           D12           D13
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0	1 3 5 7 9 11 13 15	Function           RESET           D7           D6           D5           D4           D3           D2           D1	PIN No.           2           4           6           8           10           12           14           16	Function           GND           D8           D9           D10           D11           D12           D13           D14
CN11 1 0 2 0000000000000000000000000000000	PIN NO.           1           3           5           7           9           11           13           15           17	Function           RESET           D7           D6           D5           D4           D3           D2           D1           D0	PIN No.           2           4           6           8           10           12           14           16           18	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19	Function           RESET           D7           D6           D5           D4           D3           D2           D1           D0           GND	PIN No.           2           4           6           8           10           12           14           16           18           20	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21	Function           RESET           D7           D6           D5           D4           D3           D2           D1           D0           GND           DREQ	PIN No.           2           4           6           8           10           12           14           16           18           20           22	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           OND
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23	Function           RESET           D7           D6           D5           D4           D3           D2           D1           D0           GND           DREQ           IOW	PIN No.           2           4           6           8           10           12           14           16           18           20           22           24           20	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           GND           GND
CN11 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25	Function           RESET           D7           D6           D5           D4           D3           D2           D1           D0           GND           DREQ           IOW           IOR	PIN No.           2           4           6           8           10           12           14           16           18           20           22           24           26	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           GND           GND
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25           27           29	Function RESET D7 D6 D5 D4 D3 D2 D1 D0 GND DREQ IOW IOR IOR IOR V	PIN No.           2           4           6           8           10           12           14           16           18           20           22           24           26           28           30	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           GND           GND           GND           GND
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25           27           29           31	Function RESET D7 D6 D5 D4 D3 D2 D1 D0 GND DREQ IOW IOR IOR IORDY DACK IRO	PIN NO. 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           GND           GND           GND           GND           GND           GND           GND           GND           ALE           GND           IOCS16
CN11 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25           27           29           31           33	Function RESET D7 D6 D5 D4 D3 D2 D1 D0 GND DREQ IOW IOR IOR IORDY DACK IRQ A1	PIN NO.           2           4           6           8           10           12           14           16           18           20           22           24           26           28           30           32           34	Function         GND         D8         D9         D10         D11         D12         D13         D14         D15         N.C         GND         GND         GND         GND         GND         ALE         GND         IOCS16         PDIAG
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25           27           29           31           33           35	Function RESET D7 D6 D5 D4 D3 D2 D1 D0 GND GND GND IOR IOR IOR IOR IOR IOR IOR IOR A1 A0	PIN NO.           2           4           6           8           10           12           14           16           18           20           22           24           26           28           30           32           34           36	FunctionGNDD8D9D10D11D12D13D14D15N.CGNDGNDGNDGNDALEGNDIOCS16PDIAGA2
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25           27           29           31           33           35           37	Function           RESET           D7           D6           D5           D4           D3           D2           D1           D0           GND           DREQ           IOW           IOR           IORDY           DACK           IRQ           A1           A0           CS0	PIN NO.           2           4           6           8           10           12           14           16           18           20           22           24           26           28           30           32           34           36           38	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           GND           GND           GND           ALE           GND           IOCS16           PDIAG           A2           CS1
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25           27           29           31           33           35           37           39	Function           RESET           D7           D6           D5           D4           D3           D2           D1           D0           GND           DREQ           IOW           IOR           IORDY           DACK           IRQ           A1           A0           CS0           HD ACT	PIN NO.           2           4           6           8           10           12           14           16           18           20           22           24           26           28           30           32           34           36           38           40	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           GND           GND           ALE           GND           IOCS16           PDIAG           A2           CS1           GND
CN11 1 0 2 0 0 0 0 0 0 0 0 0 0 0	PIN No.           1           3           5           7           9           11           13           15           17           19           21           23           25           27           29           31           33           35           37           39           41	Function RESET D7 D6 D5 D4 D3 D2 D1 D0 GND DREQ IOW IOR IOR IOR IOR IOR VCC	PIN NO.         2         4         6         8         10         12         14         16         18         20         22         24         26         28         30         32         34         36         38         40         42	Function           GND           D8           D9           D10           D11           D12           D13           D14           D15           N.C           GND           GND           GND           ALE           GND           IOCS16           PDIAG           A2           CS1           GND           VCC

# 2.16 Front Panel Connector: CN21

This header can be connected to a front panel power switch. The front panel connector includes headers for these I/O connections: Power / Suspend LED

This header can be connected to an LED that will light when the computer is powered on and LED flash when OS into standby mode. *HDD LED* 

This header can be connected to an LED to provide a visual indicator that data is being read from or written to an IDE hard drive. For the LED to function properly, the LED drive must be connected to the onboard IDE controller.

## Speaker

A external speaker can be installed on the SYS7360V3EA as a manufacturing option. The external speaker enabled by connect 4 pin hosing connector to external speaker on pins 9, 11, 13, 15 of the front panel connector. The onboard speaker can be removed by mounting optional, and an off board speaker can be connected in its place. The speaker (onboard or off board) provides error beep code information during the POST in the event that the computer cannot use the video interface.

	PIN No.	Sign name	PIN No	. Sign name
CN21	1	Power BT	2	VCC
1 0 2	3	GND	4	IDE ACT
$3 \circ \circ 4$	5	RESET	6	NC
7 0 8	7	GND	8	VCC
9 0 0 10	9	VCC	10	VCC
$11 0 0 12 \\ 13 0 0 14$	11	GND	12	For GPO0
15 16	13	GND	14	NC
	15	BUZZER	16	NC
Speaker	9, 11, 13, 15	Power Bu	tton	1, 3
Reset Button	5, 7	HDD LED		2, 4
Power LED	10, 12			

### CHAPTER 2 -Hardware Installations



## 2.17 External ATX control Power Connector: CN22

CN22	PIN No.	Function	Housing:
	3	5V SBY	XHP-3 (JST)
3 O 2 O	2	PS-ON (soft ON/OFF)	
1	1	GND	

# 2.18 Compact Flash Connector: CN9

The CPU card SYS7360V3EA provides a Compact lash interfaces. This interface is a very small removable mass storage device. It provides compatibility plus True IDE functionality compatible with ATA/ATA-4.

CHAPTER 2	2 –Hardware	Installations
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			PIN No.	Function	PIN No.	Function
	CN9		1	GND	2	D3
		1	3	D4	4	D5
1		2	5	D6	6	D7
	00		7	CS0	8	A102
			9	ATASEL#	10	A092
	00		11	A082	12	A072
	00		13	VCC	14	A062
	00		15	A052	16	A042
			17	A032	18	A02
	00		19	A01	20	A00
	00		21	D0	22	D1
	00		23	D2	24	IOCS16
			25	CD2#	26	CD1#
	00		27	D111	28	D121
	00		29	D131	30	D141
	00		31	D151	32	CS11
			33	VS1#	34	IOR
	00		35	IOW	36	WE3#
	00		37	INTQ	38	VCC
	00		39	CSEL#	40	VS2
			41	RESET	42	IORDY
40	00	50	43	INPACK	44	REG3#
49		50	45	DASP#	46	PDIAG
			47	D081	48	D091
			49	D101	50	GND

# 2.19 System FAN Connector: FAN2

FAN2 is a 3-pins box-header for the system cooling fan power connector. The fan must be a 12V fan. Pin 3 is for Fan speed sensor input. Pin 2 is for +12V power supply.

	PIN No.	Function	Connector type for Cable
1 <b>FAN2</b>	1	GND	
2 0	2 +	+12V	Housing: 5102-03 (molex) Contact: 5103 (molex)
Ľ]	3	FAN sense	

# CN27 GPIO PORT 2X5 2.0mm Pin Header

TTL level bi-directional pin ,internal pull Hi +5V

CN27	PIN No.	Sign name	PIN No.	Sign name
1 0 2	1	DI-0	2	DO-0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	3	DI-1	4	DO-1
7 0 0 8 9 0 0 10	5	DI-2	6	DO-2
	7	DI-3	8	DO-3
	9	GND	10	GND

Smbus ID = 30h Smbus Port = 5000h

GPI24 connect GPO12 GPI23 connect GPO13 GPI11 connect GPO14 GPI10 connect GPO15

Program GPIO Function:

1. Input/Output Configuration Register setting.

2. Polarity Inversion Register setting.

3. Send Output port Data or Check Input port Data.

Program Smbus Write:

- 1. Check Smbus Busy
- 2. Set Smbus Port + 4 = ID (30h)
- 3. Set Smbus Port + 3 = Inedx
- 4. Set Smbus Port + 5 = Write Date
- 5. Set Smbus Port + 2 = Write Command(48h)

Program Smbus Read:

1. Check Smbus Busy

- 2. Set Smbus Port + 4 = ID (31h)
- 3. Set Smbus Port + 3 = Inedx
- 4. Set Smbus Port + 2 = Write Command(48h)
- 5. Get Date = Smbus Port + 5

# **Chapter 3 Jumper Setting**

# 3.1 RS-422/485 Terminator: JP13

JP13	Terminator	Function
JP13 1 0 0 2 3 0 0 4 5 0 0 6 7 0 8	-	No terminating resister (Default)
JP13 1 2 3 0 0 4 5 0 0 6 7 0 0 8	CTS for RS-422	terminating resister provided
JP13 1 ○ ○ 2 3 ● 4 5 ○ ○ 6 7 ○ ○ 8	RTS for RS-422	terminating resister provided
JP13 1 0 0 2 3 0 0 4 5 ■ 6 7 0 0 8	RXD for RS-422/485	terminating resister provided
JP13 1 0 0 2 3 0 0 4 5 0 0 6 7 8	TXD for RS-422/485	terminating resister provided

# 3.2 RS232/422/485 Selector: JP14/JP18



## Transmit date control in half-duplex mode

In half-duplex mode, the transmission buffer must be controlled to prevent transmit data from causing a collision. The SIS-8600-LV uses the RTS signal and bit 1 in the modem control register to control transmit data.

### Modem control register

(Setting I/O address +4H) bit 1: 0 ... RTS High (Disables transmission)

1 ... RTS low (Enables transmission)

### Setting the RS-422/RS-485 receiver disable control jumper

When the RS-422/RS-485 port is used, the RTS signal is used for driver enable control Connecting JP1 Pins 4 and 6 disables the receiver at the same time, preventing the port from receiving output data to an external device.



CHAPTER 3 – Jumper Setting



### I/O addresses and instructions

The table below lists I/O addresses for use as COM2.

I/O address	DLAB	Read/Writ e	Register	
	0	W	Transmitter holding Register	THR
02F8H	0	R	Receiver buffer Register	RBR
	1	W	Divisor latch Register (LSB)	DLL
	1	W	Divisor latch Register (MSB)	DLM
02F9H	0	W	Interrupt enable Register	IER
02FAH	Х	R	Interrupt ID Register	IIR
02FBH	Х	W	Line control Register	LCR
02FCH	Х	W	Modem Control Register	MCR
02FDH	Х	R	Line status Register	LSR
02FEH	Х	R	Modem Status Register	MSR
02FFH	Х	R/W	Scratch Register	SCR

# 3.3 ATX/AT Power supply select: JP1, JP22

In case for different type of power supply, the user needs setting up these jumpers for more system stability.

JP1	JP22	Function
JP8 0 1 2 3	JP17 I 0 1 2 3	ATX
JP8 0	JP17 0	AT

# 3.4 CF Master / Slave selector: JP8

JP8	Function
JP8	Set to Master
JP8 □ O	Set to Slave

# 3.5 Clear CMOS Content: JP2

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program. The RAM data contains the password information is powered by the onboard button cell battery. User can erase the CMOS memory content by short pin2 and pin3 of JP16 together.

An external coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of eight years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to  $\pm 1$  minutes/month at 25°C with 3.3V applied.

JP2	Function
JP2	Normal Operation (Default)
JP2	Clear CMOS Content

# Chapter 4 CPU card Resources

# 4.1. I/O MAP

Address (hex)	Description
00-1F	DMA Controller
20-3F	Interrupt Control (PIC)
40-5F	Timer / Counter
(60h)	KBC Data
(61h)	Misc Function & Speaker Ctrl
(64h)	KBC Command / Status
70-77	RTC/CMOS/NMI-Disable
78-7F	-available for system use-
80	-reserved- (debug port)
81-8F	DMA Page Registers
90-91	-available for system use-
92	System Control
93-9F	-available for system use-
A0-BF	Slave Interrupt Controller
C0-DF	Slave DMA Controller
E0-FF	-available for system use-
100-CF7	-available for system use-
CF8-CFB	PCI Configuration Address
CFC-CFF	PCI Configuration Data
D00-FFFF	-available for system use-

# 4.2. MEMORY MAP

Address Range (H)	Size	Description
100000-18000000	383MB	Extended memory
E8000-FFFFF	96KB	System BIOS
E0000-E7FFF	32KB	System BIOS (Available as UMB)
C8000-DFFFF	96KB	Available high DOS memory (open to ISA and PCI buses)
A0000-C7FFF	160KB	Video memory and BIOS
00000-9FFFF	640KB	Conventional memory

# 4.3. DMA Channels

DMA	Data Width	System Resources
0	8 or 16bits	Audio
1	8 or 16bits	Audio / parallel port
2	8 or 16bits	Diskette drive
3	8 or 16bits	Parallel port (for ECP) /audio
4		Reserved – cascade channel
5 16bits		Open
6	16bits	Open
7	16bits	Open

# 4.4. Interrupters

IRQ #	System Resources		
NMI	I/O Channel check		
0	Reserved, interval timer		
1	Reserved, keyboard controller		
2	Reserved, cascade interrupt from slave PIC		
3	COM2*		
4	COM1*		

IRQ #	System Resources
5	LPT2 (Plug and Play option) /audio/user available
6	Diskette drive controller
7	LPT1*
8	Real time clock
9	User available
10	USB/User available
11	Windows Sound System/User available
12	PS/2 mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

• \* Default, but can be changed to another IRQ

# **Chapter 5 Software Utilities**

This chapter introduces the software utilities supplied for SYS7360V3EA which including a 10/100M Ethernet driver, VIA Apollo CLE266 VT8623/VT8235 chipset VIA Service Pack (VIA 4 In 1) / Graphics drivers for CRT/Flat Panel Driver and watchdog function configuration utility.

# 5.1. VIA CLE266 VT8623/VT8235 chipset Driver

VIA Service Pack (VIA 4 In 1)

VIA Service Pack (VIA 4 In 1) is Copyright(C) 1999 VIA Technologies, Inc.

Table of Contents:

- About VIA 4 In 1
- Setting Up
- Update
- Technical Support
- Special Note (WinFast AGP VGA users only)

About VIA 4 In 1:

VIA 4 In 1 driver includes four system drivers to improve the performance and maintain the stability of systems using VIA chipsets. These four drivers are:

- VIA Registry (INF) Driver
- VIA AGP VxD driver, VIA ATAPI Vendor Support Driver
- VIA PCI IRQ Mini port Driver. For Windows NT users
- VIA IDE Bus Mastering driver is the only driver to be installed in your system.

VIA Registry (INF) Driver is to be installed under Windows. The driver will enable the VIA Power Management function.

VIA AGP VxD Driver is to be installed if you are using an AGP VGA device.

#### CHAPTER 5 – Software Utilities

VIAGART.VXD will provide service routines to your VGA driver and interface directly to hardware, providing fast graphical access.

The ATAPI IDE driver enables the performance enhancing bus mastering functions on ATA-capable Hard Disk Drives and ensures IDE device compatibility.

VIA PCI IRQ Mini port Driver is to be installed under Windows 98 only, it sets the system's PCI IRQ routing sequence.

### Setting Up:

You may Install and Uninstall VIA driver by selecting the proper options.

- **Step 1:** To setup the driver, double click the "SETUP.EXE" icon or run "SETUP.EXE" under VIA 4 In 1 Driver directory.
- Step 2: Bypass the "Welcome" dialog by clicking "Next"
- Step 3: In "Select Component" dialog, choose driver(s) you wish to install by clicking the check box of each driver. Selected driver(s) will display tick(s). After selecting proper driver(s), click next

Step 4: Driver options select

### VIA ATAPI Vendor Support Driver dialog:

Install

Uninstall

Enable/Disable DMA Mode

### VIA\_GART AGP Driver

Install VIA AGP VxD in turbo mode

Install VIA AGP VxD in Normal Mode

Uninstall

### Viamach.INF

Install

CHAPTER 5 – Software Utilities

### VIA PCI IRQ Miniport Driver

Install, Uninstall

Step 5: Reboot system to complete driver setup process

# 5.2. Graphic Driver

### Introduction

The CPU card SYS7360V3EA is integrated VGA controller for VGA / LCD designs.

### **Driver** Support

- Windows 95
- Windows 98
- Windows NT4.0
- Windows 2000
- Windows XP

# 5.3. LAN Driver

### Introduction

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The CPU card SYS7360V3EA is adopted the Realtek RTL8139D for PCI bus LAN designs.

The LAN DRIVER file is base driver set for all major operating systems, including drivers for DOS, Netware server, and WIN9x.

## Before install the LAN utilities please refer to the files \*.txt in the subdirectory \info\ first.

# 5.4. Update new version BIOS

- Steps 1: Make a record of your original or existing BIOS Setup parameters. Press [Del] during the Power-On-Self-Test to enter BIOS Setup Program and write down the value of each parameter in order to re-configure your System after BIOS updating
- Step 2: Make a System Disk. Put a 3.5" disk in Drive A. For MS-DOS, Key in "format a:/s" and press [Enter]. For Windows, select My Computer, click 3.5" Floppy (A:), select File/Format from Command Bar. On the "Format 3.5" Floppy (A:) " menu, select "Copy system files" and then click [Start] button.
- Step 3: Download the updated BIOS bin file from web site.
- Step 4: Copy the updated BIOS bin file and awdflash.exe file to the System Disk.
- Step 5: Put the System Disk in Drive A and re-start your computer from Drive A.
- Step 6: Begin to update your BIOS. Enter [awdflash] command, the "Flash Memory Writer" message will appear on screen. Enter the updated BIOS file name at "File Name to Program:". Enter the backup file name for the existing BIOS at "File Name to Save:". Press [Y] to proceed with the BIOS updating.
- Step 7: Re-configure your system. Remove the System Disk and re-start your computer. Press [Del] during the Power-On-Self-Test to enter BIOS Setup Program. Reset the relevant parameters according to your record of the Original setting. Save and Exit BIOS Setup program to re-boot your system.

# 5.5. Hardware Monitor

Hardware Monitor function is included in Hardware Monitor controller of W83697HF on SYS7360V3EA.

The watchdog timer serves as a safeguard against possible system lock-up in your industrial computer system. In most industrial environments, there are heavy equipment, generators, high-voltage power lines, or power drops that have adverse effects on your computer system. For instance, when a power drop occurs, it could cause the CPU to come to a halt state or enter into an infinite loop, resulting in a system lock-up.

With the watchdog timer enabled, a RESET can be automatically generated unless the CPU periodically triggers the timer within the time-out interval. That is, while the system gets hung up, the running program can't trigger the timer periodically. The timer will generate a reset signal to reboot the system. This feature allows a running program to restart in an orderly way when a power glitch or any abnormal condition occurs.

The watchdog timer comes with 255-level time-out interval, 1 to 255 seconds per interval, which can be adjusted by software setting. There is a tolerance of 2 second for this time-out interval. For example, if the time-out interval has been set to 32 seconds, your program should trigger the watchdog timer before 28 seconds are escaped. Otherwise, after 28-32 seconds are escaped, the system will automatically reboot. To keep the system running normally, your program should trigger the watchdog timer every 28 seconds.

The I/O port is defined at address 2eH. You can trigger/enable disable the timer by writing port2e.

Here is a example for programming Watch dog timeout in "debug" mode if your IO program address is 2E:

o 2e 87 o 2e 87 o 2e 2b (setting multiplexed pin to be WDTO function) o 2f d0 o 2e 07 o 2f 08 o 2e f5 o 2f 08( unit for minute) or 0(unit for second) o 2e f6 o 2f xx (any value by user select) o 2e 30 o 2f 01 when time-out even occur you may watch the status register o 2e f7 i 2f if you want to disable WDTO o 2e f6 o 2f 00

**Note:** The timer's intervals have a tolerance of  $\pm 2$  seconds.

You can read Temperature, Voltage and Fan Sensor output of SBC.

5.6.1. Temperature

Two Thermistors are mounted on SBC as following. You can read Temperature of this position.

### 5.6.2. Voltage

You can read 3.3V, +5V, +12V, Vcore, VBAT of SBC. Vcore: CPU core voltage VBAT: Battery voltage.

5.6.3. Speed Sensor

FAN Speed Sensor signal is input in CN1, 2 of pin3 when you use CPU or

SYSTEM FAN with speed sensor.

You can read FAN speed.

## <Caution>

You mast use FAN with speed sensor if you would like to read FAN Speed.

# Chapter 6 BIOS Setup

# 6.1. Introduction

This chapter discusses Award's Setup program built into the FLASH ROM BIOS. The Setup program allows users to modify the basic system configuration. This special information is then stored in battery-backed RAM so that it retains the Setup information when the power is turned off.

The rest of this chapter is intended to guide you through the process of configuring your system using Setup.

## **Starting Setup**

The Award BIOS is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

- 1. By pressing <Del> immediately after switching the system on, or
- by pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self-Test).

## Press DEL to enter SETUP.

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed

and you will again be asked to ...

Press F1 to continue, DEL to enter SETUP

## **Using Setup**

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Key	Function
Up Arrow	Move to the previous item
Down Arrow	Move to the next item
Left Arrow	Move to the item on the left (menu bar)
Right Arrow	Move to the item on the right (menu bar)
	Main Menu: Quit without saving changes
Esc	Submenus: Exit Current page to the next higher level menu
Move Enter	Move to the item you desired
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
	Main Menu Quit and not save changes into CMOS
Esc key	Status Page Setup Menu and Option Page Setup Menu Exit current page and return to Main Menu
F1 key	General help on Setup navigation keys
F5 key	Load previous values from CMOS
F6 key	Load the fail-safe defaults from BIOS default table
F7 key	Load the optimized defaults
F10 key	Save all the CMOS changes and exit

## **Getting Help**

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

## In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS<sup>TM</sup> supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

## A Final Note About Setup

The information in this chapter is subject to change without notice.		
Phoenix - Hwardbius		
► Standard CMOS Features	► Frequency Control	
► Advanced BIOS Features	Load Fail-Safe Defaults	
► Advanced Chipset Features	Load Optimized Defaults	
► Integrated Peripherals	Set Supervisor Password	
▶ Power Management Setup	Set User Password	
► PnP/PCI Configurations	Save & Exit Setup	
► PC Health Status	Exit Without Saving	
Esc : Quit F9 : Menu in BIOS ↑↓ → ← : Select Item F10 : Save & Exit Setup		
Time, Date, Hard Disk Type		

# 6.2. Main Menu

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Once you enter the Award BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu. Note that a brief description of each highlighted selection appears at the bottom of the screen.

### Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

## Standard CMOS Features

Use this menu for basic system configuration.

## Advanced BIOS Features

Use this menu to set the Advanced Features available on your system.

## Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system's performance.

## **Integrated Peripherals**

Use this menu to specify your settings for integrated peripherals.

## Power Management Setup

Use this menu to specify your settings for power management.

## PnP / PCI Configuration

This entry appears if your system supports PnP / PCI.

## Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

## Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

### Supervisor / User Password

Use this menu to set User and Supervisor Passwords.

## Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

## Exit Without Save

Abandon all CMOS value changes and exit setup.

# 6.3. Standard CMOS Setup

Phoenix - AwardBIOS CMOS Setup Utility Standard CMOS Features

Date (mm:dd:yy) Time (bb:mm:ss)	Thu, Jan 1 2001	Item Help
<ul> <li>IDE Primary Master</li> <li>IDE Primary Slave</li> <li>IDE Secondary Master</li> <li>IDE Secondary Slave</li> </ul>	[ None] [ None] [ None] [ None] [ None]	Menu Level ► Change the day, month, year and century
Drive A Drive B	[1.44M, 3.5 in.] [None]	
Video Halt On	[EGA/VGA] [All , But Keyboard]	
Base Memory Extended Memory Total Memory	640K 64512K 65536K	
<pre>↑1→+:Move Enter:Select</pre>	+/-/PU/PD:Value F10:Save	ESC:Exit F1:General Help

F5: Previous Values F6: Fail-Safe Defaults F7: O timized Defaults

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.

## Main Menu Selections

This table shows the selections that you can make on the Main Menu

Item	Options	Description
Date	Month DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Primary Master	Options are in its sub menu(described in Table 64)	Press <enter> to enter the sub menu of detailed options</enter>
IDE Primary Slave	Options are in its sub menu(described in Table 64)	Press <enter> to enter the sub menu of detailed options</enter>
IDE Secondary Master	Options are in its sub menu(described in Table 64)	Press <enter> to enter the sub menu of detailed options</enter>

Item	Options	Description
IDE Secondary Master	Options are in its sub menu(described in Table 64)	Press <enter> to enter the sub menu of detailed options</enter>
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Displays the amount of conventional memory detected during boot up
Extended Memory	N/A	Displays the amount of extended memory detected during boot up
Total Memory	N/A	Displays the total memory available in the system

## IDE Adapters

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive.

Use the legend keys to navigate through this menu and exit to the main menu. Use Table 3 to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection Press Enter		Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None Auto Manual	Selecting 'manual' lets you set the re- maining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	Normal	Choose the access mode for this hard

Item	Options	Description
	LBA	disk
	Large	
	Auto	
The following option 'Manual'	ons are selectable on	ly if the 'IDE Primary Master' item is set to
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** <b>Warning</b> : Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	***
Sector	Min = 0 Max = 255	Number of sectors per track

# 6.4. Advanced BIOS Features Setup

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

Phoenix	- AwardBI	OS CMOS	Setup	Utility
	Advanced	BIOS Fea	atures	-

Virus Warning	[Disabled]	Item Help
CPU Internal Cache External Cache CPU L2 Cache ECC Checking Processor Number Feature Quick Power On Self Test First Boot Device Second Boot Device Boot Other Device Boot Up Floppy Drive Boot Up Floppy Seek Boot Up Floppy Seek Boot Up NumLock Status Gate A20 Option Typematic Rate Setting X Typematic Rate (Chars/Sec) X Typematic Rate (Chars/Sec) Security Option OS Select For DRAM > 64MB Video BIOS Shadow	[Enabled]         [Enabled]         [Enabled]         [Enabled]         [Floppy]         [HDD-0]         [CDR0M]         [Enabled]         [Disabled]         [Enabled]         [Enabled]         [Disabled]         [Fast]         [Disabled]         6         250         [Setup]         [Non-052]         [Enabled]	Menu Level ► Allows you to choose the VIRUS warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep

1↓→+:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

### Virus Warning

When enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive.

**NOTE:** Many disk diagnostic programs that access the boot sector table can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

Description	Choice
CPU L2 Cache ECC Checking When you select Enabled, memory checking is enabled when the external cache contains ECC SRAMs.	CPU L2 Cache Enabled [•] Disabled []
Processor Number Feature Enabled or disabled the processor number feature function.	Processor Number Feature Enabled [•] Disabled [] 
Quick Power On Self Test Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work	Quick Power On Self Test         Enabled       [•]         Disabled       [.]         ]       ]         ]       ]

Description	Choice
First/Second/Third/Other Boot Device The BIOS attempts to load the operating system from the devices in the sequence selected in these items.	First Boot Device         Floppy       []         HDD-0       []         HDD-1       []         HDD-2       []         HDD-3       []         HDD-3       []         JTP100       []         LAN       []         Disabled       []         1]:Move ENTER: Accept ESC: Abort
Swap Floppy Drive This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B. If the system has two floppy drives, you can swap the logical drive name assignments.	Swap Floppy Drive Disabled [ <b>n</b> ] Enabled []
Boot Up Floppy Seek When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PCs have 40-track floppy drives, we recommend that you set this field to Disabled to save time. Seeks disk drives during boot up. Disabling speeds boot up.	Boot Up Floppy Seek Disabled [•] Enabled [ ]
Boot Up NumLock Status Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.	Boot Up NumLock Status         On          Off          Off          I  :Move       ENTER: Accept

Description	Choice
Gate A20 option Gate A20 refers to the way the system addresses memory above 1 MB (extended memory). When set to Fast, the system chipset controls Gate A20. When set to Normal, a pin in the keyboard controller controls Gate A20. Setting Gate A20 to Fast improves system speed, particularly with OS/2 and Windows	Gate A20 Option Normal [] Fast [•] 11:Move ENTER:Accept ESC:Abort
Typematic Rate Setting When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and typematic delay.	Typematic Rate Setting         Disabled []         Enabled []         #]         1:Move ENTER:Accept ESC:Abort
Typematic Rate (Chars/Sec) When the typematic rate setting is enabled, you can select a typematic rate (the rate at which character repeats when you hold down a key) of 6, 8, 10,12, 15, 20, 24 or 30 characters per second.	Typematic Rate (Chars/Sec)         6          8          10          12          15          24          30          1          1          1          24          1          1          1          1          1          1          1          24          1          1          1          1          1          1          1          1          1          1          1          1          1          1          1          1 <t< td=""></t<>
Typematic Delay (Msec) When the typematic rate setting is enabled, you can select a typematic delay (the delay before key strokes begin to repeat) of 250, 500, 750 or 1000 milliseconds.	Typematic Delay (Msec)         250       [•]         500       []         750       []         1000       []         1000       []         11:Move ENTER:Accept ESC:Abort

Description	Choice		
Security Option			
Select whether the password is required every time the system boots or only when you enter setup. If you have set a password, select whether the password is required every time the System boots, or only when you enter Setup. System: The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt. Setup: The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.	Security Option Setup [■] System [] 11:Move ENTER:Accept ESC:Abort		
<b>Note:</b> To disable security, select PASS you will be asked to enter passwor <enter>, it will disable security. Once boot and you can enter Setup freely.</enter>	SWORD SETTING at Main Menu and then d. Do not type anything and just press the security is disabled, the system will		
OS Select For DRAM > 64MB Select OS2 only if you are running OS/2 operating system with greater than 64 MB of RAM on your system.	OS Select For DRAM > 64MB           Non-OS2         [•]           OS2            [•]           ]		
Video BIOS Shadow Enabled the video BIOS Shadow or select the disabled.	Video BIOS Shadow Enabled [■] Disabled [] 11:Move ENTER:Accept ESC:Abort		

# 6.5. Advanced Chipset Features Setup

Phoenix - AwardBIOS CMOS Setup Utility Advanced Chipset Features

||→+:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

### DRAM Clock / Drive Control

	Phoenix - AwardBIOS CMOS Setup Ut DRAM Clock/Drive Control	ility
SB	Frequency	

Current FSB Frequency	Item Help
DRAM Clock [By SPD] DRAM Timing [By SPD] DRAM CAS Latency 2.5 Bank Interleave Disabled Precharge to Active(Trp) 3T Active to Precharge(Tras) 6T Active to CMD(Trcd) 3T DRAM Command Rate [2T Command]	Menu Level ►►

il--:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5: Previous Values F6: Fail-Safe Defaults F7: 0 timized Defaults

Description	Choice
DRAM Clock The chipset supports synchronous and asynchronous mode between host clock and DRAM clock frequency.	DRAM Clock 66 MHz [ ] 100 MHz [ ] 133 MHz [ ] By SPD [ ] 11:Move ENTER:Accept ESC:Abort
DRAM Timing This setting determines whether DRAM timing is configured by reading the contents of the SPD (Serial Presence Detect) EPROM on the DRAM module. Selecting Yes makes SDRAM Cycle Length and Bank Interleave automatically determined by BIOS according to the configurations on the SPD.	DRAM Timing Manual [] By SPD [•]   :Move ENTER:Accept ESC:Abort
DRAM CAS Latency Set the time between SDRAM read command and when the data actually becomes available.	DRAM CAS Latency 2.5 [*] [1]:Move ENTER:Accept ESC:Abort
Bank Interleave Set the interleave mode of the SDRAM interface. Interleaving allows banks of SDRAM to alternate their refresh and access cycles. One bank will undergo its refresh cycle while another is being accessed. This improves performance of the SDRAM by masking the refresh time of each bank.	Bank Interleave Disabled [m] 2 Bank [ ] 4 Bank [ ]

Description	Choice
Precharge to Active (Trp) The Precharge to Active timing controls the length of the delay between the precharge and activation commands.	Precharge to Active(Trp) 2T [] 3T [•] 11:Move ENTER:Accept ESC:Abort
Active to Precharge (Tras) The Active to Precharge timing controls the length of the delay between the activation and precharge commands.	Active to Precharge(Tras) 5T [] 6T [*] []:Move ENTER:Accept ESC:Abort
Active to CMD (Trcd) Select the active to CMD timer. This timing controls the length of the delay between when a memory bank is activated to when a read/write command is sent to that bank.	Active to CMD(Trcd) 2T [.] 3T [.] 1]:Move ENTER:Accept ESC:Abort
DRAM Command Rate Select the DRAM Command Rate. This BIOS feature controls how long the memory controller latches on and asserts the command bus.	DRAM Command Rate          2T Command [•]         1T Command [•]         IT Command [•]         []:Move ENTER:Accept ESC:Abort

CHAPTER 6 -BIOS Setup

## AGP & P2P Bridge Control

AGP & P2P Br	idge Control
AGP Aperture Size [64M] AGP Mode [4X] AGP Driving Control [Auto] AGP Driving Value DA AGP Fast Write [Disabled] AGP Master 1 WS Write [Disabled] AGP Master 1 WS Read [Disabled]	Item Help Menu Level ►►
II++:Move Enter:Select +/-/PU/PD:Valu F5: Previous Values F6: Fail-Safe Description	le F10:Save ESC:Exit F1:General Help Defaults F7: O timized Defaults Choice
AGP Aperture Size (MB) Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded. Host cycles that hit the aperture range are forwarded to the AGP without any translation.	AGP Aperture Size           256M         []]           120M         []]           64M         []]           64M         []]           16M         []]           8M         []]           4M         []]           11:Nove ENTER:Accept ESC:Abort
AGP Mode Decides the setting of integrated AGP graphics.	AGP Mode 4x [#] 2x [ ] 1x [ ]

Description	Choice
AGP Driving Control This item allows you to adjust the AGP driving force. Choose Manual to key in a AGP driving Value in the next selection. This field is recommended to set in Auto for avoiding any error in your system.	AGP Driving Control Auto Manual [•]
AGP Driving Value This item allows you to adjust the AGP driving force.	AGP Driving Value Min=0000 Max=00FF Key in a HEX number : []:Move ENTER:Accept ESC:Abort
AGP Fast Write This item allows you to adjust the AGP fast write.	AGP Fast Write Disabled [•] Enabled [ ]
AGP Master 1 WS Write This implements a single delay when writing to the AGP Bus. By default, two-wait states are used by the system, allowing for greater stability.	AGP Master 1 WS Write Disabled [m] Enabled [ ]

### CHAPTER 6 -BIOS Setup

Description	Choice
AGP Master 1 WS Read This implements a single delay when reading to the AGP Bus. By default, two-wait states are used by the system, allowing for greater stability.	AGP Master 1 WS Read Disabled [m] Enabled [ ]

## CPU & PCI Bus Control

Phoenix	- AwardBIOS CMOS Setup Utility	
	CPU & PCI Bus Control	

CPU to PCI Write Buffe	er [Enabled] [Enabled]	Item Help
PCI Delay Transaction	[Disabled]	Menu Level 🕨
↑↓→+:Move Enter:Select	+/-/PU/PD:Value F10:Save E	SC:Exit F1:General Help
F5: Previous Values	<u>F6: Fail-Safe Defaults</u>	7: Optimized Defaults
Description	Chair	

Description	L	Choice
CPU to PCI Write Buffer When this field is Enabled, writes from the CPU to the PCI bus are buffered, to compensate for the speed differences between the CPU and the PCI bus. When Disabled, the writes are not buffered and the CPU must wait until the write is complete before starting another write cycle.		CPU to PCI write Buffer Disabled [] Enabled [.]

Description	Choice
PCI Master 0 WS Write When Enabled, writes to the PCI bus are executed with zero wait sates.	PCI Master 0 WS Write Enabled [*] Disabled [ ]
PCI Delay Transaction The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.	PCI Delay Transaction Disabled [.] Enabled [.]
Memory Hole You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.	Memory Hole Disabled [•] 15M - 16H [ ] []:Nove ENTER:Accept ESC:Abort
System BIOS Cacheable Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.	System BIOS Cacheable Disabled [.] Enabled [.] II:Move ENTER:Accept ESC:Abort

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	Description	Choice
Video RA Selecting video BIG resulting However, memory a	AM Cacheable Enabled allows caching of the OS ROM at C0000h to C7FFFh, in better video performance. if any program writes to this rea, a system error may result.	Video RAM Cacheable Disabled [•] Enabled [ ]
Video Sh Specify allocate fo	nare Memory Size the size of system memory to or video memory.	VGA Share Memory Size 16M [ ] 32M [■] 64M [ ] 11:Move ENTER:Accept ESC:Abort
Select Di Set the displaying	isplay Device device you want to use for g.	Select Display Device CRT [•] LCD [ ] CRT+LCD [ ] 11:Move ENTER:Accept ESC:Abort
Panel Tv	De l	
Banalup	Function	
00H	Function 640x480 TFT	
01H	800x600 TFT ( LVDS )	
02H	1024x768 TFT 2pixel/clk at 32Mhz	Panel Type
03H	1280x1024 TFT	
04H	640x480 DSTN	Min=0000
05H	800x600 DSTN	Max=000#
06H	1600x1200 TFT ( LVDS )	Key in a HEX number :
07H	1024x768 TFT 1pixel/clk at 65Mhz	they have been been been been been been been be
08H	640x480 TFT ( LVDS )	
09H	800x600 TFT)	
0AH	1024x768 TFT	11:Hove ENTER:Accept ESC:Abort
0BH	1280x1024 TFT	
0CH	1400x1050 TFT 2pixel/clk at 54Mhz	
0DH	800x600 TFT	
0EH	1024x768 DSTN	
0FH	1280x1024 DSTN	

# 6.6. Integrated Peripherals

Phoenix - AwardBIOS CMOS Setup Utility Integrated Peripherals

VIA OnChip IDE Device	[Press Enter]	Item Help
<ul> <li>VIA Onchip PCI Device</li> <li>Superio Device</li> <li>Init Display First</li> <li>PWRON After PWR-Fail</li> </ul>	[Press Enter] [Press Enter] [PCI Slot] [Off]	Menu Leve] ▶

†|→+:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5: Previous Values F6: Fail-Safe Defaults F7: O timized Defaults F5: Previous VIA VIA OnChip IDE Device Phoenix - AwardBIOS CMOS Setup Utility VIA OnChip IDE Device

OnChip IDE Channel0 [Enabled	II Item Help
IDE Prefetch Mode [Enabled Primary Master PIO [Auto] Primary Slave PIO [Auto] Secondary Master PIO [Auto] Primary Slave PIO [Auto] Primary Master UDMA [Auto] Secondary Master UDMA [Auto] Secondary Slave UDMA [Auto] IDE HDD Block Mode [Enabled	i] Menu Level ►►
[]→←:Move Enter:Select +/-/PU/PD:Va F5: Previous Values F6: Fail-Sa	alue F10:Save ESC:Exit F1:General Help afe Defaults F7: O timized Defaults
Description	Choice
	OnChip IDE Channel0
On-Chip IDE Channel 0	Disabled [ ] Enabled [∎]
The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select <i>Enabled</i> to activate each channel separately.	
	↑1:Move ENTER:Accept ESC:Abort

Description	Choice
	OnChip IDE Channel1
On-Chip IDE Channel 1	Disabled [ ] Enabled [ <b>=</b> ]
The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select <i>Enabled</i> to activate each channel separately.	
	1↓:Move ENTER:Accept ESC:Abort
IDE Prefetch Mode	IDE Prefetch Mode
The onboard IDE drive interface supports IDE prefetching for faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to	Disabled [ ] Enabled [∎]
prefectching.	↑↓:Move ENTER:Accept ESC:Abort
Primary Master/Slave PIO	IDE Primary Master PIO
The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the suptom automatically	Auto [■] Mode 0 [ ] Mode 1 [ ] Mode 2 [ ] Mode 3 [ ] Mode 4 [ ]
determines the best mode for each device.	↑↓:Move ENTER:Accept ESC:Abort
Secondary Master/Slave PIO	IDE Secondary Master PIO
The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In	Auto [ <b>m</b> ] Mode 0 [ Mode 1 [ Mode 2 [ Mode 3 [ Mode 4 [
Auto mode, the system automatically determines the best mode for each device.	↑↓:Move ENTER:Accept ESC:Abort

Choice
IDE Primary Master UDMA Disabled [] Auto [•]
IDE Secondary Slave PIO         Auto       [●]         Mode 0       []         Mode 1       []         Mode 2       []         Mode 3       []         Mode 4       []         Mode 4       []         Mode 4       []
IDE HDD Block Mode Disabled [ ] Enabled [∎] ] ]
Choico
Auto [■] Disabled []

Description	Choice
	OnChip USB Controller
OnChip USB Controller If your system contains a Universal Serial Bus (USB) controller and you have USB peripherals.	All Disabled [ ] All Enabled [ ] 1&2 USB Port [ ] 2&3 USB Port [ ] 1&3 USB Port [ ] 1 USB Port [ ] 3 USB Port [ ]
	↑↓:Move ENTER:Accept ESC:Abort
	OnChip EHCI Controller
OnChip EHCI controller	Enabled [∎] Disabled []
Select <i>Enabled</i> if your system contains a Universal Serial Bus (EHCI) controller and you have USB peripherals.	
	1↓:Move ENTER:Accept ESC:Abort
	USB Keyboard Support
USB Keyboard Support	Enabled [∎] Disabled []
Select <i>Enabled</i> if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.	
	↑↓:Move ENTER:Accept ESC:Abort
	USB Mouse Support
USB Mouse support	Enabled[■] Disabled[]
Select <i>Enabled</i> if your system contains a Universal Serial Bus (USB) controller and you have a USB mouse.	
	11:Move ENTER:Accept ESC:Abort

## Super IO Device

Phoenix - AwardBIOS CMOS Setup Utility SuperIO Device		
Onboard FDC Controller [Enabled	II Item Help	
Onboard Serial Port 1 [3F8/IRC Onboard Serial Port 1 [2F8/IRC UART Mode Select [Normal] RxD, TxD Active [Hi,Lo] IR Transmission Delay [Enablec UR2 Duplex Mode [Half] USE IR Pins [IR-Rx27 Onboard Parallel Port [378/IRC Parallel Port Mode [SPP] EPP Mode Select [EPP1.7] ECP Mode Use DMA [3]	41] 1] 1] [x2] 27] I	
†l→+:Move Enter:Select +/-/PU/PD:Va F5: Previous Values F6: Fail-Sa	alue F10:Save ESC:Exit F1:General Help afe Defaults F7: O timized Defaults	
Description	Choice	
	Onboard FDC Controller	
Onboard FDC Controller Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install and-in FDC or the system has no floppy drive, select Disabled in this field.	Disabled [ ] Enabled [•]	
	<pre>↑↓:Move ENTER:Accept ESC:Abort</pre>	
	Onboard Serial Port 1	
Onboard Serial Port 1 Select a logical COM port name and matching address for the first and second serial ports. Select an address and corresponding interrupt for the first and second serial ports.	Disabled[] 3F8/IRQ4[∎] 2F8/IRQ3[] 3E8/IRQ4[] 2E8/IRQ3[] Auto[]	
	<pre>↑↓:Move ENTER:Accept ESC:Abort</pre>	
	Onboard Serial Port 2	
Onboard Serial Port 2 Select a logical COM port name and matching address for the first and second serial ports. Select an address and corresponding interrupt for the first and second serial ports.	Disabled [ ] 3F8/IRQ4 [ ] 2F8/IRQ3 [ ■] 3E8/IRQ4 [ ] 2E8/IRQ3 [ ] Auto [ ]	
	<pre> ↑↓:Move ENTER:Accept ESC:Abort </pre>	

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Description	Choice
UART Mode Select	UART Mode Select
Enables you to select the infrared communication protocol: Standard (default)   IrDA   ASKIR, IrDA is Hewlett Packard's infrared communication protocol with a maximum baud rate up to 115.2K bps. ASKIR is Sharp's infrared communication protocol with a maximum	IrDA [ ] ASKIR [ ] Normal [∎]
baud rate up to 57.6K bps.	11:Move ENTER:Accept ESC:Abort
	RxD , TxD Active
RxD, TxD Active Defines the voltage level for Infrared module RxD (receive) mode and TxD (transmit) mode. This setting has to match the requirements of the infrared module used in the system.	Hi,Hi [ ] Hi,Lo [∎] Lo,Hi [ ] Lo,Lo [ ]
	↑↓:Move ENTER:Accept ESC:Abort
	IR Transmission Delay
IR Transmission Delay When set to "Enabled", utilizes the capability of the Keyboard computer to allow faster infrared transmission rates.	IR Transmission Delay Disabled [] Enabled [■]
IR Transmission Delay When set to "Enabled", utilizes the capability of the Keyboard computer to allow faster infrared transmission rates.	IR Transmission Delay Disabled [ ] Enabled [∎]
IR Transmission Delay When set to "Enabled", utilizes the capability of the Keyboard computer to allow faster infrared transmission rates. UR2 Duplex Mode	IR Transmission Delay Disabled [] Enabled [•]
IR Transmission Delay When set to "Enabled", utilizes the capability of the Keyboard computer to allow faster infrared transmission rates. UR2 Duplex Mode This field is available when UART Mode	IR Transmission Delay Disabled [] Enabled [ <b>•</b> ] 11:Move ENTER:Accept ESC:Abort UR2 Duplex Mode
IR Transmission Delay When set to "Enabled", utilizes the capability of the Keyboard computer to allow faster infrared transmission rates. UR2 Duplex Mode This field is available when UART Mode Select is set to either ASKIR or IrDA. This item enables you to determine the infrared (IR) function of the onboard infrared chip. The options are "Full" and "Half (default). Full-duplex means that you can transmit and send information simultaneously. Half-duplex is the	IR Transmission Delay Disabled [] Enabled [•] 11:Move ENTER:Accept ESC:Abort UR2 Duplex Mode Full [] Half [•]

Description	Choice
	Use IR Pins
Use IR Pins Use this item to set the IR pins. The options are "IR Rx2Tx2" (default) and "RxD2,TxD2"	RxD2,TxD2 [ ] IR-Rx2Tx2 [∎]
Onboard Parallel Port Select a logical LPT port name and matching address for the physical parallel (printer) port	Onboard Parallel Port         Disabled []         378/IRQ7 []         278/IRQ5 []         3BC/IRQ7 []         1:Move ENTER:Accept ESC:Abort
Parallel Port Mode Selected an operating mode for the onboard parallel port. Select Compatible or extended unless you are certain both your hardware and software support EPP or ECP mode.	Parallel Port Mode           SPP         [
ECP Mode Use DMA Select a DMA channel for the port	ECP Mode Use DMA 1 [] 3 [•] []:Move ENTER:Accept ESC:Abort
Init Display First Initialize the AGP video display before initializing any other display device on the system. Thus the AGP display becomes the primary display.	Init Display First         PCI Slot [■]         AGP []

Description	Choice
	PWRON After PWR-Fail
PWRON After PWR-Fail Select a Power On status by the BIOS setup when power fail.	Off [■] On [ ] Former-Sts [ ]
	11:Move ENTER:Accept ESC:Abort

# 6.7. Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.

Phoenix - AwardBIOS CMOS Setup Utility Power Management Setup

ACPI function	[Enabled] [User Define]	Item H	elp
HDD Power Down SUspend Mode Video Off Option Video Off Method MODEM Use IRQ Soft-Off by PWRBTN ► IRQ/Event Activity Detect	Disable] [Disable] [Suspend -> Off] [V/H SYNC+Blank] [3] [Instant-Off] [Press Enter]	Menu Level	•
11→+:Move Enter:Select +/-	/PU/PD:Value F10:Save	ESC:Exit F1:Ge	neral Help

F5: Previous Values F6: Fail-Safe Defaults F7: O timized Defaults

Description	Choice
ACPI function Select to Enabled the ACPI function and select Disabled to disable the APCI.	ACPI Function Enabled [■] Disabled []
Power management Option	Power Management Option User Define [•] Min Saving [ ] Max Saving [ ]
HDD Power Down When enabled and after the set time of system inactivity, the hard disk drive will be powered down while all other devices remain active.	HDD Power Down         Disable       [•]         1 Min       [·]         2 Min       []         3 Min       []         4 Min       []         5 Min       []         6 Min       []         7 Min       []         8 Min       []         9 Min       []         10 Min       []         11 Min       []         12 Min       []         13 Min       []         14 Min       []         15 Min       []         Y       ]         11:Move ENTER:Accept ESC:Abort
Suspend Mode Select the Suspend Mode.	Suspend Mode         Disable       []]         1       Min         2       Min         3       Min         4       Min         5       Min         6       Min         10       Min         10       Min         10       Min         10       Min         11       Min         12       Min         130       Min         1       Hour         1       Hour         1       Ithour         1       Ithour         1       Ithour         1       Ithour         1       Ithour         1       Ithour         1       Move         Ithour       Ithour         Ithour       Ithour

Description		Choice		
Video Off Option Selects the power-saving modes during which the monitor goes blank: Always On: Monitor remains on during power-saving modes. Suspend> Off: Monitor blanked when system enters <i>Suspend</i> mode.		Video Off Option Always On [] Suspend -> Off [■] 11:Move ENTER:Accept ESC:Abort		
Video Off Method This determines the manner in which the monitor is blanked.		Video Off Method Blank Screen [] V/H SYNC+Blank [] DPMS [■] 11:Move ENTER:Accept ESC:Abort		
V/H SYNC+Blank	This selection will and horizontal syn video buffer.	l cause the system to turn off the vertical chronization ports and write blanks to the		
Blank Screen	This option only w	vrites blanks to the video buffer.		
DPMS	Initial display pow	ver management signaling.		
MODEM Use IRQ If you want an incoming call on a modem to automatically resume the system from a power-saving mode, use this item to specify the interrupt request line (IRQ) that is used by the modem. You might have to connect the fax/modem to a Keyboard computer Wake On Modem connector for this feature to work		MODEM Use IRQ           NA         []           3         []           4         []           5         []           7         []           9         []           10         []           11         []           11:Move ENTER:Accept ESC:Abort		
Soft-Off by PWR-BTTN When set to "Instant-Off the power button will tu power. When set to "Delay to press the power button a than 4 seconds to turn off Otherwise, the system just mode.	(default), pressing rn off the system y 4 Sec." you have ind hold it for more the system power. goes into suspend	Soft-Off by PWR-BTTN Instant-Off [•] Delay 4 Sec [ ]		

IRQ/Event Activity Detect				
Description	Choice			
	Video Off Option			
	Always On[]			
VGA When set to <i>On</i> (default) any event occurring				
at a VGA port will awaken a system which has				
been powered down.				
	↑↓:Move ENTER:Accept ESC:Abort			
	LPT & COM			
LPT & COM	NONE [ ] LPT [ ] COM [ ]			
at a COM (serial)/LPT (printer) port will	LPT/COM [#]			
awaken a system which has been powered down				
	11:MOVE ENTER:ACCEPT ESC:ADOFT			
	HDD & FDD			
	OFF [ ] ON [ <b>=</b> ]			
When set to On (default), any event occurring				
at a hard or floppy drive port will awaken a				
system when has been powered down.				
	11:Move ENTER:Accept ESC:Abort			
	PCI Master			
	OFF [■]			
PCI Master When set to <i>On</i> (default), any event occurring				
at a PCI Master device will awaken a system				
which has been powered down				
	11:Move ENTER:Accept ESC:Abort			

Description	Choice		
Power-On by PCI card When Enabled, your can awakens the system from Suspend mode from a PCI card event.	PowerOn by PCI Card Disabled [•] Enabled [ ]		
Modem Ring Resume When set to <i>Enabled</i> , any event occurring to the Modem Ring will awaken a system which has been powered down	Modem Ring Resume         Disabled [•]         Enabled []		
RTC Alarm Resume When Enabled, your can set the date and time at which the RTC (real-time clock) alarm awakens the system from Suspend mode.	RTC Alarm Resume         Disabled []         Enabled []         inabled []         inabled []		
Date(of Month) Alarm Min= 0 Max= 31 Key in a DEC number : 11:Move ENTER:Accept ESC:Abort	Time(hh:mm:ss) Alarm Min= 0 Max= 23 Key in a DEC number : 11:Move ENTER:Accept ESC:Abort		

### IRQs Activity Monitoring

Description					(	Cł	noice			
When set to O	n (default), any	event occurr	ng at	will	awaken	а	system	which	has	been

powered down.

The following is a list of IRQ's, Interrupt **ReQuests**, which can be exempted much as the COM ports and LPT ports above can. When an I/O device wants to gain the attention of the operating system, it signals this by causing an IRQ to occur. When the operating system is ready to respond to the request, it interrupts itself and performs the service.

As above, the choices are *On* and *Off. Off* is the default.

When set On, activity will neither prevent the system from going into a power management mode nor awaken it.

Primary INTR	IRQ3 (COM 2)
OFF [ ] ON [∎]	Disabled [ ] Enabled [∎]
<pre> fl:Move ENTER:Accept ESC:Abort </pre>	11:Move ENTER:Accept ESC:Abort
IRQ4 (COM 1)	IRQ5 (LPT 2)
Disabled [ ] Enabled [∎]	Disabled [ ] Enabled [∎]
<pre> \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$</pre>	11:Move ENTER:Accept ESC:Abort
IRQ6 (Floppy Disk)	IRQ7 (LPT 1)
Disabled [ ] Enabled [∎]	Disabled [ ] Enabled [∎]
<pre> \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$</pre>	<pre> ↑↓:Move ENTER:Accept ESC:Abort</pre>

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Description	Choice
IRQ8 (RTC Alarm)	IRQ9 (IRQ2 Redir)
Disabled [ ] Enabled [∎]	Disabled [ ] Enabled [∎]
11:Move ENTER:Accept ESC:Abort	11:Move ENTER:Accept ESC:Abort
IRQ10 (Reserved)	IRQ11 (Reserved)
Disabled [ ] Enabled [∎]	Disabled [ ] Enabled [ <b>=</b> ]
1]:Move ENTER:Accept ESC:Abort	
IRQ12 (PS/2 Mouse)	IRQ13 (Coprocessor)
Disabled [ ] Enabled [∎]	Disabled [ ] Enabled [∎]
<pre> fl:Move ENTER:Accept ESC:Abort </pre>	↑↓:Move ENTER:Accept ESC:Abort
IRQ14 (Hard Disk)	IRQ15 (Reserved)
Disabled [ ] Enabled [∎]	Disabled [ ] Enabled [∎]
tl:Move ENTER:Accept ESC:Abort	11 Move ENTER Accent ESC Abort

# 6.8. PnP/PCI Configuration Setup

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own

special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.

Phoenix	- AwardBIOS	CMOS Setup	Utility
	PnP/PCI Cont	Figurations	-

PNP OS Installed	No	Item Help			
Resources Controlled By		Menu Level 🕨			
IRQ Resources	Press Enter	Select Yes if you are using a Plug and Play			
PCI/VGA Palette Snoop Assign IRQ For VGA Assign IRQ For USB		capable operating system Select No if you need the BIOS to configure non-boot			
		devices			

11→+:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5: Previous Values F6: Fail-Safe Defaults F7: O timized Defaults

Description	Choices
PNP OS Installed Select Yes if the system is operating environment is Plug-and-Play aware (e.g. Windows 95).	PMP OS Installed No [0] Tes [] 11:Move ENTER:Accept ESC:Abort
Resource Controlled by The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play – compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them	Reset Configuration Data Disabled [1] Enabled [3] f1:Nove ENTER:Accept ESC:Abort
Reset Configuration Data Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system can pat hoot	Resources Controlled By Auto(EECD) [ ] Manual [1]
not doot.	T4: Nove ENTER: Rocept ESC: Abort

IRQ n Resources

	Phoenix - AwardBIOS CMOS Setup IRQ Resources	Utility
IRQ-3 assigned IRQ-4 assigned IRQ-7 assigned IRQ-9 assigned IRQ-10 assigned IRQ-11 assigned IRQ-12 assigned IRQ-14 assigned IRQ-15 assigned	to         IPCI/ISA PnP1           to         IPCI/ISA PnP1	Item Help Menu Level >> Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture
1↓→←:Move Enter:Se	elect +/-/PU/PD:Value F10:Save	ESC:Exit F1:General Help

F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

When resources are controlled manually, assign each system interrupt as on of the following type, depending on the type of device using the interrupt.

Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ4 for serial port 1)

PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

The Choice: Legacy ISA and PCI/ISA PnP.

	PCI/VGA Palette Snoop
	Disabled [#] Enabled [ ]
PCI/VGA Palette Snoop Leave this field at Disabled.	
	:Move ENTER:Accept ESC:Abort
	Assign IRQ For VGA
Assign IRQ for VGA	Disabled [ ] Enabled [ <b>=</b> ]
Name the interrupt request (IRQ) line assigned to the VGA on your system.	
Activity of the selected IRQ always awakens the system	
	LI-Move ENTER-Accept ESC-Abort
Assign IRQ for VGA Name the interrupt request (IRQ) line assigned to the VGA on your system. Activity of the selected IRQ always awakens the system.	Disabled [] Enabled [∎]

	Assign IRQ For USB
Assign IRQ for USB Name the interrupt request (IRQ) line assigned to the USB on your system. Activity of the selected IRQ always awakens the system	Disabled [ ] Enabled [∎]
	1↓:Move ENTER:Accept ESC:Abort

# 6.9. PC Health Status



11---:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5: Previous Values F6: Fail-Safe Defaults F7: O timized Defaults The BIOS shows the PC health status in this window.

Item	Description
Current CPU Temp.	This field displays the current CPU temperature, in your computer contains a monitoring system.
Current System Temp.	This field displays the current system temperature, in your computer contains a monitoring system.
Current CPUFAN Speed	These fields display the current speed of up to three CPU fans, if your computer contains a monitoring system.
+12V / +5V / VBAT	These fields display the current voltage of input lines if your computer contains a monitoring system.

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# 6.10. Frequency/Voltage Control

Phoenix - AwardBIOS CMOS Setup Utility Frequency/Voltage Control

[Disabled]	Item Help
	Menu Level ►
	[Disabled]

\$\$ F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults\$\$ F6: Fail-Safe Defaults F7: Optimized Defaults

Description	Choice
Spread Spectrum When the system clock generator pulses, the extreme values of the pulse generate excess EMI. Enabling pulse spectrum spread modulation changes the extreme values from spikes to flat curves, thus reducing EMI. This benefit may in some cases be outweighed by problems with timing-critical devices, such as	Spread Spectrum Enabled [■] Disabled []
a clock-sensitive SCSI device.	↑↓:Move ENTER:Accept ESC:Abort

# 6.11. Defaults Menu

Selecting "Defaults" from the main menu shows you two options which are described below

### Load Fail-Safe Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

Load Fail-Safe Defaults (Y/N)? N

Pressing 'Y' loads the BIOS default values for the most stable, minimal-performance system operations.

## Load Optimized Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

## Load Optimized Defaults (Y/N)? N

Pressing 'Y' loads the default values that are factory settings for optimal performance system operations.

# 6.12. Supervisor/User Password Setting

You can set either supervisor or user password, or both of them. The differences between are:

SUPERVISOR PASSWORD: can enter and change the options of the setup menus.

**USER PASSWORD**: just can only enter but do not have the right to change the options of the setup menus. When you select this unction, the following message will appear at the center of the screen to assist you in creating a password.

## ENTER PASSWORD:

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Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

### PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup.

# 6.13. Exit Selecting

## Save & Exit Setup

Pressing <Enter> on this item asks for confirmation: Save to CMOS and EXIT (Y/N)? Y

Pressing "Y" stores the selections made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

# **Exit Without Saving**

Pressing <Enter> on this item asks for confirmation:

Quit without saving (Y/N)? Y

This allows you to exit Setup without storing in CMOS any change. The previous selections remain in effect. This exits the Setup utility and restarts your computer.

# 6.14. POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization:
	-Disable shadow RAM
	-Disable L2 cache (socket 7 or below)
	-Program basic chipset registers
C1h	Detect memory
	-Auto-detection of DRAM size, type and ECC.
	-Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init.
04h	Reserved
05h	1. Blank out screen
	2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface
	2. Initialize 8042 self-test

POST (hex)	Description
08h	<ol> <li>Test special keyboard controller for Winbond 977 series Super I/O chips.</li> </ol>
	2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional) .
	<ol> <li>Auto detect ports for keyboard &amp; mouse followed by a port &amp; interface swap (optional).</li> </ol>
	3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBIN able by OEM customers.
15h	Reserved
16h	Initial onboard clock generator if Early_Init_Onboard_Generator is defined. See also POST 26h.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or $Intel^{(\!\!\!0\!)}$ ) and CPU level (586 or 686) .
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved

POST (hex)	Description
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	<ol> <li>Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute.</li> </ol>
	<ol> <li>Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead.</li> </ol>
24h	Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information.
25h	Early PCI initialization: - Enumerate PCI bus number - Assign memory & I/O resource - Search for a valid VGA device & VGA BIOS, and put it
26h	Into C000:0. 1. If Early_Init_Onboard_Generator is not defined Onboard clock generator initialization. Disable respective Clock resource to empty PCI & DIMM slots. 2. init onboard PWM. 3. Init onboard H/W monitor devices
27h	Initialize INT 09 buffer
28h	Reserved
29h	<ol> <li>Program CPU internal MTRR (P6 &amp; PII) for 0~640K memory address.</li> </ol>
	2. Initialize the APIC for Pentium class CPU.
	<ol> <li>Program early chipset according to CMOS setup. Example: onboard IDE controller.</li> </ol>
	4. Measure CPU speed.
2Ah	Reserved
2Bh	Invoke Video BIOS.
2Ch 2Dh	<ol> <li>Reserved</li> <li>Initialize double-byte language font (Optional)</li> <li>Put information on screen display, including Award title, CPU type, CPU speed, full screen logo</li> </ol>

POST (hex)	Description
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard if Early_Reset_KB is defined e.g. Winbond 977
	series Super I/O chips. See also POST 63h
34h	Reserved
35h	Test DMA Channel 0.
36h	Reserved
37h	Test DMA Channel 1.
38h	Reserved
39h	Test DMA page registers.
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Reserved
48h	Reserved
49h	<ol> <li>Calculate total memory by testing the last double word of each 64K page.</li> </ol>
	2. Program writes allocation for AMD K5 CPU.

POST (hex)	Description	
4Ah	Reserved	
4Bh	Reserved	
4Ch	Reserved	
4Dh	Reserved	
4Eh	1. Program MTRR of M1 CPU	
	<ol> <li>Initialize L2 cache for P6 class CPU &amp; program CPU with proper cacheable range.</li> </ol>	
	3. Initialize the APIC for P6 class CPU.	
	<ol> <li>On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.</li> </ol>	
4Fh	Reserved	
50h	Initialize USB Keyboard & Mouse	
51h	Reserved	
52h	Test all memory (clear all extended memory to 0)	
53h	Clear password according to H/W jumper (Optional)	
54h	Reserved	
55h	Display number of processors (multi-processor platform)	
56h	Reserved	
57h	1. Display PnP logo	
	2. Early ISA PnP initialization	
	-Assign CSN to every ISA PnP device.	
58h	Reserved	
59h	Initialize the combined Trend Anti-Virus code.	
5Ah	Reserved	
5Bh	(Optional Feature)	
	Show message for entering AWDFLASH.EXE from FDD (optional)	
5Ch	Reserved	
5Dh	1. Initialize Init_Onboard_Super_IO.	
	2. Initialize Init_Onbaord_AUDIO.	
5Eh	Reserved	
5Fh	Reserved	

POST	Description
(hex)	
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reset \Keyboard if Early_KB is not defined.
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices.
	<ol><li>Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".</li></ol>
6Eh	Reserved
6Fh	1. Initialize floppy controller
	2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved
73h	Reserved
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM
76h	(Optional Feature) Enter AWDFLASH.EXE if: -AWDFLASH is found in floppy drive.
	-ALT+F2 is pressed
77h	Detect serial ports & parallel ports.

POST (hex)	Description
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Init HDD write protect
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported.
	-If errors occur, report errors & wait for keys
	-If no errors occur or F1 key is pressed to continue:
	<ul> <li>Clear EPA or customization logo.</li> </ul>
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook.
	2. Recover the text fond used by EPA logo (not for full screen logo)
	3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization
	2. Switch screen back to text mode
86h	Reserved
87h	NET PC: Build SYSID Structure
88h	Reserved
89h	1. Assign IRQs to PCI devices
8Ah	2. Set up ACPI table at top of memory Reserved
8Bh	1. Invoke all ISA adapter ROMs
001	2. Invoke all PCI ROMs (except VGA)
80h	Reserveu
3011	2. APM Initialization
8Eh	Reserved
8Fh	Clear noise of IRQs
90h	Reserved

CHAPTER 6 -BIOS Setup

POST (hex)	Description
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	<ol> <li>Enable L2 cache</li> <li>Program Daylight Saving</li> <li>Program boot up speed</li> <li>Chipset final initialization.</li> <li>Power management final initialization</li> <li>Clear screen &amp; display summary table</li> <li>Program K6 write allocation</li> <li>Program P6 class write combining</li> </ol>
95h	1. ate keyboard LED & typematic rate
96h	1. Build MP table
	2. Build & update ESCD
	3. Set CMOS century to 20h or 19h
	4. Load CMOS time into DOS timer tick
	5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)