The Embedded I/O Company

TEWS TECHNOLOGIES

TXMC385

Conduction Cooled, 4x 10/100/1000 Mbit/s Ethernet Adapter

Version 1.0

User Manual

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TXMC385-10R

Conduction Cooled, Four channel 10/100/1000 Mbit/s Ethernet interface back I/O, X12d and X8d mapping per VITA46.9, extended temperature range (RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	January 2015

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1 Product Description

The TXMC385 is a Conduction Cooled Switched Mezzanine Card (CCXMC) compatible module providing a four channel Ethernet 10BASE-T / 100BASE-TX / 1000BASE-T interface.

A PCI Express Switch provides access to the Intel™ 82574IT Gigabit Ethernet controllers. Each Ethernet interface supports 10, 100 and 1000 Mbit/s transmission rates for full duplex operation, 10 and 100 Mbit/s transmissions for half duplex operation, and is equipped with a 32 Kbit serial EEPROM.

The four Ethernet interfaces of the TXMC385 are capable of performing an auto-negotiation algorithm which allows both link-partners to determine the best link parameters. The TXMC385 is user configurable via configuration and register accesses over the PCI Express interface.

The TXMC385-10R routes all four 10/100/1000 Mbit/s Ethernet ports to the XMC back I/O P16 connector. Two ports are mapped in the X12d range and two ports are mapped in the X8d range specified in VITA46.9 standard.

All ports are galvanically isolated from the Ethernet controllers and LEDs on the board indicate the different network activities.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

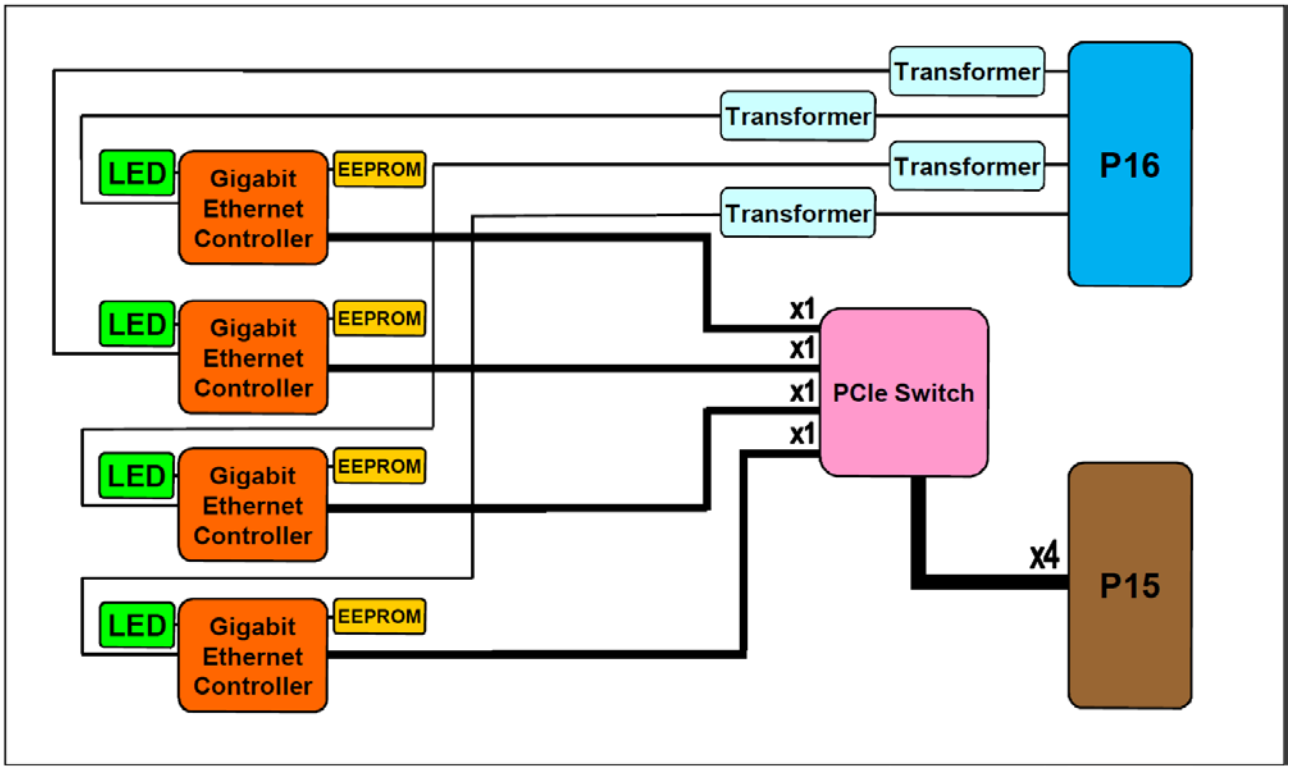

Figure 1-1 : Block Diagram

2 Technical Specification

XMC Interface		
Mechanical Interface	Conduction Cooled Switched Mezzanine Card (CCXMC) Interface conforming to ANSI/VITA 42.0-2008 (Auxiliary Standard) Standard single-width (143.75mm x 74mm)	
Electrical Interface	PCI Express (Base Specification 1.1) up to x4 compliant interface conforming to ANSI/VITA 42.3-2006 (XMC PCI Express Protocol Layer Standard)	
On Board Devices		
PCIe Switch	89HPES8T5A (IDT)	
Gigabit Ethernet Controller	For each interface: 82574IT (Intel)	
IPMI resource FRU Data EEPROM	M24C02 (STMicroelectronics)	
Ethernet Interface		
Number of Interfaces	4	
Link	10Base-T / 100Base-TX / 1000Base-T	
FIFO	For each interface: Configurable receive and transmit data FIFO, programmable in 1 KB increments	
Interrupts	PCIe Switch is able to generate • INTx (x= A, B, C, or D) legacy interrupts • Message Signaled Interrupts (MSIs)	
I/O Connector	XMC P16 back I/O (Samtec ASP-105885-01 or compatible)	
Physical Data		
Power Requirements	300mA typical @ VPWR = +12V DC (no link) app. additional 3mA per 100Mbit/s link app. additional 100mA per 1Gbit/s link 750mA typical @ VPWR = +5V DC (no link) app. additional 7mA per 100Mbit/s link app. additional 250mA per 1Gbit/s link	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	740000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	64 g	

Table 2-1 : Technical Specification

3 PCI Device Topology on TXMC385

The TXMC385 uses four Gigabit Ethernet Controllers (Intel 82574IT) each communicating via a PCIe Rev. 1.1 compliant x1 Interface. To be able to access the Ethernet controllers they are connected to the x1 Downstream Ports of a PCIe Switch (IDT 89HPES8T5A). The x4 Upstream Port of the Switch is connected to the XMC Connector communicating with the host system.

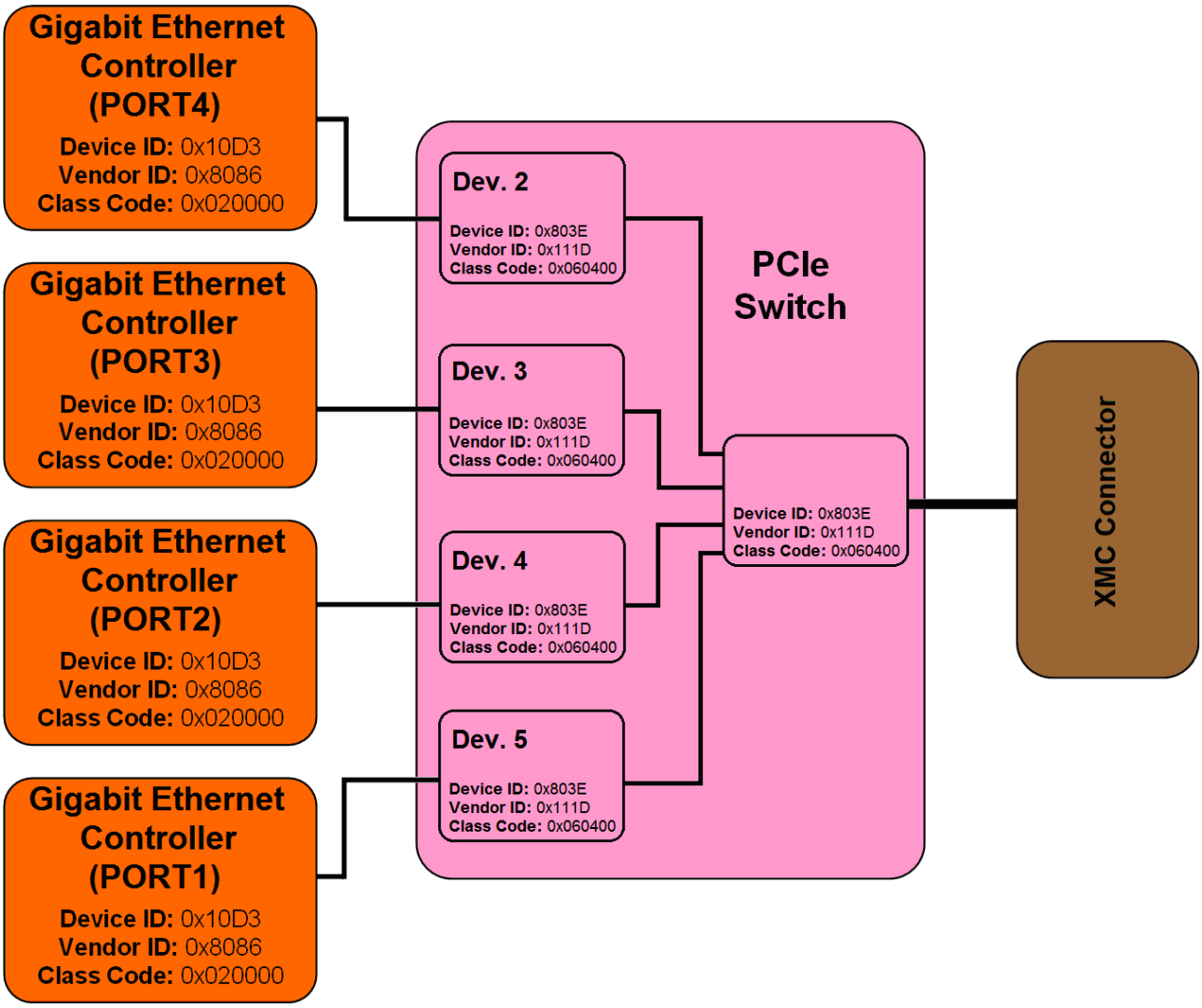

Figure 3-1 : PCI Device Topology

NOTE: Operating systems typically assign the lowest available Ethernet device number to PORT4, thus initializing the four ports in descending order.

4 Gigabit Ethernet Controller

4.1 Intel 82574IT PCI Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				Initial Values (Hex Values)
	31 24	23 16	15 8	7 0	
0x00	Device ID		Vendor ID		10D3 8086
0x04	Status Register		Command Register		0010 0000
0x08	Class Code			Revision ID	020000 00
0x0C	BIST	Header Type	Latency Timer	Cache Line Size	00 00 00 10
0x10	Base Address 0 (Memory BAR)				FFFE0000 (128 KByte)
0x14	Base Address 1 (Flash BAR)				00000000
0x18	Base Address 2 (IO BAR)				FFFFFFE1 (32 Byte)
0x1C	Base Address 3 (MSI-X BAR)				FFFFC000 (16 KByte)
0x20	Base Address 4				00000000
0x24	Base Address 5				00000000
0x28	CardBus CIS Pointer				00000000
0x2C	Subsystem ID		Subsystem Vendor ID		0000 8086
0x30	Expansion ROM Base Address				00000000
0x34	Reserved			Cap_Ptr	000000 C8
0x38	Reserved				00000000
0x3C	Max_Latency	Min_Grant	Interrupt Pin	Interrupt Line	00 00 01 00

Table 4-1 : Intel 82574IT PCI Header

5 LEDs

The TXMC385 provides four Status LEDs for quick visual inspection and debugging. Due to the fact that XMCs are mounted headfirst on the carrier card, the LED indicators are visible on the back side of the TXMC385. A marking is placed close to each LED, to indicate the Ethernet Port the LED corresponds to.

Each Ethernet Port has one LED indicator. See figures below for more details:

LED Status	Description
OFF	No cable is connected or no link is established
ON	A link is established at the corresponding Ethernet Port
BLINKING	Indicates activity: The Ethernet Port transmits or receives data

Table 5-1 : LED Status

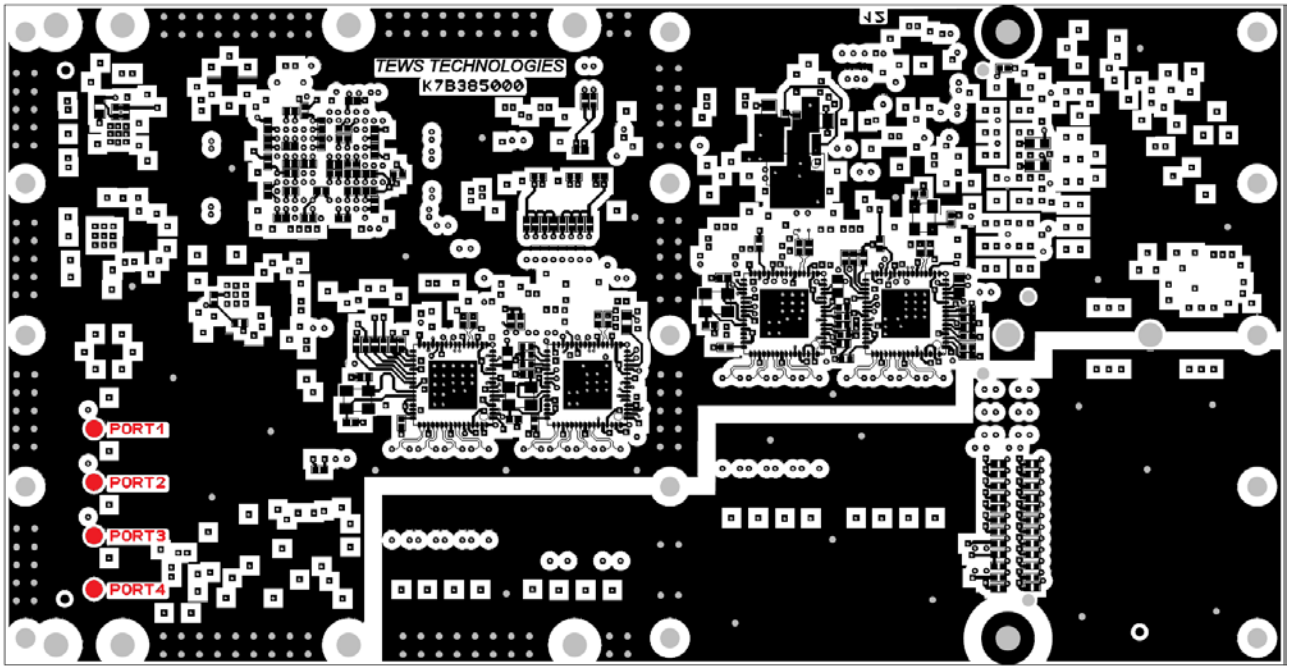

Figure 5-1 : LEDs and markings (bottom view)

6 Pin Assignment – I/O Connectors

6.1 XMC Connector P15

	A	B	C	D	E	F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	$\overline{TRST}$	GND	GND	$\overline{PERST}$
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	TCK	GND	GND	$\overline{MRSTO}$
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	Reserved	Reserved	Reserved	Reserved	Reserved	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	$\overline{MBIST}$	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	$\overline{MPRESENT}$
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	Reserved	PER0p5	PER0n5	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	Reserved	PER0p7	PER0n7	Reserved
18	GND	GND	Reserved	GND	GND	Reserved
19	REFCLK+0	REFCLK-0	Reserved	$\overline{WAKE}$	$\overline{ROOT0}$	Reserved

Table 6-1 : XMC Connector P15

6.2 XMC Back I/O Connector P16

	A	B	C	D	E	F
1	PORT3_MDI0+	PORT3_MDI0-	NC	PORT3_MDI1+	PORT3_MDI1-	NC
2	NC	NC	NC	NC	NC	NC
3	PORT3_MDI2+	PORT3_MDI2-	NC	PORT3_MDI3+	PORT3_MDI3-	NC
4	NC	NC	NC	NC	NC	NC
5	PORT1_MDI0+	PORT1_MDI0-	NC	PORT1_MDI1+	PORT1_MDI1-	NC
6	NC	NC	NC	NC	NC	NC
7	PORT1_MDI2+	PORT1_MDI2-	NC	PORT1_MDI3+	PORT1_MDI3-	NC
8	NC	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC	NC
10	NC	NC	NC	NC	NC	NC
11	PORT4_MDI0+	PORT4_MDI0-	NC	PORT4_MDI1+	PORT4_MDI1-	NC
12	NC	NC	NC	NC	NC	NC
13	PORT4_MDI2+	PORT4_MDI2-	NC	PORT4_MDI3+	PORT4_MDI3-	NC
14	NC	NC	NC	NC	NC	NC
15	PORT2_MDI0+	PORT2_MDI0-	NC	PORT2_MDI1+	PORT2_MDI1-	NC
16	NC	NC	NC	NC	NC	NC
17	PORT2_MDI2+	PORT2_MDI2-	NC	PORT2_MDI3+	PORT2_MDI3-	NC
18	NC	NC	NC	NC	NC	NC
19	NC	NC	NC	NC	NC	NC

Table 6-2 : TXMC385-10R Back I/O Connector P16 (X8d and X12d mapping per VITA46.9)

- PORT1 and PORT2 lie within the X12d mapping (VITA46.9)
- PORT3 and PORT4 lie within the X8d mapping (VITA46.9)