187445

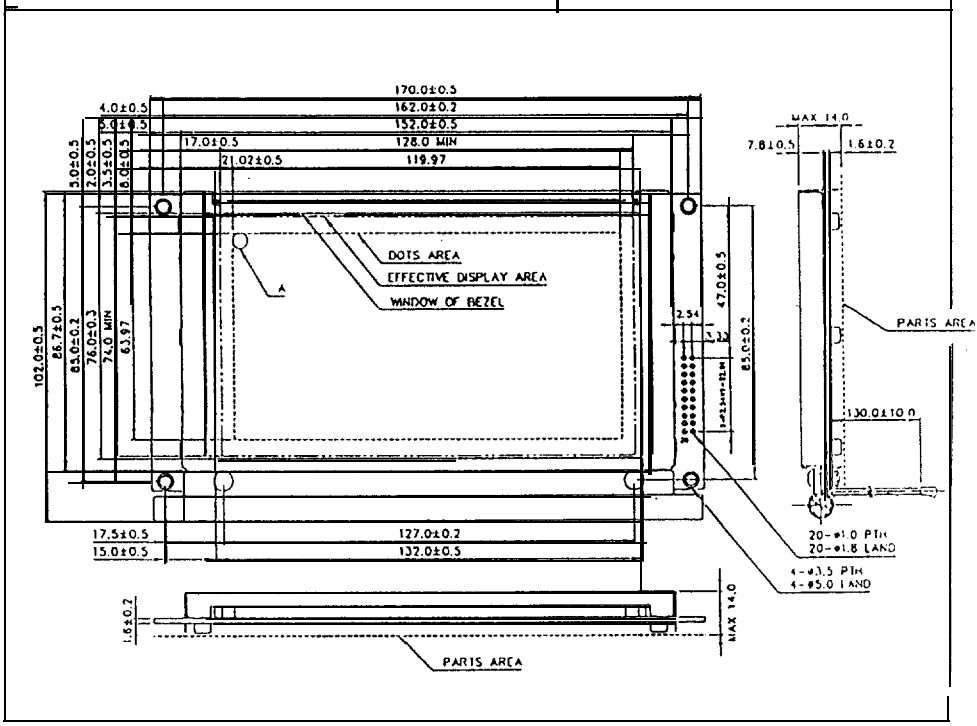
NAN YA

NLC-240x128

LCD Grafik

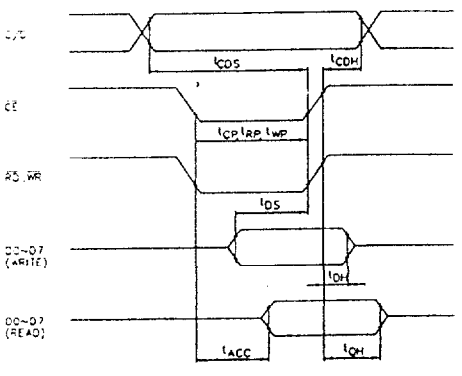
Features

- 240x128 Pixel
  40 Zeichen x 16 Zeilen
- Mit T6963C Controller
- FSTN - Technologie
- Hoher Kontrast
- CFL Backlight
- Displayhelligkeit 80 cd/m²
- 0,47x0,47mm Dotgröße
- 0,03x0,03mm Dotspace
- schwaz/weiß, -blue -Mode
- 6 : 00 (Standard) , 12: 00
- Module Abmessungen
  170 x 102 x 14,5
- Effektive Displayfläche
  132 x 76

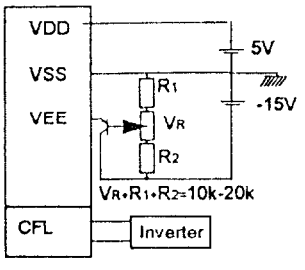


Elektrische und optische Spezifikation (Ta=25°C, Vdd=5,0V)

Beschreibung	Symbol	Min.	Typ.	Max.	[Einheiti	Testbedingung
Power supply Logik	VDD-VSS	4.5	5	5,5	V	
Input Voltage	VIH	0,7VDD	-	VDD	V	H-Level
Input Voltage	VIL	0	-	0,3VDD	v	L-Level
Power Consumtion	Pd		-	300,0	mW	VDD=5V,VEE=-10V
Supply cunent LCD	ILCD	-	-	3,5	mA	VDD=5V,VEE=-10V
LC driving Voltage	VDD-VEE	17.05	17,8	18,55	V	-
Viewing angle	θ	50		-	-	deg	cr ≥2,0
Viewing angle	ϕ	-	-	-	+/- 40	Cr ≥2,0
Contrast ratio	Cr	-	25	-		ϕ=0°, θ=0
Response time (rise)	Tr	-	200	400		ms	ϕ=0°, θ=0°
Response time (fall)	Tr	-	150	350	ms	ϕ=0°, θ=0°
Arbeitstemperatur	Top	0	-	50	°C	
Lagertemperatur	Tst	-20	-	70	°C	
C/D Set up time	tCDS	100		-	-	ns
C/D Hold Time	tcm	10		-	-	ns
CE,RD,WR clock width	tCP,tRP,tWP	80	-	-		ns
Data set up time	tDS	80		-	-	ns
Data hold time	tDH	40		-	-	ns
Access time	tACC	-	-	150		ns
Data output hold time	tOH	10	-	50		ns



Interface timing



Power supply

Internal Pin Connection

Pin	Symbol	Funktion
1	FGND	Frame ground (0V)
2	VSS	0V Power supply , GND
3	VDD	Power Supply for Logic +5V
4	VEE	Power Supply for LC-Driving
5	$\overline{WR}$	Data Write
6	$\overline{RD}$	Data Read
7	$\overline{CE}$	Chip Enable
8	C/D	Command Write $\overline{WR}$="L" C/D="H" Status Read $\overline{RD}$="L" C/D="H" Data Write $\overline{WR}$="L" C/D="L" Data Read $\overline{RD}$="L" C/D="L"
9	NC	No Connection
10	$\overline{RESET}$	Controller Reset
11	D0	Data Input / Output
12	D1	Data Input / Output
13	D2	Data Input / Output
14	D3	Data Input / Output
15	D4	Data Input / Output
16	D5	Data Input / Output
17	D6	Data Input / Output
18	D7	Data Input / Output
19	FS	Font Select FS=VDD 8x8 Pixel/Character FS=GND 8x8 Pixel/Character
20	RV	Reverse

CFL Connector (JAE-Stecker Typ IL-G-5S-S3C2)

Pin	Symbol	Funktion
1	VFL	Power supply for CFL
2	NC	No connection
3	NC	No connection
4	NC	No connection
5	VFL	Power supply for CFL

BESTELLINFORMATIONEN

Beschreibung	Bestellnummer
LCD-Modul,schwarz/weiß,CFL	187445
CFL-Inverter	183571

LCD - Controller

T 6963 C

User's Manual

(Dot matrix LCD control LSI)

[1] Introduction

T6963C is LCD controller designed to be used for control LCD Driver LSIs and display data Memories. It has an 8bit parallel data bus and control lines for reading or writing through a MPU I/F. It to be directly connected TMPZ-80.

It has 128 words Character generator ROM with the capability to control external display RAM of upto 64K bytes. Allocation of text. graphics and external character generator RAM can be easily made and the display window can be freely moved within the allocated memory range.

It supports a very broad range of LCD formats by selecting different combinations on a set of programmable inputs. It can be used in text. graphic and a combination of test and graphic modes and has various attribute functions.

[2] Features

1) Display format (pin selectable)

Columns: 32. 40. 64. 80

Lines : 2. 4. 6. 8. 10. 12. 14. 16. 20. 24. 28. 32

The maximum display size is 80characters ×32lines. But operating iresuency max. is 5. 5MHz. The actual display size max. is about 80characters ×8lines.

2) Characterfont (pin selectable)

Horizontal dots: 5. 6. 7. 8

Vertical dots : 8 (fix)

1t is necessary to define a font not 0nly text mode but graphic mode. The oscillation frequency does not change by font select.

3) DispIa.v duty : 1/16 to 1/ 128

4) Internal 128 words Character generator ROM is built-in. The0101o f T6963C-0101-BS is ROMcode. The Standard numbcr is only the 0101.

5) External display memory: 64KB max.
The display memory address of Text/Graphic/External Character generator is defined by a Software.

6) No noise on the display screen during read/write by MPU.

7) The crystal oscillator circuit built in. The frequency of crystal is adjusted by display size. (see P)
T6963C can be fed the external clock. (XI input, XO output open)
External capacitors crystal: 20-30pF
ceramic: 30-100pF
feedback resistor built in :900KΩtyp

8) TOSHIBA LCD driver LSIs (except RAM built in type) can be connected.

9) Please use static RAM for external display memory. T6963C does not have any time for refreshing.

10) The attribute function is for Text mode. It cannot be for Graphic or Combination Character mode.

[2] Note

1) After power on, it is necessary to reset. RESET is kept "L" between 5 clocks up (oscillation clock)

2) When $\overline{\text{HALT}}$ has been "L", the oscillation is stopped. It is necessary to turn off power supply for LCD. because. LCD goes down by DC bias.

3) The HALT function contains the RESET function.

4) The column/line counter and display register are cleared by RESET.
(Other registers are not cleared)
The display is been off after RESET.

5) Before command and data sending, it is necessary to check the Status.
In case of sending command of MSB is "0" (2 operands), it is necessary to always check the Status. It is impossible to save checking the Status.
(The error is happened by interrupt of hardware.

6) It is necessary to check STA0 and STA1 at the same time. Or the error is happened by sending data when executing command,

7) T6963C manages a byte (8bit) in a machine cycle (16clocks). It is impossible to send over 2 data in a machine cycle. Be careful to use for high speed MPU.

8) In case of command with Operand data, it important to send a command, Operand data has before been set.

9) The Character code of T6963C is different from an ASCII. (See P)

10) After state of RESET/HALT

Terminals	HALT	RESET
D0-D7	F	F
d0~d7	F	F
r/w	H	H
ce	H notel	H notel
ad0 -ad15	H note2	H note2
ce0, ce1	H notel	H notel
ED, HOD	final data	final data
HSCP	L	L
LP	L	L
CDATA	H	H
FR	H	H
CH1	L	KO
CH2	L	VEND
DSPON	L	L
XO	H	OSC clock

H: level H
L: level L
F: Floating (high impedance)
KO: internal state (TEXT data access) normally open.
VEND: End signal of V-counter (line count) if MDS=H, T2=L, HEND (end signal of H-count) normally open.

notel: In Attribute mode, H or L by state of Graphic Pointer.

note2: In Attribute mode, DATA of Graphic Pointer.

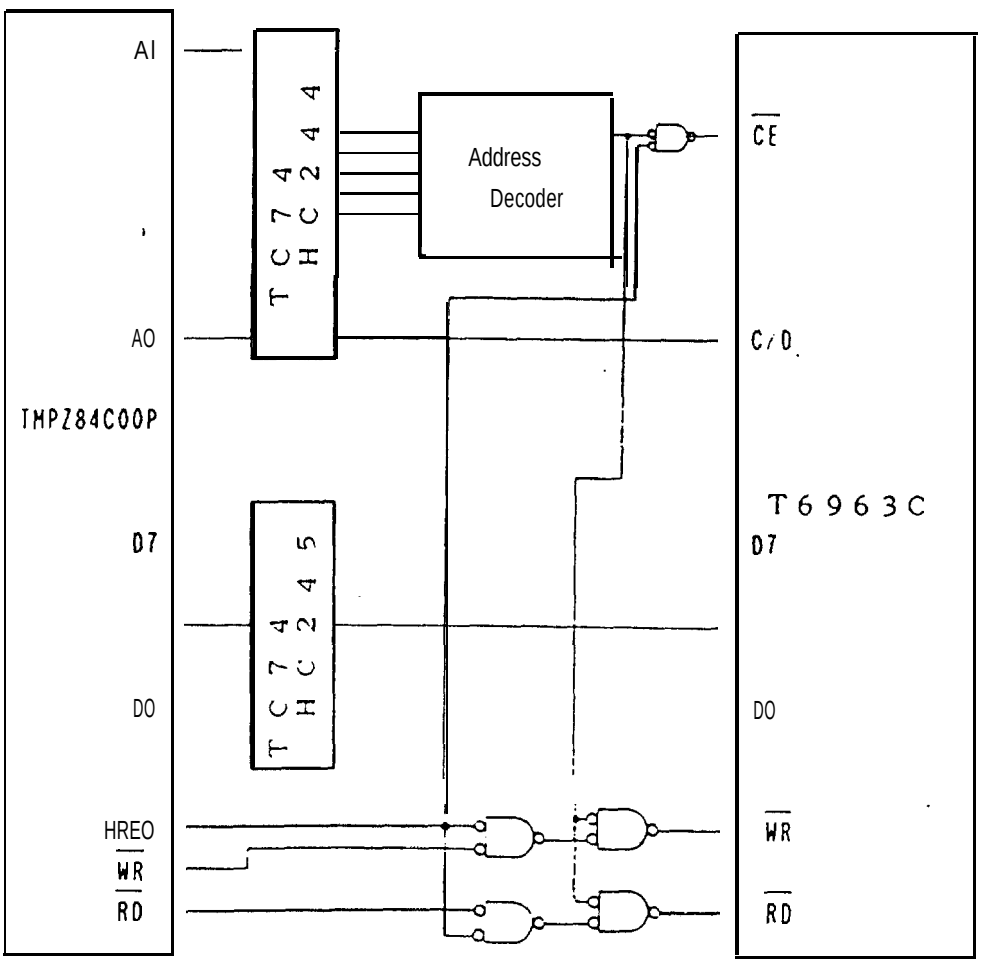
T6963C EXAMPLE OF APPLICATION CIRCUITS

T6963C is directly connected TMPZ84C00A (Z80 NOTE 1 CMOS). T6963C Application circuit can be used with TMPZ84C00A in the following case.

[1] The setting of MPU's address (MAPPED I/O)

T6963C is addressed in a MPU's address by the address decode circu'it.

	address
DAT.4 (I/O)	XXXXH
Command/Status	XXXX+1H

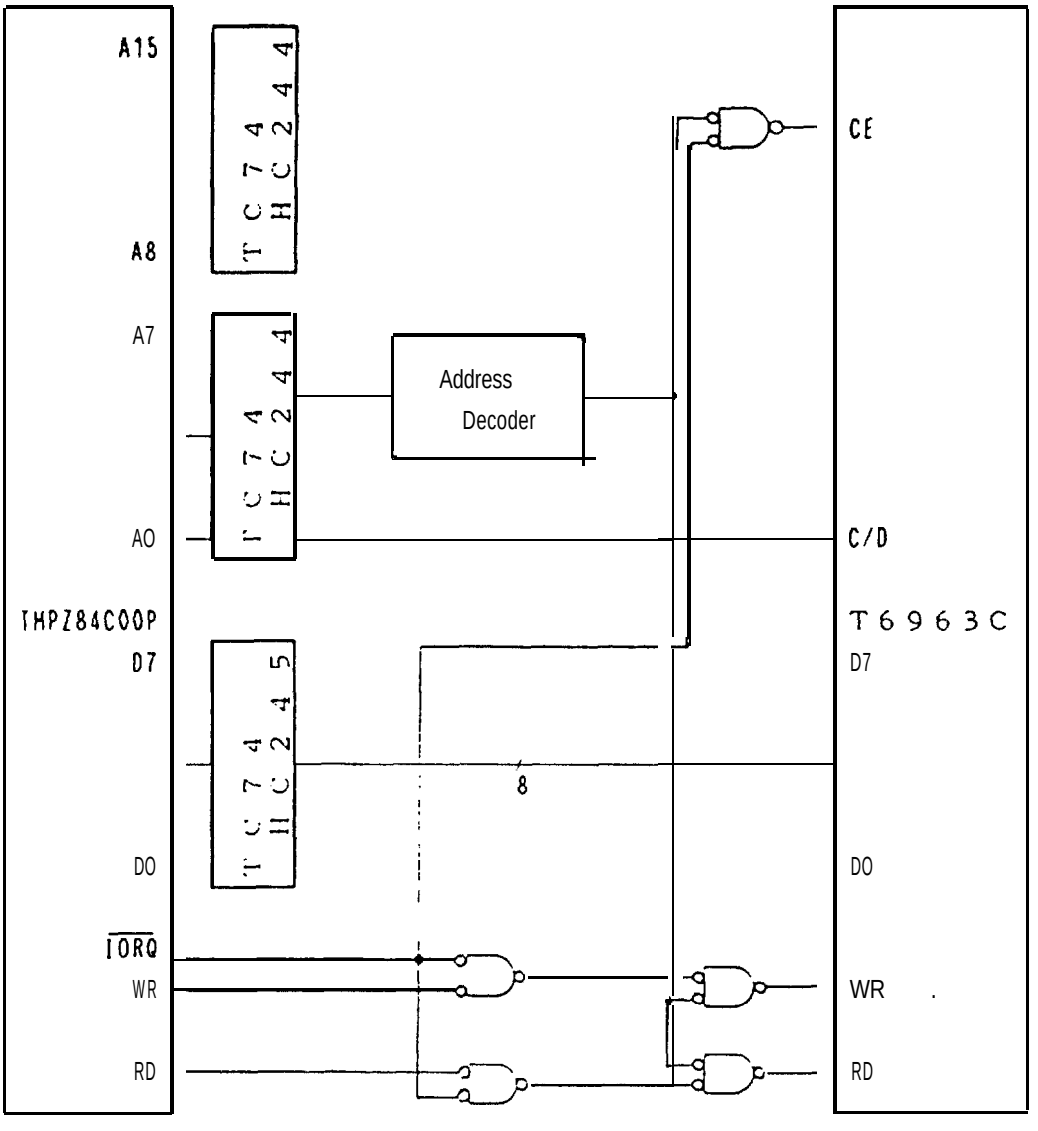


note1 : Z80 is a trademark of Zilog Inc.

[2] The setting of MPU I/O address

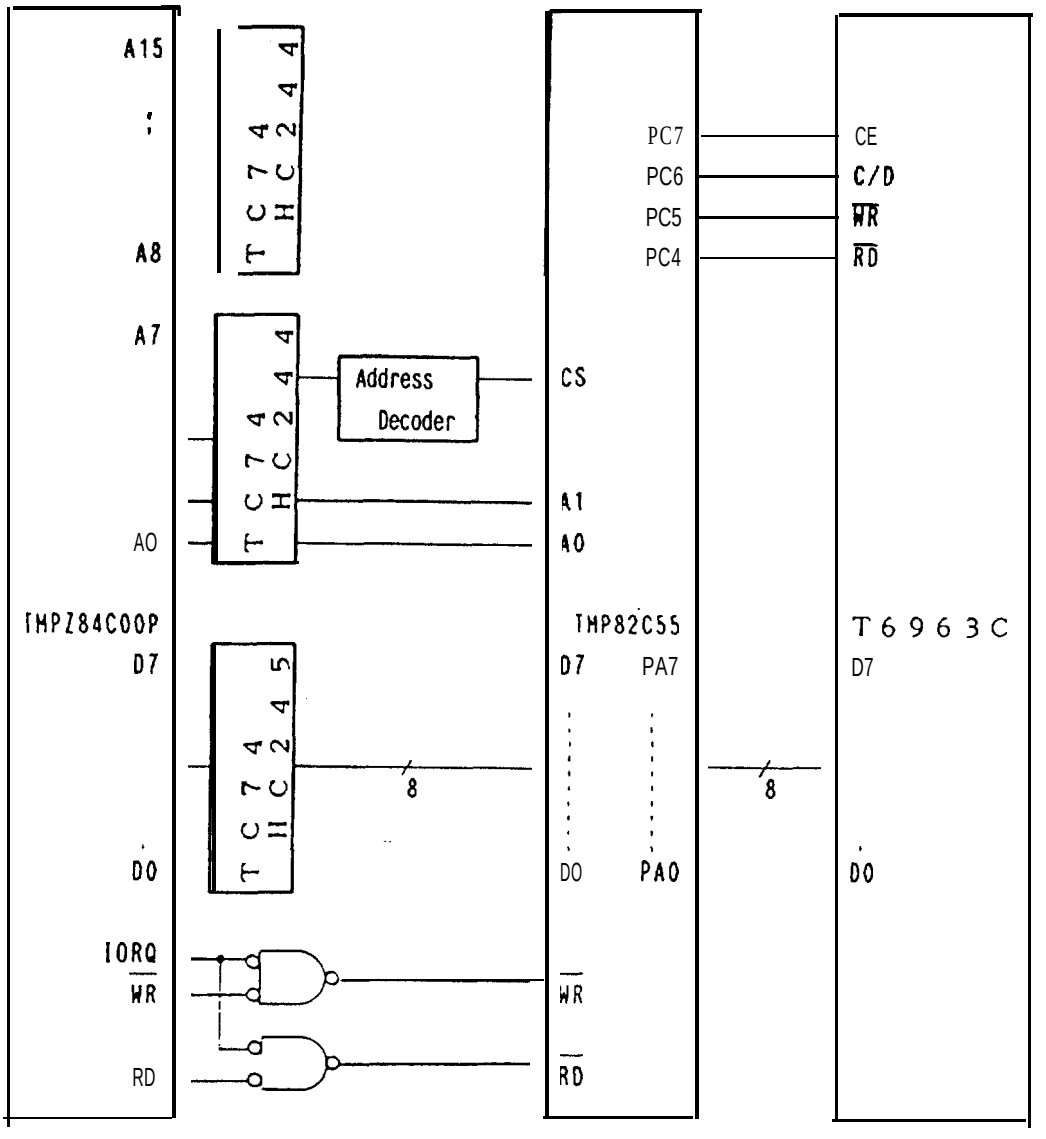
T6963C is addressed in an I/O address by the I/O address decoder.

	I/O address
DATA	XXH
Command/Status	XX+1H.



[3] The case of using PPI LSI (TMP82C55)

T6963C can be connected with PPI LSI.
The portA connects data bus.
The portC connects control bus.
(C/D, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$)



RAM interface

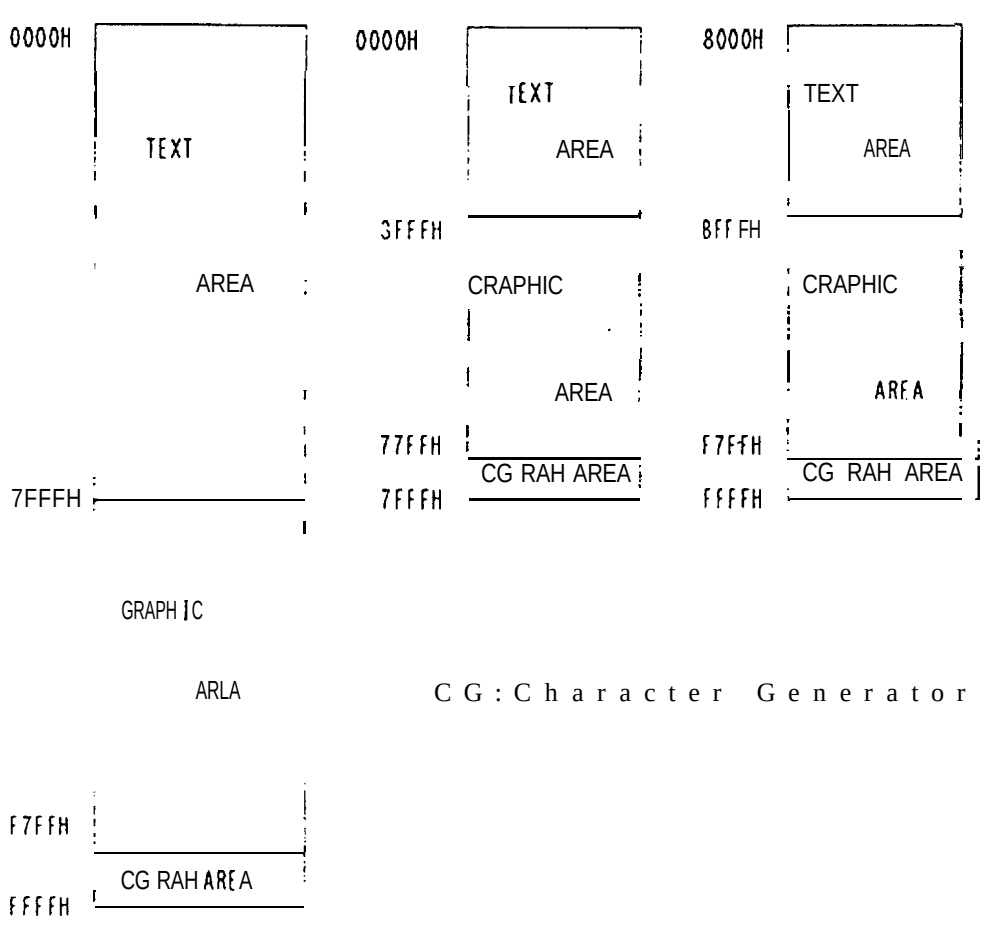
The external RAM is used for store display data (text, graphic. external CG)

The case of 1 screen driving, it can be freely allocate text data, graphic data, external CG data in memory area (64KBmax).

The case of 2 screen drivin'g, LCDI is allocated in OOOOH-7FFFH (32KBmax), LCDII is allocated in 8000H~FFFFH (32KBmax). It can be freely allocate text data. graphic data, external CG data in LCDI. In LCDII, it is necessary to allocate same address (except ad15) of LCDI. (the exchange of LCDI/LCD II is done by "ad15")

It can be use the address decoded signal sce0 (0000~07FFH), cel (0800~0FFFH) within 4KB.

EX)



CG: Character Generator

FLOWCHART OF COMMUNICATIONS WITH MPU

1] Status read
Before sending data(read/write), command it is necessary to check the Status.

Status check
Status of T6963C can be read from data lines.

$\overline{RD}$	L
$\overline{WR}$	H
$\overline{CE}$	L
C/$\overline{D}$	H
D0-D7	Status word

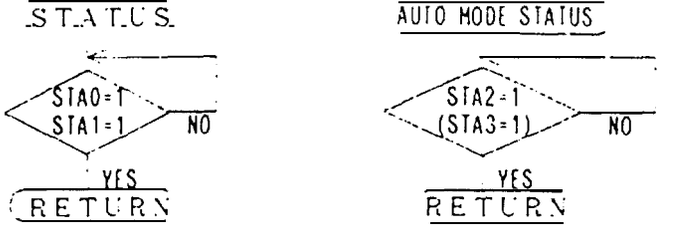
T6963C. Status word format is following.

MSB							LSB
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0
D7	D6	D5	D4	D3	D2	D1	D0

STA0	check capability of conmand execution	0: disable 1: enable
STA1	check capability of data read/write	0: disable 1: enable
STA2	check capability of auto mode data read	0: disable 1: enable
STA3	check capability of auto mode data write	0: disable 1: enable
STA4	not use	
STA5	check capability of controller Operation	0: disable 1: enable
STA6	error flag. using screen peek/copy command	0: no error 1: error
STA7	Check the condition blink	0: display off 1: normal display

Note)
1. It is necessary to check STA0 and STA1 at the same time. The error is happened by sending data at execut-ing command.
2. The status check will be enought to check STA0 STA1.
3. The STA2 STA3 are valid in auto mode ST.40 STA1 at-e invalid.

Status checking flow



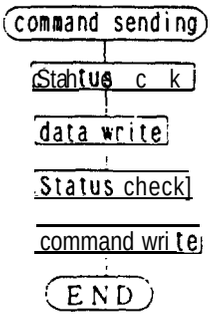
4. It is impossible to save **status** check in the **case** of command that is MSB 0. To have the delay time **cannot** be **save status** check.
   The **interrupt** of hardware is happened at the end of 1**ines. If** command of MSBO is sended in this period. the command **executing** is waited. The state of waiting doesn't be known **without** to check status. The **sending next** command or data **is** disregarded or rewrites data of waiting command. .

2] Data set

In T6963C, the data have been set and command executes.

The order of procedure of command sending

① the case of 1 data



② the case of 2 data

Note: In case of over 2 data sending, the last data (or last 2 data) is valid.

COMMAND	CODE	D1	D2	FUNCTION
REGISTER SET	00100001	X adrs	Y adrs	CURSOR POINTER SET
	00100010	data	00H	OFFSET REGISTER SET
	00100100	low adrs	High adrs	ADDRESS POINTER SET
CONTROL WORD SET	01000000	Low adrs	High adrs	TEXT HOHE ADDRESS SET
	01000001	Columns	00H	TEXT AREA SET
	01000010	Low adrs	High adrs	GRAPHIC HOHE ADDRESS SET
	01000011	Columns	00H	CRAPHIC AREA SET
MODE SET	1000x000	-		"OR" mode
	1000X001	-	-	"EXOR" mode
	1000x011	-	-	"AND" mode
	1000x100	-	-	"TEXT ATTRIBUTE" mode
	1 ooooxxx	-		INTERNAL CG ROM mode
	10001XXX	-		EXTERNAL CG RAH mode
DISPLAY MODE	10010000	-	-	DISPLAY OFF
	1001XX10	-	-	CURSOR ON, BLINK OFF
	1001XX11	-	-	CURSOR ON, Bt INK ON
	100101XX	-	-	TEXT ON GRAPHIC OFF
	100110XX	-	-	TEXT OFF. GRAPHIC ON
	100111XX	-	-	TEXT ON, CRAPHIC ON
CURSOR PATTERN SELECT	10100000	-	-	1LINE CCRSOH
	10100001	-		2LINES CURSQR
	10100010	-		3LINES CURSOR
	10100011	-	-	4LINES CURSOR
	10100100	-	-	5LINES CCRSOR
	10100101	-	-	6LINES CL'RSOR
	10100110	-	-	7LI NES CCRSOR
	10100111	-	-	8LINES CCRSOR
DATA AUTO READ/WRITE	10110000	-	-	DATA AUTO WRITE SET
	10110001	-	-	DATA AUTO READ SET
	10110010	-	-	AUTO RESET

COMMAND	CODE	D1	D2	FUNCTION
DATA READ WRITE	11000000	data	–	DATA WRITE AND ADP INCREMENT
	11000001	–	–	DATA READ AND ADP INCREMENT
	11000010	data	–	DATA WRITE AND ADP DECREHENT
	11000011		– –	DATA READ AND ADP DECREHENT
	11000100	data	–	DATA WRITE AND ADP NONVARIABLE
	11000101	–	–	DATA READ AND ADP NONVARIABLE
SCREEN PEEK	11100000	–	–	SCREEN PEEK
SCREEN COPY	11101000			SCREEN COPY
BIT SET/ RESET	11110XXX	–	–	BIT RESET
	11111XXX	–	–	BIT SET
	1111x000	–	–	BIT0(LSB)
	1111x001	–	–	BIT1
	1111x010	–	–	BIT2
	1111x011	–	–	BIT3
	1111X100	–		BIT4
	1111X101	–	–	BIT5
	1111X110	–		B1TG
	11115111	–	–	BITi(MSB)

Description of command

1) Register set

CODE	FUNCTION	D1	D2
00100001	21H CURSOR POINTER SET	XADRS	YADRS
00100010	22H OFFSET REGISTER SET	data	00H
00100100	24H ADDRESS POINTER SET	LOW ADRS	HIGH ADRS

①CURSOR POINTER SET

The position of cursor is Specified by XADRS. YADRS. The cursor Position is moved only by this command. The cursor Pointer doesn't have the function of increment and decrement. The shift of cursor are set by this command.

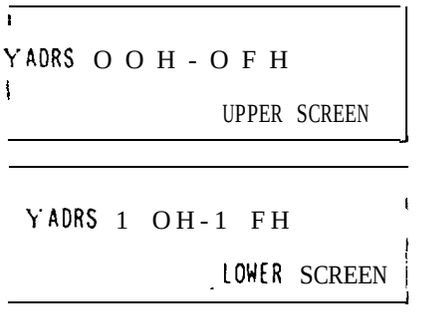
XADRS. YADRS are specified folowing

XAORS 00H-4FH (lower 7bits are valid)

YADRS 00H~1FH (lower 5bits are valid)

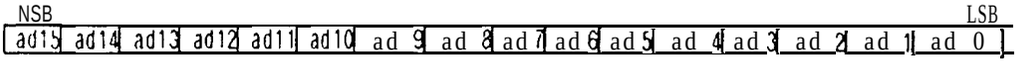
A) 1screen drive
XADRS 00~4FH

B) 2screen drive
XADRS 00-4 FH



②OFFSET REGISTER SET

The offset register is used to determine external Character generator RAM area.
T6963C has 16bit address lines as follow



The upper 5bit (ad15~ad11) are determined ,by offset register-.
The middle 8bit (ad10~ad3) are determined by Character code.
The lower 3bit (ad2~ad0) are determined by vertical counter
The lower 5bit of D1 (data) are valid.

The data format of external Character generator RAM

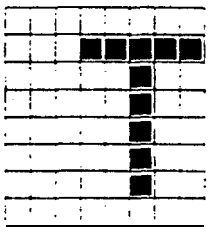
1] The relationship of display RAM address and offset register

data of offset register	CG RAM HEX. address(start-end)
00000	0000-07FFH
00001	0800-0FFFH
00010	1000-17FFH
11100	E000-E7FFH
11101	E800-EFFFH
11110	F000-F7FFH
11111	F800-FFFFH

ex1) offset register 02H
Character code 80H

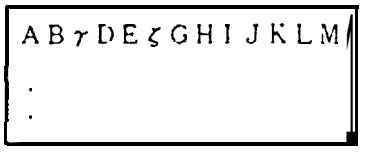
Character generator RAM start address

0001 0100 0000 0000
1 4 0 0 H



address	data
1400H	OOH
1401H	1FH
1402H	04H
1403H	04H
1404H	04H
1405H	04H
1406H	04H
1407H	00H

ex2) The relationship of display RAM data and display Character



display Character

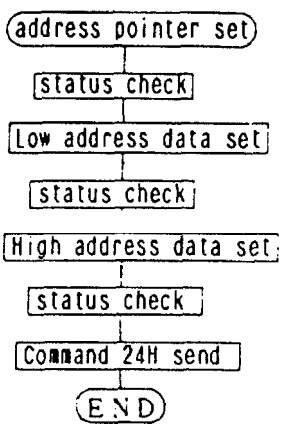
RAM DATA	Character
21H	A
22H	B
83H	γ
24H	D
25H	E
86H	ζ

γ and ζ at-e displayed by character generator RAM.

③Address Pointer set

The address pointer set command is used to indicate the start address for writing (or reading) to external RAM.

The flow chart of address pointer set comnand



2] Control word set

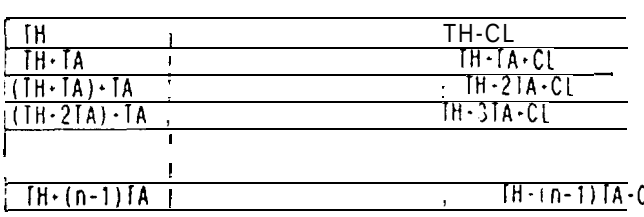
CODE	FUNCTION	D1	D2
0 1 0 0 0 0 0 0	40H TEXT HOHE ADDRESS SET	low adrs	High adrs
0 1 0 0 0 0 0 1	41H TEXT AREA SET	Co lumns	00H
0 1 0 0 0 0 1 0	4211 CRAPHIC HOHE ADDRESS SET	Low adrs	High adrs
0 1 0 0 0 0 1 1	43H GRAPHIC AREA SET	Columns	00H

The home address and column size'are defined by this command.

①Text home address set

The starting address of external dispiay RAM for Test display is defined by this commmand. The text home address shows the left end and most upper Position,

Therelationship of external display RAH address and di splay Position



ex) Text home address 0000H
Test area 0020H
HD2=H, HD3=H : 32columns
DUAL=H, MD5=L, MD0=L, MD1=H :4lines

0000H-0001H	001EH-001FH
0020H-0021H	003EH-003FH
0040H-0041H	005EH-005FH
0060H-0061H	007EH-007FH

②Graphic home address set

The starting address of external display RAM for Graphic display is defined by this command. The graphic home address shows the left end and most upper 1 ine.

The relationship of external display RAH address and display Position

CH		GH+Cl
GH+GA		GH+GA+CL
(GH+GA)+GA		GH+2GA+CL
(GH+2GA)+GA		GH+3GA+CL
GH+(n-1)GA		GH+(n-1)GA+CL

GH:GraphicHome address
GA:Graphic area number(columns)
Cl:Columns are fixed by hardware. (pin-programmable)

ex) Graphic home address OOOOH
Graphic area 0020H
MD2=H,MD3=H :32columns
DUAL=H,MDS=L,MDO=H,MD1=H :2lines

0000H	0001H		001EH 001FH
0020H	0021H		003EH 003FH
0040H	0041H		005EH 005FH
0060H	0061H		007EH 007FH
0080H	0081H		009EH 009FH
00A0H	00A1H		00BEH 00BFH
00C0H	00C1H		00DEH 00DFH
00E0H	00E1H		00FEH 00FFH
0100H	0101H		011EH 011FH
0120H	0121H		013EH 013FH
0140H	0141H		015EH 015FH
0160H	0161H		017EH 017FH
0180H	0181H		019EH 019FH
01A0H	01A1H		01BEH 01BFH
01C0H	01C1H		01DEH 01DFH
01E0H	01E1H		01FEH 01FFH

③Text area set

The columns of display are defined by the hardware setting. This command can be used to adjust columns of display.

es) LCD size: 20columns, 4lines
Texthomeaddress : OOOOH
TextArea:0014H
MD2=H,MD3=H : 32columns
DUAL=H, MDS=L, MD0=L, MD1=H : 4lines

0000	0001	·····	0013	0014	····	001F
0014	0015	·····	0027	0028	····	0033
0028	0029	·····	003B	003C	····	0047
003C	003D	·····	004F	0050	····	005B

i-----LCD ←

④Graphic area set

The columns of display are defined by the hardware setting. This command can be used to adjust columns of graphic display.

ex) LCD size: 20 columns, 2 lines
Text home address : 0000H
Text Area: 0014H
MD2=H, MD3=H : 32 columns
DUAL=H, MDS=L, MD0=H, MD1=H: 2 lines

0000	0001	· · · · · · ·	0013	0014	· · · · ·	001F
0014	0015	· · · · · · ·	0027	0028	· · · · ·	0033
0028	0029	· · · · · · ·	003B	003C	· · · · ·	0047
003C	003D	· · · · · · ·	004F	0050	· · · · ·	005B
0050	0051	· · · · · · ·	0063	0064	· · · · ·	006F
0064	0065	· · · · · · ·	0077	0078	· · · · ·	0083
0078	0079	· · · · · · ·	008B	008C	· · · · ·	0097
008C	008D	· · · · · · ·	009F	00A0	· · · · ·	00AB
00A0	00A1	· · · · · · ·	00B3	00B4	· · · · ·	00BF
00B4	00B5	· · · · · · ·	00C7	00C8	· · · · ·	00D3
00C8	00C9	· · · · · · ·	00DB	00DC	· · · · ·	00E7
00DC	00DD	· · · · · · ·	00EF	00F0	· · · · ·	00FD
00F0	00F1	· · · · · · ·	0103	0104	· · · · ·	011F
0104	0105	· · · · · · ·	0127	0128	· · · · ·	0123
0128	0129	· · · · · · ·	013B	013C	· · · · ·	0147
013C	013D	· · · · · · ·	014F	0150	· · · · ·	015B

→ LCD ←

The address in graphic area can be continuous and RAM area can be used without uneffective area, if graphic area is defined the same number as the actual column number of LCD display.

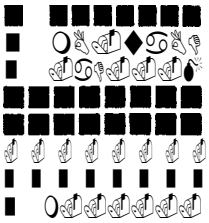
3) Mode set

CODE	FUNCTION	OPERAND
1000X000	"OR" mode	–
1000X001	"EXOR" mode	–
1000X011	"AND" mode	–
1000X100	"TEXT ATTRIBUTE" mode	–
10000XXX	INTERNAL CHARACTER GENERATOR MODE	–
10001XXX	EXTERNAL CHARACTER GENERATOR MODE	–

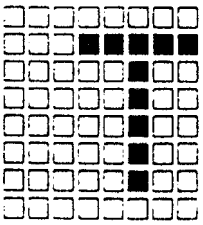
The display mode is defined by this command. The display mode don't have changed untilt o send next this command. Logically "OR", "EXOR", "AND" of text and graphic display can be displayed.

When internal Character generator mode is selected. Character code 00H~7FH are selected from built-in Character gene-rator ROM. The Character code 80H~FFH are automatically selected from external character generator RAM.

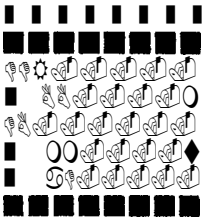
ex)



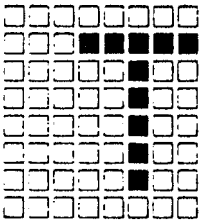
Graphic



Test



"OR"



"AND"

"EXOR"

Note: Only text display is attributed. because attribute data is located in graphic RAM area.

Attribute function

"Reverse display". "Character blink" and "Inhibit" at-e called "Attribute". The attribute data is written in the graphic area difined by C0ntrol word set command. The mode set comma n.d selects text display on'ly and graphic display cannot be displayed.

The attritute data of the 1st charac-ter in text area is writtena t the lstlbyte in graphic area . and attribute data of n-th Character is writtena t the n-th 1byte in graphic area. Attribute functi0n is defined as follow.

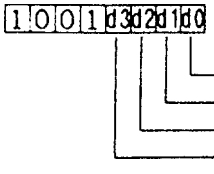
Attribute RAH lbyte | X X X X d3 d2 d1 d0

d3	d2	d1	d0	FUNCTION
0	0	0	0	normal display
0	1	0	1	reverse display
0	0	1	1	inhibit display
1	0	0	0	blink of normal display
1	1	0	1	blink of reverse display
1	0	1	1	blink of inhibit display

X: don't care

4) Display mode

CODE	FUNCTION	OPERAND
100100000	display off	–
1001XX10	cursor on. blink off	
1001XX11	cursor on. blink on	–
100101XX	text on. graphic Off	–
100110XX	text Off, graphic on	–
100111XX	text on, graphic on	–



Note: It is necessary to turn on "text display" and "graphic display" in foilowing case.

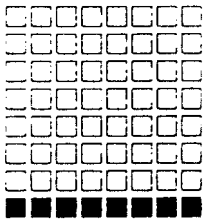
1) Combination of text/graphic display

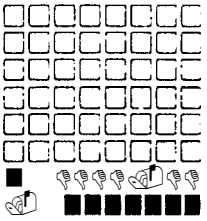
2) Attribute function

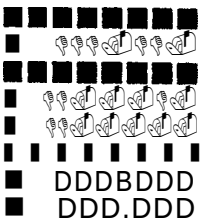
5) Cursor pattern select

CODE	FUNCTION	OPERAND
101000000	lline cursor	–
101000001	2lines cursor	–
101000010	31ines cursor	–
101000011	4lines cursor	–
101000100	5lines cursor-	–
101000101	6lines cursor	–
101000110	7lines cursor	–
101000111	81ines cursor	–

When cursor display is OS. this command selects the cursor Pattern from lline to 8lines. The cursor address is defined by cursor pointer set command.


lline cursor


2lines cursor



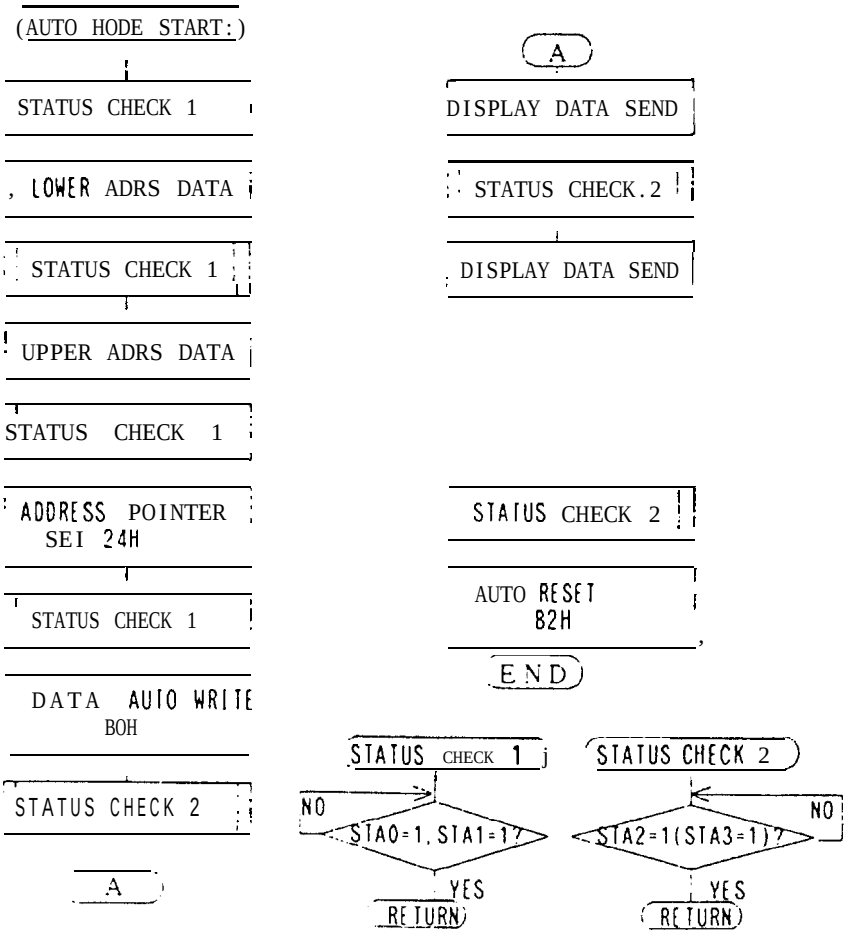
8lines cursor

6) Data auto read / write

CODE		FUNCTION	OPERAND
10110000	B0H	data auto write set	—
10110001	B1H	data auto read set	—
10110010	B2H	auto reset	

This command is convenient to send full screen data from external display RAM. After setting auto mode. "data write (or read)" command is not necessary between each data. "'Data auto write (or read)" command should follow the "Address pointer set" and address pointer is automatically increment by +1 after each data. After sending (or receiving) all data "aut0 reset" is necessary to return normal Operation because all data is regarded "display data" and no command can be accepted in the auto mode.

Note: Status check for auto mode (STA2, STA3 should be checked between each data., Auto reset should be performed after checking STA3=1 (STA2=1). Refer following flowchart.



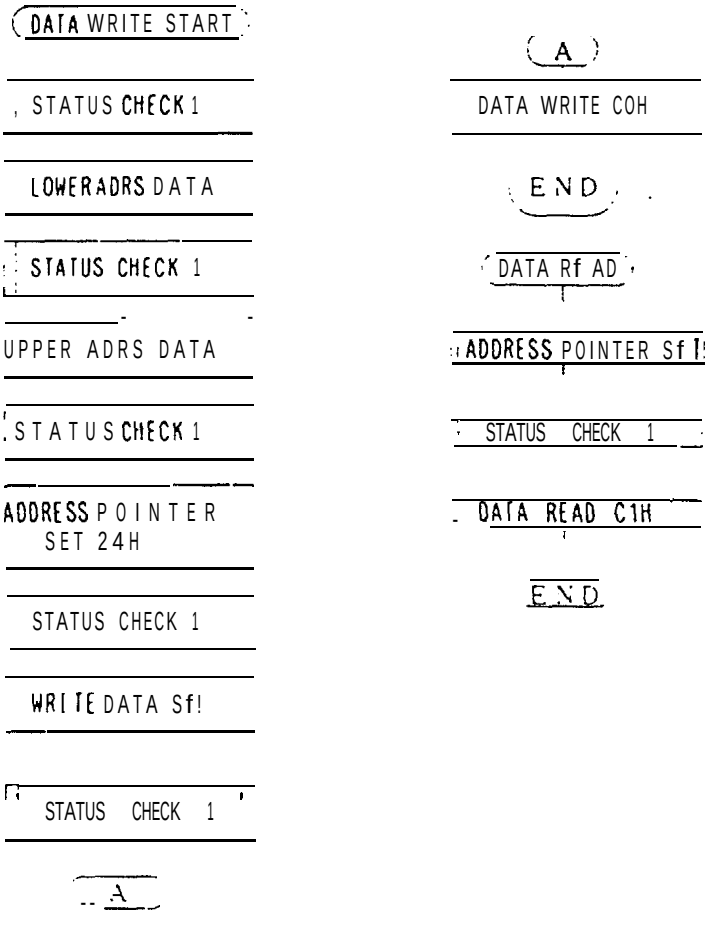
7) Data read write

CODE		FCNCTION	OPERAND
11000000	C0H	DATA WRITE AND ADP INCREMENT	data
11000001	C1H	DATA READ AND ADP INCREHENT	
11000010	C2H	DATA WRITE AND ADP DECREMENT	data
11000011	C3H	DATA READ AND AOP DECREMENT	
11000100	C4H	DATA WRITE AND ADP NONVARIABLE	data
11000101	C5H	DATA READ AND ADP NONVARIABLE	—

This command is used for data write from MPU to external display RAM, and data read from external display RAM to MPU. Data write/data read should be executed after setting address by address pointer set command. Address pointer can he auto-matically increment or decrement by setting this command.

Note: This command is necessary for each 1 byte data.

Refer following flowchart.



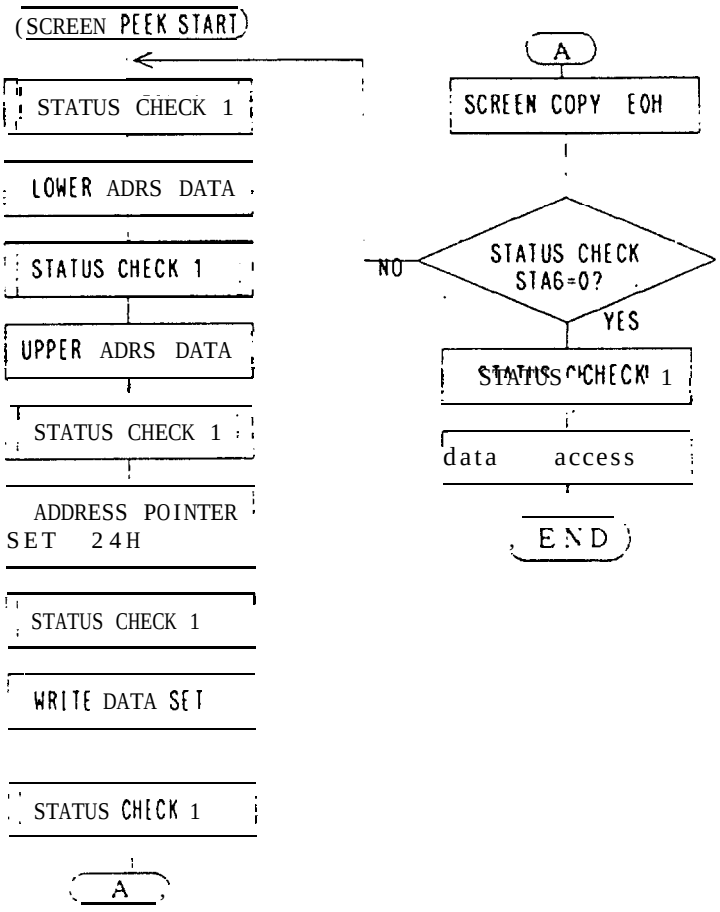
8) Screen peek

CODE	FUNCTION	OPERAND
11 100000	EOH screen peek	

This command is used to transfer displayed 1byte data to data stack and this 1byte data can be read from MPU by data access.
The logical combination data of text and graphic display on LCD screen can be read by this command.

The status (STA6) should be checked just after "screen peek" command. If the address determined by "address Pointer set" command is not in graphic area, this command ignored and status flag (STA6) is set.

Refer following flow chart.



9) Screen copy

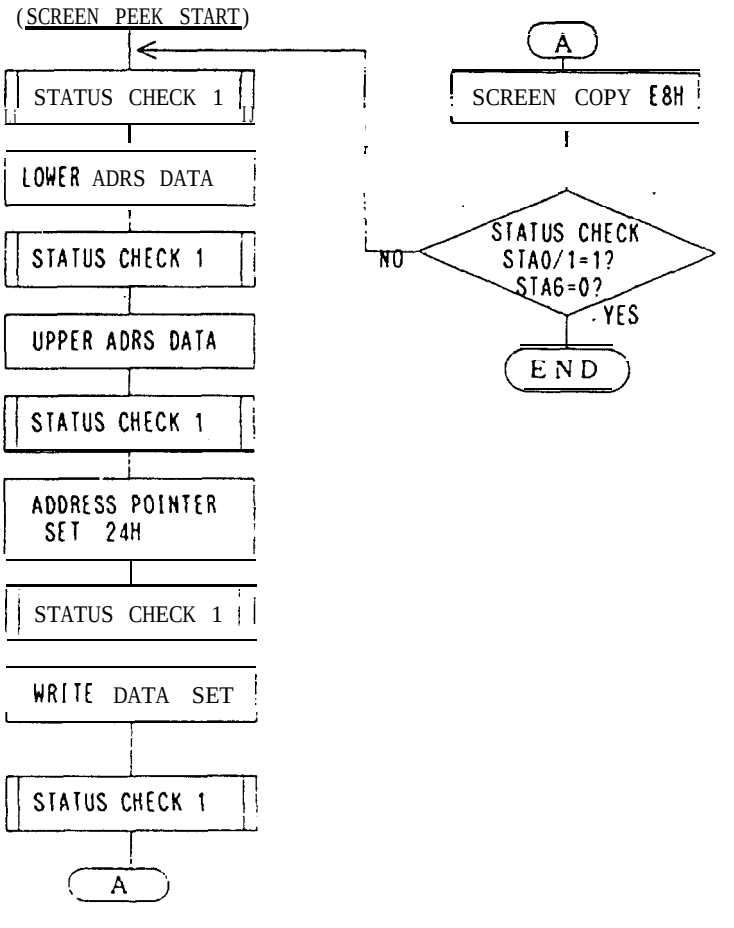
CODE	FUNCTION	OPERAND
1 1 1 0 1 0 0 0	E8H screen copy	

This command is used to copy displayed line data to graphic area. The start point of line data in the screen is determined by the address Pointer.

Note: ① When the attribute of text is used this command cannot be used. (because attribute data is in the graphic area.)

② In case of 2 screen drive, this command cannot be used. (because T6963C cannot separate upper screen data and lower screen data.)

Refer following flow chart.

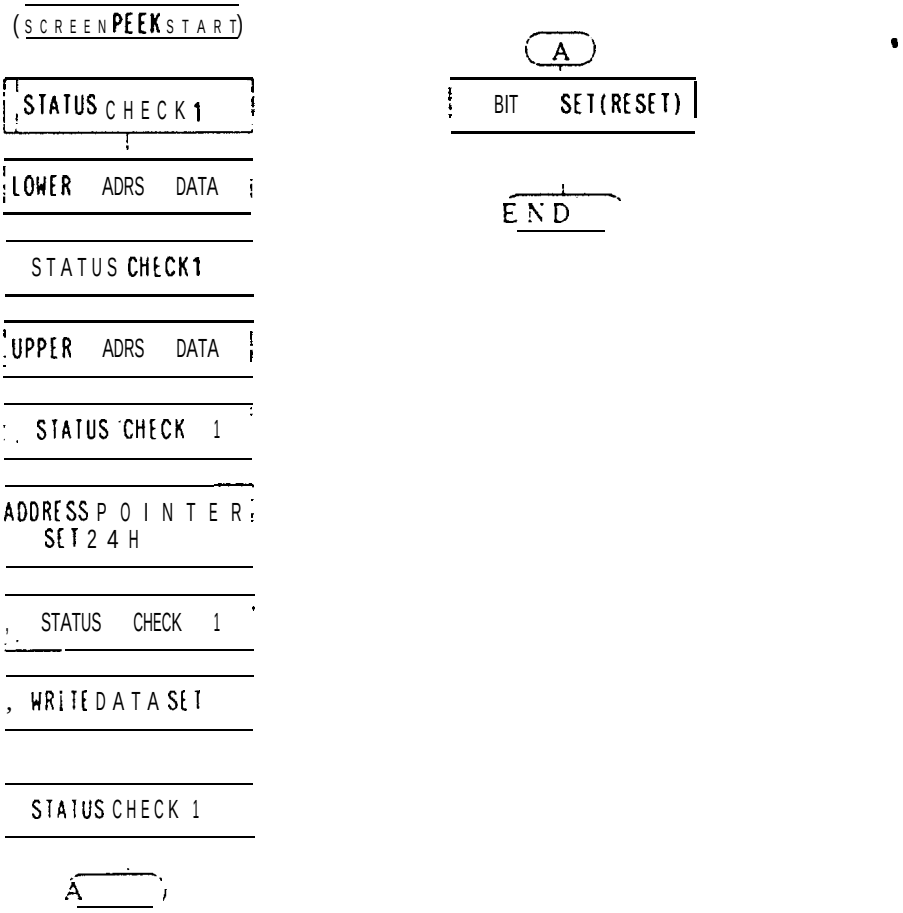


10) Bit set/reset

CODE	FUNCTION	OPERAND
1111 0XXX	bit reset	–
1111 1XXX	bit set	
1111x000	bit 0 (LSB)	
1111x001	bit 1	
1111x010	bit 2	
1111x011	bit 3	–
1111x100	bit 4	–
1111x101	bit 5	
1111x110	bit 6	
1111x111	bit *i* (MSB)	

This command is used to set or reset a bit of 1byte is specified by address Pointer. Plural bits in the 1byte data cannot be set/reset at a time.

Refer following flow chart.



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

ITEM	SYMBOL	CONDITIONS	RATING	UNIT
Supply Voltage	VDD	Ta=25 ℃	-0.3～+7.0	V
Input Voltage	VIN	Ta=25 ℃	-0.3～VDD+0.3	V
Operating Temperature	Topr		-10～+70	℃
Storage Temperature	Tstg		-55～+125	℃

Note: Values measured at VSS=0V.

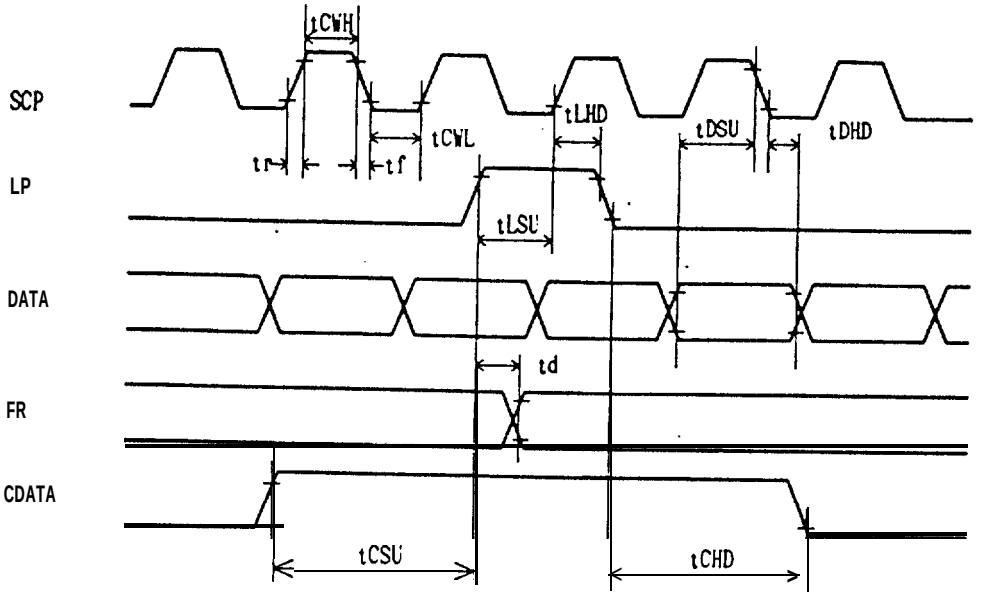
Electrical Characteristics

Test Conditions Unless Otherwise Specified, VSS=0V, VDD=+5V±10%, Ta=25℃

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	VDD		+4.5	+5.0	+5.5	V
"H" Input Voltage	VIH		VDD-2.2	—	VDD	V
"L" Input Voltage	VIL		0	—	+0.8	V
"H" Output Voltage	VOH		VDD-0.3	—	VDD	V
"L" Output Voltage	VOL		0	—	+0.3	V
"H" Output Resistance	ROH	VOUT=VDD-0.5V	—	—	400	Ω
"L" Output Resistance	ROL	VOUT=+0.5V	—	—	400	Ω
Input Pullup(note1) Resistance	RPU		50	100	200	KΩ
Operating Frequency	fosc		0.4	—	5.5	MHz
Current Conswption (Operating)	IDD(1)	VDD=5.0V (note2) f o=3.0MHz	—	3.3	6	mA
Current Consurption (Halt)	IDD(2)	VDD=5.0V	—		3	It4

(note1): Applied $\overline{T1}$, $\overline{T2}$, $\overline{RESET}$
(note2): MDS="L", MDO="L", MD1="L", MD2="H", MD3="H", FSO="L", FS1="L", SDSEL="L", $\overline{DUAL}$="H", D7～0="LHLHLHLH"

Switching Characteristics (1)

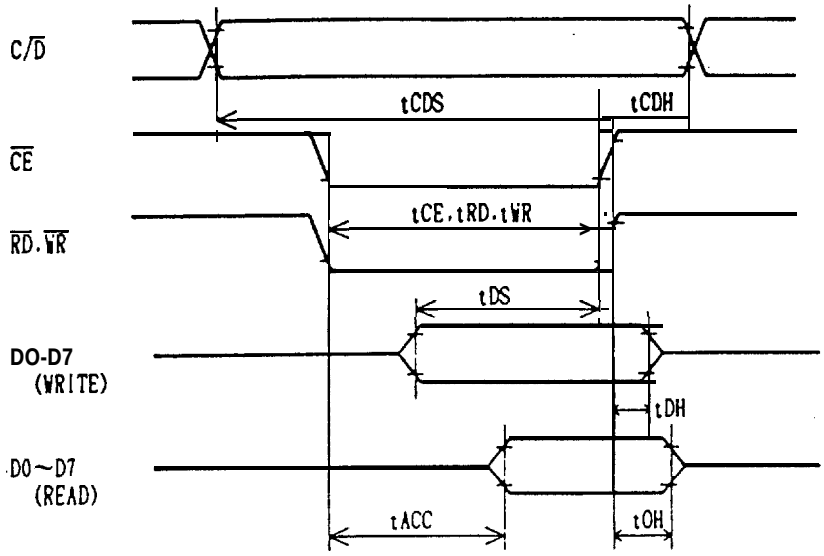


VSS=0V, VDD=+5V±10%

ITEM	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Operating Frequency	fSCP	Ta=-10~+70 °C	–	2.75	MHz
SCP Pulse Width	tCWH, tCWL		150	–	ns
SCP Rise/Fall Time	tr, tf		–	30	ns
LP Set Up Time	tLSU		150	290	ns
LP Hold Time	tLHD		5	40	ns
Data Set Up Tise	tDSU		170	–	ns
Data Hold Tise	tDHD		80	–	ns
FR Delay Time	td		0	90	ns
CDATA Set Up Time	tCSU		450	850	ns
CDATA Hold Time	tCHD		450	950	ns

Switching Characteristic (2)

Bus Timing

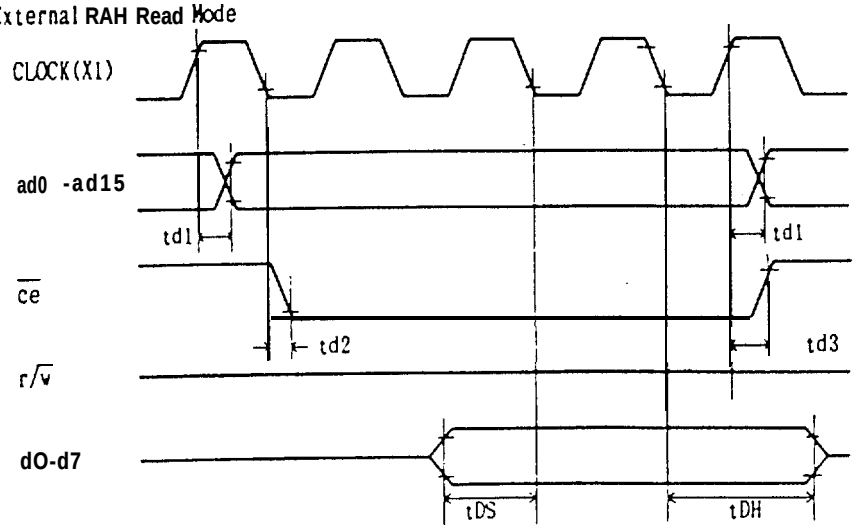


VDD=5V±10%, VSS=0V, Ta=-10 ~ +70℃

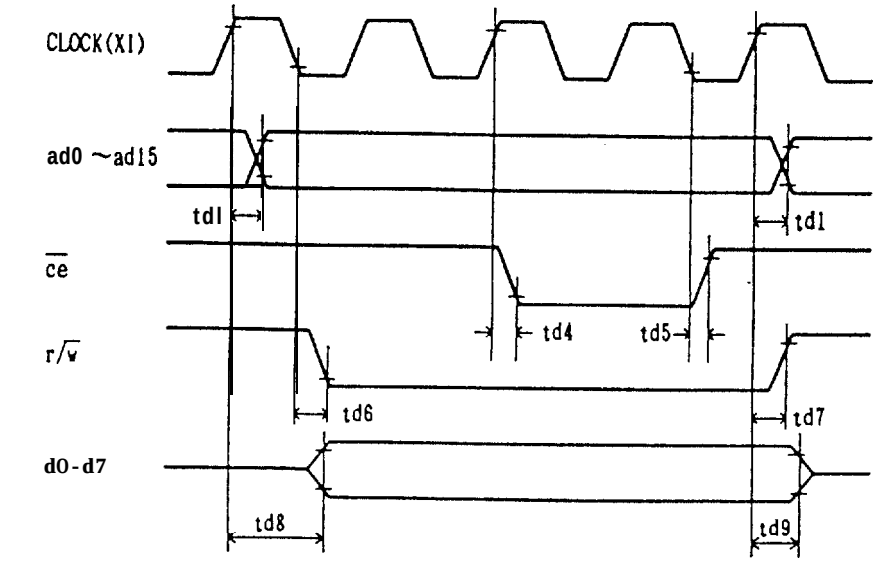
ITEM	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
C/D Set Up Time	tCDS		100	—	ns
C/D Hold Time	tCDH		10	—	ns
CE, RD, WR Pulse Width	tCE,tRD,tWR		80	—	ns
Data Set Up Time	tDS		80	—	ns
Data Hold Time	tDH		40	—	ns
Access Time	tACC		—	150	ns
Output Hold Time	tOH		10	50	ns

Switching Characteristic (3)

①External RAH Read Mode



②ExternalRAM Write !!cde



VDD=5V±10%, VSS=0V, Ta=-10 ~ +70℃

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Address Delay Time	td1		—	250	ns
ce Fall Delay Time(Read)	td2		—	180	ns
ce Rise Delay Time(Read)	td3		—	180	ns
Data Set Up Time	tDS		0	—	ns
Data Hold Time	tDH		30	—	ns
ce Fall Delay Time(Write)	td4		—	200	ns
ce Rise Delay Time(Write)	td5		—	200	ns
r/w Fall Delay Time	td6		—	180	ns
r/w Rise Delay Time	td7		—	180	ns
Data Stable Time	td8		—	450	ns
Data Hold Time	td9		—	200	ns

PIN FUNCTIONS

PIN NAME	I/O/Z	FUNCTIONS															
MDS MD0 MD1	I	Terminals for selection of the LCD size	DUAL	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
			MDS	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
			MD1	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L
			MD0	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
			LINES	2	4	6	8	10	12	14	16	4	8	12	16	20	24	28	32
			Y-DOTS	16	32	48	64	80	96	112	128	32	64	96	128	160	192	224	256
				1 screen								2 screens							
MD2 MD3	I	Terminals for selection of coluans						MD2	H		L		H		L		
								MD3	H		H		L		L		
								columns	32		40		64		80		
FS0 FS1	I	Terminals for selection of font size						FS0	H		L		H		L		
								FS1	H		H		L		L		
								FONT	5×8		6×8		7×8		8×8		
D0~D7	I/O/Z	Data I/O terminals between CPU and T6963C (D7 is MSB)															

PIN NAME	I/O/Z	FUNCTIONS
$\overline{WR}$	I	Data write. Write data into T6963C at "L".
$\overline{RD}$	I	Data read. Read data from T6963C at "L".
$\overline{CE}$	I	Chip enable for T6963C. $\overline{CE}$ must be "L" when CPU communicates with T6963C.
C/$\overline{D}$	I	$\overline{WR}$-"L"·····C/$\overline{D}$-"H": Command write C/$\overline{D}$-"L": Data write $\overline{RD}$-"L"·····C/$\overline{D}$-"H": Status read C/$\overline{D}$-"L": Data read
$\overline{HALT}$	I	"H": NORMAL "L": Stop the oscillation of clock
$\overline{RESET}$	I	"H": NORMAL (T6963C has internal pull-up resistance.) "L": Initialize T6963C.
DSPON	O	Control terminal for external DC/DC. DSPON is "L" when HALT is "L" or RESET is "L". (When DSPON turns from "L" to "H", column drivers will be cleared.)
$\overline{DUAL}$	I	"H": 1 LCD screen "L": 2 LCD screens $\overline{DUAL}$ H H L L $\overline{SDSEL}$ H L H L
SDSEL	I	"H": Sending data by Odd/Even separation. "L": Sending data by simple serial method. Upper screen HOD.ED E D HOD.ED E D Lower screen / / LOD.ED E D
$\overline{ce0}$ (LOD)	O	$\overline{ce0}$ at $\overline{DUAL}$-"H" Chip enable terminal for display memory in the range of address from 0000H to 07FFH. LSCP at $\overline{DUAL}$-"L" serial data output for odd segments of lower LCD screen.
$\overline{ce1}$ (LSCP)	O	$\overline{ce1}$ at $\overline{DUAL}$-"H" Chip enable terminal for display memory in the range of address from 0800H to 0FFFH. LSCP at $\overline{DUAL}$-"L" shift clock pulse output for column drivers of lower LCD screen.
$\overline{ce}$	O	Chip enable terminal for display memory in all range of address.
d0~d7	I/O/Z	Data I/O terminals for display memory.
ad0~ad15	O	Address Outputs for display memory (ad15-"L": for upper Screen, ad15-"H": for lower screen)
r/$\overline{w}$	O	Read/write signal for display memory.
ED	O	SDSEL-"H" Data output for even segments of both upper and lower screens. SDSEL-"L" Data output Tor segments of both upper and lower screens.
HOD	O	Data output for odd Segments of upper screen.
CDATA	O	Synchronous signal for Rov driver.
HSCP	O	Shift clock pulse for column driver of upper Screen.
LP	O	Latch pulse for column driver. Shift clock pulse for Rov driver.
FR	O	Frame signal
X1, X0	I, O	Connection to crystal oscillator.
CH1.2	O	Check Signal
T1.2	I	TEST Input
VDD	—	Power supply (+5V)
VSS		Ditto (0V)

**** The relationship between nwber of rov/colum and oscillation clock ****

The frequency of the crystal is calculated by following formula.

fosc : frequency of oscillation clock

fscp : frequency of shift clock

fR : frequency of Frame

M : Number of frequency (8M……Number of dots).

The oscillation frequency don't change at 7×8, 6x8, 5x8 fonts.

N : Number of frequency (1/8N…… duty Number of rows)

$$\frac{8M}{fscp} \times 8N = \frac{1}{fR}$$

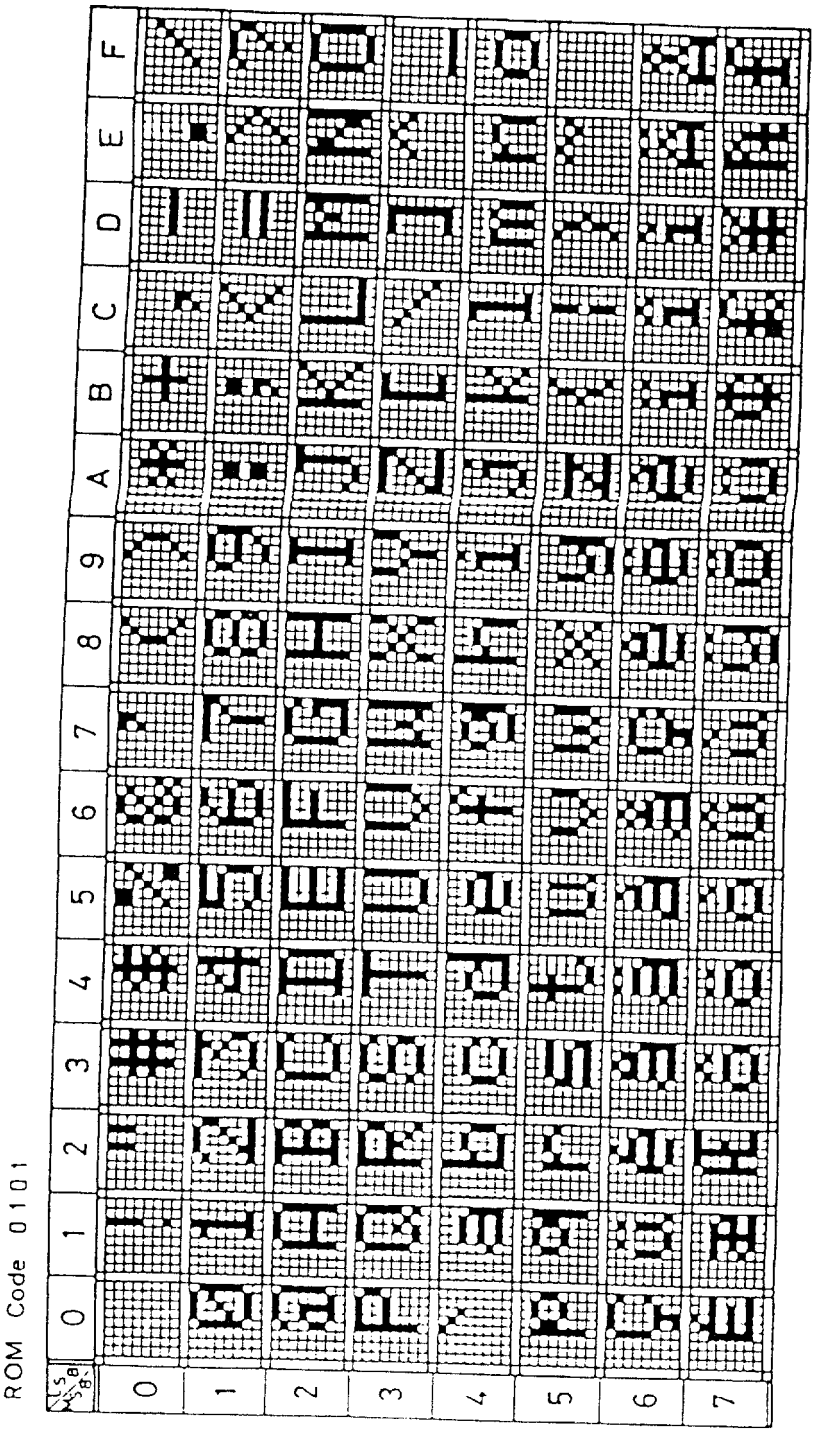
$$fosc = fR \times 64 \times 2 \times M \times N$$

UNIT : [MHz]

N \ M	32	40	64	80	duty
2	0.492	0.614	0.983	1.229	1/16
	0.983	1.229	1.966	2.458	
4	0.983	1.229	1.966	2.458	1/32
	1.966	2.458	3.932	4.915	
6	1.475	1.843	2.949	3.686	1/48
	2.949	3.686	5.898	7.372	
8	1.966	2.458	3.932	4.915	1/64
	3.932	4.915	7.864	9.830	
10	2.458	3.072	4.915	6.144	1/80
	4.915	6.144	9.830	12.286	
12	2.949	3.686	5.898	7.373	1/96
	5.898	7.373	11.776	14.746	
14	3.440	4.300	6.881	8.602	1/112
	6.881	8.601	13.763	17.203	
16	3.932	4.915	7.864	9.830	1/128
	7.864	9.830	15.729	19.660	

Note: Upper 1 screen drive, lower 2 screens drive at fR=60Hz

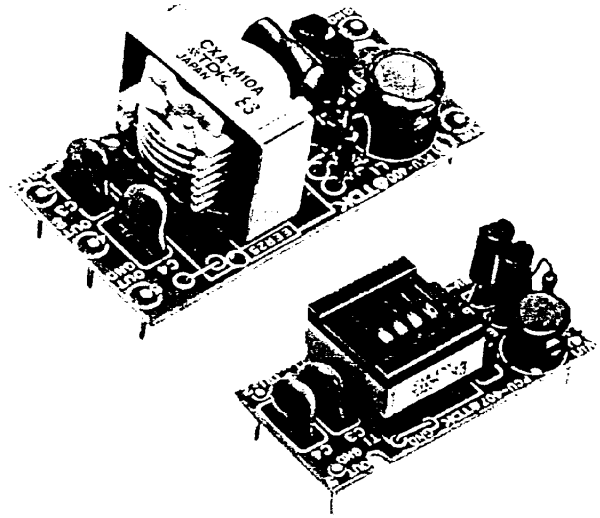
CHARACTER CODE MAP



TDK DC to AC Inverters

CXA Series, 3 to 9 Watts

TDK CXA series of DC to AC inverters are designed for driving cold cathode discharge lamps and to handle a wide range of lamp characteristics.



Features

- Constant current output ensures compatibility with a wide range of discharge lamps.
- High-efficiency resonant circuitry produces low-noise, sinusoidal-wave output.
- One-lamp/two-lamp combined-used capability allows use in four different configurations.
- Full protection against open circuits, short circuits, and overheat conditions provides dependable operation.
- Compact size and light weight facilitate PC board mounting.

Product Identification

CXA-	M	10	A-	L
1	2	3	4	5

1 Product symbol

2 Indicates the power output (W)
K: 3 watts, L: 4.5 watts, M: 6 watts, N: 6 watts, P: 9 watts.

3 Indicates the sum total output current (mA).

4 Indicates the input voltage (V)
A: 5Vdc, L: 12Vdc, M: 24Vdc.

5 Internal code

Standard Specification

Temperature and humidity range

Operating temperature range	-10 to +60°C[+14 to +140°F]
Storage temperature range	-20 to +85°C[-4 to +185°F]
Humidity	95% max. (Maximum wet-bulb temperature: 38°C[100.4°F])

Terminal connections

Terminal number	Function
1	+ Vin
2	- Vin
3	AC Vout 1
4	AC Vout 2
5	Common out

Note 1: Terminals 2 and 5 are connected by a jumper (*1). Cut this jumper to let the secondary float with respect to the primary.

Note 2: Standard application is driving two lamps. Three lamps can also be driven as follows:
1. A lamp drawing twice the inverter's rated output current can be driven by connecting terminals 3 and 4.
2. A lamp drawing 1.2 times the inverter's rated output current can be driven by opening terminal 4.
3. A lamp drawing the inverter's rated output current can be driven by connecting terminals 4 and 5.

Contact TDK if you wish to use the inverter to drive one lamp.

TDK DC to AC Inverters

CXA Series, 3 to 9 Watts *(Continued)*

PLEASE CALL FOR DETAILS
THIS RANGE IS CURRENTLY BEING REDESIGNED
PLEASE CALL FOR DETAILS

Shapes and Dimensions

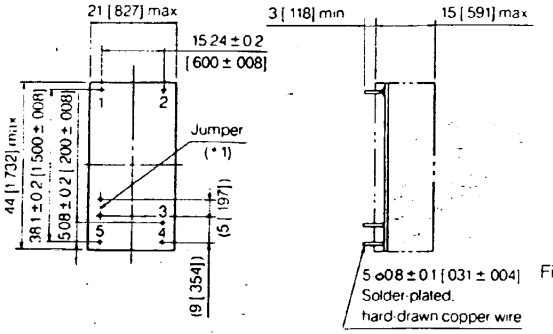


Fig. 1

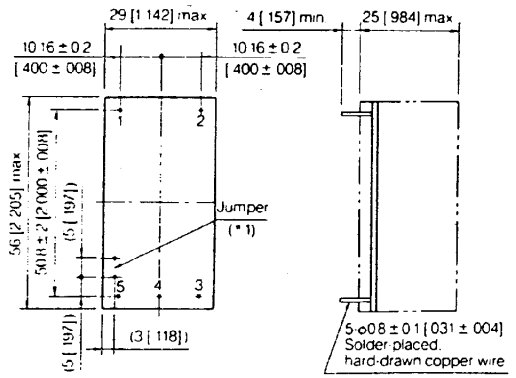


Fig. 2

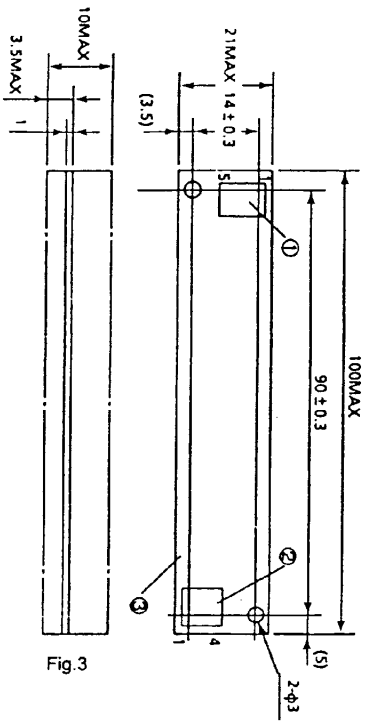


Fig.3

Dimensions in mm [inches]

Electrical Characteristics

Part No.	Input voltage (V)	Open circuit output voltage (AC Vrms) typ.	Output voltage (AC Vrms) max.	Output current (mA rms)	Efficiency (%) typ.	Frequency (kHz)	Weight (g)	Configuration
CXA-K10A	5±10%	600	300	5 x 2	80	30	11	Fig. 1
CXA-K10L	12±10%	600	300	5 x 2	80	30	11	Fig. 1
CXA-L10A	5±10%	900	450	5 x 2	80	30	11	Fig. 1
CXA-L10L	12±10%	900	450	5 x 2	80	30	11	Fig. 1
CXA-M10A-L	5±10%	1200	600	5 x 2	80	30	27	Fig. 2
CXA-M10L-L	12±10%	1200	600	5 x 2	80	30	27	Fig. 2
CXA-M10M-L	24±10%	1200	600	5 x 2	80	30	27	Fig. 2
CXA-N20L-L	12±10%	600	300	10 x 2	85	30	27	Fig. 2
CXA-P20L-L	12±10%	900	450	10 x 2	85	30	27	Fig. 2
CXA-K10L-FS	8-16±10%	1100	330	7	80	36	27	Fig. 3