Migrating from the 8XC251Sx to the 8XC251Tx

Application Note

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Revision History

Date	Revision	Description
May 1999	001	Initial release of this document
December 2003	002	Removed references to 8XC251TA, 8XC251TP

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1.0 Introduction

The 8XC251TB and TQ (referred to collectively as the 8XC251Tx) embedded microcontroller has joined the 8XC251SA, SB, SP, SQ (referred to collectively as the 8XC251Sx) as a member of the MCS® 251 microcontroller family. The 8XC251Tx is pin and code compatible with the 8XC251Sx. It also has additional features that the 8XC251Sx does not possess.

This document addresses the differences between the 8XC251Sx and the 8XC251Tx. It also addresses the implications of these differences for a user who is migrating from an existing 8XC251Sx design to an 8XC251Tx design. For a detailed description of the MCS 251 microcontroller core, and standard peripherals that are shared by both the 8XC251Sx and 8XC251Tx, please refer to the *8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ Embedded Microcontroller User's Manual* (order number 272795).

1.1 References

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

Title	Intel Order Number
8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ Embedded Microcontroller User's Manual	272795
8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ High-Performance CHMOS Microcontroller (Commercial/Express) Datasheet	272783
8XC251TB, 8XC251TQ Hardware Description	273138
8XC251TB, 8XC251TQ Datasheet	273129
AP-125, Designing Microcontroller Systems for Electrically Noisy Environments	210313
AP-155, Oscillators for Microcontrollers	230659
AP-708, Introducing the MCS® 251 Microcontroller—the 8XC251SB	272670
AP-709, Maximizing Performance Using MCS® 251 Microcontroller—Programming the 8XC251SB	272671
AP-710, Migrating from the MCS® 51 Microcontroller to the MCS 251 Microcontroller (8XC251SB)—Software and Hardware Considerations	272672
AP-70, Using the Intel MCS® 51 Boolean Processing Capabilities	203830
AP-223, 8051 Based CRT Terminal Controller	270032
AP-252, Designing With the 80C51BH	270068
AP-425, Small DC Motor Control	270622
AP-410, Enhanced Serial Port on the 83C51FA	270490
AP-415, 83C51FA/FB PCA Cookbook	270609
AP-476, How to Implement I^2C Serial Communcation Using Intel MCS® 51 Microcontrollers	272319

1.2 Comparing the 8XC251Sx and 8XC251Tx

This section presents an overview of the differences between the 8XC251Sx and the 8XC251Tx, and describes changes that an existing 8XC251Sx design would require to work with the 8XC251Tx.

The differences between the 8XC251Tx and the 8XC251Sx are briefly described here.

- The maximum operating frequency of the 8XC251Tx is 24 MHz. The maximum operating frequency of the 8XC251Sx is 16 MHz. To take advantage of the higher frequency available on the 8XC251Tx, the 16 MHz crystal on the 8XC251Sx design should be changed to a 24 MHz crystal.
- The 8XC251Tx has two serial I/O ports, while the 8XC251Sx has one. The pins for the second serial I/O port are multiplexed with other functional pins. The hardware and software changes that are required to take advantage of the second serial port are discussed in detail in Section 2.0.
- The 8XC251Tx has a new configuration option—Extended Data Float timing—that allows it to interface with slower memories. This feature is supported by a bit in the Configuration byte, UCONFIG1. The corresponding bit in the 8XC251Sx has a different function. The hardware and software changes that are required to take advantage of this feature are discussed in detail in Section 3.0 of this document.
- The 8XC251Tx is offered with factory programmed ROM. The 8XC251Sx is offered with factory programmed ROM and OTPROM/EPROM. Software written for the 8XC251Sx will work for the 8XC251Tx. For 8XC251Tx development in which OTPROM devices are needed, an alternative is to use the 8XC251Sx OTPROM before porting the code to factory programmed ROM on the 8XC251Tx. However, if the second serial port or Extended Data Float timings are needed, using the 8XC251Sx OTPROM will not suffice. To address this need, third party vendors have been engaged to provide In-Circuit Emulators.

2.0 The Second Serial I/O Port

The second serial I/O port is functionally the same as the standard serial I/O port that is shared by both the 8XC251Tx and the 8XC251Sx. This section provides information about the new special function registers (SFRs) that are associated with the second serial port. See Chapter 10 of the *8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ Embedded Microcontroller User's Manual* (Order Number 272795), for detailed information about the operation and programming of the serial I/O ports. All the SFRs and control bits for the standard serial I/O port have equivalent SFR's and control bits in the second serial I/O port. Keep this in mind when reading Chapter 10 of the *8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ Embedded Microcontroller User's Manual.*

2.1 Overview

The second serial I/O port provides synchronous and asynchronous communications modes. It operates as a universal asynchronous receiver and transmitter (UART) in three full-duplex modes (modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates. The second UART provides framing-bit error detection, multiprocessor communications, and automatic address recognition. The second serial port also operates in a single synchronous mode (mode 0).

The synchronous mode (mode 0) operates at a single baud rate. Mode 2 operates at two baud rates. Modes 1 and 3 operate over a wide range of frequencies, which are generated by timer 1 and timer 2.

The second serial I/O port signals are defined in Table 1. The special function registers are described in Table 2.

For the three asynchronous modes, the second serial I/O port transmits on the TXD1 pin and receives on the RXD1 pin. For the synchronous mode (mode 0), the second serial I/O port outputs a clock signal on the TXD1 pin and sends and receives messages on the RXD1 pin. The SBUF1 register holds received bytes and bytes that are to be transmitted. To send, software writes a byte to SBUF1; to receive, software reads SBUF1. The receive shift register allows reception of a second byte before the first byte has been read from SBUF1. However, if software has not read the first byte by the time the second byte is received, the second byte overwrites the first. The second serial I/O port sets interrupts bits TI1 and RI1 on transmission, and reception, respectively. These two share a single interrupt request and interrupt vector.

The serial port control 1 (SCON1) and the secondary serial port control (BGCON) registers configures and controls the second serial I/O port.

Table 1. Second Serial I/O Port Signals

Function Name	Type	Description	Multiplexed With
TXD1	O	**Transmit Serial Data.** TXD1 outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2 and 3 for the second serial I/O port.	**P1.3/CEX0**
RXD1	I/O	**Receive Serial Data 1.** RXD1 send and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3 for the second serial I/O port.	**P1.2/ECI**

Table 2. Second Serial I/O Port Special Function Registers (Sheet 1 of 2)

Mnemonic	Description	Address
SBUF1	**Serial Buffer 1**. Two separate registers comprise the SBUF1 register. Writing to SBUF1 loads the transmit buffer; reading SBUF1 access the receive buffer.	9BH
SCON1	**Serial Port Control 1**. Selects the second serial I/O port operating mode. SCON1 enables and disables the receiver, framing bit error detection, multiprocessor communication, automatic address recognition and the serial port interrupt bits.	9AH
SADDR1	**Serial Address 1**. Defines the individual address for a slave device.	AAH
SADEN1	**Serial Address Enable 1**. Specifies the mask byte that is used to define the given address for a slave device.	BAH
BGCON	**Secondary Serial Port Control**. Contains controls to the second serial port including the double baud rate bit, read/write access to the SCON1.7 bit as well as bits to control timer1 or 2 overflow as the baud rate generator for reception and transmission.	8FH

Table 2. Second Serial I/O Port Special Function Registers (Sheet 2 of 2)

Mnemonic	Description	Address
IE1	**Interrupt Enable Register 1**. Contains the second serial I/O port interrupt enable bit.	B1H
IPL0	**Interrupt Priority Low Control Register 1**. IPL0, together with IPH0, assigns the second serial I/O port interrupt level from 0 (lowest) to 3 (highest).	B2H
IPH0	**Interrupt Priority High Control Register 1**. IPH0, together with IPL0, assigns the second serial I/O port interrupt level from 0 (lowest) to 3 (highest).	B3H

The second serial I/O port interrupt is enabled by setting the ES1 bit in the IE1 register. The priority of the second serial I/O port's interrupt is set to one of four levels by programming the IPL1.0 and IPH1.0 bits in the IPL1 and IPH1 registers respectively. The second serial I/O port is last in the interrupt polling sequence. See Chapter 6 of the *8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ Embedded Microcontroller User's Manual* (Order Number 272795) for details of the interrupt system.

2.2 Hardware Implications

When the second serial I/O port is used, the alternate functions of RXD1 and TXD1 can no longer be used. Specifically, the PCA can no longer be clocked by an external clock input, because ECI now functions as RXD1. The PCA can, however, be clocked by one of three other methods. These are: two fixed frequencies (fixed in relation to the Oscillator frequency); Fosc/12 and Fosc/4 and Timer 0 overflow.

The other consequence of using the second serial I/O port, is Module 0 of the PCA can now be used only as a 16-bit Software Timer. The 16-bit Capture, High Speed Output, and Pulse Width Modulation modes are no longer available to Module 0, since these modes require the use of CEX0 (CEX0 functions as TXD1 when the second serial I/O port is in operation).

2.3 Software Implications

As described earlier, the second serial port is functionally equivalent to the standard serial port. Because of this, programming remains the same.

The following sections describe the special function registers that are associated with the second serial I/O port and their bit definitions.

2.3.1 SCON1

Address: 9AH

Reset Value: 0000 0000B

Bit Number	Bit Mnemonic	Function
7	FE1 SM0	**Framing Error Bit 1:** To Select this function, set the SMOD0 bit in the BGCON register. Set by hardware to indicate an invalid stop bit. Cleared by software, not by valid frames. **Second Serial I/O Port Mode Bit 0:** To select this function, clear the SMOD0 bit in the BGCON register. Software writes to bit SM0 and SM1 to select the second serial I/O port operating mode. Refer to SM1 bit for mode selections.
6	SM1	**Second Serial I/O Port Mode Bit 1:** Software write to bit SM0 and SM1 (above) to select the serial port operating mode. **SM0 SM1 Mode Description Baud Rate** 0 0 0 Shift Register Fosc/12 0 1 1 8 bit UART variable 1 0 2 9 bit UART Fosc/32* or Fosc/64* 1 1 3 9 bit UART variable * Select by programming the SMOD0 bit in the BGCON register.
5	SM2	**Second Serial I/O Port Mode Bit 2:** Software writes to SM2 enable and disable the multiprocessor communication and automatic address recognition features. This allows the second serial I/O port to differentiate between data and command frames and to recognize slave and broadcast addresses.
4	REN1	**Receive Enable Bit 1:** To enable reception, set this bit. To enable transmission, clear this bit.
3	TB8	**Transmit Bit 8:** In modes 2 and 3, software writes the ninth data bit to be transmitted to TB8. Not used in modes 0 and 1.
2	RB8	**Receive Bit 8:** Mode 0: not used. Mode 1 (SM2 clear): Set or cleared by hardware to reflect the stop bit received. Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth data bit received.
1	TI1	**Second Serial I/O Port Transmit Interrupt Flag Bit:** Set by transmitter after the last data bit is transmitted. Cleared by software.
0	RI1	**Second Serial I/O Port Receive Interrupt Flag Bit:** Set by the receiver after the last data bit of a frame has been received. Cleared by software.

2.3.2 SBUF1

Address: 9BH

Reset Value: xxxx xxxxB

To send serial data, software writes a byte to SBUF1. To receive serial data, software reads from SBUF1.

2.3.3 SADDR1

Address: AAH

Reset Value: 0000 0000B

Slave Individual Address Register1 (SADDR1) contains the device's individual address for multiprocessor communications.

2.3.4 SADEN1

Address: BAH

Reset Value: 0000 0000B

Mask Byte Register 1 (SADEN1) masks bits in the SADDR1 register to form the device's given address for multiprocessor communications.

2.3.5 BGCON

Address: 8FH

Reset Value: 0000 xxxxB

Bit Number	Bit Mnemonic	Function
7	SMOD1	**Double Baud Rate Bit:** When set, doubles the baud rate for the second serial I/O port when timer 1 is used and mode 1, 2 or 3 is selected in the SCON1 register.
6	SMOD0	**SCON1.7 Select:** When set, read/write accesses to SCON1.7 are to the FE1 bit. When cleared, read/write accesses to SCON1.7 are to the SM0 bit.
5	RCLK1	**Second Serial I/O Port Receive Clock Bit:** Selects timer 2 overflow pulses (RCLK1 = 1) or timer 1 overflow pulses (RCLK1 = 0) as the baud rate generator for the serial port modes 1 and 3.
4	TCLK1	**Second Serial I/O Port Transmit Clock Bit:** Selects timer 2 overflow pulses (TCLK = 1) or timer 1 overflow pulses (TCLK1 = 0) as the baud rate generator for the serial port modes 1 and 3.
3 - 0	-	Reserved

2.3.6 IE1

Address: B1H

Reset Value: xxxx xxx0B

Bit Number	Bit Mnemonic	Function
7 - 1	-	Reserved
0	ES1	**Second Serial I/O Port Interrupt Enable:** Setting this bit enables the second serial I/O port interrupt.

2.3.7 IPH1

Address: B3H

Reset Value: xxxx xxx0B

Bit Number	Bit Mnemonic	Function
7 - 1	-	Reserved
0	IPH1.0	**Second Serial I/O Port Interrupt Priority High Bit:** Interrupt priority of the second serial I/O port can be programmed to one of four levels, depending on the IPH1.0 and IPL1.0 bits. See Table 3.

2.3.8 IPL1

Address: B2H

Reset Value: xxxx xxx0B

Bit Number	Bit Mnemonic	Function
7 - 1	-	Reserved
0	IPL1.0	**Second Serial I/O Port Interrupt Priority Low Bit:** Interrupt priority of the second serial I/O port can be programmed to one of four levels, depending on the IPH1.0 and IPL1.0 bits. See Table 3.

Table 3. Second Serial I/O Priorities

IPH1.0	IPL1.0	Priority Level
0	0	0 (Lowest Priority)
0	1	1
1	0	2
1	1	3 (Highest Priority)

3.0 Extended Data Float Timing

The Extended Data Float Timing feature provides a solution for users who may be using slower memory devices. Essentially, this feature extends the T_{RHDZ1} AC timing specification to accommodate slower memory devices, which require a longer period of dead time between data bus cycles and address bus cycles. This feature is controlled by a bit in the Configuration byte (UCONFIG1). Bit 3 of UCONFIG1 in the 8XC251Tx is defined as EDF#. In the 8XC251Sx, Bit 3 is defined as WSB. The implications of this change are discussed below. For details of the device configuration for the 8XC251Sx, refer to Chapter 4 of the *8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ Embedded Microcontroller User's Manual* (Order Number 272795). The information in that chapter is valid for the 8XC251Tx, with the exception of the change noted in this section.

3.1 Summary of the Extended Data Float Timing Changes

EDF# is used to determine when the Extended Data Float Timing is enabled. Table 4 shows the definition of UCONFIG1 for the 8XC251Tx. Only bit 3 has been redefined.

Table 4. UCONFIG1 Bit Definitions for the 8XC251Tx

Bit Number	Bit Mnemonic	Function
7:5	-	**Reserved for internal or future use**. Set these bits when programming UCONFIG1.
4	INTR	**Interrupt Mode**: When this bit is set, interrupts push 4 bytes onto the stack (the 3 bytes of the PC and PSW1). When this bit is clear, interrupts push the 2 lower bytes of the PC onto the stack.
3	EDF#	**Extended Data Float Timings**: When cleared, the extended data float timings are enabled. When set, 8XC251Sx compatible AC timings are enabled.
2:1	WSB1:0#	**External Wait State B (region 01:)**: WSB1# WSB2# 0 0 Inserts 3 wait states for region 01: 0 1 Inserts 2 wait states for region 01: 1 0 Inserts 1 wait state for region 01: 1 1 Zero wait states for region 01:
0	EMAP	**EPROM Map**: For devices with 16 Kbytes of on-chip code memory, clear this bit to map the upper half of the on-chip code memory to region 00: (data memory). Maps FF:2000H-FF:3FFFH to 00:E000H-00:FFFFH. When this bit is set, mapping does not occur and the addresses in the range 00:E000H-00:FFFFH access external RAM.

Refer to the *8XC251TB, 8XC251TQ Datasheet* (order number 273129) for the AC timings specifications.

Table 5 shows the effect of programming EDF# and WSB#[1:0] on the extended data float timing feature. It also shows the insertion of wait states for region 01:. Note that enabling the extended data float timing allows region 01: to have 1 or 3 wait states inserted (depending on WSB#[1:0]), but not 0 or 2 wait states.

Table 5. Summary of the EDF# and WSB#[1:0] Configuration Options

EDF#	WSB#[1:0]	Wait State	Extended Data Float Timings
1	11	0	No
1	10	1	No
1	01	2	No
1	00	3	No
0	11	1	Yes
0	10	1	Yes
0	01	3	Yes
0	00	3	Yes

The external user configuration cycle (UCONF = 1 and EA# = 0) will be executed with the extended T_{RHDZ1} timing bus cycle.