USER MANUAL

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1.0 Introduction

Frequency Devices' Model VM8PF comprises a family of VMEbus filter boards offering eight channels of software programmable high performance linear analog filtering in a single width B-size (6U) VME form factor. VM8PF boards receive up to eight high level differential signal inputs through a shielded front panel connector and provide signal buffering and software programmable filtering for each channel. A second connector is wired in parallel with the input connector to facilitate filter bypassing. VM8PF boards may be configured with 824 Series four-pole or 828 Series eight-pole filters and with high pass and/or low pass transfer functions allowing user to externally cascade filters into band-pass configurations. The boards conform to VME revision C.1 as an A16/D16 Slave. Appendix A provides a functional overview of the VM8PF boards.

2.0 Unpacking and Inspection

Before unpacking the VM8PF shipping container, carefully inspect the exterior of the package for evidence of damage. After noting areas of possible shipping damage, open and unpack the shipping container, being careful to preserve the container and packing materials in case they are needed later.

CAUTION
The VM8PF Board is sensitive
to STATIC ELECTRICITY. Use proper GROUNDING TECHNIQUES
when handling the board.

Carefully remove the VM8PF board from its anti-static bag and visually inspect for evidence of damage. If the board appears to be damaged in any way, notify the shipping carrier.

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3.0 Hardware Configuration

Once the VM8PF VMEbus board has been removed from its anti-static bag and carefully inspected for damage, you are ready to configure the board's base address for your particular system. The Base Address is the only hardware configuration on the VM8PF board. The factory set Base Address is F000 (hex).

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To reconfigure the VM8PF base address, lay the board flat as shown in Figure 3-1.

The ten-position jumper block shown in Figure 3-1 is used to set the board's base address in A16 address space. A VM8PF board occupies a 64-byte block in A16 address space and may be configured on any 64-byte boundary. The ten jumper positions correspond to address lines A15 through A06. As shown in Figure 3-1, jumper position 06 corresponds to address line A06, jumper position 07 corresponds to A07, etc. An installed jumper sets logic '1' while a missing jumper sets logic '0'.

After the board's base address has been configured, the VM8PF is ready for installation in a VME system.

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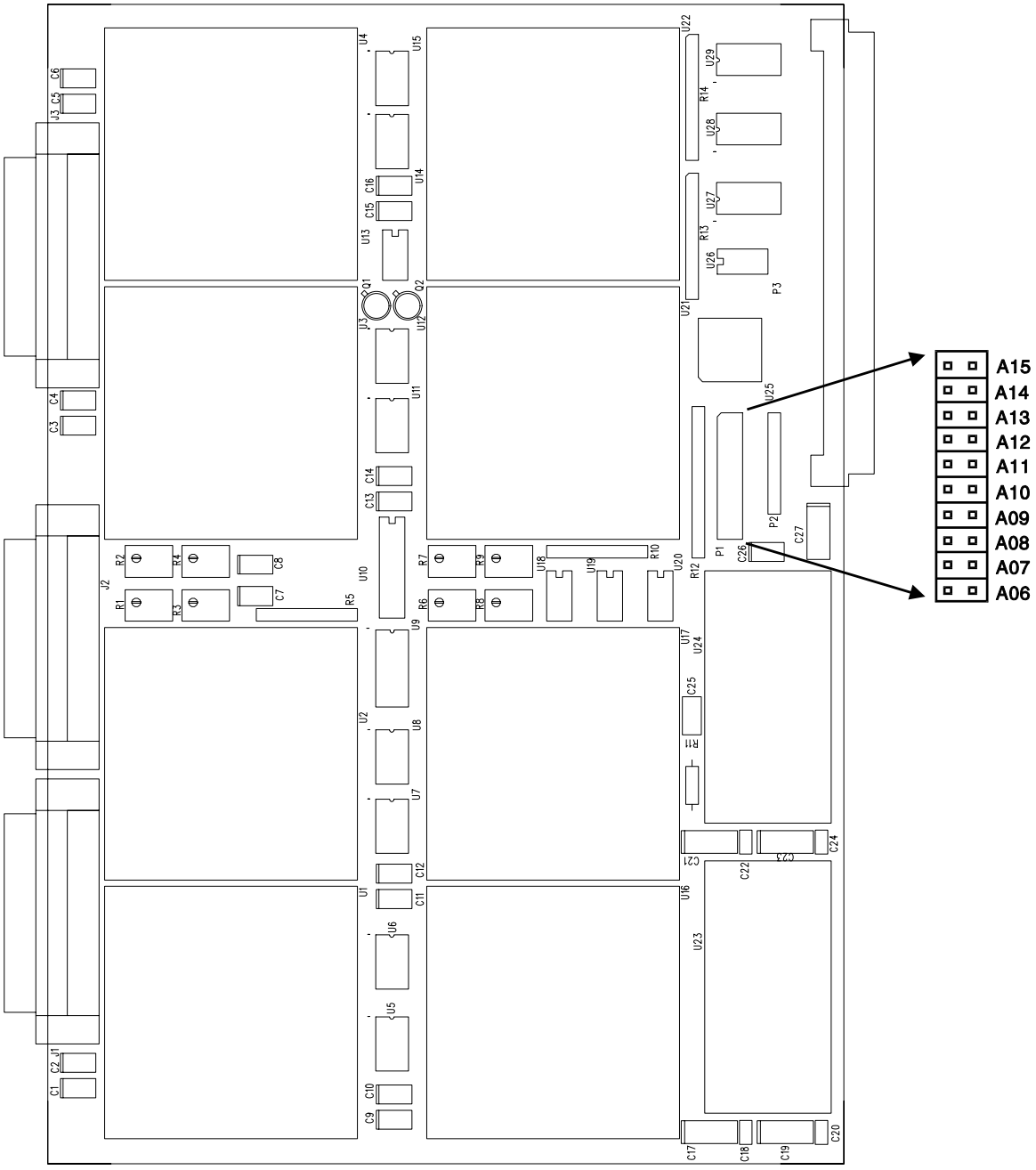
Figure 3-1
VM8PF Base Address Configuration Jumpers



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4.0 Board Installation

Frequency Devices' Model VM8PF eight channel VMEbus filter boards conform mechanically, in every respect, to the single width VME "B" size (6U) form factor. Installation of a VM8PF board into a standard VME mainframe can proceed exactly as for any other standard single width "B" size (6U) VME board.

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The VM8PF board may be installed in any available mainframe slot except Slot 0. The board does not use VMEbus interrupts or bus mastering capabilities, but passes all VMEbus daisy chained signals automatically.

The major considerations in locating the VM8PF board in the mainframe are for EMI and I/O signal cabling. To minimize interference from other boards in the system, it is good practice to keep one or more empty slots between analog signal conditioning boards and high speed digital boards in the system. When cabling the system, it is desirable to keep the analog signal cabling as short as possible and physically located away from high speed digital cabling and high voltage switching lines.

5.0 I/O Connections and the Front Panel

The following information is provided to assist the user/integrator in installing and interconnecting a VM8PF board into a VME system.

5.1 Front Panel Layout

Figure 5-1 shows the layout of the VM8PF front panel. The following sections provide detailed information about connectors, pin-out, and cabling. There are no front panel indicators or controls on the VM8PF.

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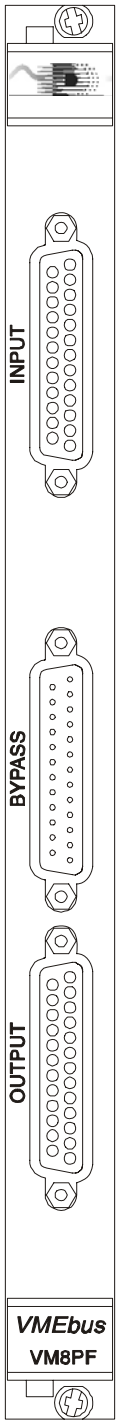
Figure 5-1
VM8PF Front Panel



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5.2 Connector/Cable Information and I/O Connections

The Analog Input connector is a 25-pin female "D" shell connector located near the top of the front panel. The Bypass connector is a 25-pin male “D” shell connector located below the Input connector. The Bypass connector is wired in parallel with the Input connector and may actually be used as the Input connector. Analog Input and Bypass connections are as follows:

	INPUT	BYPASS
FUNCTION	**DB25 FEMALE**	**DB25 MALE**
Channel 0 HI	2	12
Channel 0 LO	15	24
Signal GND	14	25
Channel 1 HI	16	23
Channel 1 LO	4	10
Signal GND	3	11
Channel 2 HI	19	20
Channel 2 LO	7	7
Signal GND	6	8
Channel 3 HI	5	9
Channel 3 LO	18	21
Signal GND	17	22
Channel 4 HI	8	6
Channel 4 LO	21	18
Signal GND	20	19
Channel 5 HI	22	17
Channel 5 LO	10	4
Signal GND	9	5
Channel 6 HI	25	14
Channel 6 LO	13	1
Signal GND	12	2
Channel 7 HI	11	3
Channel 7 LO	24	15
Signal GND	23	16

Refer to Figure 5-1 for connector orientation. The mating connectors are the Amp HD-20 family. Frequency Devices recommends that input and bypass signals be wired using cable consisting of individually shielded twisted pairs of #22 AWG stranded wire.

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The Analog Output connector is a 25-pin female "D" shell connector located near the bottom of the front panel. Analog Output connections are as follows:

FUNCTION	OUTPUT DB25 FEMALE
Channel 0	15
Signal GND	14
Channel 1	4
Signal GND	3
Channel 2	7
Signal GND	6
Channel 3	18
Signal GND	17
Channel 4	24
Signal GND	23
Channel 5	21
Signal GND	20
Channel 6	13
Signal GND	12
Channel 7	10
Signal GND	9

Refer to Figure 5-1 for connector orientation. The mating connector is the Amp HD-20 family. Frequency Devices recommends that output signals be wired using cable consisting of individually shielded twisted pairs of #22 AWG stranded wire.

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6.0 Software Overview

A two-register read/write programming interface makes the VM8PF family of VMEbus filter boards extremely easy to program. Appendix A of this User's Manual, beginning on Page 14, provides detailed information for programming the VM8PF from the VMEbus and may be used as the basis for OS-specific driver development.

7.0 Adjusting Channel DC Offset

The VM8PF module hardware includes on board trim potentiometers, one for each channel, to adjust DC offset voltage at the channel's output. The offset adjust pots are accessible from the component side of the board. A small flathead screwdriver, or similar adjustment tool, is required to make offset adjustments.

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when handling the board.

Adjusting the zero offset voltage must be done with the board powered and only after at least a 20 minute warm-up period. The user must provide an external means for obtaining precise zero volts input and for measuring channel output voltage.

Figure 7-1 shows the location of the offset adjustment potentiometers and identifies which adjustments correspond to which channels.

Turning an adjustment potentiometer clockwise increases the output voltage; counter clockwise causes the output voltage to go more negative. Adjustment range is approximately +/-25 millivolts.

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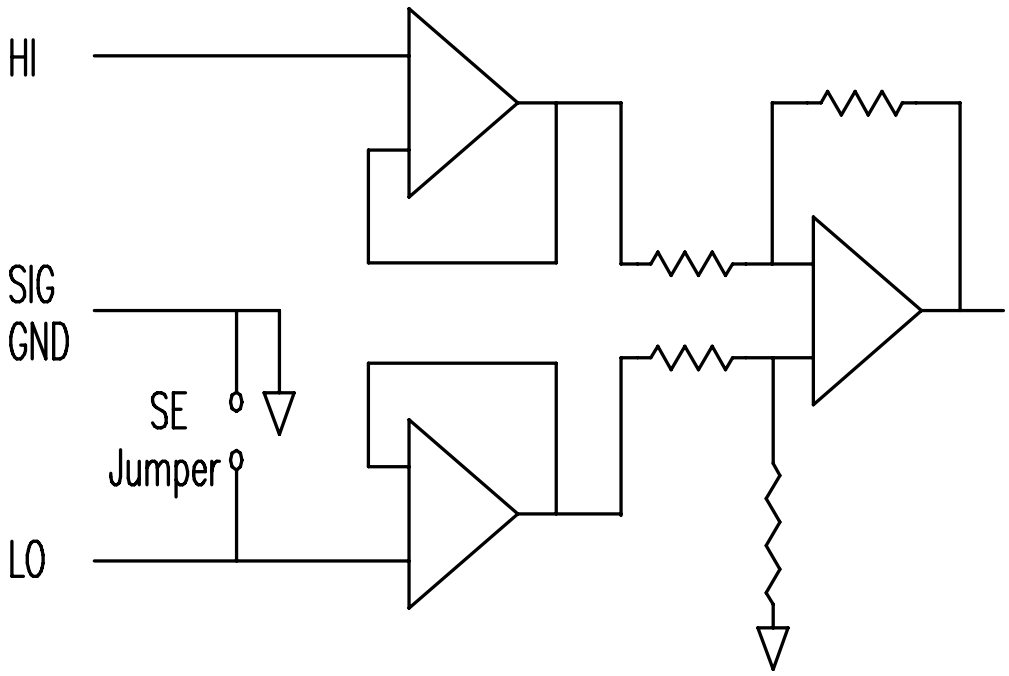
Figure 7-1
VM8PF Zero Adjustment Potentiometers



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8.0 Troubleshooting and Technical Support

If you have difficulty installing the VM8PF board, or if the board fails to operate properly, contact Frequency Devices for technical assistance. Technical assistance is available weekdays 8:00 AM to 4:30 PM Central time at 815-434-7800 or 800-252-7074. Inquiries may also be faxed to 815-434-8176 or emailed to sales@freqdev.com.

If you need to contact Frequency Devices in writing, our address is:

1784 Chessie Lane
Ottawa, IL 61350
Attn: Customer Service

Please have the following information handy prior to contacting Frequency Devices for assistance:

Model Number and Serial Number
Purchase Order Number
Your "Bill To" and "Ship To" addresses

If Frequency Devices determines the board must be returned to the factory, you will be issued a Return Material Authorization (RMA) number. Use this number on all shipping containers, repair purchase orders, and shipping documents. DO NOT ATTEMPT TO RETURN BOARDS WITHOUT FIRST OBTAINING AN RMA NUMBER.

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9.0 Warranty Information

Unless otherwise specified in writing by FDI, all FDI products sold hereunder are warranted against defects in workmanship and material under normal use and service for a period of one (1) year from the date of delivery, except that, where applicable liability for defective components purchased by FDI and are resold to the purchaser hereunder shall conform and be limited to the obligations prescribed by the original manufacturer's warranties applicable to such components.

All warranties hereunder are contingent upon proper use in the application for which the product was intended and do not cover products which have been modified or repaired without FDI approval or which have been subjected to neglect, accident, improper installation or application or on which the original identification marks have been removed or altered. These warranties will not apply if adjustment, repair or parts replacement is required because of accident, neglect, misuse, power failure, transportation or other causes other than ordinary use.

FDI's responsibility under the above warranty shall be limited to the repair or replacement, at FDI's option, free of charge to the purchaser, of any component, which fails during the one-year period; provided that the purchaser has promptly reported such failure to FDI in writing and FDI has, upon inspection, found such components to be defective. The purchaser must obtain shipping instructions for the return of any item under this warranty provision and compliance with such instructions shall be a condition of this warranty.

EXCEPT FOR EXPRESS WARRANTIES STATED ABOVE, FDI DISCLAIMS ALL WARRANTIES WITH REGARD TO THE PRODUCTS SOLD HEREUNDER, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS.

Limitation of Liability

Expressed warranties stated herein are in lieu of all obligations or liabilities on the part of FDI for damages, including but not limited to consequential damages arising out of or in connection with the use or performance of the product.

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Appendix A
Functional Description and Register Level Programming

BASIC OPERATION

With the VM8PF VMEbus filter board; the user can set filter cutoff frequency independently for each channel. The user can also read back individual filter cutoff frequency settings. This bi-directional access is especially useful when building fault tolerant systems, for diagnosing system failures, for debugging newly developed systems, and for constructing reliable test header files.

Since the filters are galvanically isolated from system ground and the filters' logic system is based on 15 Volt CMOS levels, an opto-isolated serial communications channel is used to transfer data to/from the filters one channel at a time. Figure A-1 is a block diagram of the isolated side of the serial channel.

The serial channel incorporates some features that are especially important when providing precision, low noise signal conditioning. For example, when the board is not being accessed (the normal case during a test) the serial channel is entirely static and is gated into a low power state (no isolator power consumption on the filter side). When the board is accessed to set or read back a cutoff frequency only the channel being accessed is clocked, so the other channels on the board see no logic transitions that could inject noise or induce DC offsets.

The isolated serial channel is slow compared to VMEbus transfer rates. Rather than hold the VMEbus while cutoff data is serialized and transferred over the isolation barrier, the VM8PF board uses a BUSY flag interlock while data transfer to/from the selected channel is taking place.

To write cutoff data to a filter channel the user first reads the Channel Address Register (CHADR, Base+0) and tests its BUSY bit to see if the serial interface is busy. If BUSY is set the user can go on to other things and come back to the board later, or the user can poll CHADR, waiting for BUSY to clear. Once BUSY is found clear the user writes the desired channel address to CHADR (making sure to write '0' to the BUSY bit) and then writes the cutoff data to the Data Register (DATA, Base+2). The VM8PF automatically sets the BUSY bit in CHADR, serializes and transfers the new data, and then clears BUSY once transfer is complete. The serial channel will be busy for approximately 32 microseconds.

To read cutoff data from a filter channel the user first reads the Channel Address Register (CHADR, Base+0) and tests its BUSY bit to see if the serial interface is busy. If BUSY is set the user can go on to other things and come back to the board later, or the user can poll CHADR, waiting for BUSY to clear. Once BUSY is found clear the user writes the desired channel address to CHADR while simultaneously writing the BUSY bit to '1'. The serial interface accesses cutoff data from the selected channel and clears the BUSY bit in CHADR when the requested data is available in DATA (approximately 32 microseconds later). The user waits for BUSY to clear and then reads DATA.

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Please note that, as is always the case when a flag can be controlled by two or more systems, instructions that generate read/modify/write cycles (or read followed by write cycles) should be avoided when testing the state of the BUSY bit. The safest way to test BUSY is to read CHADR into a local register and then test the state of the BUSY bit in the registered copy.

Cutoff data may be interpreted as the following:

Fword = (F_C / F_B) – 1 , where Fword is the binary representation of the resultant frequency, F_C is the cutoff frequency, and F_B is the base frequency of a specific filter module. For example, in an 828L8E-2, the base frequency is 1Hz, whereas a 828L8E-5 has a base frequency of 200Hz.

The following example shows how to set the VM8 channel 3, an 838L8E-2 filter module, to a cutoff frequency of 64Hz. It assumes a VM8 base address of $(2000)_x$:

- Find: Fword = (64 / 1) – 1 = $(63)_d$
- Determine Fword binary word (8 bits) value: $(0011\ 1111)_b$
- Determine channel binary representation (3 bits) value: $(011)_b$
- Read the CHADR in $(2000)_x$, and tests its BUSY bit to see if the serial interface is busy. Wait for BUSY to clear.
- Write the channel address to CHADR $(2000)_x$: $(0000\ 0000\ 0000\ 0011)_b$
- Write the cutoff data to DATA $(2002)_x$: $(0000\ 0000\ 0011\ 1111)_b$.

This example shows how to set the VM8 channel 6, an 838L8E-5 filter module, to a cutoff frequency of 200Hz. It assumes a VM8 base address of $(4000)_x$:

- Find: Fword = (200 / 200) – 1 = $(0)_d$
- Determine Fword binary word (8 bits) value: $(0000\ 0000)_b$
- Determine channel binary representation (3 bits) value: $(110)_b$
- Read the CHADR in $(4000)_x$, and tests its BUSY bit to see if the serial interface is busy. Wait for BUSY to clear.
- Write the channel address to CHADR $(4000)_x$: $(0000\ 0000\ 0000\ 0110)_b$
- Write the cutoff data to DATA $(4002)_x$: $(0000\ 0000\ 0000\ 0000)_b$.

Figure A-2 shows the VM8PF register map and defines the read/write function of each bit. Registers may be accessed as words or as bytes.

ERROR HANDLING

Attempting to access the VM8PF board in other than A16 address space will cause a bus timeout. Attempting long word access or unaligned transfers will cause the board to respond to the bus cycle with a bus error (BERR).

Changing the channel address while BUSY is set would result in erroneous data during a data read operation and would corrupt the settings of two or more channels during a data write operation. VM8PF hardware prevents changing of the channel selection while BUSY. Writing to the Data Register while

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BUSY is set is also inhibited in hardware. Neither event is flagged by the board, so it is important to use the BUSY interlock before writing to either register.

Reading the Data Register while BUSY is set will yield erroneous data but will not impair board operation or contaminate any filter settings. This event is not flagged, so it is important to use the BUSY interlock before reading the Data Register.

It is not possible to write '0' to the BUSY bit from the VMEbus, so this is not an error. Attempting to write '1' to the BUSY bit when it is already set is also not an error condition and therefore is not flagged.

POWER DISTRIBUTION AND GROUNDING

In an effort to minimize noise and channel-to-channel cross talk, the VM8PF uses individual linear voltage regulators and separate supply filtering for each channel. The common analog power source is a pair of low noise DC/DC converters, which are separately regulated and filtered. Each channel has its own ground and power planes that connect to the common isolated supply in a "star" arrangement.

While all channels share a common low noise analog signal ground, they are galvanically isolated from the VMEbus and chassis grounds. Thus, the VM8PF board can be ground referenced to external equipment through the I/O cabling without causing ground loops.

Figure A-1
VM8PF Filter Programming Hardware Interface

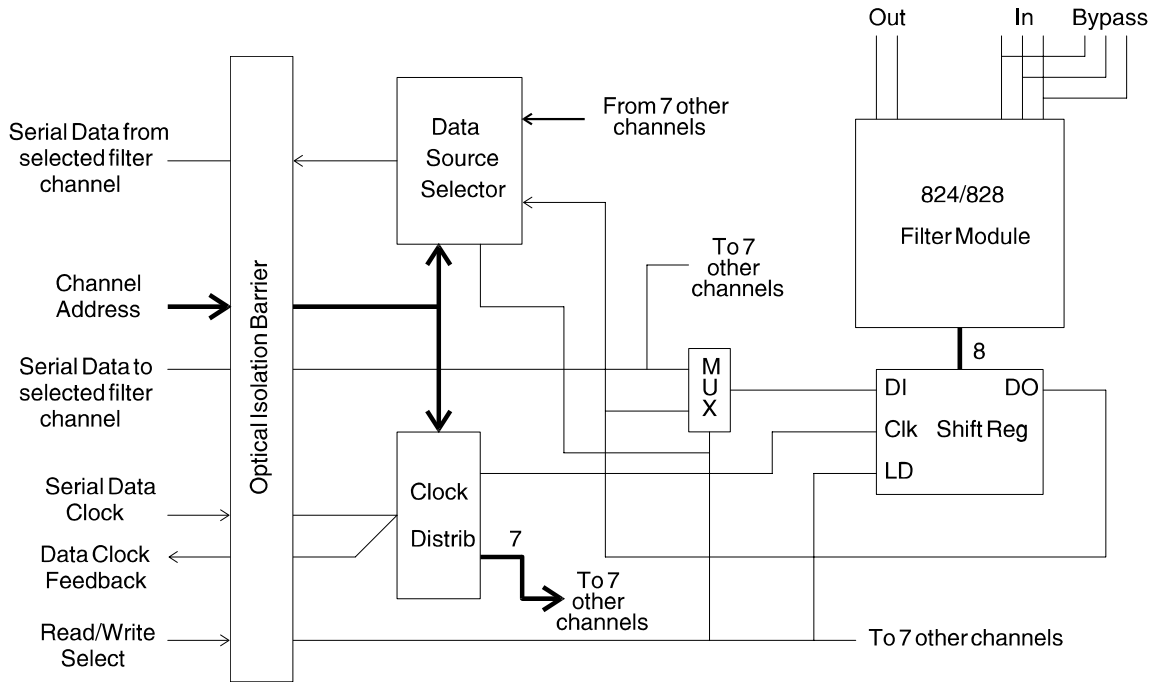

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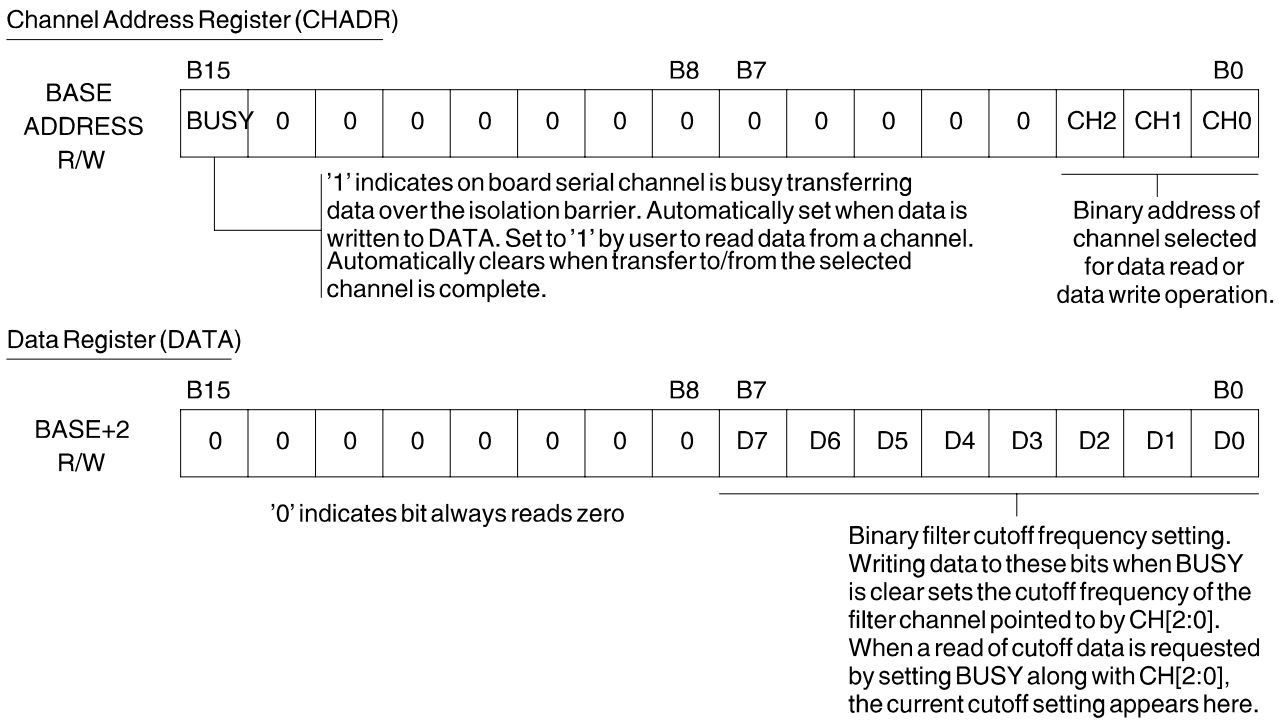
Figure A-2
VM8PF Register Map



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Appendix B
VM8PF Specifications

(@ 25°C and rated Power Input)

Analog Input

1. Input Impedance	1 MΩ
2. Input Range	+/-10V pk. linear
3. Maximum Input	+/-15V
4. Common Mode Rejection	70 dB typ., 60 dB min. DC to 1 kHz

Analog Output

5. Impedance	1Ω typ., 10Ω max.
6. Linear Operating Range	+/-10V pk.
7. Channel-to-Channel Crosstalk	-95 dB typ. DC to 100 kHz
8. Maximum Current	+/-2 mA
9. Offset Voltage	+/-2mV typ., trimmable to zero
10. Short Circuit Protection	Short to Ground

Filter Characteristics

11. See 824 and 828 Series specifications
12. External 8-bit CMOS latches hold frequency data

Gain

13. Low-pass	x1, +/-1%
High-pass	x1, +/-2%

VMEbus

14. Interface	A16/D16, D08(EO) Slave only, VME Spec. Rev. C.1

Power Required

15. From VME Backplane	+5V, 3.5 A max.

Environmental

16. Operating	0°C to +70°C
17. Storage	-25°C to +85°C
18. Humidity	0-95% non-condensing

Mechanical

19. Card Size	VMEbus 6U single slot 9.17 x 6.3 inches, (233 x 160 mm)
20. No. of Input Channels	8 Differential - DC coupled
21. No. of Output Channels	8 Single Ended - DC coupled
22. Mating Connectors	25-pin "D", Quantity 3
23. Weight	3 lbs., (1.36 kg.)

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Appendix C
VM8PF Ordering Guide

Available Low Pass Filter Options

D828L8B	8-pole Butterworth
D828L8E	8-pole, 6-zero elliptic 1.77 (-80dB)
D828L8EX	8-pole, 6-zero elliptic 1.56 (-80dB)
D828L8EY	8-pole, 6-zero elliptic 2.00 (-100dB)
D828L8L	8-pole, Bessel
D828L8D60	8-pole, constant delay (-60dB)
D828L8D80	8-pole, constant delay (-80dB)
D828L8D10	8-pole, constant delay (-100dB)
D824L8B	4-pole Butterworth
D824L8L	4-pole Bessel
D824L8Y2	4-pole Chebychev (0.2dB Ripple)
D824L8Y5	4-pole Chebychev (0.5dB Ripple)

Available High Pass Filter Options

D828H8B	8-pole Butterworth
D828H8E	8-pole, 6-zero elliptic 1.77 (-80dB)
D828H8EX	8-pole, 6-zero elliptic 1.56 (-80dB)
D828H8EY	8-pole, 6-zero elliptic 2.00 (-100dB)
D824H8B	4-pole Butterworth
D824H8Y2	4-pole Chebychev (0.2dB Ripple)
D824H8Y5	4-pole Chebychev (0.5dB Ripple)

Available Band Pass Filter Options

824BP	2-pole pair
828BP	4-pole pair

Available Band Reject Filter Options

828BR	4-pole pair

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Ordering Information

For flexibility in many applications the Frequency Devices VM8PF VMEbus Filter board may be ordered with two different filters on the same board. Channels 0 through 3 may be configured with one filter model while channels 4 through 7 are configured with a different model.

VM8PF-D828H8E-2/D828L8E-6

Channels 0, 1, 2, and 3 ← D828H8E-2 | D828L8E-6 → Channels 4, 5, 6, and 7

Note: See the D824, D828, 828BP, and 828BR Data Sheets for available models and tuning ranges.

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