Project designation

HAWK216OEM1 Camera

Document title

HAWK216OEM1 User Manual

This document is the property of Raptor Photonics and must not be copied, shown or in any way be communicated to persons other than those requiring the information for the execution of their duty.

DOCUMENT VALIDATION

	Name	Title	Date
Prepared	Paul Carson	Raptor Photonics	11th December 2013
Reviewed	Chris Davis	Raptor Photonics	27th May 2014
Reviewed			
Reviewed			
Reviewed			
Reviewed			
Approved			
Authorized			

DOCUMENT CHANGE RECORD

Issue	Change order	Date	Pages affected	Comment
0.1		11th Dec 2013		DRAFT
1.0		27th May 2014		Reviewed, updated and released
1.1		19th Aug 2014	7	Corrected IRIS pinout.

TABLE OF CONTENTS

ACRONYMS

EMCCD	Electron Multiplying Charge Coupled Device
EEPROM	Electrically Erasable Programmable Read Only Memory
FPGA	Field Programmable Gate Array
FPS	Frames per Second
LSB	Least Significant Bit
MHz	Megahertz
MSB	Most Significant Bit
PCB	Printed Circuit Board
TEC	Thermo Electric Cooler
UART	Universal Asynchronous Receiver/Transmitter

Table 1: Acronyms

1 SCOPE

This document details the design for the HAWK216OEM1 (P/N: HK216-AN-OEM1) camera.
The HAWK216OEM1 camera utilises an e2v CCD216 EMCCD sensor to provide low light imaging.
Details of the camera electrical interfaces and communication protocols are also provided.

A photograph of the complete Camera module is shown in Figure 1: Camera (Photograph).

Figure 1: Camera (Photograph)

2 DESIGN OVERVIEW

2.1 Mechanical Profile

Figure 2: Mechanical profile drawing – SolidWorks model

2.2 Physical Interfaces

2.2.1 Power, Trigger & Communications - 9 pin MicroD socket (Glenair MDM-9SBSP)

The pin-out table is shown below.
The Associated plug connector part # is: MWDM2L-9P-xxx-xx.

Pin	I/O	Signal Name	Cable Colour
1	In/Out	RS485-A	Yellow
2	In/Out	RS485-B	Orange
3	-	-	Red
4	-	GROUND	Brown
5	In	+12V	Black
6	-	-	Grey
7	-	-	Violet
8	Out	Trigger Out	Blue
9	-	-	Green

Table 2: Control & Power Connector Pinout

2.2.2 Video Out - Coaxial socket (Molex 73391-0070)

The pin-out table is shown below.

Pin	I/O	Signal Name
Inner	Out	Video
Outer	-	GROUND

Table 3: Video Connector Pinout

2.2.3 IRIS Control - 4 pin socket (Kobi 163-158N-2-E)

The pin-out table is shown below.

Pin	I/O	Signal Name
1	Out	+12V/ Damp-
2	Out	NC/Damp+
3	Out	Video/ Drive+
4	-	GROUND/ Drive-

Table 4: IRIS Connector Pinout

2.2.4 Ground

The design uses one single ground on all PCBs. Each PCB will be multilayer with at least 1 solid ground plane. Each of the flex connections between PCBs will also have a complete Ground the full width of the flex. All mounting holes are through hole plated with pads and directly connected to Ground with no thermal relief. Flood fills top and bottom are also connected to Ground.

3 DESIGN DETAILS

3.1 Electrical Design

3.1.1 Power supplies and Thermo-Electric Cooler (TEC)

Unit input power specification is +12V ±10% with a maximum of 6.6 Watts power dissipation with the TEC cooler disabled. Additional inrush current (peak power) is required when the TEC power is switched from low to high. Peak power < 13 Watts. The total, maximum steady state, unit power dissipation is 7.6 Watts.

The default set point for the TEC cooling is **+5**^{o}C. The TEC power supply is automatically adjusted to reach the set point temperature, with a limit of approximately 1 Watt.
At low ambient temperatures or with additional heat sinking the TEC efficiency is increased and consequently the power required to achieve the set point is decreased.

3.1.2 CCD216 Image Sensor

- 768*244 active element
- 11.5um x 27um pixel size
- Fully hermetically sealed case with inbuilt TEC
- 1 output
- Frame rate = 59.94 Frames/Second (fps)
- Readout noise = 45e^{-}
- 13.5 MHz pixel clock

Refer to e2v CCD216_BI datasheet for further details, available at www.e2v.com.
The CCD216 is an Electron Multiplying device which allows the application of Electron Multiplication (EMGain).

3.1.3 Communications Interface

The RS485 communication interface has the specifications as listed in Table 5: RS485 Settings.

Baud rate:	115200 bps
Data bits:	8
Parity:	None
Stop bits:	1
Flow control:	None

Table 5: RS485 Settings

These settings are fixed and cannot be altered.
The RS485 signals have an internal 120R termination resistor.

3.1.4 Analogue Video output

The camera produces interlace analogue video in the 525 line NTSC mono format, with no chrominance subcarrier, ITU-R BT.1700 (59.94Hz, 2:1 interlace, 4:3 aspect ratio).

The video output has a 75R source impedance.

3.1.5 Trigger Output

The trigger output has a 510Ω source impedance with a 100 microsecond 3.3V pulse synchronised to the video out Vertical Sync pulse.

3.2 Functionality

3.2.1 Automatic Gain Control (AGC)

The AGC is enabled by default.

The AGC has 3 input parameters that the operator can adjust to customise the camera operation for the ambient light environment, namely AGC Speed, AGC Peak/Average and AGC Auto Level.

AGC Auto Level is the image intensity that the AGC will attempt to achieve as an average/peak across the scene. This setting can be adjusted alongside **AGC Peak/Average** to achieve desired light level.

The AGC has two variables used to achieve the desired light level, namely the Electron Multiplying (EM) Gain and the IRIS aperture.
When the Auto IRIS is enabled in a low ambient light scene the AGC will fully open the IRIS shutter before adjusting the EM Gain, whereas in a high ambient light scene the AGC will reduce the EM gain before closing the IRIS shutter.

3.2.2 EM Gain

If the AGC is disabled the Electron Multiplication Gain can be manually adjusted using serial commands as detailed in section 4 Serial Communication. It should be noted that the EM Gain Maximum value stored in the EEPROM must not be exceeded.
If the EM Gain Maximum is exceeded the camera may be permanently damaged.
The EM Gain Maximum value can be read back from the camera using a GET command as detailed in section 4.4 Query Commands.

3.2.3 Exposure Period

The exposure period is fixed at approximately 15.74 milliseconds.

3.2.4 Unit Serial number

Can be read from the camera's EEPROM. Refer to section 4 Serial Communication for further details.

4 SERIAL COMMUNICATION

4.1 Overview

For version 2.7 of the Micro firmware, the Power on default settings for camera serial port are;

- 115200 baud
- 1 start bit
- 8 data bits
- 1 stop bit

UART message format from Host to camera

Command	Data 1	Data 2	.....	Data n	ETX	Chk_Sum

The first Byte is the command to the Microcontroller in the camera, following bytes contain data required by the command, and the ETX byte terminates the command. 0x50 is always used to terminate the command. An additional check sum byte may also be required to be sent by the host if check sum mode is enabled.

UART message format from camera to Host

Data 1	Data 2	.....	Data n	ETX	Chk_Sum

All or none of the above bytes may be sent in response to commands from the host depending on the commands sent by the host.

An optional mode of operation is included in the firmware for command acknowledge. Once enabled the camera will respond to all commands send by the host. After the camera has received and processed the command from the host, a single command acknowledge byte will be sent at the end of transmission (ETX) i.e. should the host command require data to be sent from the camera then the ETX byte will be sent at the end of the requested data.

Another optional mode of operation is included in the firmware is for check sum operation, this mode should only be used when the command acknowledge mode is enabled. Once the check sum mode is enabled the camera will only act upon commands that are received with the correct check sum byte sent at the end of the command packet. Note that if the check sum feature is not enabled check sum bytes may still be sent at the end of a command packet, the command will be processed and the check sum will be ignored. The check sum byte should be the result of the Exclusive OR of all bytes in the Host command packet including the ETX byte.

When check sum mode is enabled data returned from the camera will include an echo of the checksum from the host command

By default the camera will boot up with both command acknowledge and check sum operation disabled.

It is intended that the camera be operated from a higher level perspective whereby complete UART messages or groups of UART messages are used to achieve required camera functionality.
Bits in registers that have not been identified in the documentation should be ignored.

Once a command has been received by the camera all sub sequent commands from the host will be ignored until the command has been processed.

4.2 ETX/ERROR codes

Error codes will be sent as ETX characters by the camera in response to commands that have failed.

0x50	ETX	Command acknowledge, command processed successfully.
0x51	ETX_SER_TIMEOUT	Partial command packet received, camera timed out waiting for end of packet. Command not processed
0x52	ETX_CK_SUM_ERR	Check sum transmitted by host did not match that calculated for the packet. Command not processed
0x53	ETX_I2C_ERR	An I2C command has been received from the Host but failed internally in the camera.
0x54	ETX_UNKNOWN_CMD	Data was detected on serial line, command not recognized
0x55	ETX_DONE_LOW	Host Command to access the camera EPROM successfully received by camera but not processed as EPROM is busy. i.e. FPGA trying to boot.

4.3 Set Commands

Set Command	Serial Packet	Comments
Set system state	0x4F 0x**YY** 0x50	YY Bit 6= 1 to enable check sum mode YY Bit 4 = 1 to enable command ack YY Bit 1 = 0 to Hold FPGA in RESET YY Bit 0 = 1 to enable EEPROM comms YY Bits 2,3,5,7 = reserved
Set FPGA CTRL reg	0x53 0xE0 0x02 0x00 0x**YY** 0x50	YY Bit 0 - 1=TEC ON (Default=1) YY Bit 1 - unused YY Bit 2 - unused YY Bit 3 - 1 = AGC ON (Default=1) YY Bit 4 - unused YY Bit 5 - unused YY Bit 6 - unused YY Bit 7 - unused
Set AGC Auto level	0x53 0xE0 0x02 0x23 0x**MM** 0x50 0x53 0xE0 0x02 0x24 0x**LL** 0x50	10 bit value – max 0x012B = White MM bits 1..0 = level bits 9..8 LL = level bits 7..0 (default = 0x012B)
Set AGC PEAK/Average Ration	0x53 0xE0 0x02 0x2D 0x**YY** 0x50	YY 8-bit value 0 = Full Peak 255 = Full Average (default = 0x7F)
Set AGC speed	0x53 0xE0 0x02 0x2F 0x**YY** 0x50	YY Bits 7..4 = EM speed(Default=F) YY Bits 3..0 = EXP speed(Default=F)
Set EM gain (AGC must be disabled)	0x53 0xE0 0x02 0x15 0x0**L** 0x50 0x53 0xE0 0x02 0x16 0x**MM** 0x50	**Never exceed the EM Gain Maximum stored in the EEPROM.** 12 bit word; L = 4 MSBs (Upper nibble) MM = 8 LSBs
Set TEC Target temperature	0x53 0xE0 0x02 0x1A 0x0**L** 0x50 0x53 0xE0 0x02 0x1B 0x**MM** 0x50	12 bit word; L = 4 MSBs (Upper nibble) MM = 8 LSBs
Set TEST PATTERN	0x53 0xE0 0x02 0xFA 0x**YY** 0x50	YY Bit 7= 1 Gamma Enabled (Default) YY Bit 7= 0 Gamma Disabled YY Bit 6= 1 Trigger Out Enabled (Default) YY Bit 6= 0 Trigger Out Disabled Bit 3 Bit 2 Bit 1 Bit0 (of YY) 0 0 0 0 Normal(Default) 0 0 0 1 Incrementing TP 0 0 1 0 Full White 0 0 1 1 ½ White 0 1 0 0 ¼ White 0 1 0 1 Const. 64 0 1 1 0 Const. 128 0 1 1 1 Const. 256 1 0 0 0 Black 1 0 0 1 Vert Stripes

4.4 Query Commands

Query Command	Send Serial Packet	Comments
Get system status	0x49 0x50	1 Byte returned YY Bit 6= 1 Check sum mode enabled YY Bit 4 = 1 Command acknowledge enabled YY Bit 1 = 0 Hold FPGA in RESET YY Bit 0 = 1 EEPROM enabled YY Bits 2,3,5,7 = reserved
Get FPGA CTRL reg	0x53 0xE0 0x01 0x00 0x50 0x53 0xE1 0x01 0x50	YY Bit 0 - 1=TEC ON (Default=0) YY Bit 1 - unused YY Bit 2 - unused YY Bit 3 - 1 = AGC ON (Default=1) YY Bit 4 - unused YY Bit 5 - unused YY Bit 6 - unused YY Bit 7 - unused
Get AGC Auto level	0x53 0xE0 0x01 0x23 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x24 0x50 0x53 0xE1 0x01 0x50	2 bytes returned MM,LL - 10 bit value 0M bits 1..0 = level bits 9..8 LL = level bits 7..0
Get PEAK/Average setting	0x53 0xE0 0x01 0x2D 0x50 0x53 0xE1 0x01 0x50	YY 8-bit value 0 = Full Peak 255 = Full Average
Get AGC speed	0x53 0xE0 0x01 0x2F 0x50 0x53 0xE1 0x01 0x50	YY Bits 7..4 = EM speed(Default=7) YY Bits 3..0 = not used
Get EM gain Maximum	0x53 0xE0 0x01 0x35 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x36 0x50 0x53 0xE1 0x01 0x50	2 bytes returned 0M,LL – 12 bit word 0M = 4 MSBs LL = 8 LSBs
Get EM gain	0x53 0xE0 0x01 0x15 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x16 0x50 0x53 0xE1 0x01 0x50	2 bytes returned 0M,LL – 12 bit word 0M = 4 MSBs LL = 8 LSBs
Get TEC Target Temperature	0x53 0xE0 0x01 0x1A 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x1B 0x50 0x53 0xE1 0x01 0x50	2 bytes returned 0M,LL – 12 bit word 0M = 4 MSBs LL = 8 LSBs
Get TEST PATTERN state	0x53 0xE0 0x01 0xFA 0x50 0x53 0xE1 0x01 0x50	1 byte returned YY Bit 7= 1 Gamma Enabled (Default) YY Bit 7= 0 Gamma Disabled YY Bit 6= 1 Trigger Out Enabled (Default) YY Bit 6= 0 Trigger Out Disabled Bit 3 Bit 2 Bit 1 Bit0 (of YY) 0 0 0 0 Normal(Default) 0 0 0 1 Incrementing TP 0 0 1 0 Full White 0 0 1 1 ½ White 0 1 0 0 ¼ White 0 1 0 1 Const. 64

		0 1 1 0 Const. 128 0 1 1 1 Const. 256 1 0 0 0 Black 1 0 0 1 Vert Stripes s
Get CCD silicon temperature	0x53 0xE0 0x01 0x6E 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x6F 0x50 0x53 0xE1 0x01 0x50	2 bytes returned 1st byte = Top nibble (top 4 bits=0) 2nd byte = Lower byte Counts = ((1st byte x 256)+2nd byte) Conversion formula to deg C Temperature = `-25.41ln(counts) + 162.16`
Get CCD PCB temperature	0x53 0xE0 0x01 0x70 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x71 0x50 0x53 0xE1 0x01 0x50	2 bytes returned 1st byte = Top nibble (top 4 bits=0) 2nd byte = Lower byte Counts = ((1st byte x 256)+2nd byte) If counts<2048: Positive Temperature °C=counts/16 If counts>2047: Negative Temperature °C=(counts-4096)/16
Get PWR PCB temperature	0x53 0xE0 0x01 0x72 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x73 0x50 0x53 0xE1 0x01 0x50	2 bytes returned 1st byte = Top nibble (top 4 bits=0) 2nd byte = Lower byte Counts = ((1st byte x 256)+2nd byte) If counts<2048: Positive Temperature °C=counts/16 If counts>2047: Negative Temperature °C=(counts-4096)/16
Get Micro version	0x56 0x50	Two bytes transmitted from camera when command received. 1st byte Major version 2nd byte Minor version.
Get FPGA version	0x53 0xE0 0x01 0x7E 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x7F 0x50 0x53 0xE1 0x01 0x50	Set address 7E (Major Version Byte) Read address 7E, 1 byte Set address 7F (Minor Version Byte) Read address 7F, 1 byte
Get Unit Serial Number	0x4f 0x13 0x50 0x53 0xAE 0x05 0x01 0x00 0x00 0x02 0x00 0x50 0x53 0xAF 0x02 0x50 0x4f 0x12 0x50	Enable EEPROM access 2 bytes returned: 1st byte is the LSB 2nd is the MSB Disable EEPROM access

NOTES:

- Command 0x4F writes to the system status register, 0x49 reads from the system status register.

4.5 Examples

NOTE: Assume that Command Acknowledge and Check sum mode are disabled unless otherwise stated

4.5.1 Get System Status

From power up

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get system status	0x49 0x50	0x22 (Ext' comms disabled)

4.5.2 Get Micro version

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get Micro version	0x56 0x50	0x01 0x01 (V1.1)

4.5.3 Get FPGA version

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get FPGA version	0x53 0xE0 0x01 0x7E 0x50	none
	0x53 0xE1 0x01 0x50	0x01
	0x53 0xE0 0x01 0x7F 0x50	none
	0x53 0xE1 0x01 0x50	0x03 (V1.3)

4.5.4 Get FPGA version with checksum

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get FPGA version	0x53 0xE0 0x01 0x7E 0x50 0x9C	none
	0x53 0xE1 0x01 0x50 0xE3	0x01
	0x53 0xE0 0x01 0x7F 0x50 0x9D	none
	0x53 0xE1 0x01 0x50 0xE3	0x03 (V1.3)

4.5.5 Get Unit Serial Number

Note that this command will also reset the FPGA. Suggest Serial number read at power up.

Command	TX bytes (to camera)	RX'd bytes (From camera)
Enable EEPROM Comms	0x4f 0x13 0x50	none
Read back EEPROM device ID to confirm EEPROM is available for read access. Repeatedly send both commands until correct bytes returned.	0x53 0xAE 0x02 0x05 0x00 0x50	none
	0x53 0xAF 0x04 0x50	0x1E 0xA0 0x00 0xC3
Get Unit Serial Number	0x53 0xAE 0x05 0x01 0x00 0x00 0x02 0x00 0x50	none
	0x53 0xAF 0x02 0x50	0xEA 0x03 (S. no. 1002)
Disable EEPROM Comms	0x4f 0x12 0x50	none

4.5.6 Read Sensor PCB temperature

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get Sensor PCB temperature	0x53 0xE0 0x01 0x70 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x71 0x50 0x53 0xE1 0x01 0x50	0x02 0x50

		0x69 0x50 Temp = 0x269 = 617/16 = +38C

4.5.7 Enable Auto Gain control (AGC)

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get FPGA Status byte	0x53 0xE0 0x01 0x00 0x50	
	0x53 0xE1 0x01 0x50	**0x11**
Binary OR status byte with 0x08 (bit 3=1)	none	none
Send byte i.e. Enable AGC	0x53 0xE0 0x02 0x00 **0x19** 0x50	none

NOTE
- default value for AGC = ON
- default value for TEC = ON
- default value IRIS = ON

4.5.8 Disable TEC

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get FPGA Status byte	0x53 0xE0 0x01 0x00 0x50	none
	0x53 0xE1 0x01 0x50	**0x19**
Binary AND status byte with 0xFE (bit 0=0)	none	none
Send byte i.e. Disable TEC	0x53 0xE0 0x02 0x00 **0x18** 0x50	none

4.5.9 Enable Command acknowledge

Assume cmd ack = 0 to start

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get system status	0x49 0x50	0x06
Binary OR status byte with 0x10	none	none
Enable Command Acknowledge	0x47 0x16 0x50	0x50 (ack)

After ack is set

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get Micro version	0x56 0x50	0x01 0x02 0x50 (v1.2+ack)

APPENDIX A - FPGA FIRMWARE UPLOAD

CAMERA EPROM

The camera EEPROM is divided into 15 sectors with address spaces as outlined below. Note that each address points to a 16bit word.

/* Sector Structure...

Sector	Kwords	words	start	end	start	end
1	4	4096	0	4095	000000	000FFF
2	4	4096	4096	8191	001000	001FFF
3	4	4096	8192	12287	002000	002FFF
4	4	4096	12288	16383	003000	003FFF
5	4	4096	16384	20479	004000	004FFF
6	4	4096	20480	24575	005000	005FFF
7	4	4096	24576	28671	006000	006FFF
8	4	4096	28672	32767	007000	007FFF
9	32	32768	32768	65535	008000	00FFFF
10	32	32768	65536	98303	010000	017FFF
11	32	32768	98304	131071	018000	01FFFF
12	32	32768	131072	163839	020000	027FFF
13	32	32768	163840	196607	028000	02FFFF
14	32	32768	196608	229375	030000	037FFF
15	32	32768	229376	262143	038000	03FFFF

SECTOR 1 - is used for Manufacture specific data i.e. serial number etc.

SECTORS 2-15 are used to hold the FPGA configuration information.

To program a new FPGA configuration
1. Sectors 2-15 must be erased
2. a new bit file must be uploaded to Sectors 2-15

Note that SECTOR 1 must not be ERASED as this contains detailed data about the camera.

SECTOR ERASE

The following command is used to erase a sector.

SECTOR xx ERASE - 0x53 0xAE 0x05 0x04 0xAA 0xBB 0xCC 0x00 0x50

Where the Hex Number AABBCC represents an address in the sector to be erased. After the SECTOR erase command has been issued a small delay is required for the ERASE to take place. Successful erase can be determined by polling the sector with the following command.

0x53 0xAF 0x01 0x50

If a value of 0xFF is returned the sector erase is complete.

Example Sector ERASEs

SECTOR 2 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x10 0x00 0x00 0x50

0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 3 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x20 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 4 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x30 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 5 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x40 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 6 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x50 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 7 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x60 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 8 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x70 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 9 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 10 ERASE - 0x53 0xAE 0x05 0x04 0x01 0x00 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 11 ERASE - 0x53 0xAE 0x05 0x04 0x01 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 12 ERASE - 0x53 0xAE 0x05 0x04 0x02 0x00 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 13 ERASE - 0x53 0xAE 0x05 0x04 0x02 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 14 ERASE - 0x53 0xAE 0x05 0x04 0x03 0x00 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 15 ERASE - 0x53 0xAE 0x05 0x04 0x03 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)

SECTOR PROGRAMMING

Bursts of 32 DATA bytes (sixteen 16bit words) should be sent to the EPROM using a single command, the EPROM will auto increment the addresses.

Burst write command
0x53 0xAE 0x25 0x02 0xAA 0xBB 0xCC 0xN1 0xN2 0xN3 .....0xN32 0x00 0x50

The address of the burst write is given by AABBCC, 32 DATA bytes as read from bit file are sent N1-N32 Address AABBCC should start at the base address of sector 2 i.e. 0x001000 and increment by 16 for every burst command until the end of file.

At the end of file the last burst may not require 32bytes due to the file size, if this is the case the last 32 should be padded out to 32. Data in padding ignored.

Notes :
- It is recommended to operate the camera with Command Ack. Waiting for a command Ack will ensure burst writes have taken place before moving to the next burst write.
- The bit stream contains a check sum that is used by the FPGA during power up. If data is corrupted during upload the FPGA will not boot.
- Verification that FPGA has successfully booted can be done by reading the FPGA version number.

Example command list

Command	TX bytes (to camera)	RX'd bytes (from camera)	Comments
Enable Command Acknowledge	0x47 0x12 0x50	0x50 (ack)	
Enable FPGA programming	0x4f 0x03 0x50	0x50	
Erase EEPROM sector 2	0x53 0xAE 0x05 0x04 0x00 0x10 0x00 0x00 0x50	0x50	
Confirm Sector 2 erase (by reading LSByte)	0x53 0xAF 0x01 0x50	0xFF 0x50	Poll until 0xFF is returned
Erase EEPROM sectors 3-15 and confirm erase after each sector.	As above with relevant sector address	As above	Poll after each sector is erased until 0xFF is returned
Burst write 32 bytes of bit file	0x53 0xAE 0x25 0x02 0x00 0x10 0x00 0xN1 0xN2 0xN3 .....0xN32 0x00 0x50	0x50	1st burst starting at Sector 2 address.
Multiple burst writes of 32 bytes of bit file	0x53 0xAE 0x25 0x02 0xAA 0xBB 0xCC 0xN1 0xN2 0xN3 .....0xN32 0x00 0x50	0x50	Address 0xAABBCC starts at sector 2 base address and needs to be incremented by 16 for each successive burst until end of file.
Enable External Comms	0x4f 0x02 0x50	0x50	FPGA will now boot with new firmware, need to delay approx. 500msec
Get FPGA version	0x53 0xE0 0x01 0x7E 0x50	0x50	Version 1.13
	0x53 0xE1 0x01 0x50	0x01 0x50	
	0x53 0xE0 0x01 0x7F 0x50	0x50	
	0x53 0xE1 0x01 0x50	0x0D 0x50	
Disable External Comms	0x4f 0x22 0x50	0x50	Disable External Comms