User Manual

Industrial Ethernet PHY

Single PHY ASSP

uPD60610
uPD60611

Renesas Electronics
www.renesas.com

Doc number R19UH0082ED0201
April 9, 2013

Notice

The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

“Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

“High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti- crime systems; safety equipment; and medical equipment not specifically designed for life support.

“Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.

Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.

Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority- owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

General Precautions in the Handling of ASSP Products

The following usage notes are applicable to the series of these ASSP products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of ASSP Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.The characteristics of ASSP in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Patent for IEEE1588

A number of patents exist for systems related to IEEE1588. Renesas would request that customers ensure they comply with the relevant rights for these patents. Renesas does not accept any responsibility for infringement of any patent rights by the customer.

How to Use This Manual

Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the PHY. It is intended for users designing application systems incorporating the PHY. A basic knowledge of electric circuits, logical circuits, and PHYs is necessary in order to use this manual. The manual comprises an overview of the product; descriptions of the PHY, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the uPD60610/60611 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description. Note: Refer to the application notes for details on using peripheral functions.	User's manual Industrial Ethernet PHY Single PHY ASSP	This User's manual R19UH0082ED0201
Application Note	Information on board design and wiring. Examples of schematics and board layout.	Application Note industrial Ethernet Single PHY ASSP Layout recommendation and design rule	R19AN0014ED0101
Application Note	Information on using and configuring special functions and application examples.	Application Note Industrial Ethernet PHY ASSP Programming Guide	R19AN0010ED0100
Renesas Technical	Product specifications, updates on documents,	Customer Notification	R19TU0003ED0100

Update	etc.	Ethernet PHY Operating Precautions	

Notation of Numbers and Symbols

Abbreviation	Full Form
Register p.n	Register n at PHY address p
Register p.n.b	Bit ‘b’ in register address n at PHY address p
Register PHY.n	PHY stands for PHY address “0” or “1” so this would mean register n in any of the two PHYs, can by PHY address 0 or PHY address 1.

Register Notation

Abbreviation	Full Form
RW	Readable or writeable
SC	Self Clearing
RO	Read Only
WO	Write Only
LH	Latch High, when the device sets the register it stays high until actively written to 0 even if the condition that set it disappears
LL	Latch Low, the register stays low until actively written to 1
NASR	Not affected by software reset
WC	Cleared by hardware after writing
RC	Cleared after reading by hardware

List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
Autoneg	Autonegotiation
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
FD	Full Duplex Mode
HD	Half Duplex mode
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PU	Pull Up
PD	Pull Down
PWM	Pulse Width Modulation
SFR	Special Function Register
VCO	Voltage Controlled Oscillator
PTP	Precision Timer Protocol

Table of Contents

General Description 12
1.1 Overview of product features 12
1.2 Special product features 13
1.3 Applications 13

Pin Functions 14
2.1 Pinning Information 14
2.1.1 Pin Layout 14
2.1.2 Port Pins 15

System Diagram 17
3.1 Device block diagram 17

Global Hardware Description 18
4.1 Register Access 18
4.2 General SMI Control Register 7.31 19
4.3 Power Control Register 7.30 19
4.4 PHY Status Register 7.28 20
4.5 Strap option Register 7.27 20
4.6 PHY LED Status Register 7.24 21
4.7 Interrupt Status register 7.20 22
4.8 Interrupt Mask register 7.21 23
4.9 GPIO 24
4.9.1 GPIO_CONFIG_0 Register 7.0 24
4.9.2 GPIO_CONFIG_1 Register 7.1 25
4.9.3 GPIO_CONFIG_2 Register 7.2 26
4.9.4 GPIO_CONFIG_3 Register 7.3 26
4.9.5 GPIO_CONFIG_4 Register 7.4 27
4.10 LED configuration 28
4.11 LED-Mux 30
4.12 Strap Options 31

PHY 32
5.1 General Description 32
5.2 Clock Generator PLL 33
5.3 Analogue Frontend 33
5.3.1 Adaptive Equalizing 33
5.3.2 100Base TX Receiver ADC 33
5.4 Digital Signal Handling 33
5.4.1 DSP 33
5.4.2 Baseline Wander Correction 33

5.4.3 NRZI/MLT-3 Encoding / Decoding 34
5.4.4 Scrambler / Descrambler 34
5.4.5 5B/4B Encoding / Decoding 34
5.5 Functional Description 36
5.5.1 Collision detection 36
5.5.2 Carrier Sense detection 36
5.5.3 Auto Crossover (MDI/MDI-X) 36
5.5.4 Auto-Polarity 37
5.5.5 Auto-Negotiation 37
5.5.6 Bad Line recognition 43
5.5.7 Latency 51
5.5.8 Special Isolate 52
5.6 PHY Register List 53
5.6.1 Register PHY.0 - Basic Control 53
5.6.2 Register PHY.1 - Basic Control 54
5.6.3 Register PHY.2 - PHY Identifier 55
5.6.4 Register PHY.3 - PHY Identifier 55
5.6.5 Register PHY.4 - Auto-Negotiation Advertisement 56
5.6.6 Register PHY.5 - Auto-Negotiation Link Partner Ability (Base Page) 57
5.6.7 Register PHY.5 - Auto-Negotiation Link Partner Ability (Next Page) 58
5.6.8 Register PHY.6 - Auto-Negotiation Expansion 58
5.6.9 Register PHY.7 - Auto-Negotiation Next Page Transmit 59
5.6.10 Register PHY.16 - Silicon Revision 59
5.6.11 Register PHY.17 - Mode Control/Status 60
5.6.12 Register PHY.18 - Special Modes 61
5.6.13 Register PHY.19 - Elastic Buffer Status register (Loopback Mode only) 61
5.6.14 Register PHY.20 – Reserved 62
5.6.15 Register PHY.21 – Reserved 62
5.6.16 Register PHY.22 – Reserved (TSTREAD2 / TSTWRT) 62
5.6.17 Register PHY.23 – BER Counter 63
5.6.18 Register PHY.24 – FEQ monitor Register 64
5.6.19 Register PHY.25 – Diagnosis Control/Status Register 65
5.6.20 Register PHY.26 – Diagnosis Counter Register 66
5.6.21 Register PHY.27 - Special Control/Status Indications 66
5.6.22 Register PHY.28 - Reserved 67
5.6.23 Register PHY.29 - Interrupt Source Flags 67
5.6.24 Register PHY.30 - Interrupt Enable 67
5.6.25 Register PHY.31 - PHY Special Control/Status 68
External Components 69
6.1 Clock 69
6.2 Internal Regulator 69
6.3 Power Up Sequence 69
Support of IEEE1588 (uPD60611 only) 70
7.1 IEEE1588 70

7.2 Register access to PTP 71
7.3 1588 Clock Control 71
7.3.1 CLOCK_STATUS Register 6.0 72
7.3.2 CLOCK_READ Register 6.1 72
7.3.3 CLOCK_WRITE Register 6.2 73
7.3.4 CLOCK_OFFSET Register 6.3 73
7.3.5 CLOCK_DRIFT Register 6.4 74
7.4 Frame Handling Unit 74
7.4.1 One step mode 75
7.4.2 Transparent Mode 75
7.4.3 Timestamp Status Register 6.6 76
7.4.4 Timestamp Configuration Register 6.7 77
7.4.5 TIMESTAMP_LINE_EVENT Register 6.8 78
7.4.6 PTP_CONFIG Register 6.9 79
7.4.7 PHY_DELAY_TX Register 6.11 82
7.4.8 PHY_DELAY_RX Register 6.12 82
7.5 Input Capture Unit 83
7.5.1 Input Event Control Register 7.12 84
7.5.2 Input Capture Pin Control register 7.8 85
7.5.3 Input Capture Pin Control register 7.9 85
7.5.4 Input Capture Pin Control register 7.10 86
7.5.5 INPUT_EVENT_DATA_READ_WORD Register 7.15 87
7.5.6 INPUT_EVENT_DATA_BLOCK_READ Register 7.14 88
7.5.7 INPUT_CAPTURE_DATA_POINTER Register 7.13 88
7.6 Pulse Generator Unit 89
7.6.1 Pulse Output Control Register 7.16 90
7.6.2 PULSE_STARTTIME Register 7.17 91
7.6.3 PULSE_WIDTH Register 7.18 92
7.6.4 PULSE_INTERVAL Register 7.19 92

Electrical Characteristics 93
8.1 AC Timing 93
8.1.1 Serial Management Interface (SMI) Timing 93
8.1.2 Reset Timing 94
8.1.3 Clock Timing 95
8.1.4 100Base-TX Timings 96
8.1.5 10Base-T Timings 98
8.1.6 RMII 10/100Base-TX Timings 100
8.1.7 Sequence for turn on 102
8.2 DC Characteristics 103
8.2.1 Absolute Maximum Ratings 103
8.2.2 Recommended Operating Conditions 104
8.2.3 DC Electrical Characteristics 105
8.2.4 100Base-TX Differential Parameters on Secondary Side of Transformer. 106
8.2.5 100Base-FX Output Characteristics 106

Physical dimensions **107**

Revision history **108**

General Description

The extended single channel 10/100 Ethernet PHY uPD60610 and the uPD60611 are fully integrated Physical layer devices to connect to standard IEEE802.3 Ethernet networks.

This devices specifically focus on low latency and low jitter to support today's industrial Ethernet standards. In addition it features hardware support for IEEE1588 V2. Renesas Electronics' specific enhanced diagnosis features allow a permanent cable quality monitoring for easy maintenance in factory automation.

The PHY can connect to unshielded twisted-pair (UTP) cable via external magnetics or to optical fiber via fiber PMD modules. To the upper layer (MAC) it interfaces to an Ethernet MAC layer through the IEEE 802.3 Standard Media Independent Interface (MII) or reduced MII interface.

The uPD60611 includes hardware support for PTP according to IEEE1588 Version 1 and 2. To support this a 80 bit clock is included in the PHY, based on this clock timestamps can be taken based on received and transmitted frames and based on events on external pins. The resolution for timestamps of received and transmitted telegrams is down to 1 ns by using internal PHY data. The device also supports one step and two step timestamp insertion and offers some special hardware support for transparent mode. It further offers a special signal to share the internal clock with other Renesas PHYs which then run on the same PTP clock.

1.1 Overview of product features

- Single channel PHY
- Fully standard compliant with IEEE 802.3i/802.3u for 100BASE-TX, 100BASE-FX and 10BASE-T
- Integrated PMD sub-layer featuring adaptive equalization and baseline wander correction
- IEEE 802.3u auto-negotiation and parallel detection
- Full and half duplex operation
- Supports automatic polarity detection and correction
- Supports automatic MDI/MDI-X crossover
- Supports IEEE1588 V1 and V2 (uPD60611 only)
- Highly configurable I/O configuration (uPD60611 only)
- 2.5V and 3.3V MAC interface
- Flexible MAC interface: MII and RMII
- Serial management port (MDC/MDIO)

- Supports user programmable interrupts
- Enables software power-up/down and automatic power up/down by energy detection
- Single 3.3 V power supply with optional separated 1.5V
- Operating temperature: $T_{ambient}$ = -40 to +85°C ($T_{junction}$ from -40 to +125°C)

1.2 Special product features

- Low latency and low jitter for industrial networking
- Fast link-up option in auto-negotiation
- Fast link-loss detection
- Cable monitoring and error detection
- Permanent cable quality tracking
- Enhanced system testability (such as bypass, loopback and cable length measurement by TDR)
- 1 ns resolution timer for hardware support of IEEE1588 (uPD60611 only)
- Timestamping function to timestamp incoming and outgoing telegrams and pin activity (uPD60611 only)
- Output pins controllable by internal PTP clock (uPD60611 only)

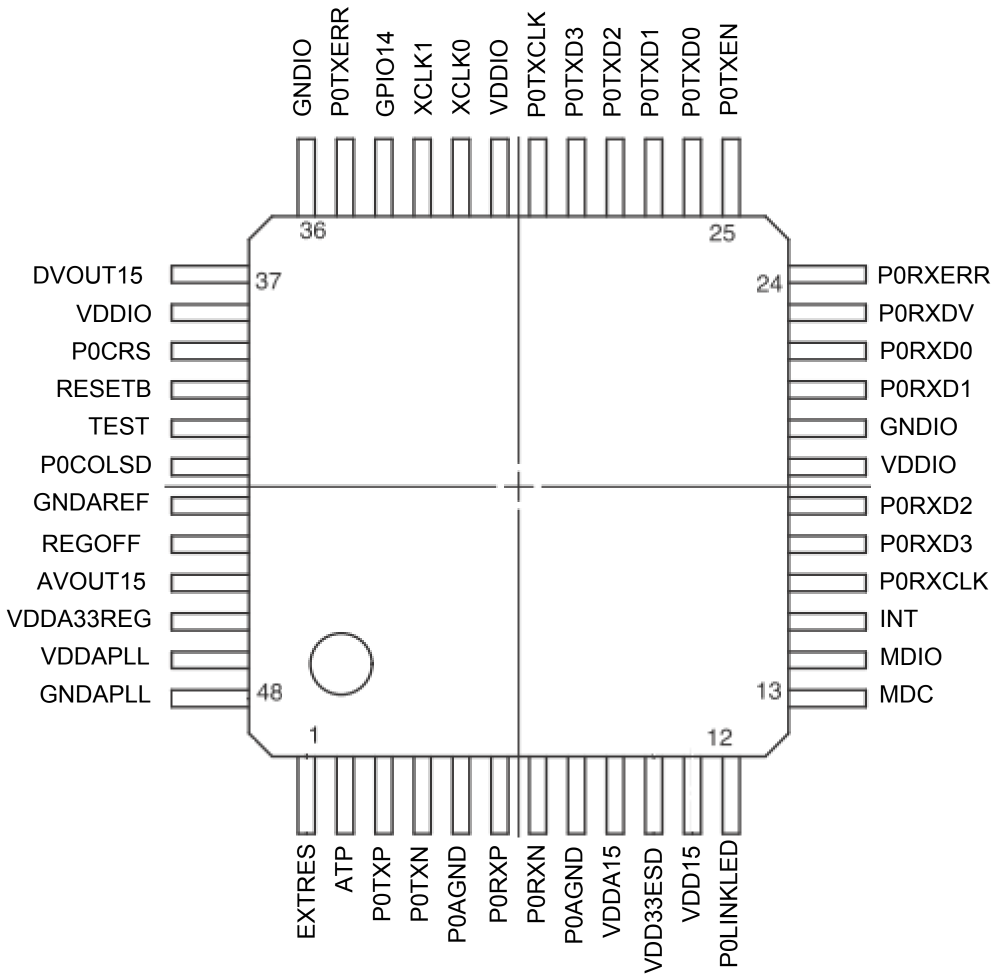
1.3 Applications

- Industrial networking such as Profinet, Ethernet/IP, CIPsync, ModbusTCP, EtherCAT and SercosIII
- 10/100 Mbps LAN on motherboard (LOM) and network interface card (NIC)
- Switches, routers and repeaters with 10/100 Mbps capable ports
- Mobile base stations
- Test and measurement applications
- Home servers, broadband routers, printers, and IP phones
- Telecom base stations
- Real-time networking

Pin Functions

2.1 Pinning Information

2.1.1 Pin Layout



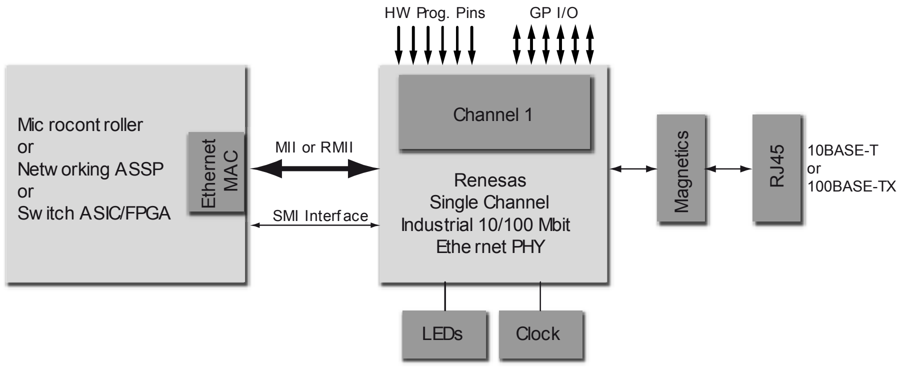
2.1.2 Port Pins

Power Supply	Pins LQFP48	Comment
VDDIO	19, 31, 38	3.3V/2.5V IO power supply
VDD33ESD	10	3,3V input for ESD enhancement
P0AGND	5, 8	Analog GND for PHY
GNDIO	20, 36	GND for I/O
VDD15	11	1.5V Digital VDD
GNDAPLL	48	Analog GND for PLL
VDDA15	9	Analog 1.5V power supply for PHY
VDDAPLL	47	Analog 1.5V power supply for PLL
VDDA33REG	46	3.3V power supply for voltage regulator
DVOUT15	37	Output voltage regulator for digital part
AVOUT15	45	Output voltage regulator for analog part
GNDAREF	43	Analog GND
REGOFF	44	Regulator disable Hi: Regulator Off Lo: Regulator On

Pin Name	I/O	Function	Alternate Function	Pin LQFP48	Comment
EXTRES	I	External Resistor		1	Connect to GND via 12.4kΩ resistor
ATP	I	Production test		2	Pull Down (5kΩ)
P0TXP	O	Media Interface		3	
P0TXN	O			4	
P0RXP	I			6	
P0RXN	I			7	
P0LINKLED	IO	GPIO	GPIO0	12	
MDC	I	MII		13	
MDIO	IO			14	
INT	O	GPIO	GPIO4	15	
P0RXCLK	I	MII	GPIO3	16	
P0RXD3	O	MII	GPIO7	17	
P0RXD2	O		GPIO8	18	
P0RXD1	O			21	
P0RXD0	O			22	
P0RXDV	O			23	
P0RXERR	O			24	
P0TXEN	I			25	
P0TXD0	I			26	
P0TXD1	I			27	
P0TXD2	I		GPIO11	28	
P0TXD3	I		GPIO10	29	
P0TXCLK	O		GPIO5	30	
XCLK0	I	50MHz (RMII Mode)		32	Clock input in external clock mode
XCLK1	O			33	Open in external clock mode
GPIO14	IO	GPIO		34	
P0TXERR	I	MII	GPIO9	35	
P0CRS	O		GPIO6	39	
RESETB	I			40	
TEST				41	Connect to GND
P0COLSD		MII	GPIO19	42	

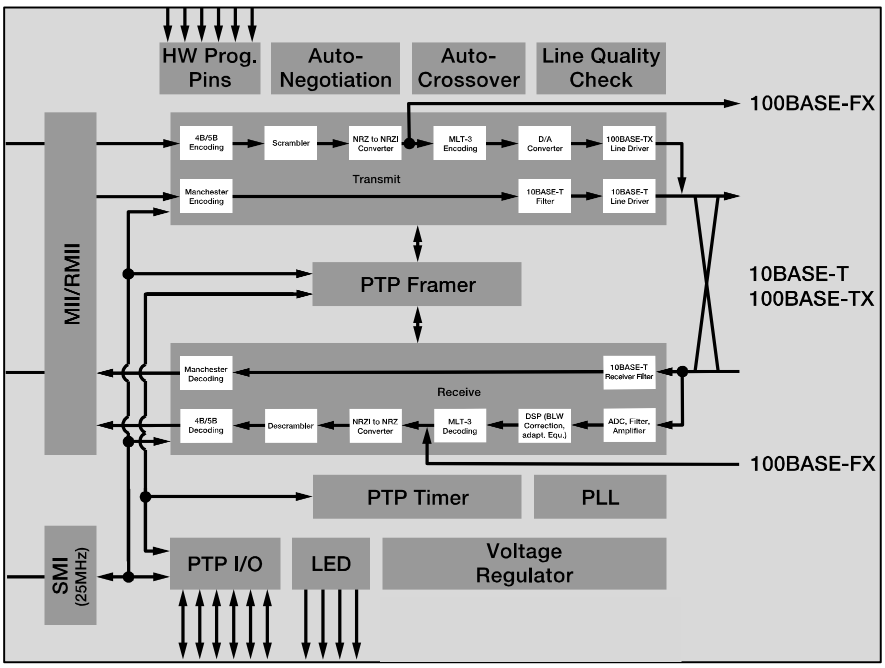
System Diagram

The picture below shows the system diagram. The PHY is connected to the MAC through a MII or RMII interface. On the other side it is connected either to a CAT5 cable through some magnetics or to a fibre cable.



3.1 Device block diagram

The device consists of two PHY's each connected to a PTP Framer block used to de-/encode the PTP frames and timestamp them, a PTP timer block containing the PTP clock and a I/O block for general configuration and I/O handling. The PTP support is only available on the PTP version.

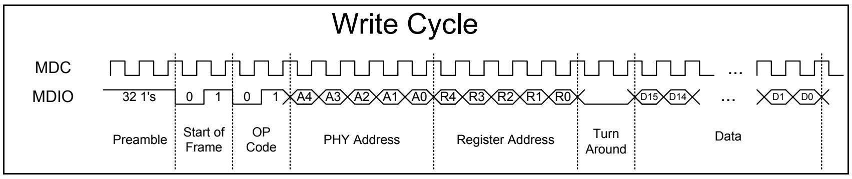


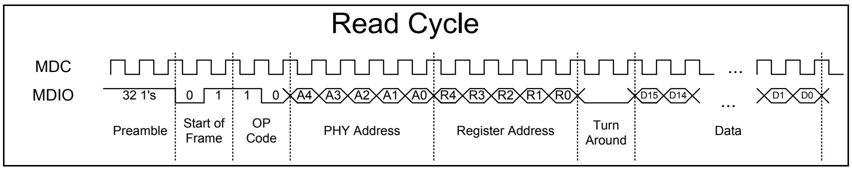
Global Hardware Description

The device consists of an Ethernet PHY with hardware support of IEEE1588. In addition it includes a control block which is used to control shared resources such as LED outputs, interrupts, and low power modes. All are interfaced through a two wire bidirectional Serial Management Interface.

4.1 Register Access

All registers can be accessed through the MII / SMI interface. The SMI is a serial interface defined in IEEE802.3 for access to PHY registers. The following picture shows a typical access using the SMI interface:





The PHY address denotes the address of the PHY, while the register address is the address of the register within the addressed PHY. The device uses the PHY addresses to support access to the PTP block and the Global Configuration registers. The address table is as follows:

PHY Address (Binary)	Ressource	Comments
NM000	PHY0	
NM001	Reserved	
NM010	Reserved	
NM011	Reserved	
NM100	Reserved	
NM101	Reserved	
NM110	PTP	
NM111	GLOBAL_CONFIG PTP	

The values of the bits N and M can be configured as a strap option.

4.2 General SMI Control Register 7.31

The following register is used for configuration of the SMI:

Bit	Name	Description	Mode	Reset
15	SOFTRESET	1: Initiates a software reset of the complete device (stays active until cleared by software) 0: Release Reset	W	0
14	SMI_SHORT _PREAMBLE	1: Enable short preamble support. 0: Short Preamble mode for SMI interface not enabled	RW	0
13	RESET		WC	0
12:4	Reserved	Write as 0	RW	0
3	Reserved	Write as 0	RW	0
2	Reserved	Write as 0	RW	0
1	Reserved	Write as 0	RW	0
0	PHY0_ DISREGARD _ADDRESS	1: PHY 0 ignores the PHY address when the device is being written 0: The PHY checks for the PHY address	RW	0

4.3 Power Control Register 7.30

The following register is used for configuration of the power options:

Bit	**Name**	**Description**	**Mode**	**Reset**
15:14	Reserved		RW	
13:12	Reserved		RW	
11	STOP	1: Device is completely disabled, only access to registers 7.25-7.31 in the GLOBAL_CONFIG area is possible. 0: Device is enabled	RW	0
10	PULSE_ PWD	0: Pulse Output logic is enabled 1: Pulse Output logic for GPIO is powered down	RW	1
9	CAP_PWD	0: Capture logic is enabled 1: Capture logic for GPIO is powered down	RW	1
8	PTP_PWD	0: PTP is enabled 1: PTP is powered down	RW	1
10:1	Reserved		RW	
0	PHY0PWD	1: The analog and digital part of the PHY0 is powered down. 0: PHY0 is enabled	RW	0

4.4 PHY Status Register 7.28

The following register shows the status of the PHYs.

Bit	Name	Description	Mode	Reset
15:10	Reserved	Write as 0	RW	0
9	Reserved	Write as 0	R	0
8	PHY0_LINK	0: PHY 0 has no link 1: PHY 0 has link	R	0
7:2	Reserved	Write as 0	RW	0
1	Reserved	Write as 0	R	0
0	PHY0_ SYSRST	1: PHY is powered up and able to operate, Reset not active 0: PHY is still powering up	R	0

The SYSRST registers are set by the PHY after the PLL has been powered up and has stabilized. They need to be 1 for the device to operate and to get access to all functions. Otherwise the internal 125 MHz clock is not available.

4.5 Strap option Register 7.27

The following register shows the strap option value latched after reset

Bit	Name	Description	Mode	Reset
15	QUICK_AUTONEG	Autonegotiation strap setting	RO	Strap option
14	AUTO_NEG	Quick Autonegotiation strap setting	RO	Strap option
13	AUTO_MDIX	Auto MDIX strap setting	RO	Strap option
12	FAST_JK	Fast JK strap setting	RO	Strap option
11	DUPLEX	Duplex strap setting	RO	Strap option
10	ADDR4	PHY address bit 4 strap setting	RO	Strap option
9	ADDR3	PHY address bit 3 strap setting	RO	Strap option
8	ETHERCAT	MII timing strap setting	RO	Strap option
7	MII	MII/RMII strap setting	RO	Strap option
6:2	Reserved	Reserved	RO	0
1	PHY1 TX	100BASE-TX / 100BASE-FX strap setting for PHY1	RO	Strap option
0	PHY0 TX	100BASE-TX / 100BASE-FX strap setting for PHY0	RO	Strap option

4.6 PHY LED Status Register 7.24

The following register shows the status of the PHYs after power up. To read the LED status for the PHYs first PHY_SELECT must be written with the number of the required PHY and then the data for this PHY can be read from the register. The ACTIVE_LED_BLINK bit can be used to control the LED outputs of the device. If a GPIO is configured for link detection setting this register will cause the GPIO to blink while data transmission is ongoing.

Bit	Name	Description	Mode	Reset
15	Reserved	Write as 0	R	0
14	P0SD	Signal Detect signal is active	R	0
13	PHY_TXACT	1: PHY had TX activity since last reading 0: PHY had no TX activity since last reading Cleared when read	R/LH	0
12	PHY_RXACT	1: PHY had RX activity since last reading 0: PHY had no RX activity since last reading Cleared when read	R/LH	0
11	PHY_FD	1: PHY runs on full duplex 0: PHY runs not on fill duplex	R	0
10	PHY_LINK	1: PHY has LINK 0: PHY has no LINK	R	0
9	PHY_100MB	1: PHY runs on 100 MBit 0: PHY runs not on 100 MBit	R	0
8	PHY_10MB	1: PHY runs on 10 MBit 0: PHY runs not on 10 MBit	R	0
7:4	LED_MODE	Configure LED output (see chapter 4.9)	RW	0
3	ACTIVE_LED_BLINK	1: Link LED blinks if activity is detected and ON if link is up 0: Link LED does not blink on activity When written this is set for the PHY number in PHY_SELECT	RW	0
2:0	PHY_SELECT	Select number of the PHY for which the other bits of this register will be read. 000: Write to PHY0 Others: Reserved	RW	0

4.7 Interrupt Status register 7.20

To have a centralised register to get a summary of all possible interrupt sources an interrupt status register is placed at the top level in addition to the specific interrupt registers. The bits in this register are only set if the corresponding interrupt is enabled in the interrupt source modules.

Bit	Name	Description	Mode	Reset
15	RESERVED		R/LH	0
14	CAP_TS_STORED_INT	uPD60611 only The PTP capture unit stored an event	R	0
13	CAP_MEM_FULL_INT	uPD60611 only PTP capture buffer is full	R	0
12	PTP_PERIOD_INT	uPD60611 only Pulse generator started new period	R	0
11:10	Reserved		R	0
9	TIMESTAMP_RX0_INT	uPD60611 only PHY0 has received a telegram which caused a timestamp to be taken	R	0
8	TIMESTAMP_TX0_INT	uPD60611 only PHY0 has transmitted a telegram which caused a timestamp to be taken	R	0
7:4	Reserved		R	0
3	PHY0_LINK_DOWN_INT	PHY0 has triggered a Link Down Interrupt	R	0
2	PHY0_BER_OVER_INT	PHY0 has triggered a BER Interrupt	R	0
1	PHY0_FEQ_INT	PHY0 has triggered a FEQ interrupt	R	0
0	PHY0_GENERAL_INT	PHY0 has triggered one of its internal interrupts except for Link Down, BER and FEQ interrupts	R	0

4.8 Interrupt Mask register 7.21

To have a centralised register to get a summary of all possible interrupt sources an interrupt mask register is placed at the top level in addition to the specific interrupt registers. Note that this is just an additional option to mask all interrupts at a central register, all Interrupts need to be enabled at their respective location within the PHY or PTP register set. Therefore the mask register is be default enabled while the interrupt sources are by default disabled.

Bit	Name	Description	Mode	Reset
15	Reserved		RW	0
14	CAP_TS_STORED_INT_MASK	uPD60611 only 0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
13	CAP_MEM_FULL_INT_MASK	uPD60611 only 0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
12	PTP_PERIOD_INT_MASK	uPD60611 only 0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
11:10	Reserved			
9	TIMESTAMP_RX0_INT_MASK	uPD60611 only 0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
8	TIMESTAMP_TX0_INT_MASK	uPD60611 only 0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
7:4	Reserved		RW	0
3	PHY0_LINK_DOWN_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
2	PHY0_BER_OVER_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
1	PHY0_FEQ_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
0	PHY0_GENERAL_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0

4.9 GPIO

The GPIO pins are highly configurable to adjust the device to the requirements of the application. So for example if RMII is used the freed pins can be used for additional PTP, debugging or LED signals. The GPIO registers are located in the GLOBAL_CONFIG address range.

Each GPIO pin has a 4 bit configuration register assigned. The register configuration is only used if the pin is not used for Ethernet handling. So for example if MII is used many pins are used for MII. In this case the GPIO configuration register is an input.

Most GPIO can be assigned to one of four LED signals.

4.9.1 GPIO_CONFIG_0 Register 7.0

Bit	Pin	Description	Mode	Reset
15:12	GPIO3	Same as GPIO0 except: 0111: Clock signal with 1ms 1000: Clock signal with 0.1ms 1001: Reserved 1010: RXCLK	RW	1111 RXCLK
11:8	Reserved	Write as 0.	RW	1000
7:4	Reserved	Write as 0.	RW	1010
3:0	GPIO0	0000: No change when written 0001: GPIO is Output for PPS (Pulse per second) uPD60611 only 0010: Fixed 0. 0011: GPIO is Output for PTP-OUT1 (Output of Pulse Out unit 1) uPD60611 only 0100: GPIO is Output for PTP-OUT2 (Output of Pulse Out unit 2) uPD60611 only 0101: GPIO is Output for PTP-OUT0 (Output of Pulse Out unit 0) uPD60611 only uPD60611 only 0110: GPIO is Output for PTP packet received on PHY 0. If PTP is disabled on this PHY the start of any telegram will activate the pin. uPD60611 only 0111: GPIO is Output for LED0 1000: GPIO is Output for LED1 1001: GPIO is Output for LED2 1010: GPIO is Output for LED3 1011: GPIO is Output for Start of a Frame on TX uPD60611 only 1100: GPIO is Output for Start of Frame on RX uPD60611 only 1101: GPIO is Output for INT	RW	0111 LED0

		1110: GPIO is Output for CHIP_SYNC uPD60611 only 1111: GPIO is Input		

4.9.2 GPIO_CONFIG_1 Register 7.1

Bit	Name	Description	Mode	Reset
15:12	GPIO7	MII mode: always P0RXD3, regardless of setting. RMII mode: Same as GPIO0 except 0111: always 0 1000: always 1 1001: Reserved 1010: Reserved	RW	1111 Input
11:8	GPIO6	Same as GPIO0 except 0110: P0CRS in MII mode PLLREADY in RMII mode Indicates that PLL is operating 0111: Clock signal with 1ms 1000: Clock signal with 1µs 1001: Reserved 1010: Reserved	RW	MII: 0110 P0CRS RMII: 0110 PLLREADY
7:4	GPIO5	Same as GPIO0 except 0111: Reserved 1000: Reserved 1001: Reserved 1010: TXCLK (25 Mhz)	RW	1010 (RMII) 1111(MII)
3:0	GPIO4	Same as GPIO0	RW	1101 Interrupt

4.9.3 GPIO_CONFIG_2 Register 7.2

Bit	Name	Description	Mode	Reset
15:12	GPIO11	MII mode: P0TXD2 RMII mode: Same as GPIO0	RW	1111
11:8	GPIO10	MII mode: P0TXD3 RMII mode: Same as GPIO0	RW	1111
7:4	GPIO9	Same as GPIO0.	RW	0110(MII) 1000(RMII)
3:0	GPIO8	MII mode: always P0RXD2, regardless of setting. RMII mode: Same as GPIO0 except 0111: always 0 1000: always 1 1001: Reserved 1010: Reserved	RW	1111

4.9.4 GPIO_CONFIG_3 Register 7.3

Bit	Name	Description	Mode	Reset
15:12	Reserved	Write as 0.		
11:8	GPIO14	Same as GPIO0 except 0110: PLLReady (PLL operating and locked)	RW	0110: PLLREADY
7:4	Reserved	Write as 0.	RW	1111
3:0	Reserved	Write as 0.	RW	1111

4.9.5 GPIO_CONFIG_4 Register 7.4

Bit	Name	Description	Mode	Reset
15:12	GPIO19	FXMode: Input for SD signal MII mode: COL signal Else same as GPIO0	RW	0110 P0COL
11:8	Reserved	Write as 0.	RW	1111
7:4	Reserved	Write as 0.	RW	1111
3:0	Reserved	Write as 0.	RW	1111

4.10 LED configuration

The device offers a very flexible configuration for the LED outputs. Most of the GPIO can be assigned to one of four LED sources which may be driven by one of the signals in the following table:

Name	Description
LinkA_LED	Link By setting bit ACTIVE_LED_BLINK in the LED_STATUS register this can be used to light when a link is established and to blink when there is activity on the line
FD_LED	This LED is turned on whenever the device is configured for Full Duplex in fix mode or after the Autonegotiation process is finished and has resolved into FD mode.
HD_LED	Link is established in Half Duplex mode. This LED is turned on after a link is actually established in HD mode. It is not turned on when the device is configured in HD fix mode.
100BT_LED	Link is established in 100 BT mode
10BT_LED	Link is established in 10 BT mode
ACT_LED	LED blinks when there is activity
MUX_100BT/10BT	Pin is shared for two LED signaling 100BT and 10 BT speed. Active Low refers to 100BT.
MUX_LINKA/FD	Pin is shared for two LED signaling Link/Activity and Full Duplex mode. Active Low refers to LINKA.
MUX_LINKA/HD	Pin is shared for two LED signaling Link/Activity and Half Duplex mode. Active Low refers to LINKA.
MUX_LINKA/ 100BT	Pin is shared for two LED signaling Link/Activity and 100BT mode. Active Low refers to LINKA.
MUX_LINKA/ 10BT	Pin is shared for two LED signaling Link/Activity and 10BT mode. Active Low refers to LINKA.
SD	Signal Detect. Only used in FX mode

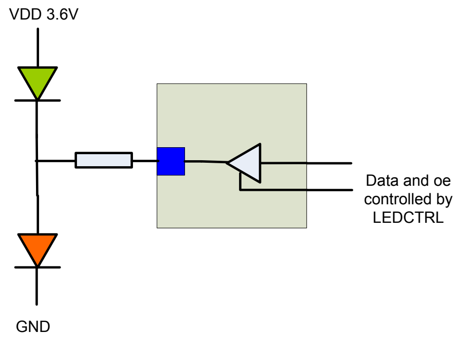
The setting in the LEDMODE register 24.7:4 configures the drivers for LED0…LED3

Mode	LED output	Data input	Comment
0	LED0	LinkA	Link with activity blink option depending on setting of ACTIVE_LED_BLINK register
	LED1	FD	
	LED2	MUX 100BT / 10BT	Active Low refers to 100BT
	LED3	Activity	
0001	LED0	MUX LinkA / FD	Mux frequency >> blink frequency
	LED1	SD	
	LED2	MUX 100BT / 10BT	Active Low refers to 100BT
	LED3	Activity	
0010	LED0	MUX LinkA / HD	Mux frequency >> blink frequency
	LED1	SD	
	LED2	MUX 100BT / 10BT	Active Low refers to 100BT
	LED3	Activity	
0011	LED0	Mux LinkA / 100BT	Mux frequency >> blink frequency
	LED1	MUX 100BT / FD	Active Low refers to 100BT
	LED2	MUX ActTX / ActRX	Activity from PHY (128ms)
	LED3	SD	
0100	LED0	Mux LinkA / 10 BT	Mux frequency >> blink frequency. Active Low refers to 100BT
	LED1	FD	
	LED2	SD	
	LED3	HD	
0101	LED0	MUX LinkA / SD	Active Low refers to LinkA
	LED1	MUX 100BT / 10 BT	Active Low refers to 100BT
	LED2	Activity	
	LED3	MUX FD/HD	Active Low refers to FD
0110	LED0	MUX LinkA / FD	Active Low refers to LinkA
	LED1	SD	
	LED2	MUX 100BT / 10 BT	Active Low refers to 100BT
	LED3	Activity	
0111	LED0	Mux LinkA / HD	Mux frequency >> blink frequency. Active Low refers to LinkA
	LED1	Activity	
	LED2	10BT	
	LED3	Mux 100BT / HD	Active Low refers to 100BT
1000	LED0	LinkA	

	LED1	HD	
	LED2	MUX 100BT / 10BT	Active Low refers to 100BT
	LED3	Activity	
1001	LED0	MUX LinkA / 100BT	Active Low refers to LinkA
	LED1	SD	
	LED2	100BT	
	LED3	FD	
1010	LED0	LinkA	
	LED1	MUX SD/Activity	Active Low refers to SD
	LED2	MUX FD/HD	Active Low refers to FD
	LED3	MUX 100BT/10BT	Active Low refers to 100BT
1011	LED0	LINKA	
	LED1	MUX FD/HD	
	LED2	MUX 100BT/10BT	Active Low refers to 100BT
	LED3	Activity	
1100-1111	LED0	Reserved	
	LED1	Reserved	
	LED2	Reserved	
	LED3	Reserved	

4.11 LED-Mux

To connect two LED to single pin a special logic is integrated which allows to control two LED on a single pin. A schematic of this logic is shown below:



Normally the input pin of the device is tri-stated so both LED are off. By pulling the pin to either VDD or GND one of the two LED can be turned on. In case both LED need to be turned the pin will toggle in a high frequency so both LED are on, although they may be a little darker. This mode is called MUX… in the previous chapter-

4.12 Strap Options

The device offers several configurations which can be selected as strap options. The related I/Os have resistors of approx 40 kΩ as pull-up or pull-down integrated which configure the device as described below. To change this configuration an external resistor of maximum 5 kΩ must be connected to this pin. An external resistor supporting the internal resistor is also advisable in case the device is used in a very noisy environment.

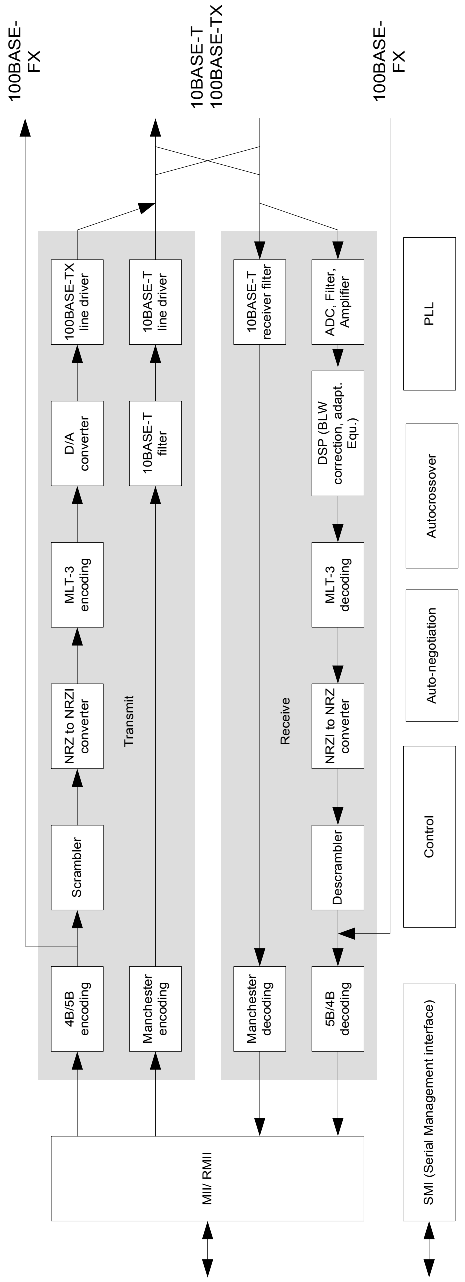
The following table shows the possible configuration options and the related pins. Unless otherwise noted all configuration options apply to both PHYs.

Pin Name	Function	Default value
P0RXD3	0: Autoneg disabled, 100BaseT 1: Autoneg enabled, 100BaseT	1, PU
P0RXD2	If Autoneg disabled: 0: Half Duplex 1: Full Duplex If Autoneg enabled: 0: Parallel detect ends in half duplex mode 1: Forced Full Duplex in parallel detect	1, PU
P0RXCLK	0: Disable Quick Autonegotiation If Autoneg enabled: 1: Quick Autonegotiation, shortest times If Autoneg disabled 1: Special Isolate. In this mode the PHYs will not set up a link unless programmed and enabled through the SMI.	1, PU
P0RXERR	0: Configure RMII Interface 1: Configure MII Interface	1, PU
P0TXCLK	0: Standard Mode, “JK” required for Start of Frame detection 1: Fast Mode, Only “J” required for Start of Frame detection. Do not use in RMII Mode.	1, PU
P0CRS	0: AUTOMDI-X disabled. 1: AUTOMDI-X enabled	1, PU
P0RXDV	0: FX Mode for PHY0, in this case the values of Autoneg, Duplex, Quick Autoneg are ignored for this PHY. 1: TX Mode for PHY0	1, PU
P0RXD0 / P0RXD1	Configures the upper two bits N and M of the PHY addresses 00: device uses address 00xxx for SMI 01: device uses address 01xxx for SMI 10: device uses address 10xxx for SMI 11: device uses address 11xxx for SMI	00, PD

PHY

5.1 General Description

The block diagram for each is shown below:



5.2 Clock Generator PLL

The PLL is a 125 MHz PLL which generates the clock for the 125 MHz part. It generates 32 output phases. The DSP selects which of these phases is used to sample the incoming signal. A single PLL is used for both PHYs. Therefore a Power Down of a PHY will only power down the PLL if both PHYs are powered down.

5.3 Analogue Frontend

The analogue frontend consists of two Programmable Gain Amplifiers, a low pass filter and the ADC.

5.3.1 Adaptive Equalizing

The adaptive equalizer compensates for phase and amplitude distortion caused by the Physical channel consisting of magnetics, connectors, and CAT-5 cable. The equalizer can restore the signal for any good quality CAT-5 cable.

5.3.2 100Base TX Receiver ADC

The Receiver ADC is part of the analog block. It is clocked with a 125 MHz clock which can be selected by the DSP from one of 32 phases shift.

5.4 Digital Signal Handling

The following chapters describe how the signal is handled in the digital part of the PHY.

5.4.1 DSP

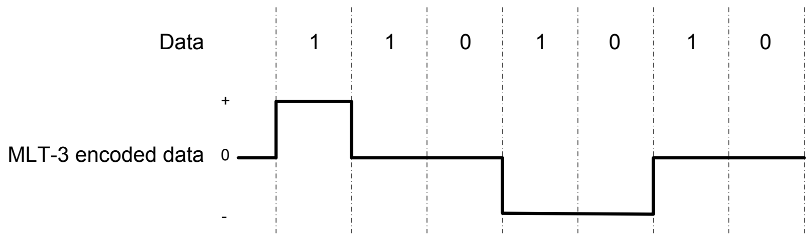
The DSP is re-shaping the received signal so it can be further processed. The ADC is sampling the signal at an interval of 125 Mhz which is the sampling frequency of the signal. However the frequency of the signal is significantly lower than that due to the MLT-3 coding. Based on the received and decoded signal the DSP can measure the quality of the signal and either adjust its internal filters or adjust the sampling phase of the ADC. One of the internal filters can be read and observed to observe the cable quality.

5.4.2 Baseline Wander Correction

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the drop characteristics of the transformer will become significant and baseline wander (BLW) on the received signal will result. To prevent corruption of the received data, the DSP corrects for baseline wander.

5.4.3 NRZI/MLT-3 Encoding / Decoding

MLT3 is a specific version of a NRZI coding using a trilevel code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”. Basically it uses the NRZI coding as input but the ‘1’ is flipped to ‘-1’ every second time. The main advantage is that it reduces the effective frequency on the cable to 1/4 or 125/8 MHz. The decoder converts the MLT-3 data coming from the DSP to a NRZ data stream. The conversion of data to NRZI/ MLT-3 encoded data is shown in the following picture.



This code is used on the Ethernet data lines in 100TX mode.

5.4.4 Scrambler / Descrambler

To reduce EMI the data sent is scrambled before it goes on the line and descrambled in the receiver. This reduces the emission of specific frequencies and spreads the emissions on a wider frequency band.

Scrambling the data helps eliminate large narrow-band peaks for repeated data patterns, and spreads the signal power more uniformly over the entire channel bandwidth. The seed for the scrambler is generated from the PHY address, ensuring that in multiple-PHY applications each PHY will have its own scrambler sequence.

The descrambler descrambles the decoded NRZ ciphertext bit from the MLT-3 decoder. The ciphertext bit stream is decoded by addition (modulo 2) of a key stream to produce a plaintext bit stream.

During reception of IDLE symbols, the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

5.4.5 5B/4B Encoding / Decoding

The data on the line is coded 4B/5B and decoded on the receive path. The main purpose is to remove repeated values, i. e. 0000 is replaced by 11110 to ensure there is a signal change after a certain period. In addition it allows to find faulty transmissions and add some control data.

The following table shows the relationship between payload data and the 5B Interpretation.

PCS code-group [4:0]	Name	MII (TXD/RXD) [3:0]	Interpretation
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 0 1 1	5	0 1 0 1	Data 5
0 1 1 1 0	6	0 1 1 0	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data A
1 0 1 1 1	B	1 0 1 1	Data B
1 1 0 1 0	C	1 1 0 0	Data C
1 1 0 1 1	D	1 1 0 1	Data D
1 1 1 0 0	E	1 1 1 0	Data E
1 1 1 0 1	F	1 1 1 1	Data F
1 1 1 1 1	I	Undefined	IDLE; Used as inter-stream fill code
1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; Always used in pairs with K
1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; Always used in pairs with J
0 1 1 0 1	T	Undefined	End-of-Stream Delimiter, Part 1 of 2; Always used in pairs with R
0 0 1 1 1	R	Undefined	End-of-Stream Delimiter, Part 2 of 2; Always used in pairs with T
0 0 1 0 0	H	Undefined	Transmit Error; Used to force signaling errors
0 0 0 0 0	V	Undefined	Invalid code
0 0 0 0 1	V	Undefined	Invalid code
0 0 0 1 0	V	Undefined	Invalid code
0 0 0 1 1	V	Undefined	Invalid code
0 0 1 0 1	V	Undefined	Invalid code
0 0 1 1 0	V	Undefined	Invalid code
0 1 0 0 0	V	Undefined	Invalid code
0 1 1 0 0	V	Undefined	Invalid code
1 0 0 0 0	V	Undefined	Invalid code
1 1 0 0 1	V	Undefined	Invalid code

5.5 Functional Description

5.5.1 Collision detection

When transmissions from two stations overlap, the resulting contention is called a collision. Collisions occur only in half duplex mode, where a collision indicates that there is more than one station attempting to use the shared Physical medium.

5.5.2 Carrier Sense detection

Carrier Sense (CRS) is asserted by the core when either transmit or receive medium is non-idle. For the half duplex mode, Carrier sense is asserted during transmission or reception. For Full duplex mode, Carrier sense is asserted during reception.

5.5.3 Auto Crossover (MDI/MDI-X)

The core automatically detects and corrects for the MDI/MDI-X crossover in the TX modes. Auto-Crossover is disabled in FX Mode. If this function is disabled, crossover may be corrected manually through the Serial management interface. The status of the crossover function can be read in the status register. The detection process is started whenever the PHY is turned on and Auto Crossover is activated. As soon as the partner PHY is transmitting it will immediately do the adjustment.

5.5.3.1 Auto-Crossover when using 100BT Fix Mode

In 100BT manual mode the transmitter transmits continuously idles on the TX line. As the incoming echo from the transmitter path needs to be blocked there is no chance to listen on that line. Therefore a special non standard implementation is done called 100BT idle burst mode. The idle burst mode has two states, a period of idle burst and a period of random silence mode to detect incoming signals on the TX line. The time for the next transmission will be picked randomly. The decision to do a switchover will be done based on the reception of two signals within a specific time period.

The PHY will transmit bursts of 1 µs after a waiting time of 0 - 63 µs. In parallel it checks on both lines if a signal can be received. If a valid signal is received on the RX line, it will continue normal operation. If a valid signal is received on the TX line it will wait for 500µs and then revert the setting (exchange TX and RX). Again after a time of 0 - 63µs it will send a burst of 1 us and in parallel check if there is a signal on one of the lines. This will continue until a valid signal is detected on the RX line.

The PHY will only do a crossover if it detects signals on the actual TX line. On an open line it will not exchange the RX/TX lines as it cannot receive any signals.

The duration of this process can be between <1 µs if the signal is initially recognized correctly and approx. 565µs if the crossover has to be done.

5.5.3.2 Auto-Crossover when using Autoneg or 10BT Mode

Since the auto-negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link, the energy detection upon FLPs bursts is the same as the NLPs. The NLP is a pulse transmitted every 16±8 ms. and its pulse width is 100ns. Typical burst width is 2 ms.

After reset the PHY will check for the a signal on the incoming lines. As it is in its "Break_link_timer" state it will not start transmission before this timer is expired. If there is a signal detected in that period it will adjust the MDI/X accordingly and continue. If no signal is detected it will start transmitting the FL-Pulses to establish a connection. As the switchover is in general done during the duration of the Break_link_timer there is no additional time required for Auto-Crossover in Autoneg Mode.

5.5.3.3 Auto-Crossover when connecting Autoneg and 100BT Mode

This is a situation, in which one link partner A is in auto-negotiation mode and the other partner F is set to 100 Mb/s fix mode.

After power-up the forced PHY F will start sending FLP while the other link partner A is in Transmit disable state. So while PHY A will wait for its ***break_link_timer*** time (1200ms-1500ms) the forced PHY F will turn itself off randomly for every time period of ***sample timer*** (62±2us) to listen for a signal on its TX line. It will not change its transmit line pair though unless it detects a contention. PHY A adjusts its Autocrossover state as it received a signal during its break_link_timer expiration time. When PHY A moves to ABILITY_DETECT mode and transmits FLP PHY F detects these pulses. As PHY A has already adjusted its autocrossover mechanism correctly there is no need for PHY F to do so.

5.5.4 Auto-Polarity

The core automatically detects and corrects for polarity reversal in wiring in 10BASE-T mode. The result of polarity detection is indicated by the flag "XPOL", bit 4 in register 27. Polarity is checked at end of packets in 10BASE-T.

5.5.5 Auto-Negotiation

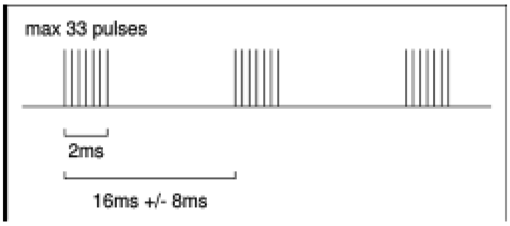
The objective of the auto-negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. Auto-negotiation protocol is a purely Physical layer activity and proceeds independently of the MAC controller.

Prior to the start of any kind of negotiation the PHY is required by the IEEE 802.3 Chapter 28 to wait the Break_Link_Timer time which is defined to be between 1200 ms and 1500 ms. This time is defined to make sure both PHYs are reset and reach a defined status prior to starting the negotiation process.

For the auto-negotiation function the two PHY communicate by sending FLP (Fast link Pulse) bursts for exchanging information with its link partner. A FLP burst consists of 33 pulse positions. The 17 odd-numbered pulse positions contain a link pulse and represent clock information. The 16 even-numbered pulse positions represent data information. The data transmitted by an FLP burst is known as a "Link Code Word". These are fully defined in clause 28 of the IEEE 802.3 specification.

After the Break Link Timer has expired, the link down status is achieved and if auto-negotiation is enabled the PHY starts to send FLP bursts while trying to receive signals on its receive path. If it detects signals according to 10BaseT, 100BaseTX or 100BaseT standard it will wait for FLP bursts and check the received signals until the autoneg_wait_timer period of typically 500ms has expired and then switch to fix mode according to the received signal.

The following picture shows the FLP burst.



These 33 pulses contain an acknowledge bit which is cleared at the start of the sequence. Each partner starts to send FLP bursts and tries to receive them from the other with the acknowledge bit cleared.

After one partner has successfully received three identical FLP bursts it continues sending FLP bursts with the acknowledge bit set. The other partner will wait until it has received this answer for three times. After that both partners will send 6-8 FLP bursts with the acknowledge bit set to ensure that they have understood each other successfully. After that both PHYs will resolve the information and decide on the optimum configuration.

Therefore it is required that at least 9 FLP bursts are sent to initiate a successful auto-negotiation. Thus a successful auto-negotiation will last at least 72 ms up to 216 ms depending on the burst length, if all transmissions are successful and the next page function is not used. In case a pulse is distorted the process will start over again.

To improve the linkup time for two Renesas PHYs the nominal 16ms frame rate is reduced to allowed 8 ms and shortening the frame transmission time. In this case two Renesas PHYs are able to negotiate within 72 ms without hurting the IEEE spec.

This core supports auto-negotiation and implements the “Base page”, defined by IEEE 802.3. It also supports the optional “Next page” function to get the remote fault number code.

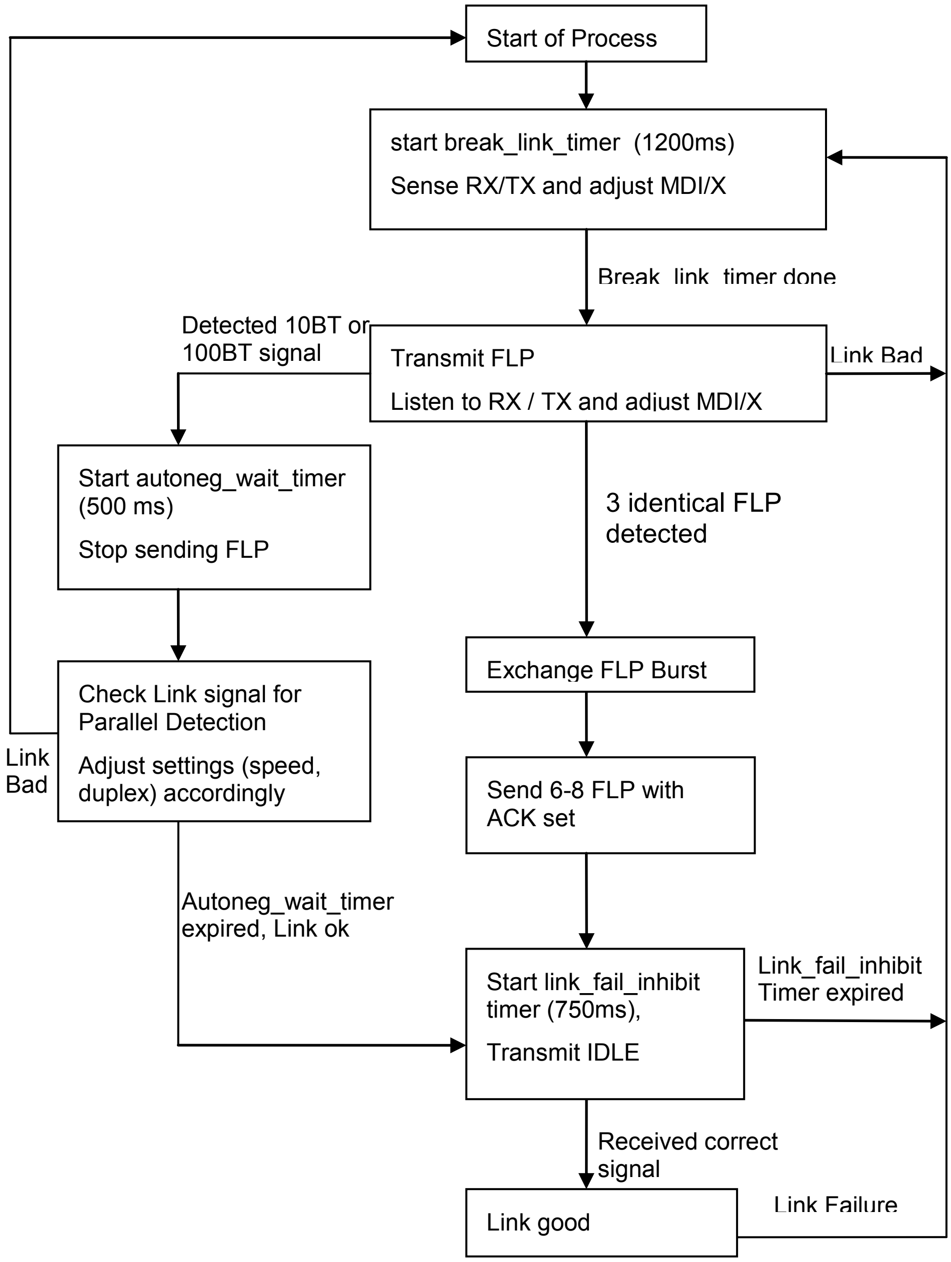
5.5.5.1 Improved Link-Up time (Quick Autonegotiation)

In many applications a link up time of approx. 2 seconds as required by IEEE 802.3 is too long. To reduce the link up time the values of the BREAK_LINK_TIMER and the AUTONEG_WAIT_TIMER which are the main contributors to the long link up time can be configured to shorter values. Thus the initial Link-Up procedure can be significantly shortened. Note that this process is only shortened if both PHYs are capable of using the shortened times. If one PHY is not able to do this the normal link up times can be expected.

The BREAK_LINK_TIMER is required to assure that the partner PHY is definitely entering Link Down mode by disabling the transmission for the timer runlength. However most PHY detect a missing link within a couple of µs and are targeting <15µs for industrial protocols so a timer length of >1250ms is not required in most cases. So depending on the partner PHY the link up time can be reduced down to 80ms.

The AUTONEG_WAIT_TIMER is used if the auto-negotiation state machine detects link signals when waiting for the FLP from the other PHY. In this case it is assumed that the other PHY is running on either 10 MBit or 100 MBit fix mode. The PHY will then wait for the duration of the AUTONEG_WAIT_TIMER to check if there are FLP or some other signals coming. After the AUTONEG_WAIT_TIMER has expired and there were no other signals the link is established. Otherwise the process is restarted. As the AUTONEG_WAIT_TIMER in this case slows down the Link Up process its value can also be configured.

The following picture gives a very simplified overview on the auto-negotiation process with the related timers:



The general behaviour can be configured with the external strap pins. This can be used to use either the standard timing or the reduced timing with a Break_Link_Timer of 80ms and an Autoneg_wait_timer of 35ms.

The following table shows the values in ms that can be configured by the strap option:

Quick Autoneg Strap Option	**Break_Link_Timer**	**Autoneg_wait_timer**
Enabled	80	35
Disabled	1250	850

5.5.5.2 Disabling Auto-Negotiation

Auto-negotiation can be disabled by register setting or by setting the appropriate strap pins. When auto-negotiation is disabled, the speed and duplex modes are decided by setting management interface registers or Parallel Detection.

5.5.5.3 Priority Resolution

There are four possible matches of the technology abilities. In the order of priority these are:

100M full duplex (highest priority)

100M half duplex

10M full duplex

10M half duplex

Since two devices (local device and remote device) may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. Full duplex solutions are always higher in priority than their half duplex counterparts.

10BASE-T is the lowest common denominator and therefore has the lowest priority. If a link is formed via parallel detection, then bit 0 in Register PHY.6 is cleared to indicate that the link partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, bit 4 of register PHY.6 is set. Register PHY.5 is used to store the link partner ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then register PHY.5 is updated after completion of parallel detection to reflect the speed capability of the link partner.

5.5.5.4 Next Page Function

Additional information, exceeding that required by base page exchange, is also sent via “next pages”. This core supports the optional “next page” function.

Next page exchange occurs after the base page has been exchanged. Next page exchange consists of using the normal auto-negotiation arbitration process to send next page messages. Two message encodings are defined: Message pages, which contain predefined 11 bit codes, and unformatted pages.

Next page transmission ends when both ends of a link segment set their next page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its next page information, it shall transmit message pages with null message codes and the NP bit set to logic zero while its link partner continues to transmit valid next pages. Auto negotiation capable devices shall recognize reception of message pages with null message codes as the end of its link partner’s next page information.

The default value of the next page support is disable (bit 15 of register 4). To enable next page support, bit 15 of Register 4 should be set to “1”. Auto-negotiation should be restarted, and the message code should be written to bit [10:0] of register 7.

5.5.5.5 Re-negotiation

When auto-negotiation is enabled, it is re-started by one of the following events

1. Link status is down.
2. Setting Auto-Negotiation Restart bit to high.

Auto-negotiation is started (not re-started) when 1) H/W reset, 2) S/W reset or 3) setting Auto-Negotiation Enable from low to high.

5.5.5.6 Parallel Detection

The parallel detection function allows detection of link partners that support 100BASE-TX and/or 10BASE-T, but do not support auto-negotiation or are set to fix mode. The core is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Link Pulses. If the core detects either mode, it automatically reverts to the corresponding operating mode.

In this case the link is always half duplex as defined in the IEEE spec. If a link is formed via parallel detection, then reg 6.0 is cleared to indicate that the link partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, reg 6.4 is set. reg 5 is used to store the link partner ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then reg 5 is updated after completion of parallel detection to reflect the speed capability of the link partner.

Similar to the auto-negotiation process the PHY waits for the Break_Link_Timer duration before starting parallel detection. After reception of the first link signals the parallel detection process waits for another 500 ms to check if FLP bursts are received.

5.5.5.7 Parallel Detection -> Speculative Full Duplex

In modern Ethernet systems it is not very likely that a 100 MBit fix mode PHY is actually using half duplex. However if the IEEE 802.3 is fulfilled the PHY doing auto-negotiation will revert to half duplex operation following the parallel detect operation. Thus the result of the parallel detect mode may be one Fix-mode configured PHY running at 100 MBit full duplex and the other Autonegotiation configured PHY running at 100 MBit half duplex. Although communication is possible this will lead to a very high number of errors as the half duplex configured PHY will continuously detect collisions and interrupt its transmission when the full duplex PHY is transmitting and receiving simultaneously.

To avoid this situation the PHY can be configured to go into full duplex instead of half duplex in parallel detection mode by means of a strap option.

5.5.6 Bad Line recognition

The PHY features a number of functions to control and observe the line to be able to ensure a reliable connection.

5.5.6.1 BER-Monitor

The PHY can continuously measure the bit error rate (BER) on the line and trigger an interrupt or put the link down, if a configurable threshold is reached.

Bit errors are detected by checking the received symbols against the list of allowed symbols. There are two basic conditions for this check:

1. IDLE situation: When the PHY is in idle mode it should only receive IDLE symbols or the start of frame delimiter which is a J symbol. All other symbols are indicating that a bit error has happened and are counted as error.

2. Data transmission: During data transmission there are 32 possible symbols of which only 19 are valid symbols. The rest indicate a bit error and will be counted as such. Note that the /H/ symbol is also counted as an error symbol.

A pre-condition of the BER mechanism operation is the lock of the descrambler, it will try to adjust itself while receiving IDLE patterns and is considered locked if a reasonable number of IDLE patterns have been received and descrambled. Unless the descrambler is locked, the BER monitor is not operable, and no data can be received.

5.5.6.2 Register PHY.23 – BER Counter Control Register

Bit	Name	Description	Mode	Default
23:15	BER_LNK_OK	Link quality indication – indicates state of link monitor. '0' – Not in 'Good Link' state '1' – In 'Good Link' state Will go up as soon as the counter is below the trigger level after start up. Can be used to detect reliably link up after start up.	R	0
23:14	BER_CNT_LNK_EN	1: A trigger on the BER or on the FEQ monitor will cause a link down. 0: A trigger on the BER/FEQ will just cause the state machine to leave “Good Link” state.	RW	1
23.13:11	BER_CNT_TRIG	Trigger level for BER Count to define link up/down Counter in 2^(n -1) errors 0: >0 errors will trigger 1: >1 triggers 2: >2 triggers 3: >4 triggers 4: >8 triggers 5: > 16 triggers 6: >32 triggers 7: > 64 errors triggers	RW	2
23.10:7	BER_WINDOW	Length of time for BER counter in 0.005 * 2^n ms 0: BER counter functions disabled 1: 0.01 ms 2: 0.02 ms 3: 0.04 ms … 14: 81,92 ms 15: unlimited run window. Writing a 0 resets the BER counter and restarts the time window.	RW	1 (0.01 ms)
23:6:0	BER_COUNT	Counter for bit errors, shows the amount of errors in the past time window. Is updated every 100 µs if BER_WINDOW = 15	R	0x0

Example setting:

Typically the BER on a line should be in the range of 10exp-11. A significant increase of this number is an indication of a bad connection caused by some issue with the cable, connectors or partner PHY.

Thus a typical setting could be as follows:

BER_CNT_LNK_EN = 1	Enable Link Down in case of exhaustive bit errors
BER_CNT_TRIG = 2	This setting will set the maximum allowed amount of bit errors. A smaller value may lead to link downs in case of single errors which may happen even on a good line. BER_WINDOW = 14 This will give the maximum time window. In combination with a BER_CNT_TRIG of 2, three bit errors in this time window will put the link down. After every 81.92ms the counter is reset, so single bit errors are deleted. As the logic will put the link down as soon as three bit errors are detected, this has no bad influence on the detection time for a line failure.

So in this case the value for the BER_COUNTER_CONTROL register is 0x4700. This can be done at any time. In addition Interrupt 10 in the Interrupt Mask register should be enabled to notify the CPU of such an event.

5.5.6.3 FEQ-Monitor

In order to optimize the reception of the incoming data, the DSP continuously adapts its filters to the incoming signal. To be able to monitor the line quality one of the DSP filter coefficients can be monitored and an interrupt or link down can be triggered, if programmable limits are exceeded.

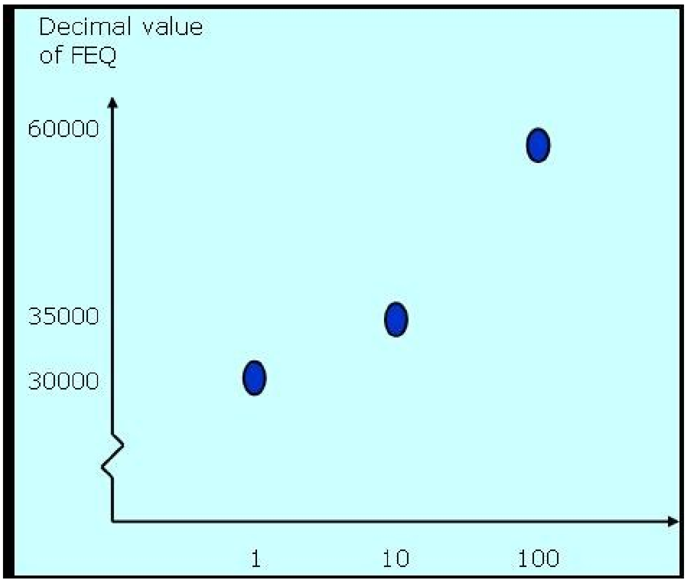
The FEQ2 coefficient changes as the DSP tries to readapt to match a changed line characteristic caused for example by a line break or increased resistance due to corrosion. This change is done within 1 to 9µs when the line condition changes depending on line length and cable quality. So by using the FEQ monitor line changes can be safely detected within 9 µs.

The FEQ2 value is latched at link up time. By programming the FEQ2_DELTA field in register 24 the allowed deviation of this value can be set. Whenever the FEQ2 is outside of this border due to changes in line condition an interrupt or link down is initiated. Note that after a link down the FEQ2 value is relatched so then a link is established based on the then actual FEQ2 value. In this case the application needs to take control and decide how to continue.

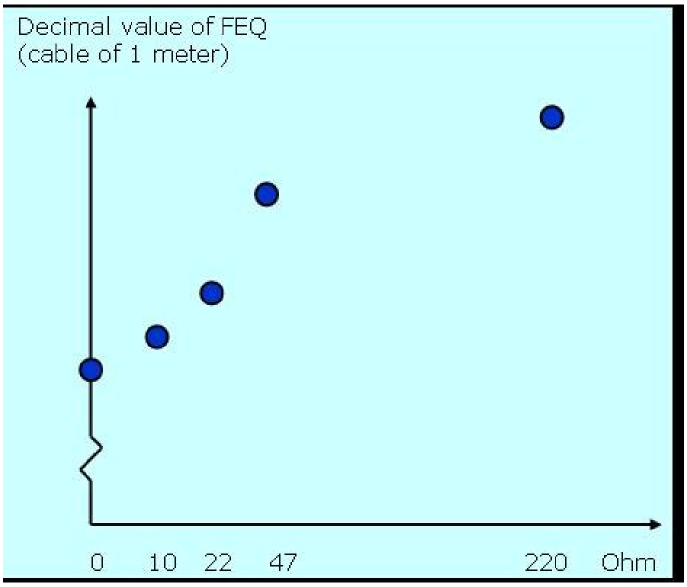
5.5.6.4 Register PHY.24: FEQ Monitor Control Register

Bit	Name	Description	Mode	Default
24.15:0	FEQ_DELTA	Minimum change of value compared to the reference value latched when the monitor is enabled after link up which will trigger the FEQ interrupt and link down. If the FEQ value differs by more than FEQ_DELTA the link goes down if the BER_CNT_LNK_EN is 1 and the BER monitor is enabled, The interrupt is triggered if enabled. 'FFFF' – will disable monitor and cause the reference value to be re-latched continuously. 'FFFE' – will not change the FEQ_DELTA value but read out the current reference value when FEQ_VAL is read instead of the current value. Writing any other value will disable this mode.	W	0xFFFF
24.15:0	FEQ_VAL	If FEQ_DELTA == 7FFF FEQ reference value. Else Current FEQ2 coefficient.	R	Undefined

The following picture gives an example of the value of the FEQ coefficient depending on the line length in meters.



The following picture gives an example of the dependency of the FEQ coefficient on the resistance of the line. The 0 Ohm resistance is the value for a 1 meter line, for the other values a resistor has been added to the RX line.



The blue circles indicate the typical variation of the FEQ2 value.

Example:

Typically the FEQ value will not change while the link is up, except if the cable condition changes. A value for FEQ_DELTA of 1000 is typically a good setting to detect cable condition changes reliably without being too sensitive. The optimal value for the FEQ_DELTA depends on the quality of the cables and connectors used and should be optimized based on the requirements of the application.

To enable the FEQ monitor settings should be:

FEQ_DELTA = 0x3E8

BER_CNT_LINK_EN = 1

With these settings the FEQ monitor will sample the line condition after link up and will put the link down, if these change. Note that a bad line after link down is taken as a reference, thus the software should check the value by reading FEQ_VAL after link up and comparing this to a known good value. This should be determined after installation has been done. Generally typical values can be taken from the picture above. Interrupt 9 should also be enabled to inform the CPU about such an event.

5.5.6.5 TDR-Measurement

Cable breaks can be localized using the built in TDR measurement logic. This block sends out defined pulses and measures the time it takes for the reflected wave to travel forth and back. Several configuration options allow to optimize the measurement to achieve down to 0.8m of accuracy. The register to configure this is described below:

Bit	Name	Description	Mode	Default
15	Reserved	Write with 0, ignore on read	RW	
14	DIAG_INIT	When set to '1' , create one cycle pulse - init TDR test	RW (self cleared)	0
13:8	ADC_MAX_ VALUE	Shows the signed maximum/minimum value of the reflected wave. After the TDR process has been started the PHY will send out a trigger pulse and wait for the reflected wave for 255 clock cycles of 8 ns. After the time has elapsed the DIAG_DONE bit is set. The ADC MAX_VALUE will indicate the maximum of the received wave if positive or the minimum if negative.	R	
13:8	ADC_Trigger	Threshold for pulse detection. 0xf correlates to 1.5V, 0 to 0V MSB should always be 0.	W	
7	DIAG_DONE	Indicate that the counter has been stopped either by counter overrun or by a ADC trigger. Cleared after reading	R	0
6	DIAG_POL	0: Counter stopped by positive trigger level 1: Counter stopped by negative trigger level	R	0
5	DIAG_SEL_LINE	1: perform diagnosis on TX line 0: perform diagnosis on RX line	RW	0
4:0	PW_DIAG	Pulse width for Diagnosis 0: Diagnosis turned off Other: Pulse width = value*8ns	RW	0

Bit	Name	Description	Mode	Default
15:8	CNT_WINDOW	Minimum time after which the counter stops. Used to filter out any pulses or reflections generated from the local connector or similar sources. One tick equals approx. 0.8m	RW	0
7:0	DIAGCNT	Indicates the location of the received signal which exceeded the threshold ; When DIAG_INIT is set to '1' - initiated by HW to '000000' . '1111111' – indicates no reflection. Any value different from zero indicates a valid measurement. When no cable is present, the value will be '000001' (assuming threshold is set to the correct value). One counter tick equals approx. 0.8 m	RO	0

Example:

Before using the TDR logic it must be assured, that a PHY connected to the other side of the line is not transmitting any data. As typically such measurement is only done if the cable is broken there should be no link anyway, but it should be assured that the link is manually put down. Note that there is no reflected wave on a working link as reflections only occur at locations where the cable is broken or at the end of an open line. So the TDR measurement cannot be used to measure cable length of a connected cable. On the other hand a missing refection is a sign of a good cable setup.

There is no way to force a partner PHY to turn off its transmission so this has to be done manually at the partner PHY.

The typical configuration for the start is:

CNT_WINDOW = 1	This value should in any case be slightly higher than the PW_DIAG value. A value of two will filter out any pulses that return sooner than 0,8 m from the PHY.
DIAG_INIT = 1	This will start the pulse immediately
ADC_Trigger = 0x5	This sets the value for the trigger level to 0.5 V
PW_DIAG = 0x1	This sets the pulse width to 8 ns. Generally a smaller pulse may not be able to travel down a long cable and return as it is too weak, a wider pulse may be too wide to measure a short cable as it is still transmitting when the reflection is already returning.
DIAG_SEL_LINE:	Set to 0 or 1 depending on which line pair should be measured.

After writing to the register the result can be read immediately. The results can be interpreted as:

ADC_MAX_VALUE: The maximum measured value of the reflected wave. This can be used to fine tune the value for the next ADC_TRIGGER value. Typically the ADC_Trigger should be set to half of the measured ADC_MAX_VALUE. A value of 0 indicates that no reflection was detected.

DIAG_DONE: Should be one, otherwise the measurement has not been finished. In this case the register needs to be read again. However typically access through the SMI is so slow that the time between the write access to start the measurement and the read to read the results is much longer than the measurement.

DIAG_POL: Indicates the polarity of the reflected wave. If positive the end of the line was open, if negative the end of the line has a shortcut.

DIAG_CNT: This register contains the travel time for the signal in 8ns steps. If there is no reflected wave the counter is at 0x1F. If no cable is connected the value typically is 0x01, however if the CNT_WINDOW is larger than 0x01 this reflected wave will not trigger the counter and DIAG_CNT is set to 0x1F.

A DIAG_CNT of 0x1F can have a number of causes.

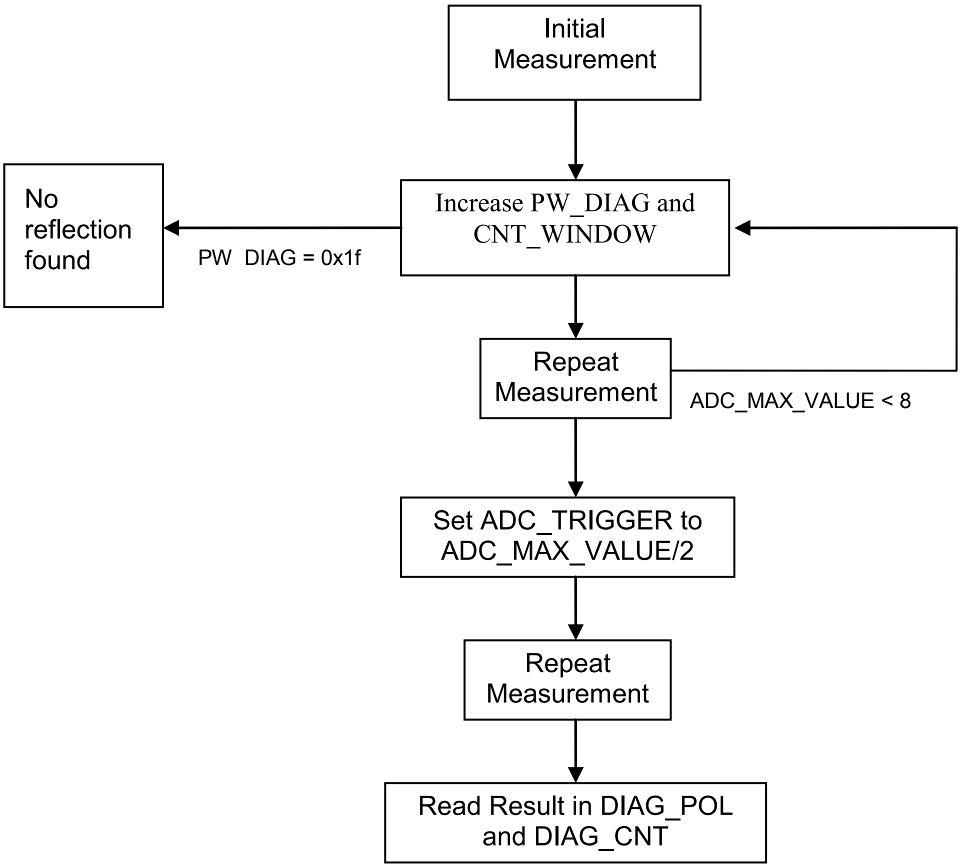
1. The line is properly terminated. In this case there will be no reflection.

2. The cable is too long for the pulse width. In this case PW_DIAG and CNT_WINDOW should be increased and the measurement restarted.

3. The cable is too short for the selected CNT_WINDOW or even unconnected.

4. ADC_TRIGGER is set too high.

The following diagram shows the typical flow when doing the TDR measurement.



The distance to the break or short is the result in DIAG_CNT * 0.8m.

If no reflection can be found this can have the following reasons:

1. The line is properly terminated. In this case there will be no reflection.

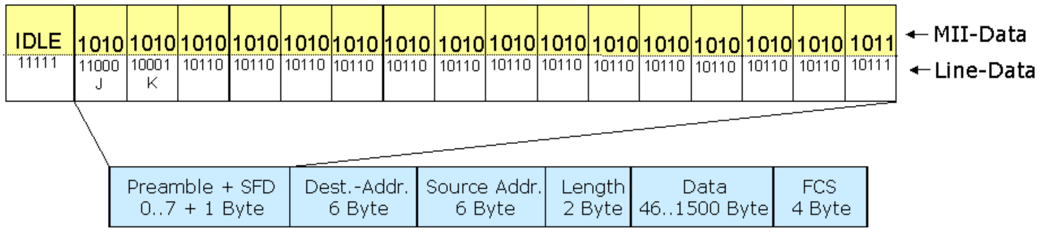
2. The distance to the line break or short cable is too short (< 0.8m) or the cable is completely unconnected.

5.5.7 Latency

The latency is the amount of time it takes for data to pass through the PHY from the line interface to the MII and also from the MII to the line interface on the TX side. For industrial real-time applications a short latency is very important as it has a significant influence on the cycle times that can be achieved and the accuracy at which a system can be operated. This has two implications, one is the amount of latency which should be reduced as much as possible, even more important is the jitter, i. e. the latency should always stay the same.

Although the Renesas PHY has already a very short latency, the PHY has a special mode that will reduce the latency even further. This mode is called “J-only mode” and is available on all devices of the PHY family.

A new telegram is initiated by two symbols “J” and “K” as shown in the picture below:



Before data is sent it is transformed from a 4 bit notation at the MII to a 5 bit notation on the line to ensure that enough changes are available for the clock regeneration. In addition the 5 bit coding allows for transmission of additional control symbols to indicate start of frame and end of frame. So a start of frame is indicated by the symbol 11000 or “J” followed by a 10001 or “K”.

Standard devices (conforming to the Ethernet standard) must detect the leading “J”- and “K”- symbol of a telegram as start-of-frame, before they can start to output data on the MII interface. Thus two symbols have to be received before output can be started on the MII interface. The Renesas PHY offers a special mode to only decode the leading J-symbol and start receiving the data immediately. The PHY will thus output data on the MII following the first “J” symbol without having to wait for the reception of the “K” symbol.

This reduces the roundtrip delay by 40ns. This PHY family is thus able to support a roundtrip delay <200ns. In the unlikely case that the “J” detection was due to a bit error and the next “K” symbol is not received the RX_ERR signal is asserted and reception resumed.

5.5.8 Special Isolate

In many applications it may be desirable to have a more flexible option to configure the PHY compared to strap options which need to be decided when the board is produced. Usually a PHY will read the configuration from the strap pins and immediately after power up will try to connect. This does not leave time for a controlling MAC to change the configuration before the communication and setup with the partner PHY has been started. In special isolate mode the PHY will not connect to its partner PHY but stay quiet on the line until enabled in software. Thus a controlling MAC has time to configure the PHY according to the application and the special configuration can be controlled by firmware instead of hardware.

5.6 PHY Register List

The PHY registers can be accessed at PHY address 0 for PHY 0 or PHY address 1 for PHY 1. These registers control only the PHY they belong to. Some of these registers are duplicated on the PHY address 7 registers to ease software handling.

5.6.1 Register PHY.0 - Basic Control

Bit	Name	Description	Mode	Default
15	RESET	1 = software reset 0 = normal operation When setting this bit do not set other bits in this register	RW/SC	0
14	LOOPBACK	1 = enable internal loopback mode 0 = disable internal loopback mode	RW	0
13	SPEED_ SELECTION	1 = 100 Mb/s 0 = 10 Mb/s This bit is ignored if auto-negotiation is enabled (0.12=1).	RW	1
12	AUTO-NEGOTIATION_ ENABLE	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process	RW	Strap option
11	POWERDOWN	1 = General Power down 0 = normal operation	RW	0
10	ISOLATE	1 = Electrically isolate PHY from MII 0 = Normal operation	RW	0
9	RESTART_ AUTONEGOTIATION	1 = restart auto-negotiation process 0 = normal operation	RW/SC	0
8	DUPLEX_MODE	1 = Full duplex 0 = Half Duplex This bit is ignored if auto-negotiation is enabled (0.12=1).	RW	Strap option
7	COLLISION_TEST	1 = enable COL signal test 0 = disable COL signal test	RW	0
6:0	RESERVED	Write as 0, ignore on Read	RO	0

Writing to Reg. 0 in order to change modes from 10BT to 100BT and vice versa (Autoneg disabled), will take approximately 2us. Mode changes from HD to FD and vice versa is instantaneously.

5.6.2 Register PHY.1 - Basic Control

Bit	Name	Description	Mode	Default
15	100BASE_T4	1 = 100BASE-T4 able 0 = no 100BASE-T4 ability	RO	0
14	100BASE_TX_FULL_DUPLEX	1 = 100BASE-TX ability with full duplex 0 = no 100BASE-TX full duplex ability	RO	1
13	100BASE_TX_HALF_DUPLEX	1 = 100BASE-TX ability with half duplex 0 = no 100BASE-TX half duplex ability	RO	1
12	10MB_FULL_DUPLEX	1 = 10Mb/s ability with full duplex 0 = no 10M b/s full duplex ability	RO	1
11	10MB_HALF_DUPLEX	1 = 10Mb/s ability with half duplex 0 = no 10Mb/s half duplex ability	RO	1
10:6	RESERVED	Ignore on read	RO	0
5	AUTO-NEGOTIATION COMPLETE	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	RO	0
4	REMOTE FAULT	1 = remote fault condition detected 0 = no remote fault condition detected	RO/LH	0
3	AUTO-NEGOTIATION ABILITY	1 = able to perform auto-negotiation 0 = unable to perform auto-negotiation	RO	1
2	LINK STATUS	1 = link is up 0 = link is down	RO/LL	0
1	JABBER DETECT	1 = jabber condition detected 0 = no jabber condition detected	RO/LH	0
0	EXTENDED CAPABILITY	1 = extended register capabilities 0 = basic register set capabilities only	RO	1

5.6.3 Register PHY.2 - PHY Identifier

Bit	Name	Description	Mode	Default
15:0	PHY ID NUMBER	Assign to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI)	RO	0xb824

5.6.4 Register PHY.3 - PHY Identifier

Bit	Name	Description	Mode	Default
15:10	PHY ID NUMBER	Assigned to the 19th through 24th bits of the OUI	RO	0x0a
9:4	MODEL NUMBER	Manufacturer’s model number	RO	0x1
3:0	REVISION NUMBER	Manufacturer’s revision number	RO	0x4

5.6.5 Register PHY.4 - Auto-Negotiation Advertisement

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = next page capable 0 = no next page ability	RW	0
14	RESERVED	Write as “0”, Ignore on read	RO	0
13	REMOTE FAULT	1 = remote fault detected 0 = no remote fault detected	RW	0
12	RESERVED	Write as “0”, ignore on read	RW	0
11:10	PAUSE OPERATION	00 = no PAUSE 01 = asymmetric PAUSE toward link partner 10 = Symmetric PAUSE 11 = both symmetric PAUSE and asymmetric PAUSE toward local device	RW	00
9	100BASE-T4	1 = 100BASE-T4 able 0 = no 100BASE-T4 ability This core does not support 100BASE-T4	RO	0
8	100BASE-TX FULL DUPLEX	1 = 100BASE-TX full duplex able 0 = no 100BASE-Tx ability	RW	1
7	100BASE-TX	1 = 100BASE-TX able 0 = no 100BASE-TX ability	RW	1
6	10BASE-T FULL DUPLEX	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability	RW	1
5	10BASE-T	1 = 10Mbps able 0 = no 10Mbps ability	RW	1
4:0	SELECTOR FIELD	00001 : IEEE Std. 802.3	RW	00001

5.6.6 Register PHY.5 - Auto-Negotiation Link Partner Ability (Base Page)

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = additional next page will follow 0 = last page	RO	0
14	ACKNOWLEDGE	1 = successfully received link partner’s link code word 0 = not successfully received link partner’s link code word	RO	0
13	REMOTE FAULT	1 = remote fault condition 0 = no remote fault condition	RO	0
12:11	RESERVED	Ignore on read	RO	0
10	PAUSE OPERATION	1 = pause operation is supported by remote MAC 0 = pause operation is not supported by remote MAC	RO	0
9	100BASE-T4	1 = 100BASE-T4 able 0 = no 100BASE-T4 ability	RO	0
8	100BASE-TX FULL DUPLEX	1 = 100BASE-TX with full duplex 0 = no 100BASE-TX full duplex ability	RO	0
7	100BASE-TX	1 = 100BASE-TX able 0 = no 100BASE-TX ability	RO	0
6	10BASE-T FULL DUPLEX	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability	RO	0
5	10BASE-T	1 = 10Mbps able 0 = no 10Mbps ability	RO	0
4:0	SELECTOR FIELD	00001 : IEEE Std. 802.3	RO	00001

5.6.7 Register PHY.5 - Auto-Negotiation Link Partner Ability (Next Page)

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = additional next page will follow 0 = last page	RO	0
14	ACKNOWLEDGE	1 = successfully received link partner's link code word 0 = not successfully received link partner's link code word	RO	0
13	MESSAGE PAGE	0 = unformatted page 1 = message page	RO	0
12	ACKNOWLEDGE 2	0 = cannot comply with message 1 = will comply with message	RO	0
11	TOGGLE	0 = previous value of the transmitted link code word equaled logic one. 1 = previous value of the transmitted link code word equaled logic zero.	RO	0
10:0	MESSAGE/ UNFORMAT TED CODE FIELD	11 bit code word received from link partner	RO	All 0

5.6.8 Register PHY.6 - Auto-Negotiation Expansion

Bit	Name	Description	Mode	Default
15:5	RESERVED	Ignore on read	RO	0
4	PARALLEL DETECTION FAULT	1 = fault has been detected 0 = no fault has been detected	RO/LH	0
3	LINK PARTNER NEXT PAGE ABLE	1 = link partner is next page able 0 = link partner is not next page able	RO	0
2	NEXT PAGE ABLE	1 =local device is next page able 0 = local device is not next page able	RO	1
1	PAGE RECEIVED	1 = a new page has been received 0 = a new page has not been received	RO/LH	0
0	LINK PARTNER AUTO-NEGOTIATION ABLE	1 = link partner is auto-negotiation able 0 = link partner is not auto-negotiation able	RO	0

5.6.9 Register PHY.7 - Auto-Negotiation Next Page Transmit

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = next page exists 0 = next page does not exist	RW	0
14	RESERVED	Write as “0”, ignore on read	RO	0
13	MESSAGE PAGE	1 = message page 0 = unformatted page	RW	1
12	ACKNOWLEDGE2	0 = cannot comply with message 1 = will comply with message	RW	0
11	TOGGLE	1 = previous value equaled logic zero 0 = previous value equaled logic one	RO	0
10:0	MESSAGE/ UNFORMATTED CODE	11 bit code word to be transmitted to link partner	RW	0x001

5.6.10 Register PHY.16 - Silicon Revision

Bit	Name	Description	Mode	Default
15:10	RESERVED	Ignore on read	RO	0
9:6	SILICON REVISION	Four bit silicon revision identifier	RO	0001
5:0	RESERVED	Ignore on read	RO	0

5.6.11 Register PHY.17 - Mode Control/Status

Bit	Name	Description	Mode	Default
15:14	RESERVED	Write as 0; ignore on read.	RW	0
13	EDPWRDOWN	Enable the energy detect power-down mode: 0 = energy detect power-down is disabled 1 = energy detect power-down is enabled	RW	0
12	RESERVED	Write as 0; ignore on read.	RW	0
11:10	RESERVED	Write as 0; ignore on read.	RW	0
9	FARLOOP BACK	Remote loopback enable All the received packets are sent back simultaneously (in 100BASE-TX/FX only).	RW	0
8	FASTEST	Auto-negotiation test mode 0 = normal operation 1 = activates test mode Note: This bit can be used for simulation. In this mode, expanded time of S/W reset becomes shorter,too.	RW	0
7	AUTOMDIX_EN	AutoMDIX enable bit 1 = Auto-detect MDI/MDIX mode 0 = Manual set of MDI/MDIX mode According to bit MDI mode (Reg17.6). AutoMDIX is disabled in FX Mode.	RW	Strap option
6	MDI MODE	MDI/MDIX mode control/status 1 = MDIX mode 0 = MDI mode When AutoMDIX_en (17.7) is disabled, this bit is used for manual control of MDI/MDIX mode. If AutoMDIX_en (Bit 17.7) is enabled it shows the status and will not be written to	RW	0
5	RESERVED	Write as 0, ignore on read	RW	0
4:3	RESERVED	Write as 0, ignore on read	RW	0
2	FORCE GOOD LINK STATUS	1 = Force 100BASE-X link active 0 = normal operation Note: this bit should be set only testing	RW	0

1	ENERGYON	Indicates whether energy is detected on the line. If no valid energy is detected within 256ms, this bit goes to 0.	RO	0
0	RESERVED	Write as 0, ignore on read	RW	0

5.6.12 Register PHY.18 - Special Modes

Bit	Name	Description	Mode	Default
15:11	Reserved	Write as 0, ignore on read	RW NASR	0
10	FX_MODE	Enable 100BASE-FX mode 1 = FX mode enable When PHYMODE should be set to “0011” or “0010” only.	RW NASR	Strap option
9:	Reserved	Write as “0”. Ignore on read	RW	0
8:5	PHYMODE	PHY mode of operation. Is set according to strap pin setting after reset. 0000:	RW NASR	Indirect Strap option
4:3	PHY_ADD_DEV	PHY address upper two bits The PHY address is used to address the whole device and for the initialization of the Cipher (Scrambler) key.	RW NASR	Strap option
2:0	PHY_ADD_MOD	PHY address lower three bits The PHY address is used to address the PHY and for the initialization of the Cipher (Scrambler) key.	RW NASR	000

5.6.13 Register PHY.19 - Elastic Buffer Status register (Loopback Mode only)

Bit	Name	Description	Mode	Default
15:8	reserved	Ignore on read	RO	
7	T_EL_BUF_OVF	Transmitter elastic overflow	RO/LH	0
6	T_EL_BUF_UDF	Transmitter elastic underflow	RO/LH	0
5	R_EL_BUF_OVF	Receiver elastic overflow	RO/LH	0
4	R_EL_BUF_UDF	Receiver elastic underflow	RO/LH	0
3:0	reserved	Ignore on read	RO	

5.6.14 Register PHY.20 – Reserved

Bit	Name	Description	Mode	Default
15:0	Reserved	Ignore on read	RW	0

5.6.15 Register PHY.21 – Reserved

Bit	Name	Description	Mode	Default
15:0	Reserved	Ignore on read	RO	0

5.6.16 Register PHY.22 – Reserved (TSTREAD2 / TSTWRT)

Bit	Name	Description	Mode	Default
15:0	Reserved	Ignore on read	RW	0

5.6.17 Register PHY.23 – BER Counter

Bit	Name	Description	Mode	Default
15	BER_LNK_OK	Link quality indication – indicates state of link monitor FSM. '0' – FSM is not in 'Good Link' state '1' – indicates FSM in 'Good Link' state Will go up as soon as the counter is below the trigger level after start up. Can be used to detect reliably link up after start up.	RO	0
14	BER_CNT_ LNK_EN	1: A trigger on the BER or on the FEQ monitor will cause a link down 0: A trigger on the BER/FEQ will just cause the state machine to leave "Good Link" state.	RW	1
13:11	BER_CNT_TRIG	Trigger level for BER Count to define link up/down counter in 1 * 2^(n -1) errors 0: >0 errors will trigger 1: >1 error will trigger 2: >2 errors will trigger 3: >4 errors will trigger 4: >8 errors will trigger 5: >16 errors will trigger 6: >32 errors will trigger 7: >64 errors will trigger	RW	2
10:7	BER_WINDOW	Length of time for BER Counter in 0.005 * 2^n ms 0: BER Counter functions disabled 1: 0.01 ms 2: 0.02 ms 3: 0.04 ms ….. 14 : 81.92ms 15: unlimited run	RW	1 (0.01 ms)
6:0	BER-COUNT	Counter for bit errors, shows the amount of errors in the past time window or every 100 µs if BER_WINDOW = 15 . Writing a 00 resets the BER counter and restarts the time window.	RO	0x0

5.6.18 Register PHY.24 – FEQ monitor Register

Bit	Name	Description	Mode	Default
15:0	FEQ_DELTA	Minimum change of value compared to the reference value latched when the monitor is enabled, which will trigger the FEQ interrupt and link down. If the FEQ value differs by more than that value, the link goes down, if the BER_CNT_LNK_EN is 1 and the BER Monitor is enabled, The interrupt is triggered if enabled. 'FFFF' – will disable monitor and cause the reference value to be relatched continuously 'FFFE' – will not change the FEQ_DELTA value but enable to read out the current reference value, when FEQ_VAL is read, instead of the current value. Writing any other value will disable this mode.	W	0xFFFF
15:0	FEQ_VAL	If FEQ_DELTA == FFFE Bit 17:2 of the reference value. Else Bits 17:2 of the current FEQ2 coefficient.	RO	

5.6.19 Register PHY.25 – Diagnosis Control/Status Register

Bit	Name	Description	Mode	Default
15	Reserved	Write with 0, ignore on read	RW	
14	DIAG_INIT	When set to '1' , create one cycle pulse - init TDR test	RW (self cleared)	0
13:8	ADC_MAX_ VALUE	Shows the signed maximum/minimum value of the reflected wave. After the TDR process has been started the PHY will send out a trigger pulse and wait for the reflected wave for 255 clock cycles of 8 ns. After the time has elapsed the DIAG_DONE bit is set. The ADC MAX_VALUE will indicate the maximum of the received wave if positive or the minimum if negative.	RO	
13:8	ADC_Trigger	Threshold for pulse detection. – should be 0.5V / 00111 for cable length detection or 1.5V / 01111 for no cable detection. MSB should always be 0.	WO	
7	DIAG_DONE	Indicate that the counter has been stopped either by counter overrun or by a ADC trigger. Cleared after reading	RO	0
6	DIAG_POL	0: Counter stopped by positive trigger level 1: Counter stopped by negative trigger level	RO	0
5	DIAG_SEL_LINE	1: perform diagnosis on TX line 0: perform diagnosis on RX line	RW	0
4:0	PW_DIAG	Pulse width for Diagnosis 0: Diagnosis turned off Other: Pulse width = value*8ns	RW	0

5.6.20 Register PHY.26 – Diagnosis Counter Register

Bit	Name	Description	Mode	Default
15:8	CNT_WINDOW	Minimum time after which the counter stops. Used to filter out any pulses or reflections generated from the local connector or similar sources. One tick equals approx. 0.8m	RW	0
7:0	DIAGCNT	Indicates the location of the received signal which exceeded the threshold ; When DIAG_INIT is set to '1' - initiated by HW to '000000' . '1111111' – indicates no reflection. Any value different from zero indicates a valid measurement. When no cable is present, the value will be '000001' (assuming threshold is set to the correct value). One counter tick equals approx. 0.8 m	RO	0

5.6.21 Register PHY.27 - Special Control/Status Indications

Bit	Name	Description	Mode	Default
15:13	Reserved	Write as “000”. Ignore on read	RW	0
12	SWRST_FAST	SW reset counter testing 1 = accelerates SW reset counter from 256us to 10 us for production testing.	RW	0
11	SQEOFF	Disable the SQE test(Heartbeat) 1 = SQE test is disabled 0 = SQE test is enabled. Set ‘1’ when repeater mode	RW NASR	0
10:6	Reserved	Write as 0, ignore on read.	RW	0
5	FEFIEN	Far End fault indication enable 1 = FEFI generation and detection are enabled. This is the reset value if FXMODE is enabled by strap option 0 = FEFI generation and detection are disabled	RW	Strap option
4	XPOL	Polarity state of the 10BASE-T 1 = Reversed polarity 0 = normal polarity	RO	0
3:0	Reserved	Ignore on read.	RO	1011

5.6.22 Register PHY.28 - Reserved

Do not write or read this register

5.6.23 Register PHY.29 - Interrupt Source Flags

Bit	Name	Description	Mode	Default
15:11	Reserved	Ignore on Read		0
10	INT10	BER counter trigger	RC	0
9	INT9	FEQ trigger	RC	0
8	Reserved	Ignore on read	RC	0
7	INT7	1 = ENERGYON generated	RC	0
6	INT6	1 = auto-negotiation complete	RC	0
5	INT5	1 = remote fault (TX Mode) or Far End Fault (FX-Mode) detected	RC	0
4	INT4	1 = link down	RC	0
3	INT3	1 = auto-negotiation Last Page acknowledge	RC	0
2	INT2	1 = parallel detection fault	RC	0
1	INT1	1 = auto-negotiation page received	RC	0
0	Reserved		RO	0

5.6.24 Register PHY.30 - Interrupt Enable

Bit	Name	Description	Mode	Default
15.11	Reserved	Write as 0, Ignore on read	RO	0
10:9	MASK BIT	1 = interrupt source is enabled 0 = interrupt source is masked	RW	0
8	Reserved	Write as 0, Ignore on read	RO	0
7:1	Mask Bits	1 = interrupt source is enabled 0 = interrupt source is masked	RW	0
0	Reserved	Write as 0, Ignore on read	RO	0

5.6.25 Register PHY.31 - PHY Special Control/Status

Bit	Name	Description	Mode	Default
15:14	Reserved	Write as 0. ignore on read.	RW	0
13	Reserved	Write as 0. ignore on read.	RW	0
12	AUTODONE	Auto-negotiation done indication 1 = auto-negotiation is done 0 = auto-negotiation is not done or disabled (or not active)	RO	0
11:7	Reserved	Write as “00000”. Ignore on read	RW	0
6	ENABLE 4B5B MII MODE	1 = Enable 4B/5B Encoding/Decoding. MAC interface must be configured in 0 = Bypass encoder/decoder	RW	1
5	Reserved	Write as 0, ignore on Read.	RW	0
4:2	SPEED INDICATION	HCDSPEED value: 001 = 10Mbps half-duplex 101 = 10Mbps full-duplex 010 = 100BASE-TX half-duplex 110 = 100BASE-TX full-duplex	RO	000
1	RX_DV_J2T	’0’ – rx_dv rises on “JK” delimiter falls on “TR” delimiter ‘1’ – J_ONLY_MODE, rx_dv rises on “J” delimiter falls on “T” delimiter. . Do not use in RMII Mode	RW	0
0	SCRAMBLE DISABLE	1 = disable data scrambling 0 = enable data scrambling	RW	0

External Components

6.1 Clock

The devices can be operated on an external 25 MHz clock in MII mode or an external 50 MHz clock in RMII mode. In addition for MII mode it contains an internal oscillator which may generate the required 25 MHz clock using an external 25 MHz crystal connected to the pins XCLK1 and XCLK0.

6.2 Internal Regulator

The device contains an internal voltage regulator which generates the internal 1.6 V for the core from the external 3.3V power supply. It can be disabled by tying REGOFA and REGOFFD to 3.3V and connecting the pins mentioned below directly to a 1.6 V power supply. Otherwise the REGOFFA and REGOFFD pins must be connected to GND.

6.3 Power Up Sequence

In case the internal voltage regulator is not used and the 1.5V supply is supplied form an external source a special power up sequence is not required. However the time of power supply rise and the point when both power supplies are stable must be within 100 ms.

Support of IEEE1588 (uPD60611 only)

Renesas Electronics’ Ethernet PHY uPD60611 supports the precision time protocol (PTP) according to IEEE1588 to support requirements towards higher precision and faster production.

The PHY supports IEEE1588 V1 and V2 including transparent clock mode and one-step or two-step mode. Furthermore the PHY is able to timestamp incoming messages with a resolution of 1ns.

The following clock modes are supported:

- Ordinary clock
- Boundary clock
- Transparent clock

The PHY can timestamp events on any of the GPIO pins. Based on the internal synchronized clock it may generate up to three output signals which may generate single pulses or repetitive pulses with programmable pulse length. It is also possible to output a Pulse-Per-Second (PPS) signal. Resolution for the event timestamping unit and the pulse generation unit is 8ns. Reception of a PTP message, transmission of a PTP message, an event on the event unit and the pulse generator can generate an interrupt.

7.1 IEEE1588

The basic purpose of IEEE1588 is to synchronize clocks in different nodes and have them run on the same time and frequency. One clock in a node is selected as the master clock and all other clocks called “slave clocks” in the system are synchronized to this clock called “master clock”. Special PTP telegrams are exchanged between the nodes to distribute the time value of the master clock. To compensate the travel time it is measured for the PTP telegrams. Based on the master clock time value and the travel time of the telegram the slave clocks can be adjusted and synchronized.

To measure the travel time timestamps can be taken when telegrams leave the PHY or are received by the PHY. The more precise these timestamps can be taken, the more precise the calculation of the travel time and the better the synchronization of the clocks that can be achieved. For the transmit telegrams the data is always sent at the clock edge of the 125 MHz clock and therefore the timestamping logic, which is running at the same clock as the transmit logic has an optimum accuracy. However receive telegrams can arrive at any time within the 125MHz/8ns clock period so the receive timestamping logic always has an error of up to 8ns depending on the actual arrival time of the data within the clock period.

To optimize the reception of the incoming data the receive DSP continuously shifts the time at which the data is sampled to the optimal time. This is done by using one of 8 phases of the 125MHz clock coming out of the PLL. Thus the selected phase of the PLL is a precise indicator for the exact sampling time at which the incoming data arrived at the PHY. As each of these phases represents a 1ns timeslot it can be used to define the exact arrival time within the 8ns clock period. This data is also stored together with the timestamp.

There are two ways timestamps can be transmitted between the nodes. One way is called “One Step”. In this mode the timestamp for transmit telegrams can be directly embedded in the telegram itself when it is transmitted. However this approach increases the latency of the path through the PHY but it reduces required software overhead. The other option is to use a “Two Step” approach. In this mode the timestamp of the telegram is taken when it is transmitted and the timestamp is send in a “follow up” telegram. This option requires more traffic and more software overhead but incurs a lower latency on the path.

7.2 Register access to PTP

Many registers within the PTP block are 80 bits or 48 bits wide to control the whole width of the time representation. To read or write these registers they need to be accessed 5 times (5 * 16 bit words = 80 bits) in a row. Unless otherwise noted accesses are done with the least significant word (bits 15:0) first.

7.3 1588 Clock Control

The clock handles the time which is to be synchronized between the different nodes. To be adjusted it can be either directly set, accelerated or decelerated and adjusted over a defined period.

The accessible clock is 80 bit wide with the upper 48 bits counting the seconds and the lower 32 bit counting the nanoseconds. Thus the overflow is not at 0xffffffff but at 0x3b9acA00(10^9 ns). Internally the clock additionally handles additional 30 bits of sub-nanosecond resolution to handle drift correction.

As the clock of the device is running at 125 MHz the clock value is basically increased by 8ns with every clock cycle. This 8ns value can be adjusted to speed up the clock or slow it down. So although the clock is still incremented based on the 125 MHz clock it can be fine-tuned so the value reflects the real time.

To access the clock the register has to be accessed five times with 16 bits each.

7.3.1 CLOCK_STATUS Register 6.0

The CLOCK_STATUS register is used to control the clock and the several registers used to access the PTP clock.

Bit	Name	Description	Mode	Default
15	reserved	Write as 0, ignore on read	RW	0
14	EN_OFFSET_CORR	1: Enable and start offset correction 0: Disable offset correction Automatically cleared after the offset correction is finished.	RW	0
13	OFFSET_RUN	1: offset correction in process 0: offset correction done	RO	0
12	EN_DRIFT_CORR	1: enable drift correction 0: disable drift correction	RW	0
11:9	CLOCK_READ_POS	Value of pointer pointing to the CLOCK_READ register. If 0 next read is from least significant word of clock latch.	RO	0
8:6	CLOCK_WRITE_POS	Value of pointer pointing to the CLOCK_WRITE register. If 0 next write goes to least significant word of clock latch.	RO	0
5:3	OFFSET_WRITE_POS	Value of pointer pointing to the CLOCK_OFFSET register. If 0 next write goes to the least significant word off offset latch.	RO	0
2:0	DRIFT_WRITE_POS	Value of pointer pointing to the CLOCK_DRIFT register. If 0 next write goes to the least significant word off offset latch.	RO	0

7.3.2 CLOCK_READ Register 6.1

The CLOCK_READ register is used to read the actual value of the clock. It must be accessed five consecutive times to read the complete data. Any read to another register will reset the internal pointer and the next read will then again read the highest word. All accesses are done with the most significant word first.

Bit	Name	Description	Mode	Default
79:0	CLOCK_READ	Clock read register.	RO	0

7.3.3 CLOCK_WRITE Register 6.2

This register can be used to set the clock to a value. It must be written five consecutive times. The data is latched into the clock when the 5th word is written. All accesses are done with the most significant word first.

Bits	Name	Description	Mode	Default
79:0	CLOCK_WRITE	Clock write register	WO	

7.3.4 CLOCK_OFFSET Register 6.3

This register is used to adjust the clock to a new value. To avoid sudden jumps the offset is not added at once, instead the “OFFSET” is added/subtracted to the clock value after “OFFSET_INTERVAL” for “OFFSET_COR_COUNT” times. Thus the clock is slowly adapted to the new value and jumps are avoided.

All values are latched internally when the offset correction is stopped either when it is finished or if it is manually disabled and reenabled with the EN_OFFSET_CORR register bit.

Bit	Name	Description	Mode	Default
47	OFFSET_SIGN	Sign, 1: Subtract offset 0: Add offset	WO	0
46:44	OFFSET	Increase value in ns.	WO	0
43	Reserved	Write as 0	WO	0
42:32	OFFSET_INTERVAL	Interval in steps 0: No interval 1: No interval 2: add every 2nd step 3: add every 3rd step …	WO	0
31:30		Write as 0	WO	0
29:0	OFFSET_COR_COUNT	Count, how often the “step” value is added	WO	0

7.3.5 CLOCK_DRIFT Register 6.4

This register contains a correction value, which can be used to continuously correct the clock value to compensate for oscillator drift. The value in the DELTA_VAL register is summed up every clock cycle (125MHz), as soon as the sum has exceeded 0x3fffffff a value of 1 an additional ns is depending on the DELTA_SIGN bit added/subtracted from the clock value. This register is latched internally when the EN_DRIFT_CORR register bit is set.

The value for the DELTA_VAL register is calculated based on the following formula:

$$DELTA\_VAL = \frac{drift \cdot 10^{3} \cdot 2^{30}}{125[MHz] / (1 \pm drift)}$$

$$where:$$

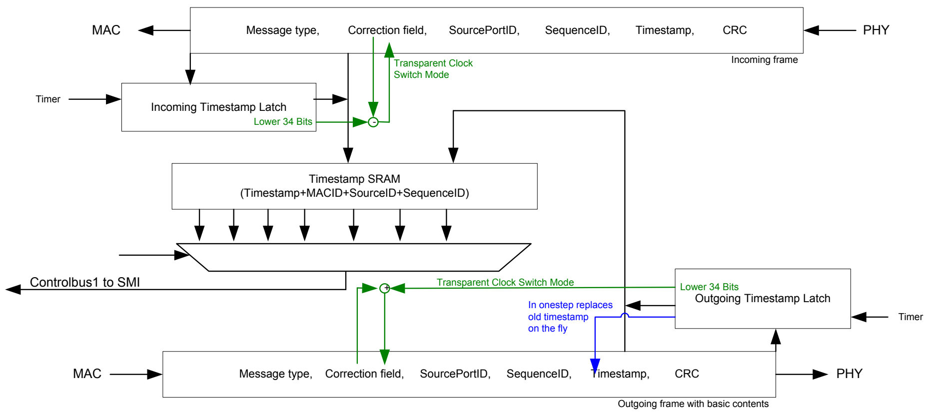
$$drift[s/s]\ is\ correction\ value\ for\ clock$$

$$\pm : use + when\ DELTA\_SIGN = 1, use - when\ DELTA\_SIGN = 0$$

Bit	Name	Description	Mode	Default
31	DELTA_SIGN	Sign of the delta value. 1: Clock is slowed down 0: Clock is speeded up	RW	0
30	Reserved	Ignore on read, write as 0	RW	0
29:0	DELTA_VAL	Delta in fractions of ns, by which the increment value is corrected. So bit 29 represents ½ ns, bit 28 1/4th ns, bit 27 1/8th ns, etc.	RW	0

7.4 Frame Handling Unit

The following picture shows the block diagram for the frame handling unit. The incoming frame is time stamped as it arrives and the timestamp is then stored together with other frame related information in the timestamp SRAM. When a frame is sent, it is time stamped and the timestamp is stored together with the frame related information in the SRAM. This data enables software to handle two step PTP. When an event happens either due to transmission or reception of a PTP message an interrupt can be generated.



7.4.1 One step mode

For one step PTP the timestamp is stored in the outgoing timestamp latch and is on the fly integrated in the timestamp field of the frame. The CRC is corrected accordingly. Note that for one step clock the latency is increased as the insertion of the time stamp in the frame requires some processing of the frame.

7.4.2 Transparent Mode

Transparent Clock is used to improve the accuracy of the time synchronization in long networks by eliminating the uncertainty it takes for synch frames to pass through switches. Depending on the load of the switch the residence time of a synch telegram in the switch varies. By measuring the time a synch frame stays in the switch and writing this value into the frame the accuracy is greatly improved as the slave clock can use this value to adjust its calculation of the master clock value.

To support Transparent Clock mode in hardware the PHY modifies the respective telegrams. When a PTP synch telegram is received in transparent clock mode, the lower 2(sec)+32(ns) bits of the timestamp value taken at reception are converted to ns and subtracted from the correction field. When a PTP telegram is sent, the transmit timestamp lower 2(sec)+32 (ns) bits are converted to ns and added to the correction field. Thus the correction field is incremented by the difference between transmit and reception and the correction field correctly updated even if a telegram is received on one PHY and transmitted on the other. This handling can be enabled separately for each PHY and for transmit and receive.

The Transparent Clock function can only be used in one step mode. In two step mode the Transparent Clock function is not required but can be handled by using one of the Ordinary Clock modes for time stamping and handling the protocol in software based on the FollowUp telegrams.

7.4.2.1 End to End Transparent Clock

For End to End Transparent clock the time a synch telegram takes to pass through the node is measured and either stored in the correction field of the telegram or the correction field of the FollowUp telegram. The correction field at the slave then contains the time that the telegram spend in the different switches etc. which act as a transparent clock. The PTP stack can use this value to calculate the raw line delay and eliminate the jitter that comes from the varying residence times in the switches.

7.4.2.2 Peer to Peer Transparent Clock

For peer-to-peer transparent clock each node measures the delay to all surrounding nodes using the PdelayReq and Pdelay_Resp mechanism. Thus all line delays in a network are known. Each node through which a Synch message passes adds the own residence time plus the line delay of the incoming link to the correction field. When this synch telegram arrives at the slave node it contains the complete line delay plus the residence times in its correction field except for the very last link. The delay on the last link is known to the slave and thus the complete line delay is known. Although this method is more complex than the End to End transparent clock it offers much faster reconfiguration in case of line breaks.

7.4.3 Timestamp Status Register 6.6

The Timestamp Status register shows the status for each buffer. .

Bit	Name	Description	Mode	Default
15:10		Reserved write as 0, ignore on read	RW	
9	BUF_EMPTY_TX_PHY0	1:Buffer not empty for TX buffer PHY0 0:Buffer empty for TX buffer PHY0	RO	0
8	BUF_EMPTY_RX_PHY0	1:Buffer not empty for RX buffer PHY0 0:Buffer empty for RX buffer PHY0	RO	0
7:2		Reserved write as 0, ignore on read	RW	
1	OVERFLOW_BUF_TX_PHY0	1:Buffer overflow for TX buffer PHY0. 0: No overflow Cleared when read	RO	0
0	OVERFLOW_BUF_RX_PHY0	1: Buffer overflow for RX buffer PHY0. 0: No overflow Cleared when read	RO	0

7.4.4 Timestamp Configuration Register 6.7

The Timestamp Configuration register is used to configure the framer unit and is used to select which register of the timestamp memory is read.

Bit	Name	Description	Mode	Default
15:8		Reserved, write as 0, ignore on read	RW	
7	DISCARD_OLDEST_TIMESTAMP	0: Do not overwrite timestamp if buffer overruns / newest timestamp is lost 1: Overwrite oldest timestamp if buffer overruns / oldest timestamp is lost	RW	0
6:4	TIMESTAMP_SELECT	Address at which timestamp buffer is read for the following access to the TIMESTAMP_LINE_EVENT_WORD register. 001: Next read will get TX timestamp 000: Next read will get RX timestamp Others: Undefined	RW	0
3:1		Reserved, ignore on read, write as 0	RW	
0	TS_EN_PHY0	1: Enable timestamping for PHY0 depending on setting in PTP_CONFIG_REGISTER 0: Disable timestamping for PHY0	RW	0

7.4.5 TIMESTAMP_LINE_EVENT Register 6.8

The TIMESTAMP_LINE_EVENT register gives access to the timestamp memory which stores the time stamps generated by the framer logic when a PTP frame was transmitted or received. It stores transmit or receive timestamps separately for TX and RX frames. The TIMESTAMP_SELECT bits in the TIMESTAMP_CONGIGURATION register define if the TX or the RX buffer is accessed. The timestamp memory can hold up to four timestamps for RX and four timestamps for TX, A read will always retrieve the oldest valid dataset.

A timestamp set is combined of the timestamp itself, the source port identity and the sequence ID stored in a 192 bit wide register. This is organized as shown below:

Bit	Name	Description	Mode	Default
191:176	MESSAGE_ID	Message Type of the received message 001: PTP Sync message 010: PDelayReq message 011: PDelayResp message 100 : Delay Req. message	RO	Undefined
175:96	TIMESTAMP	Timestamp of the related event described in bits 95:0. Bits 175:128: seconds Pits 127:96: ns	RO	Undefined
95:16	SOURCEPORTIDENTITY	sourcePortIdentity extracted from the PTP telegram . If TS_ALL_FRAMES_nn is set and a NonPTPFrame is received this field is empty.	RO	Undefined
15:0	SEQUENCE_ID	Rolling number assigned by sending port and extracted from telegram. If TS_ALL_FRAMES is set, and also normal non-PTP telegrams are timestamped there may be no SEQUENCE_ID in the telegram, thus the SEQUENCE_ID is generated internally starting with 0.	RO	Undefined

To read a data set the timestamp memory register has to be accessed 12 times. The least significant word is read first. The TIMESTAMP_SELECT register must be written prior to each individual access to the timestamp memory register.

7.4.6 PTP_CONFIG Register 6.9

The PTP Config register is used to configure the framer unit. The config register for PHY 0 is located at address 6.9.

Bit	Name	Description	Mode	Default
15:12		Reserved, ignore on read, write as 0	RW	
11	TS_ALL_ FRAMES_RX	1: Enable timestamping for all received telegrams. The IPV4 and IPV6 filter bits are still used. 0: Do not enable timestamping for all received telegrams	RW	0
10	TS_ALL_ FRAMES_TX	1: Enable timestamping for all transmitted telegrams. The IPV4 and IPV6 filter bits are still used. 0: Do not enable timestamping for all transmitted telegrams. Only PTP telegrams are timestamped.	RW	0
9	L2	1: Timestamp all Layer 2 PTP telegrams (only for V2 messages) 0: Do not timestamp layer 2 telegrams	RW	0
8	IPV4	1: Timestamp PTP frames containing IPV4 telegrams 0: Do not timestamp IPV4 telegrams	RW	0
7	IPV6	1: Timestamp PTP frames containing IPV6 telegrams (only for V2 messages) 0: Do not timestamp IPV6 telegrams	RW	0
6	ONE_STEP	1: Enable one step mode for the PHY. In this mode the taken transmit timestamp is integrated in the frame on the fly and the CRC corrected. In this mode the transmit timestamp is not stored in the timestamp memory. 0: Select two step mode, the transmit timestamp is not integrated in the outgoing frame.	RW	0
5:4	P2P_DELAY_ WRITE_POS	Current position of the PORT_DELAY_PHY register	RO	0
3:2	MODE_TX	Set the PTP mode for TX 00: BC_PTP_V1: Boundary clock mode for PTP-V1 telegrams.	RW	1

		01: BC_PTP_V2: Boundary clock mode for PTP-V2 Telegrams 10: TC_E2E_PTP_V2: Transparent clock end-to-end mode for V2 telegrams 11: TC_P2P_PTP_V2: Transparent clock peer-to-peer mode for V2 Telegrams For all other messages(non-PTP messages) no timestamp is taken unless the TS_ALL_FRAMES_TX is set.		
1:0	MODE_RX	Set the PTP mode for RX 00: BC_PTP_V1: Boundary clock mode for PTP Version 1 telegrams For Sync and Delay_Req frames the timestamp is taken and stored in the timestamp buffer. 01: BC_PTP_V2: Boundary clock mode for PTP Version 2 frames 10: TC_E2E_PTP_V2: Transparent clock end-to-end mode for PTP V2 telegrams 11: TC_P2P_PTP_V2: Transparent clock peer-to-peer mode for V2 telegrams For all other messages(non-PTP message) no timestamp is taken unless the TS_ALL_FRAMES_RX is set.	RW	1

The following table gives an overview on how the different telegram types are handled depending on the configuration. An empty field means that nothing is done.

TX Path:

Frame type	OC/BC V1 One Step	OC/BC V1 Two Step	OC/BC V2 E2E/P2P One Step	OC/BC V2 E2E/P2P Two Step	TC E2E One Step	TC P2P One Step
Sync	Store TS	Copy TS to TS field	Copy TS to TS field	Store TS	Add TS to Cor. field	Add TS to Cor. field
FollowUp	-	-				
DelayReq	Store TS	Store TS	Store TS	Store TS	Add TS to Cor. field	
DelayResp	-	-				
PeerDelayReq	-	-	Store TS	Store TS	Add TS to Cor. field	Store TS
PeerDelayResp	-	-	Add TS to TS field	Store TS	Add TS to Cor. field	Add TS to Cor. field
PeerDelayResp FollowUp	-	-				

RX Path:

Frame type	OC/BC V1 One Step	OC/BC V1 Two Step	OC/BC V2 E2E/P2P One Step	OC/BC V2 E2E/P2P Two Step	TC E2E One Step	TC P2P One Step
Sync	Store TS	Store TS	Store TS	Store TS	Sub TS from Cor. field, Store TS	Sub TS from Cor. Field Store TS
FollowUp	-	-				
DelayReq	Store TS	Store TS	Store TS	Store TS	Sub TS from Cor. field,	
DelayResp	-	-				
PeerDelayReq	-	-	Sub TS from Cor. field	Store TS	Sub TS from Cor. field,	Sub TS from Cor. field
PeerDelayResp	-	-	Store TS	Store TS	Sub TS from Cor. field	Store TS
PeerDelayResp FollowUp	-	-				

7.4.7 PHY_DELAY_TX Register 6.11

The PHY_DELAY_TX_PORT register is used to adjust the timestamp by the latency of the PHY's TX path. This is by default set to 0 but may be corrected to also compensate for delays caused by the transformer. PTP assumes that the line delay including the PHY latency in both directions is identical, this may not be the case if PHYs from different vendors are used in a network. In this case the PHY_DELAY_TX_PORT and PHY_DELAY_RX_PORT values should be set. This value should be set to 40.

Bit	Name	Description	Mode	Default
15:0	PHY_DELAY_ TX_PORT	Value in ns by which timestamps taken for the PHY on the TX side are corrected.	RW	0

7.4.8 PHY_DELAY_RX Register 6.12

The PORT_DELAY_RX_PORT register is used to adjust the timestamp by the latency of the PHYs RX path. This is by default set to 0 but may be corrected to also compensate for delays caused by the transformer. Typically this value should be 190 if Fast-JK mode is used, otherwise 230.

Bit	Name	Description	Mode	Default
15:0	PHY_DELAY_ RX_PORT	Value in ns by which timestamps taken for the PHY on the RX side are corrected.	RW	0

7.5 Input Capture Unit

The input capture unit can be used to timestamp events on any of the GPIO pins. The timestamps are stored in a special memory area which can be accessed through the SMI through dedicated registers. The memory is configured as a FIFO structure, timestamps are written in consecutive addresses. To read out certain addresses can be selected. Up to 64 timestamps can be stored.

Each GPIO has its own edge detection unit which can be configured to react on rising edge, falling edge or both. If an event happens, the value of the timer is latched locally. Each pin has its own counter to count the events that have happened. The value of this counter is stored as “rolling number” together with the timestamp. Thus it can be easily checked if an event has been missed if the rolling number value has gaps when the timestamp is read. The input capture unit also stores the GPIO number at which the event occurred and the edge that triggered the event together with the timestamp data. Each detection unit can store up to one event which needs to be stored before the next event occurs.

The input capture unit needs 4 clock cycles of 125 MHz to store an event, thus the maximum frequency at which the input edges can be captured is < 31.25 MHz. If multiple events happen simultaneously they are stored in the order of the GPIO pin number, i.e. GPIO1 is stored before GPIO2. If a new event happens before the event is stored the old event data is lost. As the input capture unit is shared for all pins this frequency applies to all enabled pins together. In any case the limiting factor for edges is the speed at which the data can be read through the SMI.

7.5.1 Input Event Control Register 7.12

The Input Event Control register is used to configure the input event unit.

Bit	Name	Description	Mode	Default
15	ALL_PTR_RES	Reset all pointers	WC	0
14		Reserved, ignore on read, write as 0	RW	0
13	READ_WORD_NEXT	1: Reading next word, when accessing Read Register 0: No impact	RW	0
12	OVRRUN_ANY_GPIO	0: No overrun on any GPIO 1: One of the edge detection unit got a pulse before it could handle the previous one. This means that the frequency of pulses on the GPIO is too high.	RW	0
11	TIMEOUT_ANY_GPIO	0: No Timeout on any GPIO 1: An edge detection unit latched an event, but it could not be stored timely. This means that the frequency of all GPIO events together is too high.	RC	0
10	TIMESTAMP_ ENABLE	1: Enable time stamping unit 0: Disable time stamping unit	RW	0
9	TS_ OVWR_EN	0: New timestamps can overwrite older ones when the buffer is full 1: New timestamps are not stored if memory has not been read out (no overwrite) and the buffer is full.	RW	0
8	TS_RAM_ OVERFLOW	1: Timestamps were overwritten 0: Timestamps were not overwritten	RO	0
7:6		Reserved, ignore on read, write as 0	RW	0
5:0	TIMESTAMP_ WRITE_POS	Pointer to the timestamp for the next event (96 bit word pointer) incremented by the event manager after writing	RO	0

7.5.2 Input Capture Pin Control register 7.8

The Input Capture Pin Control register is used to enable timestamping for GPIO 0 to 7 and is used to configure the edge on which it should trigger.

Bit	Name	Description	Mode	Default
15:14	IN_CAP_GPIO7	00: Disable event timestamping for GPIO7 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
13:12	IN_CAP_GPIO6	00: Disable event timestamping for GPIO6 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
11:10	IN_CAP_GPIO5	00: Disable event timestamping for GPIO5 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
9:8	IN_CAP_GPIO4	00: Disable event timestamping for GPIO4 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
7:6	IN_CAP_GPIO3	00: Disable event timestamping for GPIO3 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
5:4	Reserved	Write as 0	RW	0
3:2	Reserved	Write as 0	RW	0
1:0	IN_CAP_GPIO0	00: Disable event timestamping for GPIO0 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0

7.5.3 Input Capture Pin Control register 7.9

The Input Capture Pin Control register is used to enable timestamping GPIO 8 to 15and is used to configure the edge on which it should trigger.

Bit	Name	Description	Mode	Default
15:14	Reserved	Write as 0	RW	0
13:12	IN_CAP_GPIO14	00: Disable event timestamping for GPIO14	RW	0

		01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges		
11:10	Reserved	Write as 0	RW	0
9:8	Reserved	Write as 0	RW	0
7:6	IN_CAP_GPIO11	00: Disable event timestamping for GPIO11 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
5:4	IN_CAP_GPIO10	00: Disable event timestamping for GPIO10 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
3:2	IN_CAP_GPIO9	00: Disable event timestamping for GPIO9 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
1:0	IN_CAP_GPIO8	00: Disable event timestamping for GPIO8 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0

7.5.4 Input Capture Pin Control register 7.10

The Input Capture Pin Control register is used to enable timestamping GPIO 16 to 21 and is used to configure the edge on which it should trigger.

Bit	Name	Description	Mode	Default
15.14	Reserved	Write as 0	RW	0
13:12	Reserved	Write as 0	RW	0
11:10	Reserved	Write as 0	RW	0
9:8	Reserved	Write as 0	RW	0
7:6	IN_CAP_GPIO19	00: Disable event timestamping for GPIO19 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
5:4	Reserved	Write as 0	RW	0
3:	Reserved	Write as 0	RW	0
1:0	Reserved	Write as 0	RW	0

7.5.5 INPUT_EVENT_DATA_READ_WORD Register 7.15

The INPUT_EVENT_DATA_READ _WORD register gives access to the stored timestamps. To read the complete timestamp the register has to be accessed six times. The least significant word is read first. The location of the data is as follows:

Bit	Name	Description	Mode
95:16	TIMESTAMP	Timestamp of the related event described in bits 15:0.	RO
15:14	BUFFER_ STATUS	00: Timestamp buffer is empty 01: Next timestamp is available 10: Only two buffer for timestamp left 11: Buffer is full (immediate next read required or data will be lost)	RO
13	TIMESTAMP_ EDGE	1: Rising edge triggered the event 0: Falling edge triggered the event	RO
12:8	TIMESTAMP_ GPIO	GPIO number of the pin that triggered the event 00000: GPIO0 00001: GPIO1 00010: GPIO2 …	RO
7	TIMER_ERROR	1: Timer overflow, the event has not been processed on time and the timestamp may be broken 0: The timestamp is intact	RO
6	OVERRUN	1: An event was detected on the pin but could not be processed 0: All events were processed on time	RO
5:0	TIMESTAMP_ NUMBER	Rolling number for events on that pin	RO

As it may not be required to read the complete timestamp since the first words usually do not change very often it is possible to get a direct access to the next timestamp. In this case the INPUT_EVENT_DATA_BLOCK_READ register can be read which will always give access to the LSW of the next timestamp in memory.

To read a timestamp the INPUT_EVENT_DATA_BLOCK_READ is read first once and returns bits 15:0 of the next timestamp data. Then the INPUT_EVENT_DATA_WORD_READ is read up to 5 times and reads out bits 31:16, bits 47:32 and so on. To get bits 15:0 of the next timestamp the INPUT_EVENT_DATA_BLOCK_READ has to be read. Thus it is not required to read the complete timestamp.

7.5.6 INPUT_EVENT_DATA_BLOCK_READ Register 7.14

Bit	Name	Description	Mode	Default
15:0	TIMESTAMP_ READ_ BLOCK	Returns the least significant word (bits 15:0) of the next timestamp	RO	0

7.5.7 INPUT_CAPTURE_DATA_POINTER Register 7.13

Bit	Name	Description	Mode	Default
15		Reserved, ignore on read, write as 0	RO	0
14:8	FILLING_LEVEL	Amount of data sets in the memory 0: Event memory is empty 64: Event memory is full	RO	0
7:6		Reserved, ignore on read.	RO	0
5:0	TIMESTAMP_ READ_POS_BL OCK	Value of the read pointer to the data sets event memory. 0: Next read will read from address 0 of timestamp memory … 63: Next read will read from address 63 of timestamp memory	RO	0

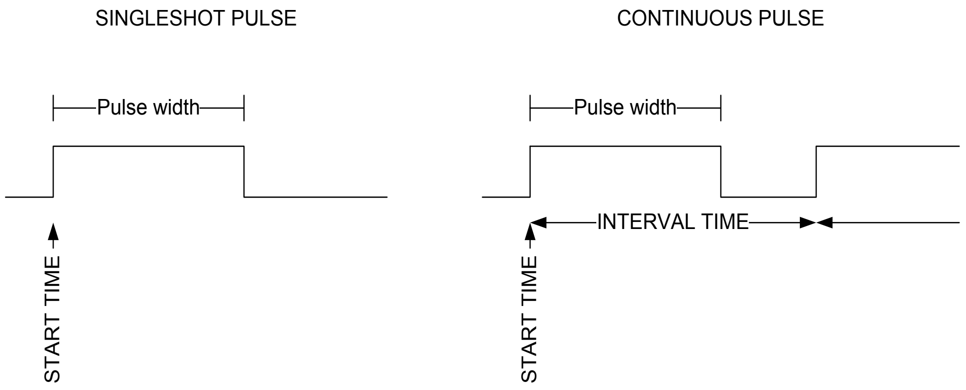
7.6 Pulse Generator Unit

The device has three pulse generator units which can generate pulses or events based on the PTP timer. Each of them can run in two different modes: single-shot or continuous pulse generation.

A pulse is triggered when the START_TIME exceeds the time from the PTP timer. Although the START_TIME has a resolution of 1/32 ns the exact output time may be up to 8 ns later as the output signal is running on the 125 MHz clock. However internally the start time is calculated with 1/32 ns accuracy so the error does not add up.

To program a new pulse generation disable the current pulse generation for the respective channel, write the values and re-enable the pulse generation by writing PULSE_GO with one and setting PULSE_CONFIG to the required value.

For continuous pulse the start times are calculated by taking the previous start time, adding the interval time, comparing the result to the timer and generating the next pulse when the timer value exceeds the start time.



There are four registers to control the pulse generators. All registers are shadow registers which can be written first and are transferred to the pulse channel in PULSE_CHANNEL at the moment the PULSE_GO bit is written with ‘1’. After writing the PULSE_CHANNEL register, these registers are updated with the actual value for this channel and can be read.

7.6.1 Pulse Output Control Register 7.16

The Pulse Output Control register controls the pulse units. All data written is stored for the channel selected in PULSE_CHANNEL.

Bit	Name	Description	Mode	Default
15:10		Reserved, write as 0, ignore on read	R/W	
9	LATCH_WIDTH	Latch newly written data from PULSE_WIDTH register and use for next pulse. This bit is typically set after the PULSE_WIDTH register has been written and when the new values should be applied. Until this is done the old value is used.	WC	0
8	LATCH_INTERVAL	Latch newly written latch interval data from the PULSE_INTERVAL register and use for next pulse. This bit is set after the PULSE_INTERVAL register has been written and the new values should be applied. Until this is done the old value is used.	WC	0
7	PULSE_GO	Latch PULSE_STARTTIME and use for next pulse. This bit is usually set after the PULSE_STARTTIME register has been written and the new values should be applied. To update the start time the pulsegen unit has to be stopped first.	WC	0
6	INT_EN	Enable interrupt for this channel An interrupt is triggered when the timer is larger than the current PULSE_STARTTIME (continuously updated according to PULSE_INTERVAL).	RW	0
5	CHANNEL_INV	Invert output of channel in 2:0	RW	0
4:3	PULSE_ CONFIG	Configuration for pulse. 00: Off 01: Single shot 10: Continuous 11: Reserved	RW	0
2:0	PULSE_ CHANNEL	000: Values in bits 9:3 and respective shadow registers PULSE_STARTTIME, PULSE_WIDTH and PULSE_INTERVAL will be written to channel 0	RW	0

		001: Values in bits 9:3 and respective shadow registers will be written to channel 1 010: Values in bits 9:3 will be written to channel 2 .		

7.6.2 PULSE_STARTTIME Register 7.17

The PULSE_STARTTIME register gives the start time for the next pulse. For continuous pulses it is incremented with the PULSE_INTERVAL value after the pulse has been triggered. The updated value can be read after writing the PULSE_CHANNEL value. Do not set the PULSE_STARTTIME to a value in the past. This register has to be accessed five times with the most significant word first.

Word	Name	Description	Mode	Default
79:0	INITIAL_PULSE_STARTTIME	Initial start time for pulse. 79:32 Seconds 31:0: Nanoseconds	WO	0

7.6.3 PULSE_WIDTH Register 7.18

This register has to be accessed three times in a row with the most significant word first.

Bit	Name	Description	Mode	Default
47:38	Reserved	Write as 0.	RW	0
34:5	PULSE_ WIDTH_NS	Pulse high width nanoseconds for single and continuous pulse. The shortest pulse width value is 24 ns.	RW	0
4:0	PULSE_ WIDTH_FNS	Pulse high width fractions of nanoseconds for single and continuous pulse. The shortest pulse width value is 24 ns.	RW	0

7.6.4 PULSE_INTERVAL Register 7.19

This register has to be accessed three times in a row with the most significant word first.

Bit	Name	Description	Mode	Default
47:35	Reserved	Write as 0	WO	0
34:5	PULSE_ INTERVAL_NS	Pulse interval nanoseconds after which the next pulse is generated (only for continuous pulse). The maximum value is 999,999,999ns or hex3B9AC9FF The shortest pulse interval value is 24 ns.	WO	0
4:0	PULSE_ INTERVAL_FNS	Pulse interval fractions of nanoseconds after which the next pulse is generated (only for continuous pulse). The shortest pulse interval value is 24 ns.	WO	0

Electrical Characteristics

8.1 AC Timing

8.1.1 Serial Management Interface (SMI) Timing

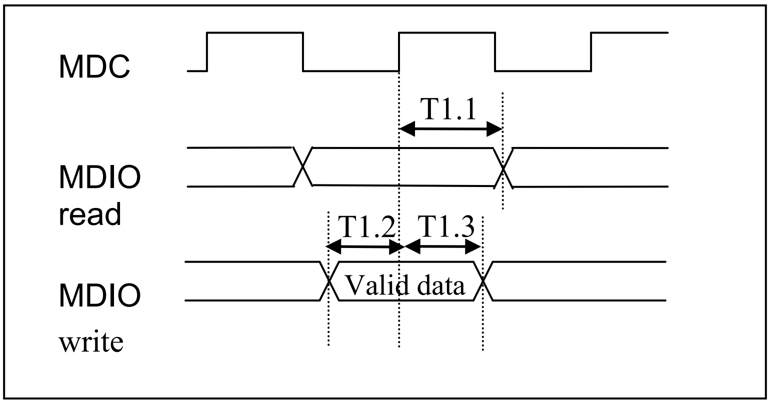


Figure 1: SMI Timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T1.1	MDC to MDIO delay	0		15	ns	Data output from PHY
T1.2	MDC to MDIO setup	10			ns	
T1.3	MDC to MDIO hold	10			ns	
	MDC frequency			25	MHz	

8.1.2 Reset Timing

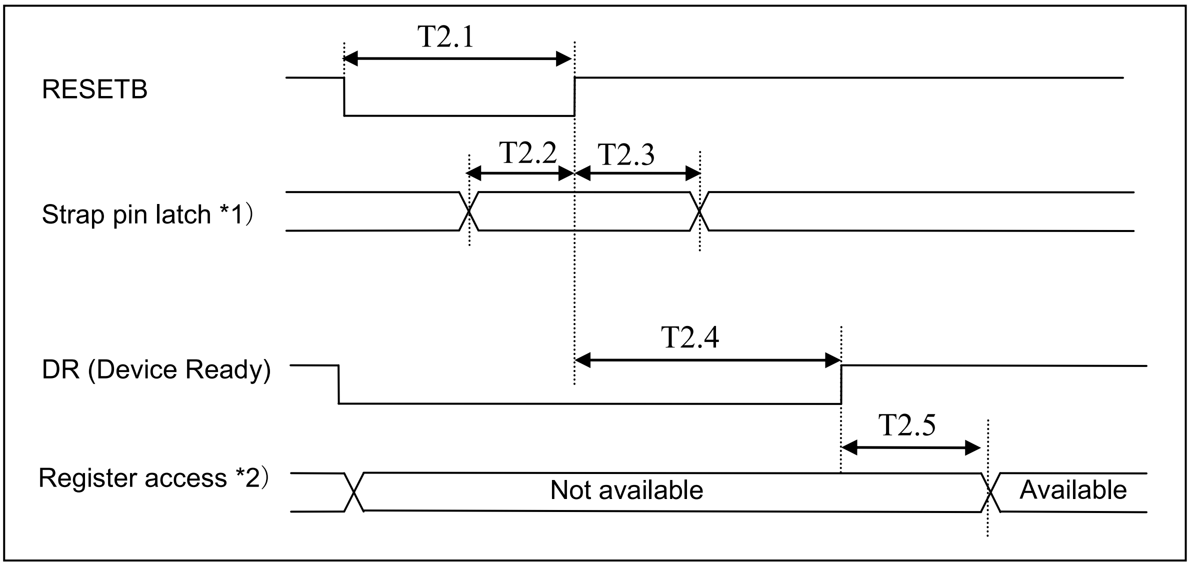


Figure 2: Reset Timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T2.1	RESETB pulse width	100			us	
T2.2	Strap input setup to RESETB rising	200			ns	
T2.3	Strap input hold after RESETB rising	400			ns	
T2.4	Device Ready rising after RESETB rising		600		us	
T2.5	Register access available after Device Ready rising			5	ms	

*1) Strap options are latched. (Refer to 4.9 Strap Options)
*2) PHY register access through SMI is available T2.5 after Device Ready rising

8.1.3 Clock Timing

Para-meter	Description	Min	Typ	Max	Units	Notes
	Reference clock frequency (25MHz / 50 MHz selectable)		25		MHz	MII
			50		MHz	RMII
	Clock frequency tolerance	-100		100	ppm	
	Duty cycle	40	50	60	%	
	Jitter tolerance		20		ps (rms)*1)	

*1) Root Mean Square

8.1.4 100Base-TX Timings

8.1.4.1 100M MII Receive Timing

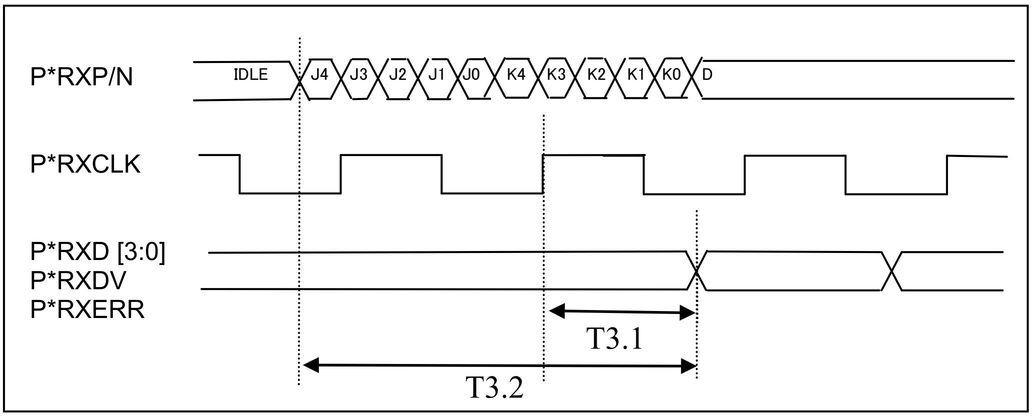


Figure 3: 100BT MII receive timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T3.1	Received signals output delay after rising edge of P*RXCLK ***1)**	15		28	ns	
T3.2	Start of RX-bit to P*RXDV valid		170		ns	RX_DV_J2T (Register0.31.1) set
			210		ns	RX_DV_J2T (Register0.31.1) cleared
	P*RXCLK frequency		25		MHz	
	P*RXCLK duty-cycle	45	50	55	%	

*1) Note that glitch may occur on output signals between min and max value of T3.1 after rising edge of P*RXCLK. However, it is compliant with IEEE802.3 standard because the setup time at the input of MAC is 13ns (=Period 40ns - max value > 10ns) and the hold time is 15ns (= min value > 10ns).

8.1.4.2 100M MII Transmit Timing

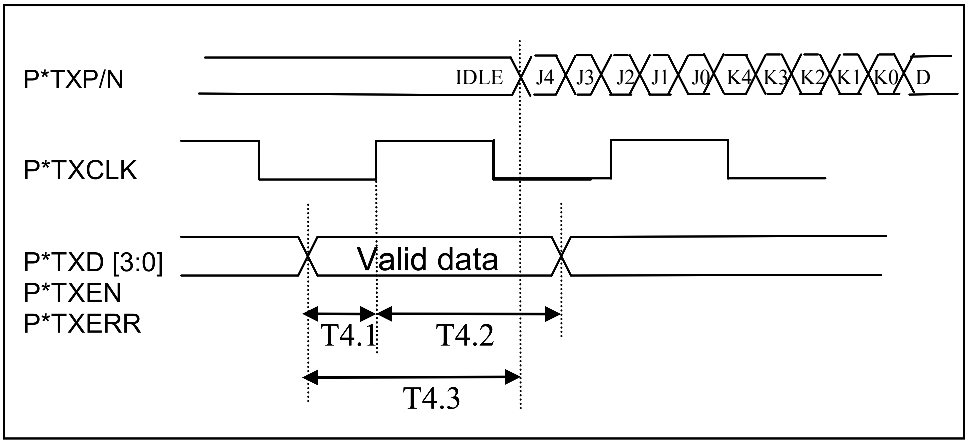


Figure 4: 100BT MII Transmit Timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T4.1	Transmit signals setup to rising edge of P*TXCLK	14			ns	
T4.2	Transmit signals hold to rising edge of P*TXCLK			0	ns	
T4.3	P*TXD valid to start of TX-bit		50		ns	
	P*TXCLK frequency		25		MHz	
	P*TXCLK duty-cycle	45	50	55	%	

8.1.5 10Base-T Timings

8.1.5.1 10M MII Receive Timing

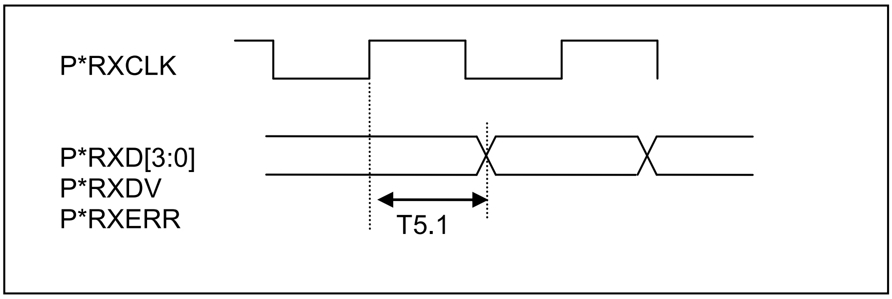


Figure 5: 10BT MII receive timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T5.1	Received signals output delay after rising edge of P*RXCLK	100		300	ns	
	P*RXCLK frequency		2.5		MHz	
	P*RXCLK duty-cycle	45	50	55	%	

8.1.5.2 10M MII Transmit Timing

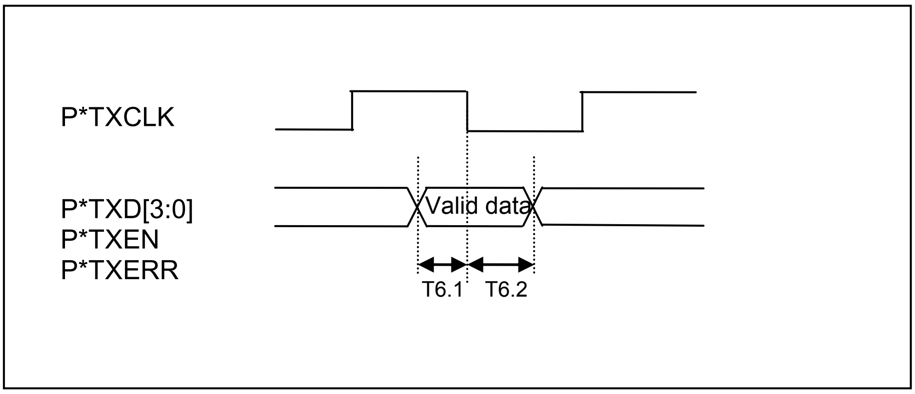


Figure 6: 10BT MII transmit timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T6.1	Transmit signals setup to falling edge of P*TXCLK	0			ns	
T6.2	Transmit signals hold to falling edge of P*TXCLK			100	ns	
	P*TXCLK frequency		2.5		MHz	
	P*TXCLK duty-cycle	45	50	55	%	

8.1.6 RMII 10/100Base-TX Timings

8.1.6.1 RMII Receive Timing

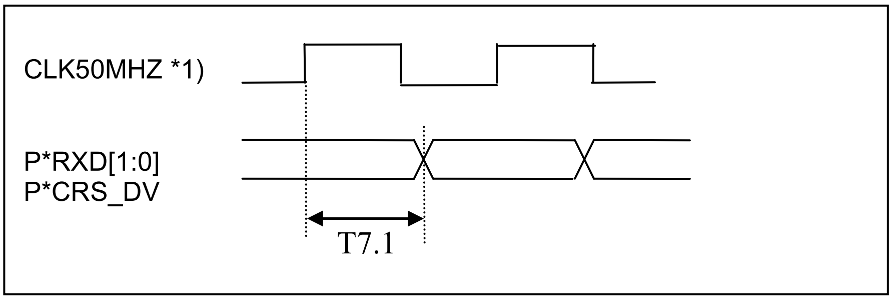


Figure 7: RMII receive timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T7.1	Receive signals output delay after rising edge of CLK50MHZ	2		14	ns	
	CLK50MHZ frequency		50		MHz	

*1) External 50MHz clock input.

8.1.6.2 RMII Transmit Timing

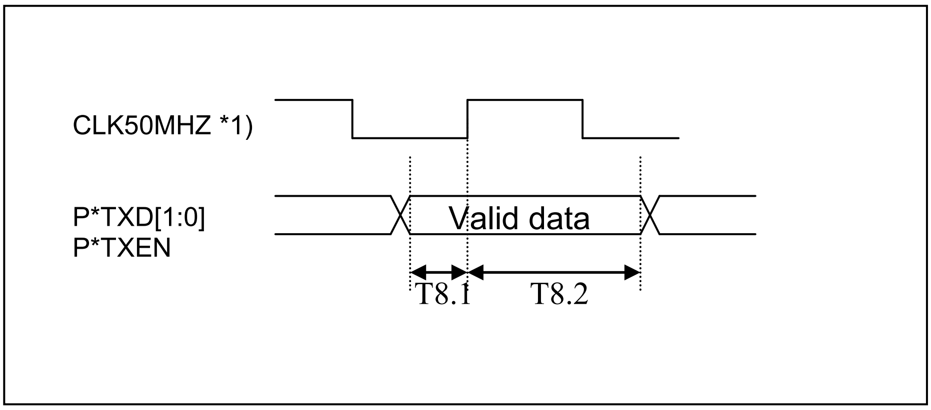


Figure 8: RMII transmit timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T8.1	Transmit signals setup to rising edge of CLK50MHZ	4			ns	
T8.2	Transmit signals hold to rising edge of CLK50MHZ	2			ns	
	CLK50MHZ frequency		50		MHz	

*1) External 50MHz clock input.

8.1.7 Sequence for turn on

RESETB must be released after all external power is ready.

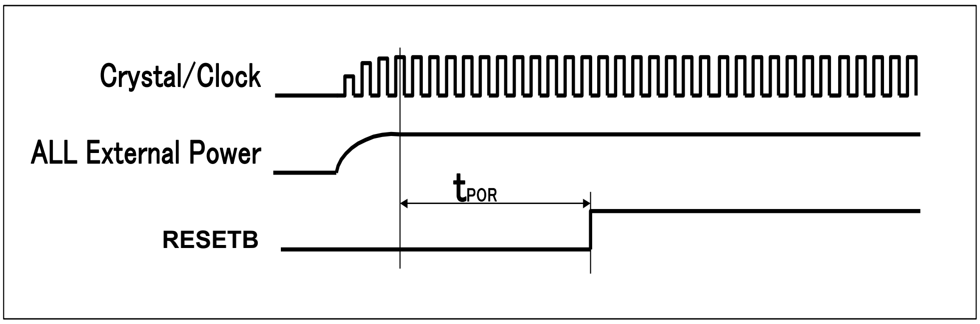


Figure 9: Reset timing

Parameter	Description	Min	Typ	Max	Units	Notes
t_{POR}	Power on Reset timing	4			ms	

8.2 DC Characteristics

8.2.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Units
Analogue power supply voltage	P1VDDMEDIA, P0VDDMEDIA, VDDAPLL		-0.5 to +2.0	V
Digital Power Supply Voltage	VDD15		-0.5 to +2.0	V
I/O Voltage	VDDIO		-0.5 to +4.6	V
Analog 3.3V power supply	VDDACB		-0.5 to 4.6	V
Analog 3.3V power supply	REGAVDD REGBVDD		-0.5 to 4.6	V
Analog 3.3V power supply	VDD33ESD		-0.5 to 4.6	V
Output Current	P0LINKLED/GPIO0P0ACTLED/GPIO1, P1LINKLED/GPIO2, P1ACTLED/GPIO3, P0100BTLED/GPIO4, P1100BTLED/GPIO5, P0TXERR/GPIO9,P0TXD3/GPIO10,P0TXD2/GPIO11,P0TXCLK,P1TXERR/GPIO15,P1TXD3/GPIO16,P1TXD2/GPIO17,P1TXCLK,MDIO0TXD1		21	mA
Output Current	P0CRS/P0CRS_DV/GPIO6, P0RXD3/GPIO7, P0RXD2/GPIO8,P0RXD1,P0RXD0,P0RXCLK, P0RXERR,P0RXDV,P1CRS/P1CRS_DV/GPIO12,P1RXD3/GPIO13,P1RXD2/GPIO14,P1RXD1,P1RXD0,P1RXCLK,P1RXERR,P1RXDV,,P0COL/GPIO18,,P1COL/GPIO19		11	mA
Storage temperature	Tstg		-65 to +150	°C

8.2.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Rating	Units
Analogue power supply voltage	P0VDDMEDIA, VDDAPLL		1.425 to 1.575	V
Digital Power Supply Voltage	VDD15		1.425 to 1.575	V
I/O Voltage	VDDIO		2.25 to 2.75 3.0 to 3.6	V
Analog 3.3V power supply	VDDACB		3.0 to 3.6	V
Analog 3.3V power supply	REGAVDD REGBVDD		3.0 to 3.6	V
Analog 3.3V power supply	VDD33ESD		3.0 to 3.6	V
Output Current	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO9,GPIO10, GPIO11,GPIO15, GPIO16,GPIO17, MDIO,P0TXCLK, P0TXEN,P0TXD1, P0TXD0,		6	mA
Output Current	GPIO6,GPIO7, GPIO8,GPIO12, GPIO13,GPIO14, MDC,P0RXCLK, P0RXERR, P0RXDV,P0RXD1, P0RXD0,		3	mA
Value for EXTRES	EXTRES		12.4±1%	kΩ
Operating ambient temperature	T_a		-40 to +85	°C

8.2.3 DC Electrical Characteristics

Parameter	Symbol	Conditions			Min	Typ	Max	Units
Current consumption	-	100B	Extnernal 1.5V supplied	3.3V		70		mA
				1.5V		110		mA
			Internal regulater used	3.3V		180		mA
				1.5V		0		mA
		10B	Extnernal 1.5V supplied	3.3V		120		mA
				1.5V		70		mA
			Internal regulater used	3.3V		170		mA
				1.5V		0		mA
Internal pull up strap resistor	R_{stru}				14.2	31.9	80.7	kΩ
Internal pull down strap resistor	R_{strd}				20.6	44.9	116.4	kΩ
Input voltage, low		VDDIO = 2.5V			0		0.7	V
Input voltage, high		VDDIO = 2.5V			1.7		VDD	V
Input voltage, low		VDDIO = 3.3V			0		0.8	V
Input voltage, high		VDDIO = 3.3V			2.0		VDD	V
Output voltage low	Vol	VDDIO=2.5V Iol=0mA					0.1	V
Output voltage high	Voh	VDDIO=2.5V Ioh=0mA			Vdd-0.1			V
Output voltage low	Vol	VDDIO=3.3V Iol=0mA					0.1	V
Output voltage high	Voh	VDDIO=3.3V Ioh=0mA			Vdd-0.1			V

8.2.4 100Base-TX Differential Parameters on Secondary Side of Transformer.

Description	Min	Typ	Max	Units	Notes
100M TX output high	.95		1.05	V	
100M TX mid-level	-50		50	mV	
100M TX output low	-.95		-1.05	V	
10M TX output high	2.2		2.8	V	

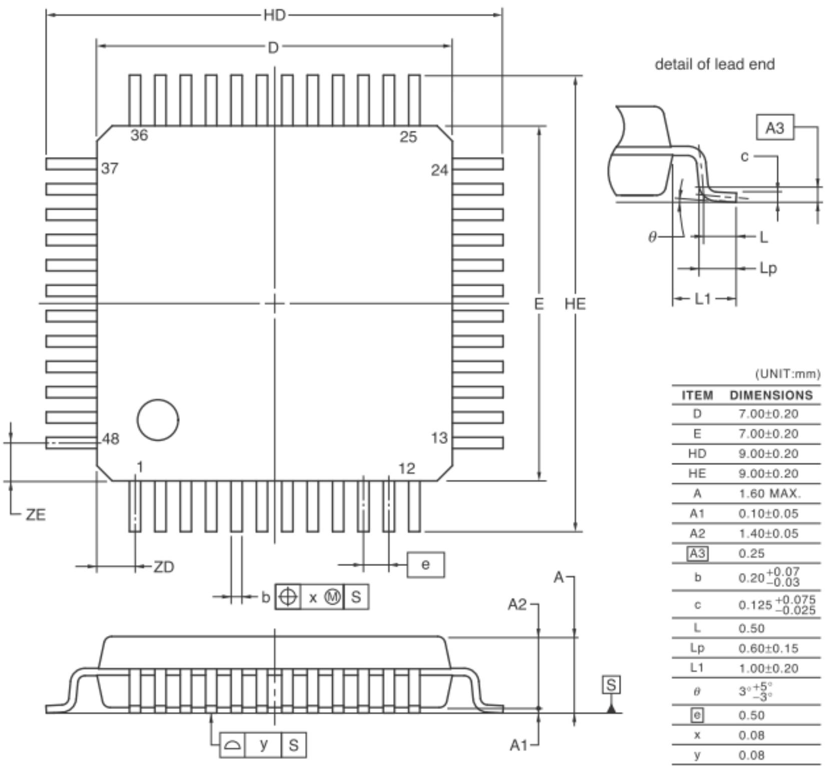
Refer to ANSI X3.263 and IEEE802.3 standard for more information.

8.2.5 100Base-FX Output Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage - Low [V] Vol-VDDIO			-1.81		-1.55	V
Output Voltage - High [V] Voh-VDDIO			-1.12		-0.88	V

Physical dimensions

48-PIN PLASTIC LQFP (FINE PITCH) (7x7)



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-GAM-1

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

Revision history

Date	Revision	Changes
April 9, 2013	2.1	Strap option register added, minor changes
March, 19 2013	2.0	Remove package other than LQFP48 Electrical characteristic updated Register description updated
Sept, 03 2012	1.1	Updated GPIO Registers, updated MII TX Timing
May 31 2011	1.0	Initial release

Industrial Ethernet PHY