sysIO Usage Guidelines for Lattice Devices

October 2005 Technical Note TN1000

Introduction

The newer Lattice device families give the user the ability to easily interface with other devices by using advanced system I/O standards. This capability is referred to as sysIO™ Standard. This application note describes the sysIO standards that are available and how they can be implemented using Lattice's design software.

Over the past several years, many factors have played heavily into the new development of I/O switching standards. The greatest factor has been the need to move signals around a board faster and with less noise. The second greatest factor has been the development of more advanced process technologies that operate at lower and lower supply voltages. To support the performance and supply voltage requirements at a system level, Lattice supports sysIO standards with its ispMACH® 5000VG, ispMACH 5000B, ispXPLD™ 5000MX, ispGDX2™ and ispXPGA™ families.

sysIO Standards

There are three classes of I/O interface standards that are implemented in Lattice's programmable devices. The first is the unterminated, single-ended interface. This group of interfaces is the most common in use today in semiconductor devices. It includes the LVTTL standard along with the 1.8V, 2.5V, and 3.3V LVCMOS interface standards. Additionally, PCI, PCIX, and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, GTL+. Usage of one of these particular I/O interfaces requires the use of an additional V_{REF} signal. At the system level a termination voltage, V_{TT}, is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The final types of interfaces implemented are the differential standards LVDS, Bus LVDS (BLVDS) and LVPECL. Table 1 lists all the sysIO standards supported for all the Lattice device families and Table 2 lists the V_{CCO}, V_{REF} and V_{TT} requirements for each of the sysIO standards supported.

Table 1. sysIO Standards Supported for the Lattice Family of Devices

sysIO Standard	ispMACH 5000VG	ispMACH 5000B	ispXPLD 5000MX	ispGDX2	ispXPGA
LVTTL	Yes	Yes	Yes	Yes	Yes
LVCMOS-3.3	Yes	Yes	Yes	Yes	Yes
LVCMOS-2.5	Yes	Yes	Yes	Yes	Yes
LVCMOS-1.8	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes
PCIX[5]	Yes	—	—	Yes	—
AGP-1X	Yes	Yes	Yes	Yes	Yes
SSTL3, Class I, II	Yes	Yes	Yes	Yes	Yes
SSTL2, Class I, II	Yes	Yes	Yes	Yes	Yes
CTT3	Yes	—	Yes	Yes	Yes
CTT2	Yes	—	Yes	Yes	Yes
HSTL, Class I	Yes	Yes	Yes	Yes	Yes
HSTL, Class III	Yes	Yes	Yes	Yes	Yes
HSTL, Class IV	—	—	Yes	Yes	—
GTL+	Yes	Yes	Yes	Yes	Yes
LVPECL	Yes[1]	Yes[1]	Yes[2]	Yes[2]	Yes[2]
LVDS	Yes[1]	Yes[1]	Yes	Yes	Yes[3]
BLVDS	—	—	—	Yes	Yes[4]

1. Only available on the CLOCK inputs.
2. Outputs require external resistor network.
3. Non-sysHSI mode outputs require external resistor network.
4. Support for outputs in non-sysHSI mode only (outputs require an external resistor network).
5. Software setting for PCIX is the same as PCI.

Table 2. sysIO Standards with the Typical Values for V_{CCO}, V_{REF} and V_{TT}

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	—	—
LVCMOS-3.3	3.3V	—	—
LVCMOS-2.5	2.5V	—	—
LVCMOS-1.8	1.8V	—	—
PCI	3.3V	—	—
PCIX	3.3V	—	—
AGP-1X	3.3V	—	—
SSTL3, Class I, II	3.3V	1.5V	1.5V
SSTL2, Class I, II	2.5V	1.25V	1.25V
CTT3	3.3V	1.5V	1.5V
CTT2	2.5V	1.5V	1.5V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
HSTL, Class IV	1.5V	0.9V	1.5V
GTL+	—	1.0V	1.5V
LVPECL	3.3V	—	—
LVDS	2.5V/3.3V[1]	—	—
BLVDS	2.5V/3.3V[1]	—	—

1. ispXPGA supports 2.5V only.

Bus Maintenance Selections

The Lattice devices supporting sysIO interfaces allow designers to choose between having a weak pull-up resistor, a weak pull-down resistor, a bus-friendly latch or nothing on every I/O and input, with the exception of TCK, TMS, TDI, TDO, and TOE. For additional information on the drive capabilities of each of the bus maintenance options, refer to the device data sheets. The TMS, TDI, TDO and TOE pins have weak pull-up circuits, while the TCK pin has nothing.

The default selection when using an unterminated I/O interface standard is a weak pull-up resistor. When using one of the terminated I/O standards on a given I/O or input pin, the software will disable bus maintenance circuitry because the terminated I/O standards will always use specific termination resistors external to the device. The same is true for clock inputs that have been paired together for differential signaling as the differential inputs are usually terminated to each other.

The V_{CC} or V_{CCO} depending on the device, sources both the pull-up resistor and the bus-friendly latch. If an input pin is configured to meet an I/O standard that has a V_{IH} greater than the source voltage of the pull-up resistor or bus-friendly latch, it is recommended that either an external pull-up resistor be used or the bus maintenance circuit be configured to be a pull-down resistor.

sysIO Options for Unterminated Interface Standards

Several additional features are available when selecting either the LVTTL or one of the LVCMOS interface standards. These features include programmable slew rate, programmable output drive strength and open drain capability.

A full description of each of the sysIO interface options is listed in the descriptions of the individual sysIO interface standards.

Programmable Slew Rate

To assist the user with noise at the system level, a programmable slew rate option has been added to every I/O pin. Signals that require high performance should use the FAST slew rate option. Care should be taken to properly terminate the signal by using a series termination resistor, so that transmission line effects and reflections do not cause problems. Signals that are not as critical should be set to SLOW slew rate. The default slew rate setting in the design software for all signals is FAST. The slew rates for the individual devices will be found in the device data sheets.

Programmable Output Drive Strength

Another method that can be used to control noise and power consumption issues is to control the output drive strength. The sink or source capability varies by the device family chosen. Refer to the appropriate Appendix for the family relevant information. Having this capability can allow for better impedance matching and improved performance for signals that are heavily loaded with capacitance. The output drive strength levels are provided in the descriptions of each of the individual sysIO interface standards and represent the minimum drive strength settings.

Open Drain I/O Configuration

All I/Os and outputs can be configured to be open-drain for use on busses that can only be driven to logic high either by another device or by using an external pull-up resistor. When an I/O is configured to be an open drain output, V_{CCO} is not required because there is no internal pull-up circuitry used, with the possible exception of the bus-maintenance circuit.

Design Guidelines for Simultaneously Switching Outputs

Anytime multiple outputs switch, ground bounce concerns must be taken into account. Ground bounce is the result of a high amount of current changing in the inductance of the ground pins, bond wires and ground plane of the device. When this happens, the voltage level of the internal ground will differ from the voltage level of the external ground, which will effectively change the level of the output signals. Additionally, the internal logic may also be affected by this phenomenon because the difference between ground and the supply voltage inside the device may be incorrect for a short period.

Lattice devices have been designed such that there is a certain maximum amount current that each bank can sink. This current varies according to the device chosen. Refer to the corresponding Appendix for detailed information. Additionally, the ground pins for each bank are independent from those in other banks to improve noise isolation due to several I/Os switching simultaneously. The voltage level difference between grounds in different banks or between a bank and the core ground should be no more than 200mV.

If the warning is generated there are a couple of simple steps that can be taken to reduce the problem. The first is to divide the higher current outputs or I/Os more evenly among the device ground pins. Doing this reduces the amount of current any single ground pin will have to sink. A second method is to use the programmable current drive option available on the unterminated sysIO standards.

Also, for signals that do not have as much capacitive loading and for signals that do not switch as fast, the current drive can be significantly reduced.

sysIO Interface Selection and Configuration

Lattice provides support for the sysIO standards through the design source files and in the Constraint Editor (CPLD) or Preference Editor (FPGA) inside the design tools. A designer can attach sysIO properties to their ABEL, VHDL or Verilog source files, which will be passed through to the fitter software. If the designer is using schematics, properties are added to the input, output and I/O ports.

sysIO Usage With ABEL

ABEL supports the sysIO standards by declaring an attribute in the ABEL source code, property for that attribute and listing the pins that are associated with that property. When using any of these attributes, the expression: `LIBRARY 'lattice';` must be included in the ABEL source file. An I/O is specified to be a specific I/O type using the expression:

```
LAT_IOTYPES (Signal_name, Type, Bank_No, Drive Current);
```

A list of the attributes and possible values for those attributes is given below in Table 3. The `OPENDRAIN` attribute, commonly used on devices that do not have the sysIO feature, will be ignored if it is used in an ABEL source file. Instead the attribute `LAT_IOTYPES` should be used with the `LVCMOS33_OD`, `LVCMOS25_OD`, or `LVCMOS18_OD` properties to implement an open-drain output or I/O. While it is possible to specify the bank, it is recommended that the software be allowed to specify this. To do this, a '-' should be used for Bank_No, otherwise Bank_No will be a value that can be obtained from the device data sheet. If a pin has been assigned to an I/O and the Bank_No conflicts with that pin assignment, the fitter will produce an error. To use the default drive strength for an I/O, a '-' should be used in the Drive_Current area. A full description of the standards and possible values for those standards is given in the descriptions of each of the sysIO standards. Bus-maintenance and output slew rate selection is achieved using the `LAT_PULL` and `LAT_SLEW` attributes, respectively.

sysIO Usage with Verilog and VHDL

Synplify® and Precision® RTL Synthesis support these sysIO standards in VHDL and in Verilog with attribute passing; much the same as pin locations, pull-ups, and slew rates are already controlled. A list of the attributes with the possible values for those attributes is shown in Table 3 below. A full description of the standards and the attributes associated with each standard is given in the descriptions of each of the sysIO standards.

Table 3. VHDL/Verilog sysIO Attributes

Attribute Name	Possible Values
IO_TYPES	LVCMOS33, LVCMOS33_OD, LVTTL, PCI, AGP_1X, LVCMOS25, LVCMOS25_OD, LVCMOS18, LVCMOS18_OD, SSTL3_I, SSTL3_II, SSTL2_I, SSTL2_II, CTT33, CTT25, HSTL_I, HSTL_III, HSTL_IV, GTL+, LVDS, BusLVDS, LVPECL
BANK_NO	0, 1, 2, 3, 4, 5, 6, 7
DRIVE	4, 5, 8, 12, 16, 20, NONE
PULL	UP, DOWN, LATCH, OFF
SLEW	FAST, SLOW

Below are examples of ABEL, VHDL and Verilog code that demonstrate usage of sysIO attributes. Additional information on constraint usage is found in the help files and usage documentation for the design software

ABEL

```
MODULE abel_io

library 'lattice';

md1..md0          pin;
Din4..Din0        pin;
Clk3..Clk0        pin;

port19..port0     pin istype 'reg';

// IO Types for input pins
LAT_IOTYPES (md0,PCI,-,-);
LAT_IOTYPES (md1,PCIX,-,-);

// IO Types for output pins
LAT_IOTYPES (port2,AGP_1X,-,-);
LAT_IOTYPES (port3,SSTL3_I,-,-);
LAT_IOTYPES (port5,SSTL2_I,-,-);
LAT_IOTYPES (port7,HSTL_I,-,-);
LAT_IOTYPES (port8,HSTL_III,-,-);
LAT_IOTYPES (port9,HSTL_IV,-,-);
LAT_IOTYPES (port10,CTT3,-,-);
LAT_IOTYPES (port11,LVTTL,-,-);
LAT_IOTYPES (port12,LVCMOS33,-,20);
LAT_IOTYPES (port13,LVCMOS33_OD,-,-);
LAT_IOTYPES (port14,LVCMOS25_OD,-,8);
LAT_IOTYPES (port15,LVCMOS18,-,5);
LAT_IOTYPES (port16,LVCMOS18_OD,-,4);
LAT_IOTYPES (port17,LVDS,-,-);
LAT_IOTYPES (port18,BLVDS,-,-);


// IO types for clock pins
LAT_IOTYPES (Clk0,LVDS,0,-);
LAT_IOTYPES (Clk2,LVPECL_D,2,-);
```

Verilog with Synplify

Syntax

```
PinType PinName /* synthesis IO_TYPES="Type, DriveCurrent" */
```

Example

```
module vlogio(md,Din,Clk0,Clk1,Clk2,Clk3,portA,portB,portC,portD,portE);

/*** IO types for Clock pins ***/
input       Clk0 /* synthesis IO_TYPES="LVDS,PIN,-,-"*/;
input       Clk2 /* synthesis IO_TYPES="LVPECL_D,PIN,-,-"*/;
input       Clk3; // will take the default type, LVCMOS33

/*** IO types for I/O pins ***/
input       [1:0] md /* synthesis IO_TYPES="PCI,PIN,-,-"*/;
input       [4:0] Din;
output [4:0] portA /* synthesis IO_TYPES="PCI,PIN,-,-"*/;
output [4:0] portB /* synthesis IO_TYPES="LVCMOS33,PIN,-,20"*/;
output [4:0] portC /* synthesis IO_TYPES="CTT33,PIN,-,-"*/;
output [4:0] portD /* synthesis IO_TYPES="LVCMOS25_OD,PIN,-,8"*/;
output[4:0] portE /* synthesis IO_TYPES="LVDS,PIN,-,- "*/;

reg         [4:0] portA;
reg         [4:0] portB;
reg         [4:0] portC;
reg         [4:0] portD;
reg         [4:0] portE;
```

Verilog with Precision® RTL Synthesis

Syntax

```
//pragma attribute PinName IO_TYPES Type, DriveCurrent;
```

Example

```
module vlogio(md,Din,Clk0,Clk1,Clk2,Clk3,portA,portB,portC,portD,portE);

input       [1:0] md;
input       [4:0] Din;
input       Clk0,Clk1,Clk2,Clk3;

output            [4:0] portA;
output            [4:0] portB;
output            [4:0] portC;
output            [4:0] portD;
output            [4:0] portE;

reg         [4:0] portA;
reg         [4:0] portB;
reg         [4:0] portC;
reg         [4:0] portD;
reg         [4:0] portE;


/*** IO types for I/O pins ***/
//pragma attribute md IO_TYPES PCI,PIN,-,-;
//pragma attribute portA IO_TYPES PCI,PIN,-,-;
//pragma attribute portB IO_TYPES LVCMOS33,PIN,-,20;
//pragma attribute portC IO_TYPES CTT33,PIN,-,-;
//pragma attribute portD IO_TYPES LVCMOS25_OD,PIN,-,8;
//pragma attribute portE IO_TYPES LVDS,PIN,-,-;

/*** IO types for Clock pins ***/
//pragma attribute Clk0 IO_TYPES LVDS,PIN,0,NONE;
//pragma attribute Clk2 IO_TYPES LVPECL_D,PIN,1,NONE;
```

Differential sysIO Macro Instantiation in HDLs

Differential Signaling Usage Model

Lattice devices support LVDS, BLVDS and LVPECL differential I/Os. This section discusses the software usage of these differential standards.

sysIO LVDS, BLVDS and LVPECL are implemented in two ways:

- The user can define the p-side of the differential pair in the design source, and then set the IO_TYPES attribute to LVDS, BLVDS or LVPECL. By setting the IO_TYPES attribute to one of these differential I/O types, the software will automatically define the n-side of the differential pair. Furthermore, the user can assign the IO_TYPES attribute in the Constraint Editor without modifying the design source.
- The user can also implement the LVDSIN, BLVDSIN, LVPECLIN, LVDSOUT, BLVDSOUT, LVPECLOUT, LVDSTRI, BLVDSTRI, LVPECLTRI, LVDSIO and BLVDSIO macros in the design source. By using the macro, the user has the ability to simulate and view both sides of the differential pair in the design source.

LVDS, BLVDS and LVPECL IO_TYPES Usage with HDL

Synplify and Precision RTL Synthesis support sysIO LVDS and BLVDS using attribute passing and the IO_TYPES attribute with VHDL and Verilog much the same as pin locations, pull-ups, and slew rates are already controlled. Similarly ABEL HDL passes properties to the place and route tools as they are currently used. Below are examples of how each HDL supports sysIO LVDS using the IO_TYPES attribute.

Verilog with Synplify

```
/* synthesis IO_TYPES=”LVDS,-” */;
```

Verilog with Precision RTL Synthesis

```
// pragma attribute [PinName] IO_TYPES LVDS,-;
```

VHDL

```
ATTRIBUTE IO_TYPES : string;
ATTRIBUTE IO_TYPES OF [PinName]: SIGNAL IS “LVDS,-”;
```

ABEL

```
LAT_IOTYPE([PinName1]:[PinName2]:...:[PinNameN],LVDS,-);
```

LVDS/BLVDS/LVPECL Macro Definition

Like the IO_TYPES attribute, the n-side of the macro does not have to be connected; leaving only the p-side to be simulated. Below are macro symbols of differential sysIO.

Figure 1. LVDSIN, BLVDSIN and LVPECLIN Macro Symbol

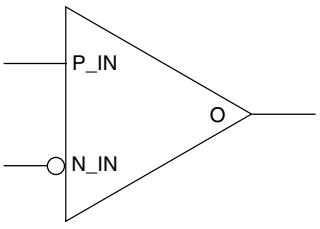


Figure 2. LVDSOUT, BLVDSOUT and LVPECLOUT Macro Symbol

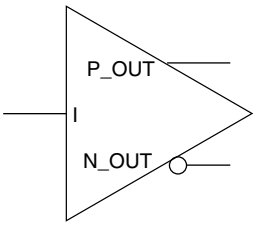


Figure 3. LVDSTRI, BLVDSTRI and LVPECLTRI Macro Symbol

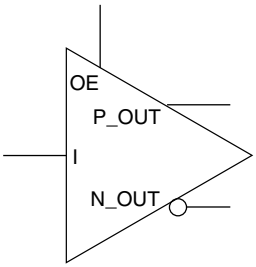
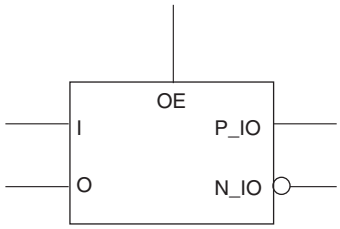


Figure 4. LVDSIO and BLVDSIO Macro Symbol



LVDS, BLVDS and LVPECL Macro Usage with HDL

Synthesis tools such as Synplify and Precision RTL Synthesis “black-box” the VHDL and Verilog instantiations and pass them through an EDIF netlist to the Lattice software. The Lattice software converts the “black-box” into the physical representation of the sysIO LVDS buffers within the device using the macros defined above.

Unlike other HDLs, ABEL requires special additions to support differential macro functionality, the Lattice design tools provide direct support for ABEL and have been modified to support differential macro functionality.

Below are VHDL, Verilog, and ABEL examples of instantiating these modules in the source code. Table 1 lists the acronyms that apply to the syntax.

Table 4. sysIO Differential I/O Acronyms

Acronym	Definition
P_IN	The p-side of the DIFFERENTIAL I/O input.
N_IN	The n-side of the DIFFERENTIAL I/O input.
O	The output of the DIFFERENTIAL I/O input or bi-directional buffer.
I	The input of the DIFFERENTIAL I/O output or bi-directional buffer.
P_OUT	The p-side of the DIFFERENTIAL I/O output.
N_OUT	The n-side of the DIFFERENTIAL I/O output.
OE	The output enable of the DIFFERENTIAL I/O output or bi-directional buffer.
P_IO	The p-side of the DIFFERENTIAL I/O bi-directional signal.
N_IO	The n-side of the DIFFERENTIAL I/O bi-directional signal.

Verilog

```
LVDSIN I1 (.P_IN(IN_P), .N_IN(IN_N), .O(NODE));
LVDSOUT I2 (.I(NODE), .P_OUT(OUT_P),.N_OUT(OUT_N));
LVDSTRI I3 (.I(NODE), .OE(OE), .P_OUT(OUT_P), .N_OUT(OUT_N));
LVDSIO I4 (.I(NODE0), .OE(OE), .O(NODE1), .P_IO(IO_P), .N_IO(IO_N));
```

VHDL

```
I1: LVDSIN
port map( P_IN => IN_P, N_IN => IN_N, O => NODE);
I2: LVDSOUT
port map( I => NODE, P_OUT => OUT_P, N_OUT => OUT_N);
I3: LVDSTRI
port map( I => NODE, P_OUT => OUT_P, OE => OE, N_OUT => OUT_N);
I4: LVDSIO
Port map(I => NODE0, OE => OE, O => NODE1, P_IO => IO_P, N_IO => IO_N);
```

ABEL

```
I1 LVDSIN(P_IN,N_IN,NODE);
I2 LVDSOUT(NODE,P_OUT,N_OUT);
I3 LVDSTRI(NODE,OE,P_OUT,N_OUT);
I4 LVDSIO(NODE0,OE,NODE1,P_IO,N_IO);
```

VHDL

Syntax

```
attribute IO_TYPES : string;

attribute IO_TYPES of PinName: signal is "Type, DriveCurrent";
```

Example

```
library ieee;
use ieee.std_logic_1164.all;

entity iovhdl is port
      (           md  : in std_logic_vector (1 downto 0);
            Din :   in std_logic_vector (4 downto 0);
            Clk0 :in std_logic;
            Clk1 :in std_logic;
            Clk2 :in std_logic;
            Clk3 :in std_logic;
            portA :out std_logic_vector (4 downto 0);
            portB :out std_logic_vector (4 downto 0);
            portC :out std_logic_vector (4 downto 0);
            portD :out std_logic_vector (4 downto 0);
portE :           out std_logic_vector (4 downto 0));


--*** Attribute declaration
ATTRIBUTE IO_TYPES: string;

--*** IO types for I/O pins ***
ATTRIBUTE IO_TYPES OF md: SIGNAL IS "PCI,PIN,-,-";
ATTRIBUTE IO_TYPES OF portA: SIGNAL IS "PCI,PIN,-,-";
ATTRIBUTE IO_TYPES OF portB: SIGNAL IS "LVCMOS33,PIN,-,20";
ATTRIBUTE IO_TYPES OF portC: SIGNAL IS "CTT33,PIN,-,-";
ATTRIBUTE IO_TYPES OF portD: SIGNAL IS "LVCMOS25_OD,PIN,-,8";
ATTRIBUTE IO_TYPES OF portE: SIGNAL IS "LVDS,PIN,-,-";


--*** IO types for Clock pins ***
ATTRIBUTE IO_TYPES OF Clk0: SIGNAL IS "LVDS,PIN,0,NONE";
ATTRIBUTE IO_TYPES OF Clk1: SIGNAL IS"LVPECL_S,PIN,1,NONE";
ATTRIBUTE IO_TYPES OF Clk2: SIGNAL IS"LVPECL_D,PIN,1,NONE";

end;
```

sysIO Usage with Schematic Capture

The sysIO standards are supported in schematics in much the same way as regular I/Os. The symbol attributes for the input, output, and I/O buffers in the generic library include three additional attributes called “IO_TYPES”, “Drive”, and “Diff_Pair”. The “IO_Standard” attribute can be set to any of the I/O standards given in Table 2. The “Diff_Pair” attribute is used for differential I/O standards. It is assigned to the p-side differential signal and set to the name of the n-side differential signal. If the “Diff_Pair” attribute is not set, the software will automatically reserve the I/O pair of the p-side differential signal and back-annotate the n-side as “signal_name_n”. The “Drive” attribute sets the drive strength of the output and bi-directional signals. The values for the “DRIVE” attribute are found in the descriptions for the standards that support this capability.

Boundary-Scan Test with sysIO interface

Boundary-scan test of a board or system is often performed before device programming to ensure proper connectivity. Device programming times are usually greater than two seconds per device and are based on the speed of the test equipment and the configuration of the programming chain. Boards with long programming chains will, naturally, take longer to program consuming precious board test time and resources. By doing the connectivity testing before programming, board test time can be minimized when an error is discovered and prevents possible contention issues as a result of the programmable devices being programmed and becoming active.

To allow for testing a board before fully programming a device, devices with the sysIO capability have also been designed with a Quick sysIO configuration capability that allows for the configuration of the I/Os without affecting the logic in the device. Only the physical nature of the I/Os is affected. This capability is provided through Lattice’s ispVM System programming software (please refer to the *ispVM System User Manual* for more information).

sysIO Banking Scheme

Each device is separated into independent groups of I/Os and inputs called banks. The number of banks is device dependent, see individual device appendix for more details. Each bank has its own resources for GND, V_{CCO} and V_{REF} and will be able to implement a subset of the supported standards, based on the V_{CCO} and V_{REF} chosen. The dedicated input and global clock pin configurations are also set based on the bank levels for V_{CCO} and V_{REF}.

I/O pins can be configured to be inputs, outputs, or bi-directional I/Os. When an I/O is configured as an input pin, its assignment to a given bank will only be a function of V_{REF}, as inputs are independent of V_{CCO}. The V_{REF} levels for the terminated sysIO standards are given in Table 1. There are no two terminated input standards that have the same V_{REF} level. As a result, only one of the terminated standards can be implemented in a given bank for inputs and I/Os. If the sysIO standard selected is one of the non-terminated interfaces, then that input can be placed in any bank.

When an I/O is configured as an output pin, its assignment to a bank is determined by the V_{CCO} of that bank. When an I/O is configured as a bi-directional I/O pin using a terminated sysIO standard, both V_{REF} and V_{CCO} are required. In this instance, other pins configured as I/Os or inputs will have to be compatible with V_{REF} and outputs will have to be compatible with V_{CCO}.

sysIO Standard Descriptions

The following are the descriptions of each of the standards that can be implemented with a Lattice sysIO Standards. The descriptions include information about the electrical characteristics of the interface standard along with the different properties that apply to the interface and acceptable values for each property. Additionally, for terminated I/O standards, circuit examples will be given to demonstrate typical termination techniques.

Any device specific information like drive strength, V_{IH}/V_{OH} values etc. are listed in the respective appendices.

LVCMOS33 (LVCMOS33_OD)

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 3.3V LVCMOS mode and the key specifications described in JEDEC Standard JESD8B

Table 5. LVCMOS33 Features List

Feature	Value[1]
External Termination Required	No
Bus Maintenance Control	**UP**, DOWN, LATCH, OFF
Slew Rate Control	SLOW or **FAST**
Drive Strength Control (I_{OH},I_{OL})	4mA, 5.33mA, 8mA, 12mA, 16mA, 20mA, 24mA
Open Drain Option	LVCMOS33_OD

1. Refer to the Appendix for device specific values. The items in bold are the default values. Refer to Appendices for default drive strength values.

Table 6. LVCMOS33 DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage	—	—	—
V_{TT}	External Termination Voltage	—	—	—
V_{OH}	Output High Voltage @ IOH	2.4	—	—
V_{OL}	Output Low Voltage @ IOL	—	—	0.4
V_{IH}	Input High Voltage	2	—	Note 1
V_{IL}	Input Low Voltage	-0.3	—	0.8

1. V_{IH} (max) value varies by device. Please refer to the appendices for device specific V_{IH} (MAX) values.

LVCMOS25 (LVCMOS25_OD)

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 2.5V LVCMOS mode and the key specifications described in JEDEC Standard JESD8-5

Table 7. LVCMOS25 Features List

Feature	Value[1]
External Termination Required	No
Bus Maintenance Control	**UP**, DOWN, LATCH, OFF
Slew Rate Control	SLOW or **FAST**
Drive Strength Control	4mA, 5.33mA, 8mA, 12mA, 16mA
Open Drain Option	LVCMOS25_OD

1. Refer to the Appendix for device specific values. The items in bold are the default values. Refer to Appendices for default drive strength values.

Table 8. LVCMOS25 DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	2.3	2.5	2.7
V_{REF}	Input Reference Voltage	—	—	—
V_{TT}	External Termination Voltage	—	—	—
V_{OH}	Output High Voltage @ I_{OH}	V_{CCO} – 0.4	—	—
V_{OL}	Output Low Voltage @ I_{OL}	—	—	0.4
V_{IH}	Input High Voltage	1.7	—	Note 1
V_{IL}	Input Low Voltage	-0.3	—	0.7

1. V_{IH} (max) value varies by device. Please refer to the appendices for device specific V_{IH} (MAX) values.

LVCMOS18 (LVCMOS18_OD)

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 1.8V LVCMOS mode and the key specifications described in JEDEC Standard JESD8-7.

Table 9. LVCMOS18 Features List

Feature	Value[1]
External Termination Required	No
Bus Maintenance Control	**UP**, DOWN, LATCH, OFF
Slew Rate Control	SLOW or **FAST**
Drive Strength Control	4mA, 5.33mA, 8mA, 12mA
Open Drain Option	LVCMOS18_OD

1. Refer to the Appendix for device specific values. The items in bold are the default values. Refer to Appendices for default drive strength values.

Table 10. LVCMOS18 DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	1.65	1.8	1.95
V_{REF}	Input Reference Voltage	—	—	—
V_{TT}	External Termination Voltage	—	—	—
V_{OH}	Output High Voltage	$V_{CCO} - 0.4$	—	—
V_{OL}	Output Low Voltage	—	—	0.4
V_{IH}	Input High Voltage	$0.65V_{CCO}$[2]	—	Note 1
V_{IL}	Input Low Voltage	-0.3	—	$0.35V_{CCO}$[2]

1. V_{IH} (max) value varies by device. Please refer to the appendices for device specific V_{IH} (MAX) values.
2. In this specification V_{CCO} refers to the V_{CCO} of the driving device. It is assumed that V_{CC} of the receiving device tracks V_{CCO}. Some devices have absolute values (eg.0.65 * 1.65=1.07 (V_{IH}) & 0.35 * 1.95 = 0.68 (V_{IL})).

LVTTL

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in LVTTL mode and the key specifications described in JEDEC Standard JESD8B.

Table 11. LVTTL Features List

Feature	Value[1]
External Termination Required	No
Bus Maintenance Control	**UP**, DOWN, LATCH, OFF
Slew Rate Control	SLOW or **FAST**
Drive Strength Control (IOH, IOL)	20mA
Open Drain Option	No

1. Refer to the Appendix for device specific values. The items in bold are the default values. Refer to Appendices for default drive strength values.

Table 12. LVTTL DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage	—	—	—
V_{TT}	External Termination Voltage	—	—	—
V_{OH}	Output High Voltage @ I_{OH}	2.4	—	—
V_{OL}	Output Low Voltage @ I_{OL}	—	—	0.4
V_{IH}	Input High Voltage	2	—	Note 1
V_{IL}	Input Low Voltage	-0.3	—	0.8

1. V_{IH} (max) value varies by device. Please refer to the appendices for device specific V_{IH} (MAX) values.

PCI

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 3.3V PCI mode and the key specifications described in the PCI Local Bus Specification, Revision 2.2.

Table 13. PCI Features List

Feature	Value
External Termination Required	No
Bus Maintenance Control	UP
Slew Rate Control	FAST
Drive Strength Control (I_{OH},I_{OL})	Set according to the PCI Specification
Open Drain Option	No

Table 14. PCI DC Characteristics

Parameter Symbol	Parameter Description	Min	Typ	Max
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage	—	—	—
V_{TT}	External Termination Voltage	—	—	—
V_{OH}	Output High Voltage @ IOH	$0.9V_{CCO}$	—	—
V_{OL}	Output Low Voltage @ IOL	—	—	$0.1V_{CCO}$
V_{IH}	Input High Voltage	$0.5V_{CCO}$[2]	—	Note 1
V_{IL}	Input Low Voltage	-0.3	—	$0.3V_{CCO}$[2]

1. V_{IH} (max) value varies by device. Please refer to the appendices for device specific V_{IH} (MAX) values
2. In this specification V_{CCO} refers to the V_{CCO} of the driving device. It is assumed that V_{CC} of the receiving device tracks V_{CCO}. Some devices use absolute values.

PCIX

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 3.3V PCIX mode and the key specifications described in the PCIX Addendum to the PCI Local Bus Specification, Revision 1.0

Table 15. PCIX Features List

Feature	Value
External Termination Required	No
Bus Maintenance Control	UP
Slew Rate Control	FAST
Drive Strength Control (IOH, IOL)	Set according to the PCIX Specification
Open Drain Option	No

Table 16. PCIX DC Characteristics

Parameter Symbol	Parameter Description	Min	Typ	Max
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage	—	—	—
V_{TT}	External Termination Voltage	—	—	—
V_{OH}	Output High Voltage @ IOH	$0.9V_{CCO}$	—	—
V_{OL}	Output Low Voltage @ IOL	—	—	$0.1V_{CCO}$
V_{IH}	Input High Voltage	$0.5V_{CCO}$[2]	—	Note 1
V_{IL}	Input Low Voltage	-0.3	—	$0.35V_{CCO}$[2]

1. V_{IH} (max) value varies by device. Please refer to the appendices for device specific V_{IH} (MAX) values device specific V_{IH} values.
2. In this specification V_{CCO} refers to the V_{CCO} of the driving device. It is assumed that V_{CC} of the receiving device tracks V_{CCO}. Some devices use absolute values.

AGP_1X

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 3.3V AGP-1X mode and the key specifications described in the Accelerated Graphics Port Interface Specification, Revision 2.0 from Intel Corporation. This specification closely mirrors the 3.3V PCI specification in many respects. The differences are in the AC drive strength and the timing specifications.

Table 17. AGP1X Features List

Feature	Value
External Termination Required	No
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control (IOH, IOL)	Set according to the AGP-1X Specification
Open Drain Option	No

Table 18. AGP1X DC Characteristics

Parameter Symbol	Parameter Description	Min	Typ	Max
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage	—	—	—
V_{TT}	External Termination Voltage	—	—	—
V_{OH}	Output High Voltage @ IOH	$0.9V_{CCO}$	—	—
V_{OL}	Output Low Voltage @ IOL	—	—	$0.1V_{CCO}$
V_{IH}	Input High Voltage	$0.5V_{CCO}$[2]	—	Note 1
V_{IL}	Input Low Voltage	-0.3	—	$0.3V_{CCO}$[2]

1. V_{IH} (max) value varies by device. Please refer to the appendices for device specific V_{IH} (MAX) values device specific VIH values.
2. In this specification V_{CCO} refers to the V_{CCO} of the driving device. It is assumed that V_{CC} of the receiving device tracks V_{CCO}. Some devices use absolute values.

SSTL3_I

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 3.3V SSTL, Class I mode and the key specifications described in JEDEC Standard JESD8-8.

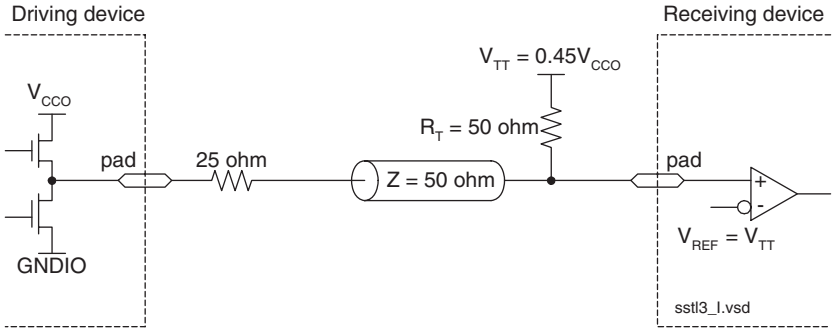
Table 19. SSTL3_I Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 20. SSTL3_I DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage $V_{REF} = 0.45V_{CCO}$	1.3	1.5	1.7
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	1.3	1.5	1.7
V_{IH}	Input High Voltage	V_{REF} + 0.2	—	V_{CCO} + 0.3
V_{IL}	Input Low Voltage	-0.3	—	V_{REF} – 0.2
V_{OH}	Output High Voltage	V_{CCO} – 1.1	—	—
V_{OL}	Output Low Voltage	—	—	0.7
I_{OH}	Output Current at V_{OH}	-8mA	—	—
I_{OL}	Output Current at V_{OL}	8mA	—	—

SSTL3_I Termination



SSTL3_II

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 3.3V SSTL, Class II mode and the key specifications described in JEDEC Standard JESD8-8.

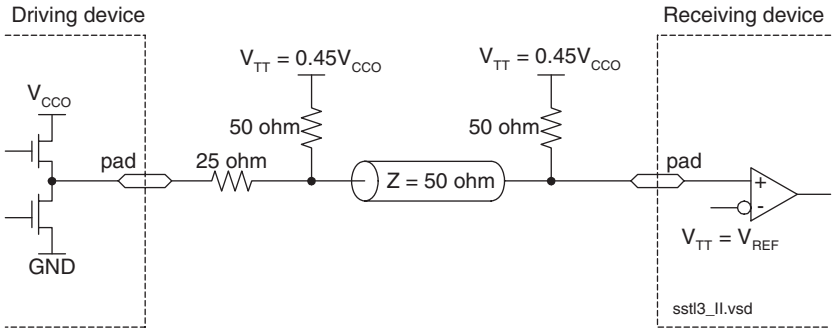
Table 21. SSTL3_II Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 22. SSTL3_II DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage $V_{REF} = 0.45V_{CCO}$	1.3	1.5	1.7
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	1.3	1.5	1.7
V_{IH}	Input High Voltage	V_{REF} + 0.2	—	V_{CCO} + 0.3
V_{IL}	Input Low Voltage	-0.3	—	V_{REF} – 0.2
V_{OH}	Output High Voltage	V_{CCO} – 0.9	—	—
V_{OL}	Output Low Voltage	—	—	0.5
I_{OH}	Output Current at V_{OH}	-16mA	—	—
I_{OL}	Output Current at V_{OL}	16mA	—	—

SSTL3_II Termination



SSTL2_I

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 2.5V SSTL Class I mode and the key specifications described in JEDEC Standard JESD8-9.

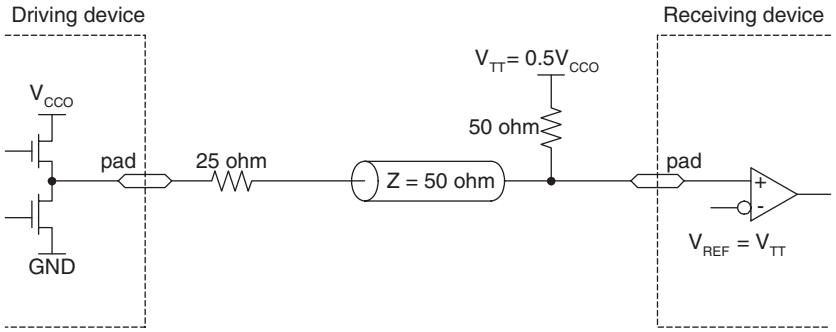
Table 23. SSTL2_I Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 24. SSTL2_I DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	2.3	2.5	2.7
V_{REF}	Input Reference Voltage $V_{REF} = 0.5V_{CCO}$	1.15	1.25	1.35
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	1.15	1.25	1.35
V_{IH}	Input High Voltage	V_{REF} + 0.18	—	V_{CCO} + 0.3
V_{IL}	Input Low Voltage	-0.3	—	V_{REF} – 0.18
V_{OH}	Output High Voltage	V_{CCO} – 0.62	—	—
V_{OL}	Output Low Voltage	—	—	0.54
I_{OH}	Output Current at V_{OH}	-7.6mA	—	—
I_{OL}	Output Current at V_{OL}	7.6mA	—	—

SSTL2_I Termination



SSTL2_II

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 2.5V SSTL, Class II mode and the key specifications described in JEDEC Standard JESD8-9.

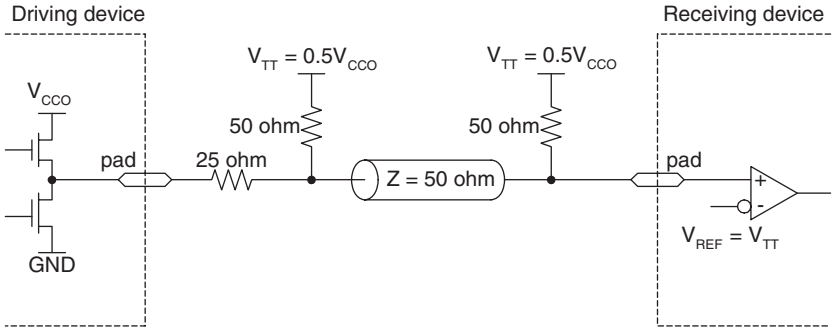
Table 25. SSTL2_II Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 26. SSTL2_II DC Characteristics

Parameter Symbol	Parameter Description	Min	Typ	Max
V_{CCO}	I/O Supply Voltage	2.3	2.5	2.7
V_{REF}	Input Reference Voltage $V_{REF} = 0.5V_{CCO}$	1.15	1.25	1.35
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	1.15	1.25	1.35
V_{IH}	Input High Voltage	V_{REF} + 0.18	—	V_{CCO} + 0.3
V_{IL}	Input Low Voltage	-0.3	—	V_{REF} – 0.18
V_{OH}	Output High Voltage	V_{CCO} – 0.43	—	—
V_{OL}	Output Low Voltage	—	—	0.35
I_{OH}	Output Current at V_{OH}	-15.2mA	—	—
I_{OL}	Output Current at V_{OL}	15.2mA	—	—

SSTL2_II Termination



CTT33

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 3.3V CTT (Center-Tap Terminated) mode and the key specifications described in JEDEC Standard JESD8-4.

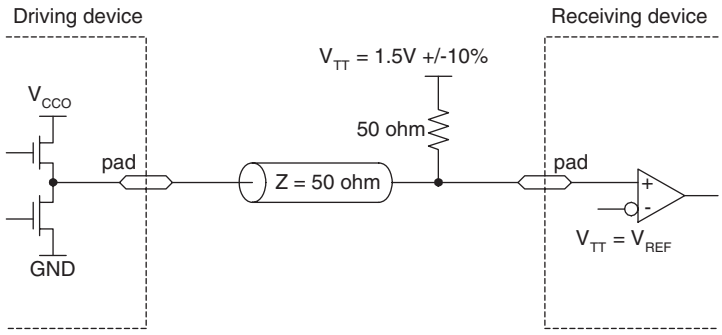
Table 27. CTT3 Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 28. CTT3 DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6
V_{REF}	Input Reference Voltage	1.3	1.5	1.7
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	1.3	1.5	1.7
V_{IH}	Input High Voltage	V_{REF} + 0.2	-	V_{CCO} + 0.3
V_{IL}	Input Low Voltage	-0.3	-	V_{REF} – 0.2
V_{OH}	Output High Voltage	V_{REF} + 0.4	-	-
V_{OL}	Output Low Voltage	-	-	V_{REF} – 0.4
I_{OH}	Output Current at V_{OH}	-8mA	-	-
I_{OL}	Output Current at V_{OL}	8mA	-	-

CTT3 Termination



CTT25

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in 2.5V CTT (Center-Tap Terminated) mode and the key specifications described in JEDEC Standard JESD8-4.

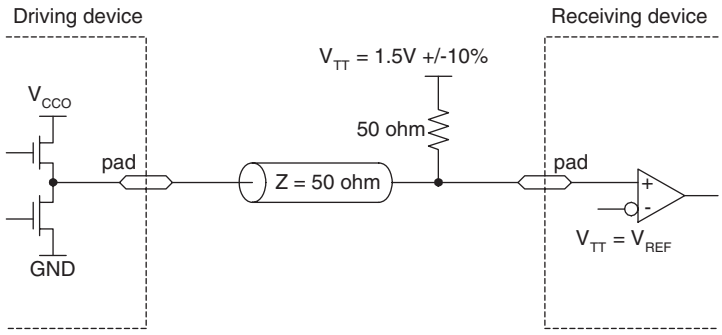
Table 29. CTT25 Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 30. CTT25 DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	2.3	2.5	2.7
V_{REF}	Input Reference Voltage	1.3	1.5	1.7
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	1.3	1.5	1.7
V_{IH}	Input High Voltage	V_{REF} + 0.2	—	V_{CCO} + 0.3
V_{IL}	Input Low Voltage	-0.3	—	V_{REF} _ 0.2
V_{OH}	Output High Voltage	V_{REF} + 0.4	—	—
V_{OL}	Output Low Voltage	—	—	V_{REF} – 0.4
I_{OH}	Output Current at V_{OH}	-8mA	—	—
I_{OL}	Output Current at V_{OL}	8mA	—	—

CTT25 Termination



HSTL_I

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in HSTL Class I mode and the key specifications described in JEDEC Standard JESD8-6.

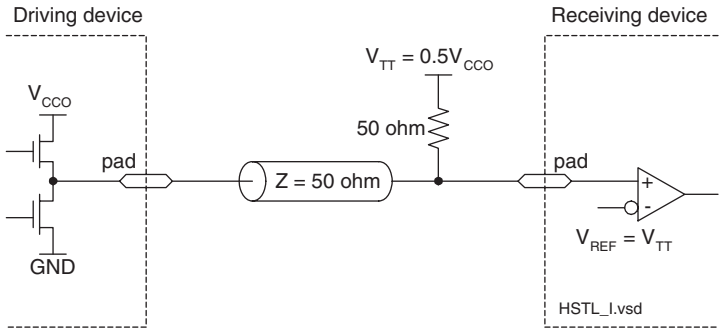
Table 31. HSTL_I Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 32. HSTL_I DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	1.4	1.5	1.6
V_{REF}	Input Reference Voltage $V_{REF} = 0.5V_{CCO}$	0.68	0.75	0.90
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	—	$0.5V_{CCO}$	—
V_{IH}	Input High Voltage	V_{REF} + 0.1	—	—
V_{IL}	Input Low Voltage	—	—	V_{REF} – 0.1
V_{OH}	Output High Voltage	V_{CCO} - 0.4	—	—
V_{OL}	Output Low Voltage	—	—	0.4
I_{OH}	Output Current at V_{OH}	-8mA	—	—
I_{OL}	Output Current at V_{OL}	8mA	—	—

HSTL_I Termination



HSTL_III

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in HSTL, Class III mode and the key specifications described in JEDEC Standard JESD8-6.

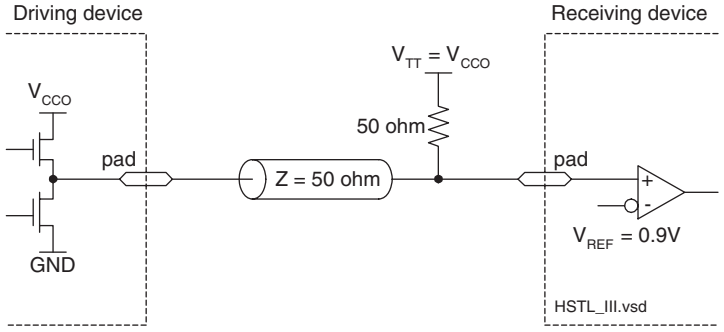
Table 33. HSTL_III Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 34. HSTL_III DC Characteristics

Parameter Symbol	Parameter Description	Min	Typ	Max
V_{CCO}	I/O Supply Voltage	1.4	1.5	1.6
V_{REF}	Input Reference Voltage $V_{REF} = 0.5V_{CCO}$	—	0.90	—
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	—	V_{CCO}	—
V_{IH}	Input High Voltage	V_{REF} + 0.1	—	—
V_{IL}	Input Low Voltage	—	—	V_{REF} – 0.1
V_{OH}	Output High Voltage	V_{CCO} - 0.4	—	—
V_{OL}	Output Low Voltage	—	—	0.4
I_{OH}	Output Current at V_{OH}	-8mA	—	—
I_{OL}	Output Current at V_{OL}	24mA	—	—

HSTL_III Termination



HSTL_IV

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in HSTL, Class IV mode and the key specifications described in JEDEC Standard JESD8-6.

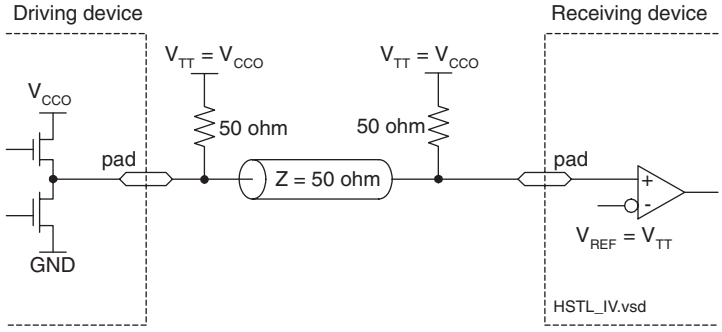
Table 35. HSTL_IV Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	No

Table 36. HSTL_IV DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	1.4	1.5	1.6
V_{REF}	Input Reference Voltage $V_{REF} = 0.5V_{CCO}$	—	0.90	—
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	—	V_{CCO}	—
V_{IH}	Input High Voltage	V_{REF} + 0.1	—	—
V_{IL}	Input Low Voltage	—	—	V_{REF} – 0.1
V_{OH}	Output High Voltage	V_{CCO} - 0.4	—	—
V_{OL}	Output Low Voltage	—	—	0.4
I_{OH}	Output Current at V_{OH}	-8mA	—	—
I_{OL}	Output Current at V_{OL}	48mA	—	—

HSTL_IV Termination



GTL+

The following tables describe the features supported by Lattice devices when the sysIO interfaces are in the GTL+ model.

Table 37. GTL+ Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	FAST
Drive Strength Control	No
Open Drain Option	Yes

Table 38. GTL+ DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.
V_{CCO}	I/O Supply Voltage	—	—	—
V_{REF}	Input Reference Voltage $V_{REF} = (2/3)V_{TT}$	—	1.0	—
V_{TT}	External Termination Voltage $V_{TT} = V_{REF}$	1.35	1.5	1.65
V_{IH}	Input High Voltage	V_{REF} + 0.2	—	—
V_{IL}	Input Low Voltage	—	—	V_{REF} – 0.2
V_{OH}	Output High Voltage	—	—	—
V_{OL}	Output Low Voltage	—	—	0.6
I_{OH}	Output Current at V_{OH}	—	—	—
I_{OL}	Output Current at V_{OL}	36mA	—	—

LVDS

The following tables describe the features supported by a Lattice device when sysIO interfaces are in LVDS mode. The LVDS interface is specified in IEEE Standard 1596.3 SCI-LVDS and ANSI/TIA/EIA-644. These specifications are electrically similar but the data transfer rates are different.

Table 39. LVDS Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	N/A
Drive Strength Control	N/A
Open Drain Option	N/A

Table 40. LVDS DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{CCO}[2]	I/O Supply Voltage	2.3	2.5	2.7	V
		3.0	3.3	3.6	V
V_{ICM}	Input Common Mode Voltage	0.2	—	1.8	V
V_{THD}	Differential Input Threshold	100	—	—	mV
V_{IN}	Input Voltage	0	—	2.4	V
V_{OH}	Output High Voltage	—	1.38	1.6	V
V_{OL}	Output Low Voltage	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between H and L	—	—	50	mV
V_{OS}	Output Voltage Offset	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	50	mV
I_{OSD}	Output Short Circuit Current	—	—	24	mA

Notes:

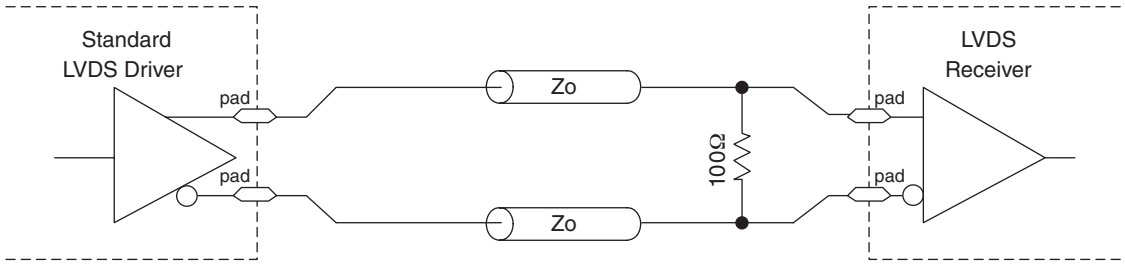
1. All the values are specified for R_T =100ohm and C_L=5pF.

2.See Table 2 for device specific capability.

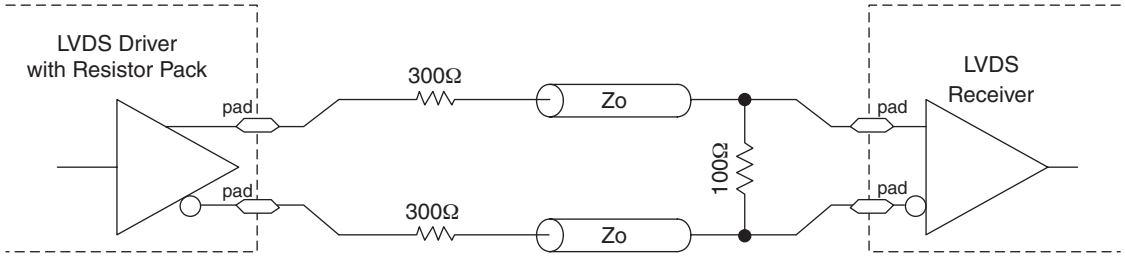
LVDS Termination

The following examples show how termination is accomplished when using the LVDS transmitter and receiver. To extract the advantages (high-speed data throughput, low EMI, power reduction) offered by LVDS, care must be taken while designing high-speed differential boards. Since the LVDS signals switch at a very fast rate (less than a nanosecond), this means almost every single interconnect will act as a transmission line.

Lattice LVDS drivers are current sourcing standard LVDS drivers. Refer to Table 1 for device specific support.



In certain devices, LVDS drivers are supported with a resistor pack as shown. Table 1 specifies the device and configuration.



A few key points to keep in mind while designing a PC board using LVDS are shown here.

- Matching the differential impedance is very important even for short interconnects. Discontinuities in differential impedance will create reflections, which will degrade the signal and show up as common-mode noise.
- Minimize skew between the conductors within a differential pair.
- Use bypass capacitors at each package and make sure that each power and ground trace is wide and short with multiple vias to minimize inductance to the power planes.
- Use multiple PCB board layers with dedicated planes for V_{CC} and Ground.
- Avoid crosstalk between CMOS/TTL signals and LVDS signals by designing the two signals on different layers of the board.

BLVDS

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in BLVDS mode. BLVDS is used in bussed multi-drop and multi-point applications over backplanes or cables. BLVDS boosts output drive current to 10mA to drive a heavily loaded bus.

Table 41. BLVDS Features List

Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	N/A
Drive Strength Control	N/A
Open Drain Option	N/A

Table 42. BLVDS DC Characteristics

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{CCO}[2]	I/O Supply Voltage	2.3	2.5	2.7	V
		3.0	3.3	3.6	V
V_{ICM}	Input Common Mode Voltage	0.2	—	1.8	V
V_{THD}	Differential Input Threshold	100	—	—	mV
V_{IN}	Input Voltage for V_{IP} or V_{IN}	0	—	2.4	V
V_{OH}	Output High Voltage for V_{OP} or V_{ON}.	—	1.4	1.8	V
V_{OL}	Output Low Voltage for V_{OP} or V_{ON}.	0.95	1.1	—	V
V_{OD}	Output Voltage Differential	240	300	460	mV
ΔV_{OD}	Change in V_{OD} between H and L	—	—	27	mV
V_{OS}	Output Voltage Offset	1.1	1.3	1.5	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	27	mV
IOSD	Output Short Circuit Current	—	36	65	mA

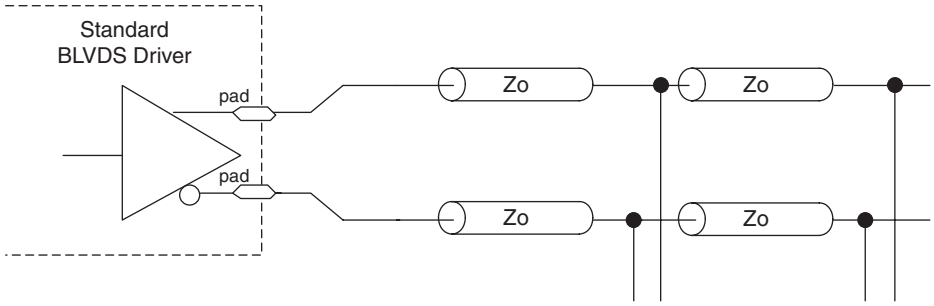
Notes:

1. All the values are specified for R_T =27ohm and C_L=10pF.
2. See Table 2 for device specific capability.

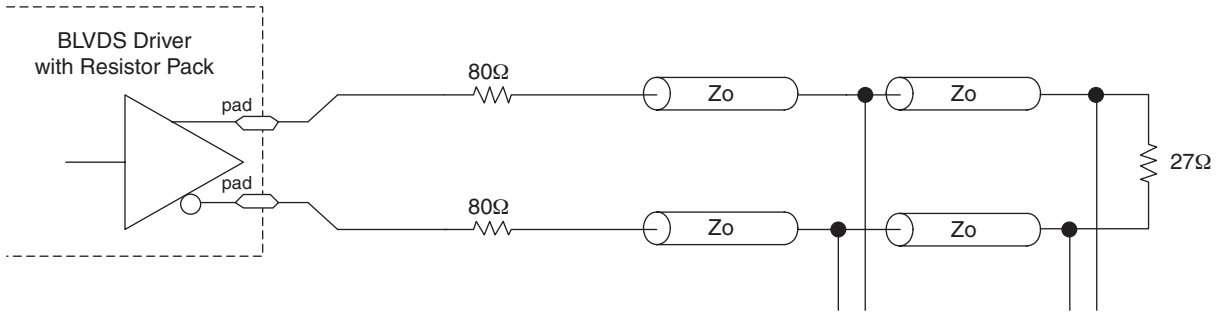
BLVDS Termination

There are two types of BLVDS drivers: the termination schemes at the driver side are similar, as in LVDS termination.

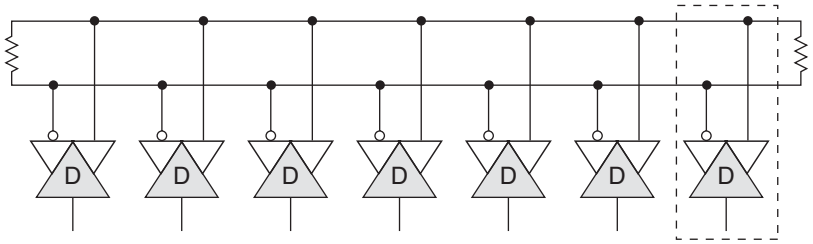
The standard BLVDS drivers are current sourcing (10mA) standard BLVDS drivers and are available for general sysIO usage or SERDES usage. See Table 1 for device specific support.



For certain devices, a resistor pack is required at the BLVDS driver side, as shown. The BLVDS drivers with resistor pack are not supported for SERDES usage. See Table 1 for device specific support.

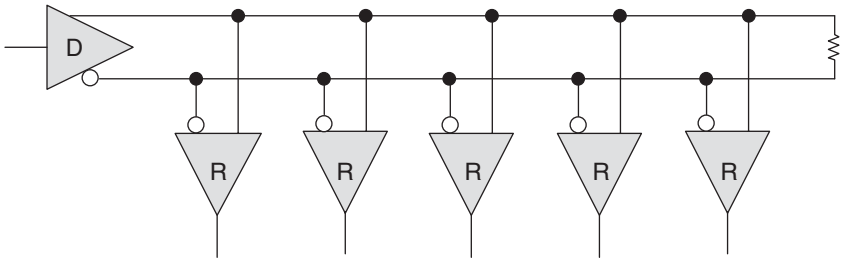


BLVDS Multi-point Application

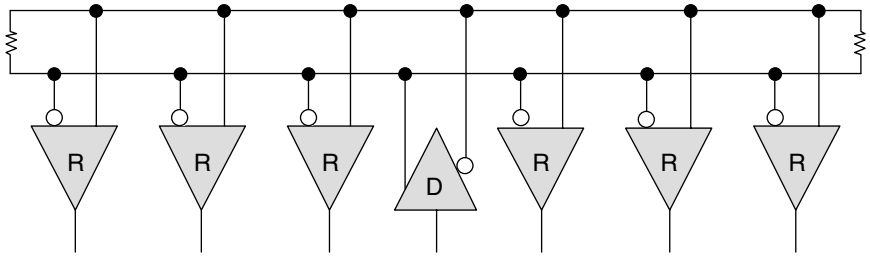


BLVDS Multi-drop Application

Single Termination



Double Termination



LVPECL

The following tables describe the features supported by a Lattice device when the sysIO interfaces are in differential LVPECL mode and the key specifications.

Table 43. LVPECL Features List

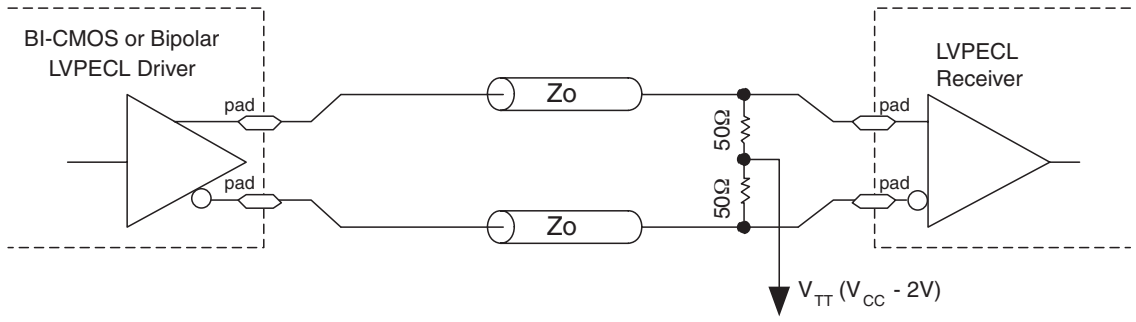
Feature	Value
External Termination Required	Yes
Bus Maintenance Control	OFF
Slew Rate Control	N/A
Drive Strength Control	N/A
Open Drain Option	N/A

Table 44. LVPECL DC Input Characteristics

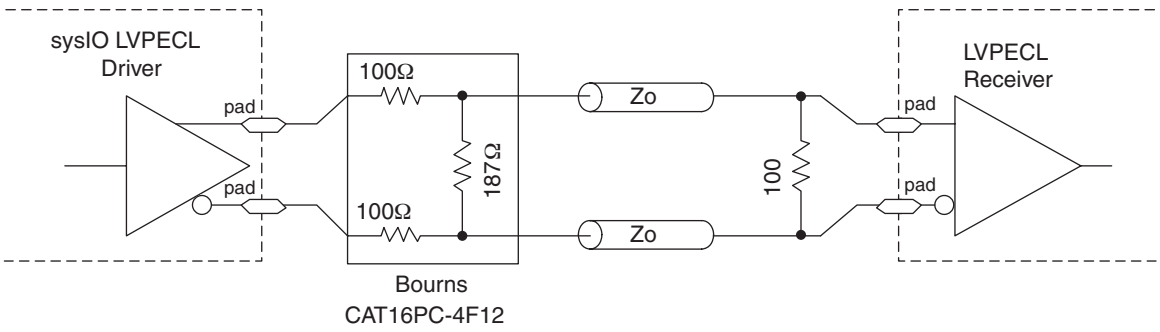
Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{CCO}	I/O Supply Voltage	3.0	3.3	3.6	V
V_{ICM}	Input Common Mode Voltage	0.2	—	1.8	V
V_{THD}	Differential Input Threshold	0.3	—	—	V
V_{OH}	Output High Voltage	1.70	—	2.41	V
V_{OL}	Output Low Voltage	0.96	—	1.57	V

LVPECL Termination

The following is an example of how termination is accomplished when using a differential LVPECL receiver. When the LVPECL driver is either bi-CMOS or bipolar in nature, the termination will be two 50Ω resistors to V_{TT} rather than a single 100Ω across the differential inputs. If V_{TT} is not available, Thevenin's equivalent circuit may be used for the termination.



Lattice LVPECL drivers require an external resistor pack. The following figure shows the interface circuit.



Appendix A ispMACH 5000VG

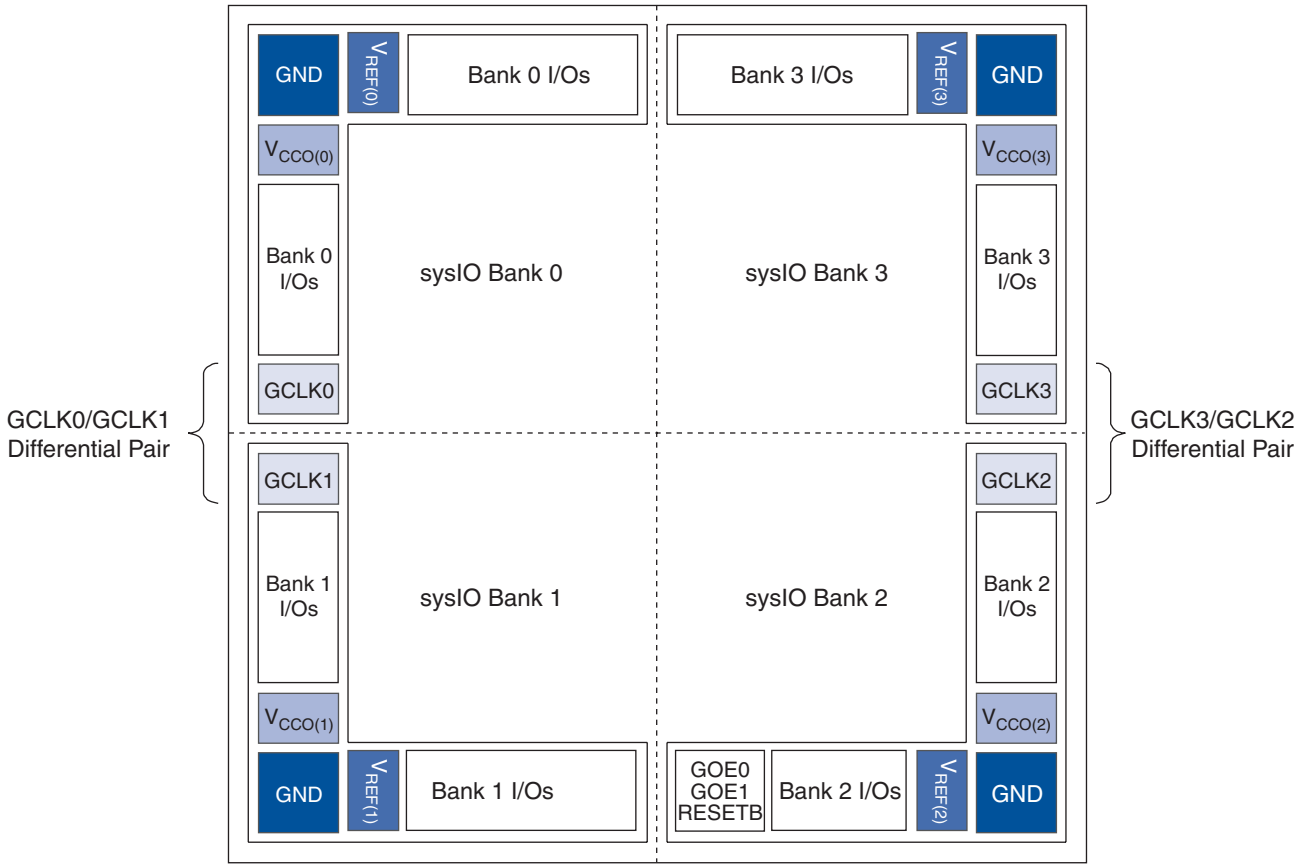
ispMACH 5000VG sysIO Banking Scheme

Each ispMACH 5000VG device is separated into four independent groups of I/Os and inputs called banks. The device has been designed such that there is a maximum of 14 sysIO standard interfaces per ground with each ground capable of sinking 96mA of current. Figure 1 shows the banking scheme for the ispMACH 5000VG family of devices.

The banks in an ispMACH 5000VG device are numbered from zero to three, as are the V_{CCO} and V_{REF} inputs for that bank. In each bank there will be a single V_{REF} pin and multiple V_{CCO} pins.

In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down or a buskeeper latch. Table 2 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

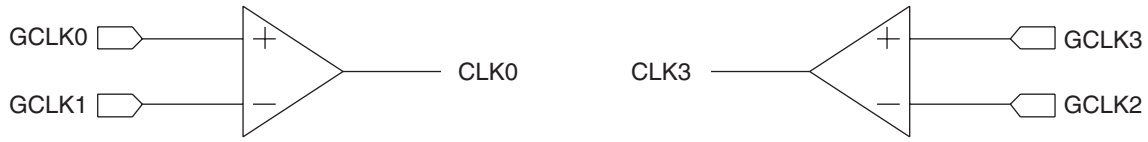
Figure 5. ispMACH 5000VG Banking Scheme



Differential Clock Inputs

As shown in Figure 1, there are two clock pins on each side of an ispMACH 5000VG device. These clock pins can be configured to meet one of the fourteen, single-ended interface standards that all of the inputs and I/Os support. Additionally, two clock pins can be paired together to interface with differential LVDS or LVPECL signals. As shown in Figure 2, when differential signaling is selected, GCLK0 or GCLK3 will be the positive input to the comparator while GCLK1 or GCLK2 will be the negative input to the comparator.

Figure 6. Clock Pairs for Differential Signaling



Each global clock input is associated with the adjacent bank of I/O cells. If a reference voltage is required for a clock input, it is obtained from the associated bank. In this way, CLK0 gets V_{REF} from bank 0, CLK1 gets V_{REF} from bank 1 and so on. This is the reason that the clock inputs are located at the bank boundaries as shown previously in figure 1. This scheme allows the clock inputs to support sysIO standards without requiring separate V_{REF} pins.

Control Pin Interfaces

The test and programming pins, TCK, TMS, TDI, TDO and TOE are independent of the banks. The TOE pin uses the core supply level $V_{CC,}$ to set the input threshold and output drive levels and is compatible to the LVCMOS 3.3 interface standard. The 1149.1 TAP pins, TCK, TMS, TDI, and TDO have their own supply pin, $V_{CCJ.}$ That supply pin must be set to be compatible with one of the three LVCMOS interface standards.

Global Output Enable Pins (GOE0, GOE1)

The global Output Enable pins support the same 14 interface standards as the user I/O pins. If an external reference voltage is required, GOE0 and GOE1 get this V_{REF} from bank 2.

Global Reset Pin

The global Reset pin supports the same 14 interface standards as the user I/O pins. If an external reference voltage is required, gets this V_{REF} from bank 2.

Device Specific sysIO Features

The two tables below lists the drive strength and the V_{IH} characteristics for the LVCMOS sysIO standards. Also, keep in mind that the internal pull-ups and buskeeper latches for the IO pins are connected to the bank V_{CCO} voltage and not the core V_{CC} for this device.

Table 45. LVCMOS Features and DC Characteristics

Standard	Drive Strength (mA)
LVCMOS33	**20**[1], 16, 12, 8, 5, 4
LVCMOS25	16, 12, **8**[1], 5, 4
LVCMOS18	12, **8**[1], 5, 4

1. Defaults are in bold.

Table 46. LVCMOS Features and DC Characteristics

Parameter	Value
LVCMOS33 - V_{IH} MAX	5.5V
LVCMOS25 - V_{IH} MAX	3.6V
LVCMOS18 - V_{IH} MAX	3.6V

Appendix B ispMACH 5000B

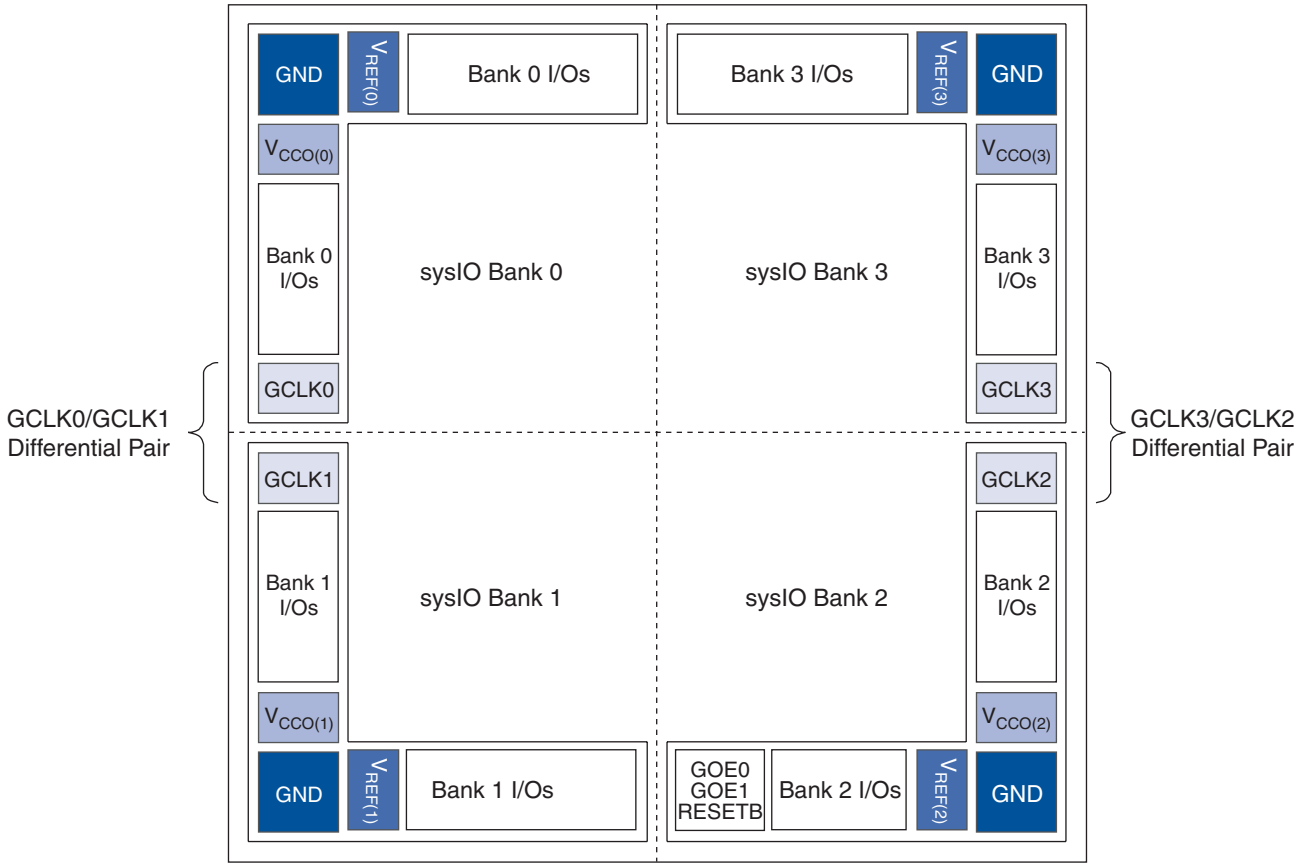
ispMACH 5000B sysIO Banking Scheme

The ispMACH 5000B devices are divided into four independent groups of I/Os and inputs called bank. The device has been designed such that there is a maximum of 14 sysIO standard interfaces per ground with each ground capable of sinking 96mA of current. Figure 3 shows the banking scheme for the ispMACH 5000B family of devices.

The banks in an ispMACH 5000B device are numbered from zero to three, as are the V_{CCO} and V_{REF} inputs for that bank. In each bank there will be a single V_{REF} pin and multiple V_{CCO} pins.

In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down or a buskeeper latch. Table 2 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

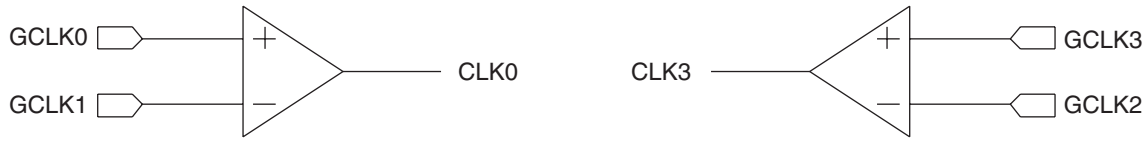
Figure 7. ispMACH 5000B Banking Scheme



Differential Clock Inputs

As shown in Figure 3, there are two clock pins on each side of an ispMACH 5000B device. These clock pins can be configured to meet one of the single-ended interface standards that all of the inputs and I/Os support. Additionally, two clock together to interface with differential LVDS or LVPECL signals. As shown in Figure 4, when differential signaling is selected, GCLK0 or GCLK3 will be the positive input to the comparator while GCLK1 or GCLK2 will be the negative input to the comparator.

Figure 8. Clock Pairs for Differential Signaling



Each global Clock input is associated with the adjacent bank of I/O cells. If a reference voltage is required for a Clock input, it is obtained from the associated bank. In this way, CLK0 gets V_{REF} from bank 0, CLK1 gets V_{REF} from bank 1 and so on. This is the reason that the Clock inputs are located at the bank boundaries as shown previously in figure 3. This scheme allows the Clock inputs to support sysIO standards without requiring separate V_{REF} pins.

Control Pin Interfaces

The test and programming pins, TCK, TMS, TDI, TDO and TOE are independent of the banks. The TOE pin uses the core supply level $V_{CC,}$ to set the input threshold and output drive levels and is compatible to the LVCMOS 3.3 interface standard. That supply pin must be set to be compatible with one of the three LVCMOS interface standards.

Global Output Enable Pins (GOE0, GOE1)

The global Output Enable pins support the same sysIO interface standards as the user I/O pins. If an external reference voltage is required, GOE0 and GOE1 get this Vref from bank 2.

Global Reset Pin

The global Reset pin supports the same sysIO interface standards as the user I/O pins. If an external reference voltage is required, gets this V_{REF} from bank 2.

Device Specific sysIO Features

The two tables below lists the drive strength and the V_{IH} characteristics for the LVCMOS sysIO standards. Also, keep in mind that the internal pull-ups and buskeeper latches for the IO pins are connected to the core V_{CC} voltage and not the bank V_{CCO} for this device.

Table 47. LVCMOS Features and DC Characteristics

Standard	Drive Strength (mA)
LVCMOS33	**20**[1], 16, 12, 8, 5, 4
LVCMOS25	16, 12, **8**[1], 5, 4
LVCMOS18	12, **8**[1], 5, 4

1. Defaults are in bold.

Table 48. LVCMOS Features and DC Characteristics

Parameter	Value
LVCMOS33 - V_{IH} MAX	3.6V
LVCMOS25 - V_{IH} MAX	3.6V
LVCMOS18 - V_{IH} MAX	3.6V

Appendix C. ispXPLD 5000MX

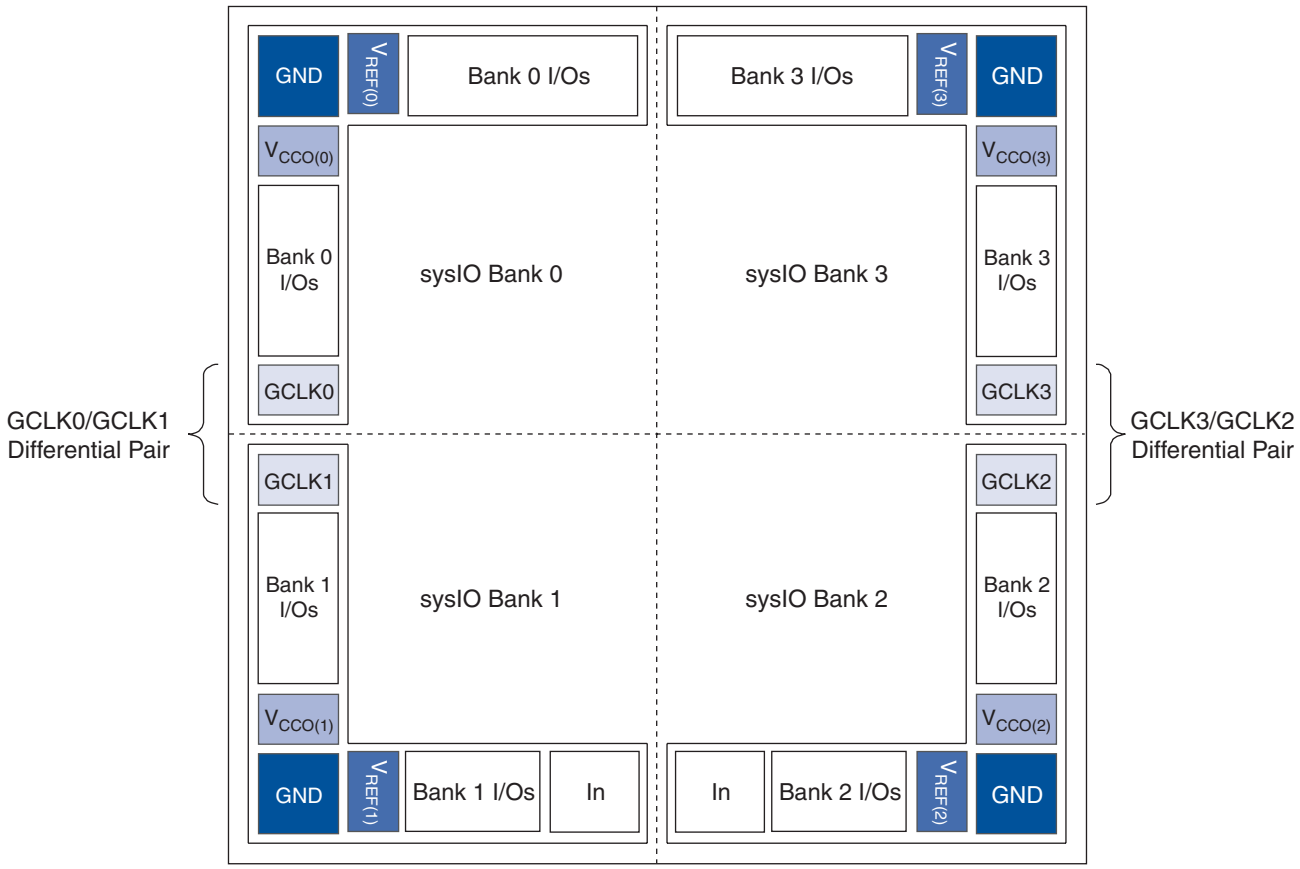
5000MX sysIO Banking Scheme

Each ispXPLD 5000MX device is separated into four independent groups of I/Os and inputs called banks. The device has been designed such that there is a maximum of 12 sysIO standards per ground. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank. Figure 9 shows the banking scheme for the ispXPLD family of devices.

The banks in the ispXPLD 5000MX device are numbered from zero to three, as are the V_{CCO} and V_{REF} inputs for that bank. In each bank there will be a single V_{REF} pin and multiple V_{CCO} pins.

In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down or a buskeeper latch. Table 2 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

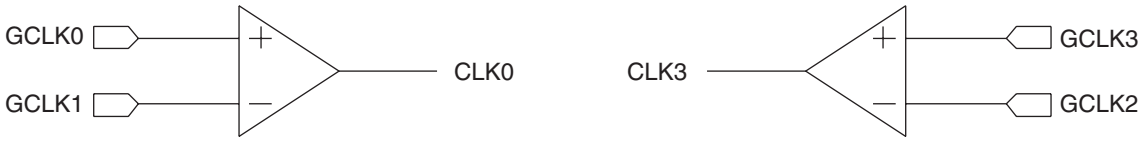
Figure 9. ispXPLD 5000MX Banking Scheme



Differential Clock Inputs

As shown in Figure 9, there are two clock pins (one for each PLL) on each side of the ispXPLD 5000MX device. These clock pins can be configured to meet one of the single-ended interface standards that all of the inputs and I/Os. Additionally two clock pins can be paired together to interface with differential LVDS or LVPECL signals. As shown in Figure 10, when differential signaling is selected, GCLK0 or GCLK3 will be the positive input to the comparator while GCLK1 or GCLK2 will be the negative input to the comparator.

Figure 10. Clock Pairs for Differential Signaling



Control Pin Interfaces

The test and programming pins, TCK, TMS, TDI, TDO and TOE are independent of the banks. The TOE pin uses the core supply level, $V_{CC,}$ to set the input threshold and output drive levels and will be compatible to the LVCMOS interface standard associated with that core supply level. The 1149.1 TAP pins, TCK, TMS, TDI and TDO, have their own supply pin, $V_{CCJ.}$

Global Output Enable Pins (GOE0, GOE1)

The global Output Enable pins support the same sysIO interface standards as the user I/O pins. If an external reference voltage is required, GOE0 and GOE1 get this V_{REF} from bank 2.

Global Reset Pin

The global Reset pin supports the same sysIO interface standards as the user I/O pins.

If an external reference voltage is required, gets this V_{REF} from bank 2.

Device-specific sysIO Features

The two tables below lists the drive strength and the V_{IH} characteristics for the LVCMOS sysIO standards. Also, keep in mind that the internal pull-ups and buskeeper latches for the I/O pins are connected to the bank V_{CCO} for this device.

Table 49. LVCMOS Features and DC Characteristics

Standard	Drive Strength (mA)
LVCMOS33	20, **16**[1], 12, 8, 5, 4
LVCMOS25	16, **12**[1], 8, 5, 4
LVCMOS18	12, **8**[1], 5, 4

1. Defaults are bolded.

Table 50. LVCMOS Features and DC Characteristics

Parameter	Value
LVCMOS33 - V_{IH} MAX	3.6V
LVCMOS25 - V_{IH} MAX	3.6V
LVCMOS18 - V_{IH} MAX	3.6V

Appendix D. ispXPGA

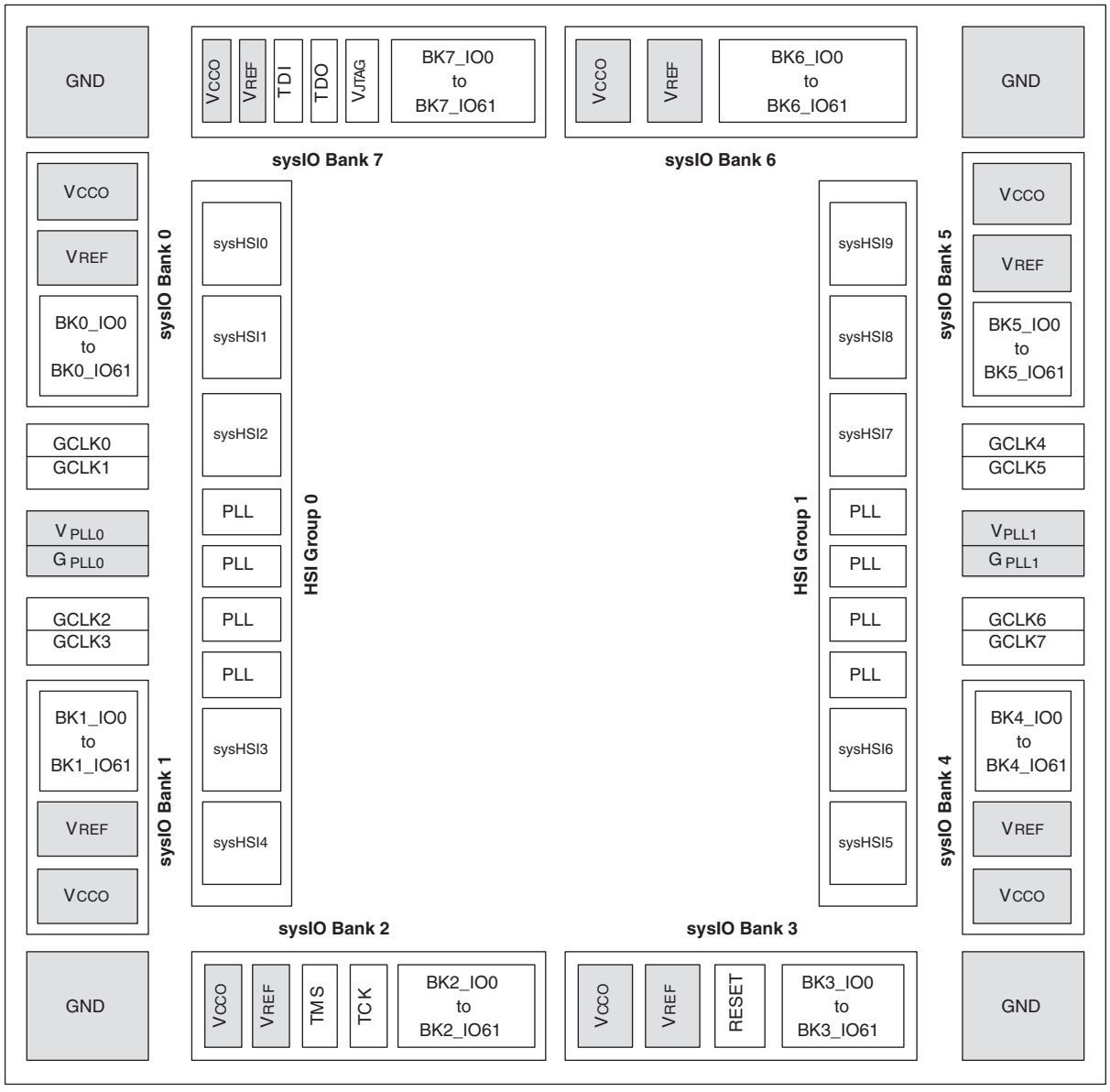
ispXPGA sysIO Banking Scheme

Each ispXPGA device is separated into eight independent groups of I/Os and inputs called banks. The device has been designed such that there is a maximum of 12 sysIO standards per ground. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank. Figure 11 shows the banking scheme for the ispXPGA family of devices.

The banks in a ispXPGA device are numbered from zero to seven, as are the V_{CCO} and V_{REF} inputs for that bank. In each bank there will be a single V_{REF} pin and multiple V_{CCO} pins.

In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down or a buskeeper latch. Table 2 lists the sysIO standards with the typical values for $V_{CCO,}$ V_{REF} and $V_{TT.}$

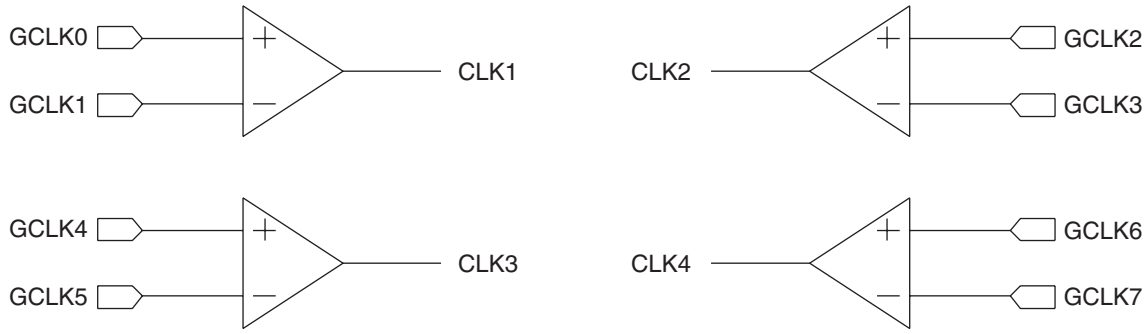
Figure 11. ispXPGA Banking Scheme



Differential Clock Inputs

As shown in Figure 11, there are four clock pins (one for each PLL) on each side of the ispXPGA device. These clock pins can be configured to meet one of single-ended interface standards that all of the inputs and I/Os. Additionally, they can be configured to interface with single-ended LVPECL signals or two clock pins can be paired together to interface with differential LVDS or LVPECL signals. As shown in Figure 12, when differential signaling is selected, GCLK0 and GCLK2 will be the positive input to the comparator while GCLK1 and GCLK3 will be the negative input to the comparator and GCLK4 and GCLK6 will be the positive input to the comparator while GCLK5 and GCLK7 will be the negative input to the comparator.

Figure 12. Clock Pairs for Differential Signaling



Control Pin Interfaces

The test and programming pins, TCK, TMS, TDI, TDO, TOE and CFG0 are independent of the banks. The TOE pin uses the core supply level, $V_{CC,}$ to set the input threshold and output drive levels and will be compatible to the LVCMOS interface standard associated with that core supply level. The 1149.1 TAP pins, TCK, TMS, TDI and TDO, have their own supply pin, $V_{CCJ.}$

Global Reset Pin

The global Reset pin supports the same sysIO interface standards as the user I/O pins. If an external reference voltage is required, gets this V_{REF} from Bank 3.

Device Specific sysIO Features

The two tables below lists the drive strength and the V_{IH} characteristics for the LVCMOS sysIO standards. Also, keep in mind that the internal pull-ups and buskeeper latches for the IO pins are connected to the bank V_{CCO} for this device.

Table 51. LVCMOS Features and DC Characteristics

Standard	Drive Strength (mA)
LVCMOS33	20, **16**[1], 12, 8, 5.33, 4
LVCMOS25	16, **12**[1], 8, 5.33, 4
LVCMOS18	12, **8**[1], 5.33, 4

1. Defaults are bolded.

Table 52. LVCMOS Features and DC Characteristics

Parameter	Value
LVCMOS33 - V_{IH} MAX	3.6V
LVCMOS25 - V_{IH} MAX	3.6V
LVCMOS18 - V_{IH} MAX	3.6V

Appendix E. ispGDX2

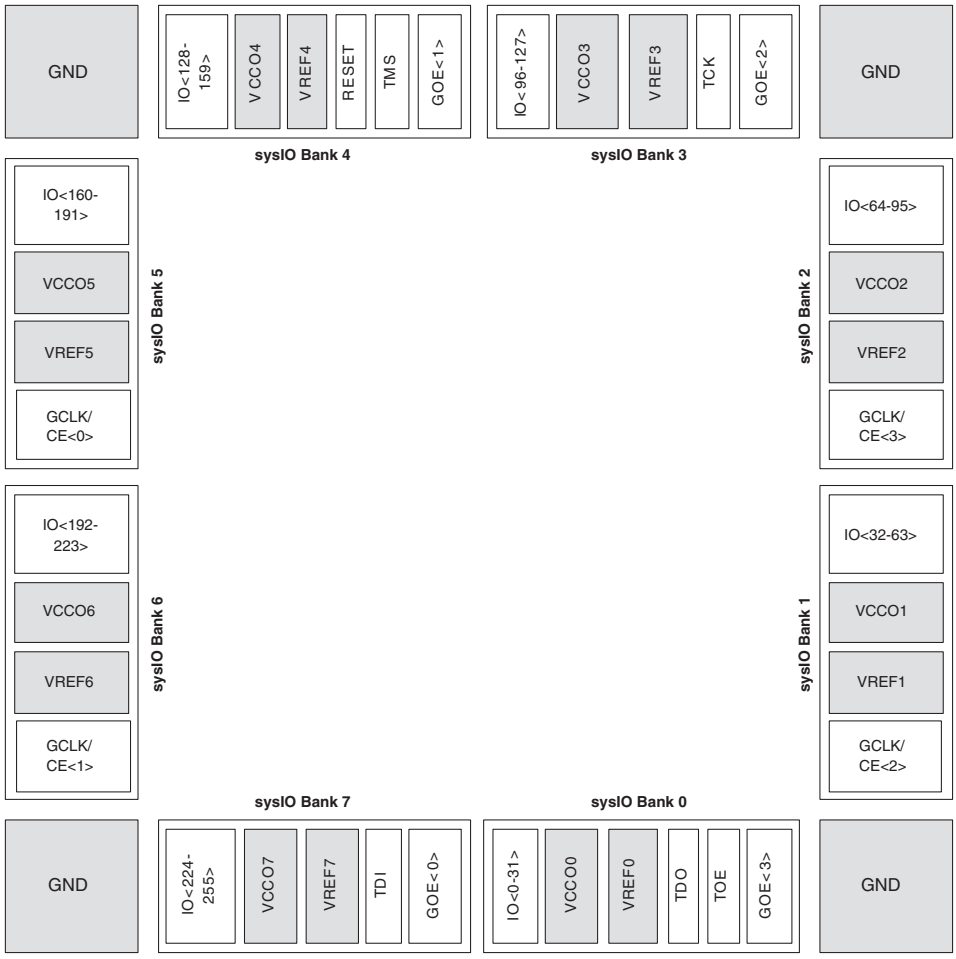
ispGDX2 sysIO Banking Scheme

Each ispGDX2 device is separated into eight independent groups of I/Os and inputs called banks. The device has been designed such that there is a maximum of eight sysIO standard interfaces per ground. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank. Figure 13 shows the banking scheme for the ispGDX2-256 family of devices.

The banks in the ispGDX2 device are numbered from zero to seven, as are the V_{CCO} and V_{REF} inputs for that bank. In each bank there will be a single V_{REF} pin and multiple V_{CCO} pins.

In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down or a buskeeper latch. Table 53 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

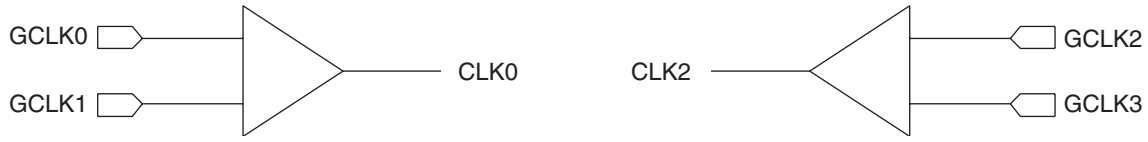
Figure 13. ispGDX2-256 Banking Scheme



Differential Clock Inputs

As shown in Figure 13, there are two clock pins on each side of an ispGDX2 device. These clock pins can be configured to meet one of the single-ended interface standards. Additionally, they can be configured to interface with differential LVDS or LVPECL signals. As shown in Figure 14, when differential signaling is selected, GCLK0 or GCLK3 will be the positive input to the comparator while GCLK1 or GCLK2 will be the negative input to the comparator

Figure 14. Clock Pairs for Differential Signaling



Control Pin Interfaces

The test and programming pins, TCK, TMS, TDI, TDO and TOE are independent of the banks. These pins are LVCMOS only and are driven by V_{CCO} pin from the adjacent bank.

The 1149.1 TAP pins - TCK, TMS, TDI and TDO have their own supply pin, $V_{CCJ.}$

Global Output Enable Pins (GOE0, GOE1, GOE2, GOE3)

The global Output Enable pins support the same sysIO interface standards as the user I/O pins. If an external reference voltage is required, GOE0 gets this V_{REF} from bank 7, GOE1 from bank 4, GOE2 from bank 3 and GOE3 from bank 0.

Global Reset Pin

The global Reset pin supports the same sysIO interface standards as the user I/O pins. If an external reference voltage is required, gets this V_{REF} from bank 4.

Device Specific sysIO Features

The two tables below list the drive strength and the V_{IH} characteristics for the LVCMOS sysIO standards. Also, keep in mind that the internal pull-ups and buskeeper latches for the IO pins are connected to the bank V_{CCO} for this device.

Table 53. LVCMOS Features and DC Characteristics

Standard	Drive Strength (mA)
LVCMOS33	20, **16**[1], 12, 8, 5, 4
LVCMOS25	16, **12**[1], 8, 5, 4
LVCMOS18	12, **8**[1], 5.33, 4

1. Defaults are bolded.

Table 54. LVCMOS Features and DC Characteristics

Parameter	Value
LVCMOS33 - V_{IH} MAX	3.6V
LVCMOS25 - V_{IH} MAX	3.6V
LVCMOS18 - V_{IH} MAX	3.6V

Appendix F: Differential sysIO Availability by Device Family

Available Macros by Differential Standard and Device

Table 55 illustrates available macros by differential standard and device when the differential I/Os are used without sysHSI Block. Table 56 illustrates macros with sysHSI Block.

Table 55. Available Macros When the Differential I/Os are Used Without sysHSI Block

	ispXPGA	ispGDX2	ispXPLD	isp5000VG/ isp5000B
LVDSIN	—	Yes	Yes	Yes[1]
LVDSOUT	—	Yes	Yes	—
LVDSTRI	—	Yes	Yes	—
LVDSIO	—	Yes	Yes	—
BLVDSIN	Yes	Yes	—	—
BLVDSOUT	Yes	Yes	—	—
BLVDSTRI	Yes	Yes	—	—
BLVDSIO	—	Yes	—	—
LVPECLIN	Yes	Yes	Yes	Yes[1]
LVPECLOUT	Yes	Yes	Yes	—
LVPECLTRI	Yes	Yes	Yes	—
LVPECLIO	—	—	—	—

1. Clock input pins only.

Table 56. Available Macros When the Differential I/Os are Used with sysHSI Block

	ispXPGA	ispGDX2
LVDSIN	Yes	Yes
LVDSOUT	Yes	Yes
LVDSTRI	Yes	Yes
LVDSIO	—	—
BLVDSIN	—	Yes
BLVDSOUT	—	Yes
BLVDSTRI	—	Yes
BLVDSIO	—	—
LVPECLIN	—	—
LVPECLOUT	—	—
LVPECLTRI	—	—
LVPECLIO	—	—

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