DPR-120 DP Reference Sink with Debug and Test Controller GUI



USER MANUAL

/// UNIGRAF

DPR-120 User Manual

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DPR-120 User Manual

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UNIGRAF DPR-120 User Manual

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1. ABOUT THIS MANUAL

Purpose

This guide is the User Manual of DPR-120 Reference Sink and DTC, Debug and Test Controller GUI for use in a PC with Windows® 8, Windows® 7 or Windows® XP operating system.

The purpose of this guide is to

- Give an overview of the product and its features.
- Give instruction for the user on how to install the software and the drivers.
- Introduce the HW features of the DPR-120 unit.
- Give instructions for the user how use the DTC GUI.

Product and Driver Version

This manual explains features found in product version **Debug and Test Controller GUI. DPR-120 DTC version 1.9.** Please consult Unigraf for differences or upgrades of previous versions.

Please consult the Release Notes document in the installation folder for details of the SW and FW versions and changes to previous releases.

Notes

On certain sections of the manual, when important information or notification is given, text is formatted as follows. Please read these notes carefully.

Note

This text is an important note

2. INTRODUCTION

Product Description

DPR-120 is a High Bit Rate 2 (HBR2) and Multi Streaming (MST) capable Reference Sink and branch device.

Debug and Test Controller GUI (DTC) is a graphical user interface for DPR-120.

Test Automation Shell and API is an optional interface for automated testing.

Product Features

No

- DP 1.2 compliant Reference Sink and Branch device
- Is able to recognize and monitor up to 4 DisplayPort Streams
- Local Sink functionality with DP 1.1 compliant monitor output
- Debug and Test Controller GUI with stream status monitoring and EDID and DPCD read write and edit functionalities.

Functionality in a Nutshell

DPR-120 is a MST and HBR2 compatible DisplayPort Reference Sink and a configurable Display Port Sink and Branch Device. The GUI allows the user to configure the features of the Sink in order to test his Source or Sink DUT in different configuration scenarios.



	e	Please note that Monitor Out port is DP 1.1a compliant. E.g. its highest resolution video mode is 2560x1600p60 (RB).
--	---	--

Note In the current release Monitor Out link is not HDCP compliant. If the monitored stream is HDCP encrypted, it will not be displayed on Monitor Out port.

SST and MST Modes

DPR-120 can operate either in Single stream (SST) mode or Multi stream (MST) mode. The selection is done with the **MST Capable** check box in *Main Link* tab in *DP Input* Group. Please find the description in Chapter 4 below.

In Single stream mode DPR-120 is seen as a single Local Sink. The local EDID and DPCD registers define its capabilities for the upstream source. The received stream for the Local sink is copied to **DP Out** port and also is the **Monitored Stream**.



In Multi stream mode, i.e. when **MST Capable** check box is selected, DPR-120 is seen as a Multi-stream capable DP Sink. The received streams are forwarded according to the intent of the Upstream Source. In the normal case one of the streams is for the *DPR-120 Local Sink* but this is not necessary the case. All four possible streams can be forwarded to downstream sinks as well.



Based on the **Stream Selection** on the *Main Link* tab in *DP Input* Group one of the input streams is selected for monitoring. The details of the streams are shown in the status fields of the Debug and Test Controller GUI and the stream is also forwarded to the *Monitor Out* port.

DPR-120 Hardware Features

The image below describes the connections and controls of DPR-120 and their description



Name	Description
DP In	DisplayPort input from the upstream Source
DP Out	DisplayPort output to the downstream Sink
Monitor Out	Copy of the DisplayPort for the local Sink
Headset Out	Analog audio output of the DP stream to the local Sink
S/PDIF In	Optical audio input.
S/PDIF Out	Optical audio output
Power In	+5 Vdc Power Supply Input
USB	USB connection to the host PC
Reset	Pushbutton to reset the unit
Status LEDs	Status 1: HDCP Status
	Status 2: Monitor Out
	Status 3: DP Out
	Status 4: DP In
	Off = Cable disconnected,
	Blinking = Cable connected but no link,
	On = Link is up
TSYNC In	Synchronizing input. TBD
TSYNC Out	Synchronizing output. TBD

3. INSTALLATION

Unpacking

The DPR-120 product shipment contains

- The DPR-120 unit
- AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +5 Vdc output)
- USB cable
- The Utilities CD containing the SW installer. An electronic copy of this User Manual is included.

Contents of the Installation CD

The DPT-120 Installation CD contains DPR-120 Setup utility including the following items:

- Windows drivers (installed during set up)
- DPT-120 firmware matching the SW version included (embedded in the GUI application, automatically updated when GUI run)
- DPR-120 Debug and Test Controller software GUI (installed during set up)
- DPR-120 Test Automation Shell (optionally installed during set up)
- User Manuals including this document.

Note:	Please install the software before connecting the DPR-120 in your PC.
Note:	System administrator's privileges are required for performing the installation.

Software Installation

Start the installation by running **DPR-120 Setup.exe**

Once the installer has started a welcome page is displayed. The welcome page shows the software package release version.

- Click Next to continue. In the next dialogs you will able to define which software components are installed.
 - A fresh version of the DPR-120 DTC Application
 - Optionally the *Device Drivers*.

The next two dialogs will allow you to define the install folder in your PC and the Start Menu folder used.

- When you are ready with the selections, click **Install** to start the installation.
- Click **Finish** to exit installation.

Firmware Update

The DPR-120 firmware matching with the DP DTC GUI SW is embedded in the GUI application code itself. When DP DTC application is launched the firmware version programmed in the hardware is automatically checked and updated if needed.

📀 Unigraf DP Debug and Test	Controller	
File Help		
	Writing Firmware: 1036304 Bytes to go	
	Cancel	
		h.

License Keys

For some feature of the DPR-120 you will need a hardware specific license key. Each license is valid for one specific device only. By using the GUI you can read the *Seed Number* of your DPR-120 unit. For a given Seed Number, Unigraf will provide you a *License Key* that will enable you to use the GUI from any PC to control your DPR-120.

You can usually find your License Key printed in a sticker that can be: glued on the unit's enclosure, included in the delivery package or among its related documents. If you cannot locate the License Key, please contact Unigraf and provide the Seed Number shown on the dialog in order to receive your License Key.

The Basic Debugging features of the DPR-120 do not require a license keys. When purchasing additional features like Compliance Test Tools and Test Automation Shell, you will be provided the license key matching the new features. The key will enable the corresponding features in the DP DTC GUI.

Insert each of the 32 character long License Keys in the field provided and click Add License. When you have inserted all licenses, click Proceed. The license keys are now saved in your PC and you can constantly use the device from this PC.

	O Unigraf DP Debug and Test Controller	
	File Help	
	Licenses installed for device DPR-120 [20WH0N94]	
	License Key	
	•mr Generic Debug < Key Not Required >	
	Remove selected Device Seed number: 704694200000	000cc
	T08C - 2VSY - F3UL - NVS2 - SDA3 - TZXL - CWDE - 5W71 + Add Lice	nse
	www.unigraf.ft	ed
		(T)1
Note	Please note that each license is bound to one specific DPR-120 unit.	The same
	license can be used with any number of PCs.	
Noto	The License Key never includes characters L.G. P. O because of the	ir similarity
Note	with the corresponding numbers. If in doubt, place use numbers V	
	with the corresponding numbers. If in doubt, please use numbers. Y	ou can use cop
	and paste to insert the License Key.	

Note

The DPR-120 must be connected to your PC for entering the License Key.

4. DEBUG AND TEST CONTROLLER GUI

Debug and Test Controller GUI (DTC) is the user interface for DPR-120. The various functionalities are divided into groups and tabs providing the user in each tab functions related a certain task or operation. Certain functions need a license and the related groups are visible only when a valid license key has been entered.

The following chapters describe the contents of the DTC and the related functions.

DP Input monitors the status and the functions related to the *DP Input* interface from the upstream Source Device. The user can monitor the streams received by DPR-120. This group is always visible and is not enabled by a license.

Terminal is a tool for running embedded DPR-120 commands.

Source DUT Testing is the group for running CTS Tests

DP Input Group

This tab has five tabs, each dedicated to certain functions.

Main Link Tab

Main Link tab contains three panels: Link Status, Link Configuration and Stream Status.

O Unigraf DP Debug and Test Controller	
File Help	
DP Input Terminal Source DUT Testing	
Main Link E-EDID MSA Log CRC Log DPCD	
Link Status	Link Configuration
Lane 0 Lane 1 Lane 2 Lane 3	Max. Lane count
Clock Recovery	1 Lane 2 Lanes 4 Lanes
Symbol lock	
Channel equalization	Max. Link rate
400 400 400 400 Voltage swing (mVpp)	1.62 Gbps 2.70 Gbps 5.40 Gbps
0x0000 0x0000 0x0000 0x0000 Error Count (Click to clear)	MST Capable
Lane count: 4 Bit rate (Chos): 5.4 (HBP2)	
Framing mode: Enhanced Scrambling: Enabled	Generate HPD pulse on Apply 🖌 Apply Changes
MST mode: Enabled	Update Link Status
Stream Status	
Monitored stream: VCP ID 0x01	Video Signal Status
Horizontal	Misc CRC
Total: 2720 Total: 1646 C	Color Encoding Format: Red CRC: 0xf7d3
Active: 2560 Active: 1600 (Color Depth per Channel: Blue CRC: 0x8265
Sync Width: (+) 32 Sync Width: (+) 6 1	
	😰 Update
De-assert HPD Pulse HPD Pulse Duration: 1000 🐺 ms	Short Pulse HPD

Link Status

Link Status displays the status of the link training and the link parameters negotiated between the DPR-120 Sink and the Upstream Source. The data is retrieved from the DPCD registers of the DPR-120 Sink and is updated automatically.

Link Configuration

Link Configuration allows the user to change the way the Sink capabilities are announced in the DPCD registers of the DPR-120 Sink. *Maximum Lane Count* and the *Maximum Link Rate* are set with the appropriate radio buttons. For enabling the *Multi Streaming* (MST) support select the **MST Capable** check-box.

To update the new status to the DPCD registers click Apply Changes.

To apply a *Hot Plug Detect* pulse automatically after updating the status, select **Generate HPD pulse on Apply**. HPD pulse duration will be defined in the *Bottom Panel*.

Stream Status

<u>Video Signal Status</u> information is retrieved from the DPR-120 Local Sink input measurement block. It indicates if valid video is received in the stream.

<u>Video Timing Details</u> are retrieved from the Main Stream Attributes (MSA) of the monitored stream. Please note that the MSA information is provided by the Source Device, it is not measured by the Sink.

The 16-bit <u>CRC</u> values of the three color components calculated by the Sink hardware. To re-read, click **Update**.

Bottom Panel

The bottom panel of the dialog is shown both in all tabs of the *DP Input* group. It includes the controls for the Hot Plug Detect (HPD) signal.

To apply a HPD Pulse with programmable duration click **Pulse HPD**. The duration will be defined in the provided field.

For applying a short pulse click Short Pulse HPD. Pulse duration is 1 ms.

Clicking the **De-assert HPD** button will cause HPD line be set to low (de-asserted) and hence no HPD pulse can be generated while HPD line set to low. Click the **Assert HPD** to re-activate the HPD line.

Total: Start: Active: Sync Width:	2720 112 2560 (+) 32	Total: Start: Active: Sync Width:	1646 43 1600 (+)6	Color Encoding Format: RGB unsp. (legacy RGB mode) Color Depth per Channel: 10	Red CRC: Green CRC: Blue CRC:	0x6be8 0xc0fa 0xe1c7
Assert HPD	-Lr Pulse	e HPD Pulse Dur	ation: 1000	🔍 ms Tr Short Pulse HPD		

E-EDID Tab

This tab provides tools for accessing the DPR-120 EDID presented to the Upstream Source Device. There are three basic functions:

- Load and save EDID data files in the host PC
- Edit the EDID contents
- Program and read the contents of the hardware EDID memory

P Input	Termina	al le	Source	DUTT	esting	,											
Ania Link	E-EDID	MCA		CRCL			-										
DID Data:	2 2010	MOA	LOG	CRC L	og L	PCD											
00000		ff f	fff	ff f	f 00	54	c7 1	36.4	0.4	~ 34	32	30	*	1r	EDID Files		
00010	14 16	01 0	4 b5	41 2	9 78	22	8f 9	95 a	d 4:	E 32	b2	2 2 5				-	1
00020	0f 50	54 f	fef	80.8	1 80	a9	40 d	i1 0	0 d:	1 40	71	4f			Load	Save as	J
00030	81 00	ъз о	0 01	01 e	2 68	00	a0 a	a0 4	0 26	e 60	30	20			HEX Editor		
00040	36 00	81 9	0 2 1	00 0	0 1e	00	00 0	00 f	e 0(0 55	5 4 e	49					
00050	47 52	41 4	6 0a	20 2	0 20	20	20 (0 00	0 0) fo	: 00	55			Clear	Append file	EDID Editor
00060	46 47	204	4 50	52 2	d 31	32	30 ()a 2	0 0	0 00	00	fd					
00070	00 31	561	d 71	1c 0	0 0a	20	20 2	20 2	0 2 (20	01	f 6					
00080	02 03	12 4	183	4f 0	0 00	29	Of 1	7f 0	7 1	5 06	5 5 5	5 3d					
00090	lf c0	00 0	0 00	00 0	0 00	00	00 0	0 00	0 0	0 00	00	00					
000a0	00 00	00 0	0 00	00 0	0 00	00	00 0	0 00	0 0	0 00	00	00					
000Ъ0	00 00	00 0	0 00	00 0	0 00	00	00 0	0 00	0 0	0 00	00	00					
000c0	00 00	00 0	0 00	00 0	0 00	00	00 0	0 00	0 0	0 00	00	00					
000d0	00 00	00 0	0 00	00 0	0 00	00	00 0	0 00	0 0(0 00	00	00					
000e0	00 00	00 0	0 00	00 0	0 00	00	00 0	0 00	0 0(0 00	00	00	Ξ				
000f0	00 00	00 0	0 00	00 0	0 00	00	00 (0 00	0 0	000	00) 8c					
															Device EDID		
															Read	Write	
													*				U Contraction of the second se
_			_		_	_	7										

EDID Files

With **Load...** and **Save as...** you can read and write a hex EDID file from your PC. Please note that the program does not alter the contents of the EDID file or verify its integrity during load and save operation.

HEX Editor

When EDID content is either loaded from a file or read from the hardware EDID memory, it is shown in the *EDID Data* panel on the left hand side of the dialog. You can edit the EDID contents by typing over the existing values. The altered content is highlighted with **RED**. Please note that Hex Editor itself does not alter the contents of the EDID data or verify its integrity.

Once you are done with editing the data, you can either save it to an *.ecd file in your PC with **Save as...** or program it to the hardware EDID memory with **Write**.



EDID Editor

You can edit the EDID structures of the data in the *HEX Editor* by clicking **EDID Editor**. EDID Editor is launched in a separate pop-up window.

Collection 1		Details of ": /0/Version/Vendor	Product ID"	
Blocks in collection		Ken	Value	
 Block 0 [VESA EDID] 		Ney	Value	
Checksum		ID Manufacturer Name	UFG	
⊿ Version		ID Product Code	0x4036	
Extension flag		ID Serial Number	0x3032344c	
Vendor & Product ID				
Basic Display Parameters and Feature Display Parameters and Feature	e	Manufacture or Model year	Manufacture Year and Week	
Display x,y Chromacity coordinates				
Established timings I and II	Ξ	Wash of manufacture	West 20	
 Standard Timings 		week of manufacture	Week 20	
4. 19-Byte data blocks		Year of manufacture	Year 2012	
 Descriptor 1 				
> Descriptor 2				
> Descriptor 3				
Descriptor 4				
4 Block 1 [CEA 861]				
Checksum				
 CEA Extensions Version 				
Sink Underscans IT video				
Basic audio				
YCbCr (4:4:4)	-			

The Main Window

The *EDID Editor* main window is divided into three logical areas. The bottom part of the window contains the command buttons, and the log view. The top-left portion shows the currently edited E-EDID blocks in a tree-form, and the top-right portion shows an edit control for the currently selected item, possibly a list of sub-keys and their names (The list is not shown for all values) and the HEX-view of the block collection.

Command Buttons

Load: Load an EDID block collection file from disk. **Save:** Save the current block collection to a disk file. **Show Hex:** Show or Hide the HEX view. **Show Log:** Show or Hide the Log view.

EDID Editor Features

The EDID Editor currently supports VESA E-EDID block versions 1.3 and 1.4. As the standard defines, the versions 1.0, 1.1 and 1.2 are supposed to be backward compatible, and therefore the VESA E-EDID decoder will also show their contents. However, in these cases it should be noted that the error checking is not compliant with restrictions given in these older versions of the standard. In addition to VESA E-EDID block, the CEA-861 versions 1, 2 and 3 EDID blocks are also fully supported as well as the VESA Block Map Extension blocks.

Practically unlimited number of extension blocks may exist in a single collection. The number of blocks is limited by VESA Specifications and possibly by available system resources. Most EDID blocks contain a structure that is very similar to a tree-structure. The EDID Editor decodes each block into a tree-view of the block. The tree-view then contains all values contained within the EDID block. The contents can then be easily browsed, using only a few mouse clicks. The EDID Editor has a support for automatic variables, such as the block checksum. When the user changes a value in an EDID block, the tool will update the checksum accordingly. The automatic variables appear as read only values for the user. A log print will be made when an automatic variable is updated by the editor.

HEX View: An optional HEX data display of all blocks in the collection. The view also shows the latest changes highlighted.

LOG View: An optional LOG view, which will contain log prints generated by the editor. Mostly it will list values that have been automatically updated due to edits.

Editing tips

Editing an EDID block is very straightforward, but there are some special cases where the user must know how to accomplish certain types of tasks.

- Enter key will apply text-edit values and combo-box selection.
- To apply new setting to *binary* values (ones that show a check-box), please click the **Set** button.
- When you see a **Quick Config** button appear below an editor, you can access a configuration menu that allows you to quickly select one of multiple pre-defined setup options.
- In CEA-861 blocks, you can add and remove 18-byte descriptors and CEA data blocks by setting the values "18-byte Descriptors in this block" and "CEA Data block count". Unfortunately re-arranging the descriptors and CEA data blocks is not supported yet, so you need to be careful when editing these.
- Enter hex values with prefix "**0**x" or "**\$**", no prefix means a decimal value.
- You can always enter HEX or DEC, even if the value is presented as HEX, and/or value range is given in HEX.
- Floating point values must be given with period "." as decimal separator, even if your localization setting defines decimal separator as comma (or other).
- Remember to click **Set** after changing a bit-value presented as a single check-box if you want the new value applied.

Note It is recommended that you back up the un-edited EDID contents to a file before editing and writing it to the card.

Saving EDID Data

When you are done with editing you can either save the EDID contents to a file in the PC or bring it in the *HEX Editor*.

For saving the data to a file in your PC click Save.

For bringing the data to the HEX Editor close the EDID Editor window by clicking the **Window Close** button in the top right hand corner of the window. You will be asked if you would like to copy and replace the EDID data in the HEX Editor. Click **Yes** to replace the data, click **No** to discard the modifications.

When you are back in the *HEX Editor*, the bytes that the *EDID Editor* changed are highlighted with **BLUE BACKGROUND**.

MSA Log Tab

MSA Log collects video status information from the stream selected In the *Main Stream* tab. The data will be stored since the DTC GUI was launched or **Clear** was clicked.

Click **Columns...** to select which data fields are shown. Please find a list of available fields and their column labels below:

Unigraf File Help	DP Debug	and Test (Controller						
DP Input	Terminal	Source	DUT Testing						
Main Link	E-EDID M	SA Log C)					
Co	lumns							Save	Clear
Timestam	VCP	ID	VSTAT	HACT	VACT	CEF	BPC		
76002919 76004774 76061963	MST: MST: MST: MST:	1 2 2	Off On Off On	2560 2560 2560 2560	1600 1600 1600 1600	RGB unsp. (legacy RGB mode) RGB unsp. (legacy RGB mode) RGB unsp. (legacy RGB mode) RGB unsp. (legacy RGB mode)	10 10 8 8 8		E
De-as	ssert HPD	_ 1	Pulse HPD	Pulse Duratio	n: 1000 🔺	ms Short Pulse HPD			

Label	Description	Default
Timestamp	Timestamp in milliseconds from the re-start of the HW	✓
VCP IP	Virtual Channel Payload ID	✓
VSTAT	Video status (On / Off)	✓
HPOL	Horizontal Sync polarity (+/-)	
HTOT	Horizontal Total in pixels	
HS	Horizontal Start in pixels	
HACT	Horizontal Active in pixels	\checkmark
HSW	Horizontal Sync width in pixels	
VPOL	Vertical Sync polarity (+/-)	
VTOT	Vertical Total in lines	
VS	Vertical Start in lines	\checkmark
VACT	Vertical Active in lines	
VSW	Vertical Sync width in lines	
CEF	Color Encoding Format	\checkmark
BPC	Color Depth per Channel	\checkmark

You can save the log in Comma Separated Values (*.csv) format in your PC by clicking **Save**.

Note When swapping between monitored streams, the first listing, indicating VSTAT=Off is caused by the monitoring circuitry. Please omit this listing.

CRC Log Tab

CRC Log collects CRC values of the three color components of the received frames from the stream selected In the *Main Stream* tab. The logging is enabled by selecting the **Enable Logging** checkbox.

You can save the log in Comma Separated Values (*.csv) format in your PC by clicking **Save**.

DP Irrout Terminal Source DUT Testing Main Link E-EDID MSA Log CRC Log DPCD Image: Enable Logging Image: Enable Logg					t Controller	and Test C	🕖 Unigraf DP Debug a File Help
Main Link E-EDID MSA Log CRC Log DPCD Enable Logging Timestamp VCP ID Red CRC Green CRC Blue CRC 76229002 MST: 1 0xr615 0xr281 0xr281 76224010 MST: 2 0xr147 0xr32b 0xr267 76244156 MST: 2 0xr103 0xr371 0xr271 76244166 MST: 2 0xr38b 0xr261 76244166 MST: 2 0xr38b 0xr371 0xr3774 0xr374 0xr364 0xr374 76244166 MST: 2 0xr38b 0xr4774 0xr474 7614166 MST: 2 0xr38b 0xr4774 0xr474 76244166 MST: 2 0xr38b 0xr4774 0xr474 76244166 MST: 2 0xr4856 0xr474					e DUT Testing	Source D	DP Input Terminal
Image: Proble Logging Image: Proble Logging Immestamp VCP ID Red CRC Green CRC Blue CRC 76229002 MST: 1 0xef15 0xcdsb 0x6281 76229019 MST: 1 0xf117 0xcdsb 0x6281 76229019 MST: 2 0xf147 0xod3b 0x6261 76241949 MST: 2 0x1147 0x932b 0xfdd71 7624194 MST: 2 0x18afb 0x7774 0xfaf4					CRC Log DPCD		Main Link E-EDID MS
Timestamp VCP ID Red CRC Green CRC Blue CRC 76229002 MST: 1 0xef15 0xcd5b 0x281 76229019 MST: 1 0xef15 0xcd5b 0x281 76229019 MST: 1 0xef15 0xcd5b 0x281 76229019 MST: 2 0xr147 0x932b 0xfdd7 76244196 MST: 2 0x1917 0x32f1 0x26f 76244166 MST: 2 0x18afb 0xf774 0xfaf4	1	Denna 🏛 dena					Taskis Lansian
Imestamp VCP ID Red CRC Green CRC Blue CRC 76229002 MST: 1 0xe115 0xc281 0xc281 762249049 MST: 1 0xr7733 0xc3bb 0xc26f 7624490 MST: 2 0x1033 0xc3r1 0xc2r1 76244186 MST: 2 0x1033 0xc3r1 0xc2r1 76244186 MST: 2 0xd8afb 0xf8f4	lear	Save 🔟 Clear					Enable Logging
76229002 MST: 1 0xef15 0x5e8a 0xe281 76229019 MST: 1 0xf7d3 0xcdsb 0x826f 7624409 MST: 2 0xf147 0x932b 0xfdd7 76244196 MST: 2 0x1053 0x3af1 0x2b1 76244166 MST: 2 0x8afb 0xf774 0xfaf4			Blue CRC	Green CRC	ID Red CRC	VCP ID	Timestamp
			0xe281 0x826f 0xfdd7 0x2cb1 0xfaf4	0x5e8a 0xcd5b 0x932b 0x3a71 0xf774	1 0xef15 1 0xf7d3 2 0xf147 2 0x1053 2 0x8afb	MST: 1 MST: 1 MST: 2 MST: 2 MST: 2	76229002 76229019 76244050 76244199 76244166
De-assert HPD Pulse HPD Pulse Duration: 1000 👘 ms			ms Short Pulse HPD	Pulse Duration: 1000	T Pulse HPD Pu	–	De-assert HPD



DPCD Tab

DPCD tab is a tool for monitoring and editing the DPR registers of the DPR-120 Sink.

The tool consists of two independent monitoring and editing windows for the DPCD data. The user can freely select the the DPCD address areas shown on each panel.

File Help DP Input Terminal Source DUT Testing Main Link E-EDID MSA Log CRC Log DPCD	
DP Input Terminal Source DUT Testing Main Link E-EDID MSA Log CRC Log DPCD	
Main Link E-EDID MSA Log CRC Log DPCD	
DPCD Decoder 1.2 + DETAILED_CAP_INFO_AVAIL = 1	Î Clear
DPCD Address range: 0x 0 Number of bytes to read: 0x 100	
000000 12 14 c4 01 01 01 01 81 00 00 00 00 00 00 00 00 00	*
000010 00 00 00 00 00 00 00 00 00 00 00	
000020 00 01 00 00 00 00 00 00 00 00 00 00 00	
000030 00 00 00 00 00 00 00 00 00 00 00	
000040 00 00 00 00 00 00 00 00 00 00 00	
000050 00 00 00 00 00 00 00 00 00 00 00	
Set Reference 😨 Refresh 😴 Write Changes	
DPCD Address range: 0x 200 Number of bytes to read: 0x 100	
000200 01 00 00 00 00 00 00 00 00 00 00 00 0	
000210 ff ff ff ff ff ff ff ff 00 00 00 00 00	
000220 00 00 00 00 00 00 00 00 00 00 00	
000230 00 00 00 00 00 00 00 00 00 00 00 00 0	
000240 00 00 00 00 00 00 00 00 00 00 00 00 0	
000250 00 00 00 00 00 00 00 00 00 00 00 00 0	
000260 00 00 00 00 00 00 00 00 00 00 00 00 0	
Set Reference 🔯 Refresh 😼 Write Changes	-
De-assert HPD Pulse HPD Pulse Duration: 1000 mm ms Thort Pulse HPD	

The *DPCD Decoder* panel on the right hand side shows the interpretation of the DPCD byte selected on the monitoring windows. The selected byte is shown with a green outline.

1ain Link	E-EDID MSA	Log CR	C Log DPC	D					
DPCD Decoder 1.2 + DETAILED_CAP_INFO_AVAIL = 1									
PCD Addre	ess range: 0x ()	Number	of bytes t	o read: 0	x 100			
00000	120a =4 0	01 01 03	1 01 81 0	0 00 00	00 00	00 00	00		A.
00010	00 00 00 0	0 00 00	0 00 00 0	0 00 00	00 00	00 00	00		
00020	00 01 00 0	0 00 00	0 00 00 0	0 00 00	00 00	00 00	00	=	
00030	10 de 90 7	0 00 0	0 00 00 2	0 c7 19	95 00	00 00	03		
00040	00 00 00 0	0 00 00	0 00 00 0	0 00 00	00 00	00 00	00		
00050	00 00 00 0	0 00 00	0 00 00 0	0 00 00	00 00	00 00	00		
Set R	Reference			🛱 Re	efresh		🖁 Write Change	s	

In the combo box above the DPCD Decoder window you can select how the DPCD data is interpreted, either as *DP 1.1 EDID*, or as *DP 1.2 EDID* with *Detailed Capability Info* selected or not (DETAILED_CAP_INFO_AVAIL = 1/0).

- ▶ By clicking **Refresh** you can re-read the data from the DPCD registers to the window in question.
- By clicking **Write Changes** you can write the portion of data shown in the window in question to the DPCD registers.

• By clicking **Set Reference** you can store currently shown data as a reference for comparison.

When you refresh the data from the DPCD registers the changed bytes will be highlighted with gray background.

The fields edited by the user will be highligted with red color.

File Help	
DP Input Terminal Source DUT Testing Main Link E-EDID MSA Log CRC Log DPCD	
DPCD Decoder 1.2 + DETAILED_CAP_INFO_AVAIL = 1	📺 Clear
DPCD Address range: 0x 0 Number of bytes to read: 0x 100	
000000 12 0a e4 01	*
DPCD Address range: 0x 200 Number of bytes to read: 0x 40	
000200 01.0 0 7 7 80.00 44.44 00.00 00.00 00.00 00 <td< td=""><td></td></td<>	
Set Reference 🕼 Refresh	Ŧ
De-assert HPD Pulse HPD Pulse Duration: 1000 👘 ms T Short Pulse HPD	

Saving and Loading DPCD Content

You can save the DPCD data in the address areas that you selected for the two windows as a file in your PC. You can save the content in three alternative formats:

- Binary *DPCD Fata File* format (*.DPD). This is Unigraf proprietary format. You can also load the DPCD content stored in this format.
- Comma Separated Values (*.CSV) for loading the data to a spreadsheet.
- *HEX Dump* (*.HEX) in a human readable text format.
- By Clicking **Save** you will be able to select the location and the format of the file.
- ▶ By Clicking Load you can load DPCD data saved in *DPCD Data File* (*.DPD) format to the editor.
- In order to program the data into the DPCD registers of DPR-120 Local Sink click Write Changes.

Note	- Writing DPCD data to the DPCD registers of the DPR-120 Local Sink will potentially affect the status and capabilities of DPR-120 as seen by the upstream
	source. - User control like Link Training or mode changes will modify the content of the
	DPCD registers
	- During a reboot of DPR-120 the DPCD registers will be returned to their default values.

Terminal

Terminal is a tool for running embedded DPR-120 commands.

ile Help Ripout	Torr	minal	1	Sour	ce D		octi	20														
- input	Ten	nina		Jour			cou	g														
erminal Out	put:																			1	Clear	_
120	Def	ore		Sir	n kr																	
DFR-120	REL	erei	100	110	18																	
neip drad rd		de a																				
apca_ra		apco	1_w1		ne	тþ																
dpcd rd	0 0:	x10	0																			
x00000:	12	14	e4	01	01	01	01	81	00	00	00	00	00	00	00	00						
0x00010:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x00020:	00	01	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x00030:	10	de	90	70	00	00	00	00	a4	b4	f9	42	00	00	00	fc						
0x00040:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x00050:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x00060:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x00070:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x00080:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x00090:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x000a0:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x000b0:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x000c0:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x000d0:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
0x000e0:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
Dx000f0:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
																						1
ommand lin	e:																					
			-	-	-	-	-	-	-	-	-	-	-	-	-	-						-

Currently there are three commands

Command	Description
help	List the available commands
dpcd_rd <address> <count></count></address>	Read DPCD register content. <address> is the start address; <count> is the number of register locations read. Both values are decimal by default, please use 0x prefix for hex.</count></address>
dpcd_wr <address> <value></value></address>	Write <value> to DPCD register <address>. Both values are decimal by default, please use 0x prefix for hex.</address></value>

Click Clear to clear the Terminal Output panel.

Source DUT Testing

Source DUT Testing section is the GUI to run the CTS Tests.

Unigraf DP Debug and Test Controller					
ile Help					
PP Input Terminal Source DUT Testing					
Test Name	Pass	Fail	Skip	Timeout	Rur
✗ (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension	0	0	0	0	0
🗡 (400.3.1.2) Successful LT with Request of Higher Differential Voltage Swing During Clock Recovery Sequence: HBR2 E	0	0	0	0	0
✗ (400.3.1.3) Successful LT to a Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0
术 (400.3.1.4) Successful LT to a Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0
🗡 (400.3.1.5) Successful LT with Request of a Higher Pre-emphasis and Post Cursor 2 Setting During Channel Equalizatio	0	0	0	0	0
🗡 (400.3.1.6) Successful LT at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence: HBR2	0	0	0	0	0
✓ (400.3.1.7) Unsuccessful LT at Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0
术 (400.3.1.8) Unsuccessful LT at Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0
★ (400.3.1.9) Unsuccessful LT due to Failure in Channel Equalization Sequence [loop count > 5]: HBR2 Extension	0	0	0	0	0
✗ (700.1.1.1) Additional DPCD Handling Test 1	0	0	0	0	0
✓ (700.1.1.2) Additional DPCD Handling Test 2	0	0	0	0	0
✗ (400.3.1.12) Successful LT to a Lower Link Rate #3: Iterate at Max Voltage Swing	0	0	0	0	0
术 (400.3.1.13) Successful LT to a Lower Link Rate #4: Iterate at Minimum Voltage Swing	0	0	0	0	0
🗡 (400.3.1.14) Successful Link Downgrade to Lowest Link Rate: Failed Clock Recovery at HBR2, Loss of Clock Recovery	0	0	0	0	0
🗡 (400.3.1.15) Successful LT with Simultaneous Request for Differential Voltage Swing and Post Cursor during Clock Rec	0	0	0	0	0
术 (400.3.2.1) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock: HBR2 Extension	0	0	0	0	0
★ (400.3.2.2) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock: HBR2 Extension	0	0	0	0	0
🗡 (400.3.2.3) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock: HBR2 Extension	0	0	0	0	0
★ (400.3.3.1) Video Time Stamp Generation	0	0	0	0	0
			-		_
Idle time between tests: 1 Seconds.				Clear Res	ults
atus Log:					
4					Þ

5. RUNNING COMPLIANCE TESTS

DP Link Layer CTS test capability is a separate add on to DPR-120 Debug and Test Controller GUI. The tests are included in the GUI, all you need to have is the license code to enable them.

In order to get details of the content of each individual *CTS Test Product* please refer to document <u>http://www.unigraf.fi/userData/unigraf/products/manuals/Guide-to-Unigraf-DP-CTS-Tool-Options.pdf</u>. If you have any additional questions, please contact Unigraf or your local representative.

DUT Capabilities

Before running the tests you have to define the capabilities of the Source DUT for the test engine. This is done in **Source DUT Testing > DUT Capabilities** tab.

Ø Unigraf DP Debug and Test Controller File Help DP Input Terminal Source DUT Testing Run Tests DUT Capabilities		
DUT Capabilities Max lanes supported: Max bit rate supported: HPD Unplug timeout (milliseconds): Video format change without LT supported Link count reduction without LT supported Link count reduction without LT supported Pre-Emphasis level 3 (1.20) supported Pre-Emphasis level 3 (9.58B) supported Spread Spectrum Supported	Time-stamp generation Lanes Lanes 11ane 2 Lanes 4 Lanes RBR 640x480@60 Hz 1280x720@60 Hz 1920x1080@60 Hz HBR 1280x720@60 Hz 1280x960@60 Hz 1920x1440@60 Hz HBR2 1280x960@60 Hz 1920x1080@610 Hz 1920x1080@120 Hz Most Packed Timings 1 1 1280x00@ 60Hz 240pp 2 Lanes 1280x1024@ 60Hz 240pp 4 2048x1536@ 60Hz 240pp Colorimetry 2048x1536@ 60Hz 240pp	• • •
Test Automation Test_LINK_TRAINING TEST_LINK_TRAINING TEST_LOEO_PATTERN TEST_AUDIO_PATTERN TEST_AUDIO_PATTERN TEST_STEREO_3D Event indicating DUT ready:	RGB YCbCr 4:2:2 YCbCr 4:4:4 18bpp VESA 24bpp CEA (TU.601) 24bpp CEA (TU.601) 24bpp VESA 30bpp CEA (TU.601) 30bpp CEA (TU.709) 30bpp VESA 24bpp CEA (TU.709) 24bpp CEA (TU.709) 24bpp CEA 30bpp CEA (TU.709) 30bpp CEA (TU.709) 30bpp CEA 30bpp CEA (TU.709) 30bpp CEA (TU.709) 30bpp CEA Select All 30bpp CEA (TU.709) 30bpp CEA (TU.709)	_

The capabilities listed on the tab are explained in detail in chapter 3 Compliance Test Operation of document VESA® DisplayPort® Link Layer Compliance Test Specification: Extension Set 1.

Note Please make sure that the capability tables are completed before running the tests. The result of the test might be misleading if the DUT capabilities and the table do not match.

> You can save the settings stored in the *DUT Capabilities* tab by selecting **File > Save CTS Settings ...** You can retrieve saved settings by selecting **File > Open CTS Settings ...**

Running the Tests

The **Source DUT Testing > Run Tests** tab lists the tests enabled with the *CTS Test Product* enabled in your Debug and Test Controller (DTC) GUI. The test name and the reference number refer to the applicable *VESA*® *DisplayPort*® *Link Layer Compliance Test Specification*. The GUI and the related FW on DPR-120 implement the test according to the specification in question. Please refer to the VESA Specification for detailed description of the procedure of the test.

For running a test, select the test with your mouse and click **Run**. For selecting multiple tests hold down the **Shift** key of your keyboard while selecting the tests.

Unigraf DP Debug and Test Controller					
Input Terminal Source DUT Testing					
un Tests DUT Capabilities					
					_
Test Name	Pass	Fail	Skip	Timeout	Run
✗ (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension	0	0	0	0	0
K (400.3.1.2) Successful LT with Request of Higher Differential Voltage Swing During Clock Recovery Sequence: HBR2 E	0	0	0	0	0
K (400.3.1.3) Successful LT to a Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0
K (400.3.1.4) Successful LT to a Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0
K (400.3.1.5) Successful LT with Request of a Higher Pre-emphasis and Post Cursor 2 Setting During Channel Equalizatio	0	0	0	0	0
K (400.3.1.6) Successful LT at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence: HBR2	0	0	0	0	0
(400.3.1.7) Unsuccessful LT at Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0
K (400.3.1.8) Unsuccessful LT at Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0
(400.3.1.9) Unsuccessful LT due to Failure in Channel Equalization Sequence [loop count > 5]: HBR2 Extension	0	0	0	0	0
(700.1.1.1) Additional DPCD Handling Test 1	0	0	0	0	0
(700.1.1.2) Additional DPCD Handling Test 2	0	0	0	0	0
(400.3.1.12) Successful LT to a Lower Link Rate #3: Iterate at Max Voltage Swing	0	0	0	0	0
K (400.3.1.13) Successful LT to a Lower Link Rate #4: Iterate at Minimum Voltage Swing	0	0	0	0	0
K (400.3.1.14) Successful Link Downgrade to Lowest Link Rate: Failed Clock Recovery at HBR2, Loss of Clock Recovery	0	0	0	0	0
✓ (400.3.1.15) Successful LT with Simultaneous Request for Differential Voltage Swing and Post Cursor during Clock Rec	0	0	0	0	0
K (400.3.2.1) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock: HBR2 Extension	0	0	0	0	0
✓ (400.3.2.2) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock: HBR2 Extension	0	0	0	0	0
K (400.3.2.3) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock: HBR2 Extension	0	0	0	0	0
K (400.3.3.1) Video Time Stamp Generation	0	0	0	0	0
A Due Task Dury 1 A Talk Key babwan kasha 1 A Canada			_	Class Day	
rest kuns: 1 v tale ume between tests: 1 v Seconds.			Ш	Clear Kes	ults
tus Log:					
					- P-

Below the list of tests you can select how many times the selected tests are performed and the time between the tests. When repeating a sequence of tests, all selected tests are performed in each repetition. E.g. when you repeat tests 1, 2 and 3 two times, the sequence is: 1, 2, 3, 1, 2, 3.

For clearing the Status Log and the Results matrix, click Clear Results.

Evaluating the Results

The test procedure advancement is defined in the *Status Log* panel. It describes the steps of each individual test in the way defined in the corresponding VESA Compliance Test Specification. Please use the Status Log and the Specification side by side when interpreting the results.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test the matrix lists the number of occurrences of each result and the number of tries performed.

🖉 Unigraf DP Debug and Test Controller						×
File Help						
DP Input Terminal Source DUT Testing						
Run Tests DUT Capabilities						
			et :			
Test Name	Pass	Fail	БКІр	Timeout	Run	<u> </u>
(400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension	0	0	0	0	0	
X (400.3.1.2) Successful LT with Request of Higher Differential Voltage Swing During Clock Recovery Sequence: HBR2 Extension	0	0	0	0	0	
(400.3.1.3) Successful LT to a Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0	
(400.3.1.4) Successful LT to a Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0	
(400.3.1.5) Successful LT with Request of a Higher Pre-emphasis and Post Cursor 2 Setting During Channel Equalization Sequence	0	0	0	0	0	
X (400.3.1.6) Successful LT at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence: HBR2 Extension	0	0	0	0	0	
✗ (400.3.1.7) Unsuccessful LT at Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension	0	0	0	0	0	=
✗ (400.3.1.8) Unsuccessful LT at Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension	0	0	0	0	0	
✗ (400.3.1.9) Unsuccessful LT due to Failure in Channel Equalization Sequence [loop count > 5]: HBR2 Extension	0	0	0	0	0	
X (700.1.1.1) Additional DPCD Handling Test 1	0	0	0	0	0	
★ (700.1.1.2) Additional DPCD Handling Test 2	0	0	0	0	0	
✗ (400.3.1.12) Successful LT to a Lower Link Rate #3: Iterate at Max Voltage Swing	0	0	0	0	0	
术 (400.3.1.13) Successful LT to a Lower Link Rate #4: Iterate at Minimum Voltage Swing	0	0	0	0	0	
🗡 (400.3.1.14) Successful Link Downgrade to Lowest Link Rate: Failed Clock Recovery at HBR2, Loss of Clock Recovery during Ch	0	0	0	0	0	
🗡 (400.3.1.15) Successful LT with Simultaneous Request for Differential Voltage Swing and Post Cursor during Clock Recovery &	0	0	0	0	0	
✗ (400.3,2,1) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock: HBR2 Extension	0	0	0	0	0	
★ (400.3,2.2) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock: HBR2 Extension	0	0	0	0	0	
🗡 (400.3,2.3) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock: HBR2 Extension	0	0	0	0	0	
★ (400.3.3.1) Video Time Stamp Generation	0	0	0	0	0	
(4.2.1.1) Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	1	0	0	0	1	
✗ (4.2.1.2) Source Retry on Invalid Reply During AUX Read after HPD Plug Event	0	0	0	0	0	
★ (4.2.2.1) EDID Read upon HPD Plug Event	0	0	0	0	0	
★ (4.2.2.2) DPCD Receiver Capability Read upon HPD Plug Event	0	0	0	0	0	-
Image: Second state Image: Second state Image: Second state Image: Second state				<u> </u> Clear I	Results	
Status Log:						
Starting test: 4.2.1.1 Source DUT Retry on No-Reply During AUX Read after HPD Plug Event						*
Set MAX LINK RATE = 14h. MAX LANE COUNT = 4						
Long HPD Pulse (700 ms)						-
4					•	

Creating a Report

You can save the test results as a report in HTML format. Select **File > Save Report** ... A dialog will open where you can insert information about the DUT and remarks about the test. Details of the used test equipment and the software and firmware version will be added automatically.

Report information	
PR-120 Serial number: 0000C001 Firmware package: Firmware package Version 1.5 [F1.3.0_N0.0.17_A0.0.21_V1.1.4] Application Version V1.5 [Dec 17 2013]	DUT Information Model: AAA Serial Number: 123 Revision: aaa
Report Information	I.2.3 Driver: 3.2.1
Tested by: N.N Remarks: (1024 chars max.)	on 2. toukokuu ta 2013
This is a test	
	Save Cancel

Viewing the Report

The report file can be viewed with any HTML browser. The report has built-in views for Report Summary, Test Summary, view of individual tests and view of all information.

DPR-120 CTS Test Report X	
C Thile://C:/Users/-/Desktop/temp.htm	
LLCIS TEST TIMING	
LLCTS_TEST_STEREO_3D	
Event indicating DUT ready = Link Training end.	
ST DETAILS, TEST 1	
(400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension	
Test Result: PASSED	
Test Settings:	
DUT Capabilities:	
Max Lanes = 4 Lanes, Max Link Rate = HBR2 (5.4 Gbps)HPD Unplug timeout: 700 ms	
Test automation:	
LLCTS TEST LINK TRAINING	
LLCTS_TEST_PATTERN	
LLCTS_TEST_AUDIO_PATTERN	
LLCTS_TEST_TIMING	
LLCIS_IESI_SIEREO_3D	
Event indicating DOT ready = Link Training end.	
Test Log	
Starting Test: (400.3.1.1) Successful LT at All Supported Lane Counts and Link Speeds: HBR2 Extension.	
Set MAX LINK RATE = 08h MAX LANE COUNT = 1	
Long HPD Pulse (200 ms)	
Wait until Source DUT writes to the LINK BW SET and LANE COUNT SET fields	
Source DUT sets LANE_COUNT_SET =1	
Source DUT sets LINK_BW_SET = 06h	
Source DUT writes TRAINING_PATTERN_SET = 1h	
CR LT iter, 1 lanes	
CK lock succeeded on all active lanes	
Source DUT writes TRAINING_PATTERN_SET = 30	
Equalization succeeded on all active lanes	
Symbol lock succeeded on all active lanes	
Source DUT writes TRAINING PATTERN SET = 0h	

APPENDIX A. PRODUCT SPECIFICATION

DPR-120

Input	1 x DisplayPort™ HBR2 and MST compliant Rx, ST Microelectronics STDP9320 controller (DP In)
Outputs	1 x DP 1.2 multi stream Tx (DP Out) 1 x DP 1.1 compliant preview monitor (Monitor Out) S/PDIF coaxial audio monitor TRS headset audio monitor
Resolutions	4096 x 2160 input & pass through 2560 x 1600 preview
Audio	Up to 2 LPCM channels at 192 kHz, 24-bits or multi- channel compressed (AC3, DTS, etc) compliant with IEC60958 / IEC61937
Control	USB 2.0 interface
Software	Debug and Test Controller GUI Test Automation Shell (option) DP RefSink CTS LL Extensions (option)
Power supply	AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +5 Vdc output)
Mechanical Size	230 x 168 x 56 mm
Weight	0.9 kg w/o power supply

All specifications are subject to change without notice.

APPENDIX B: TEST AUTOMATION SHELL

Test Automation Shell (TA Shell) is a license enabled optional feature for DPR-120. It enables the user to create simple automated test routines. All functions that are in the DTC GUI can also be accessed through the TA Shell.

Please find below a quick list of TA Shell commands. For full description of each command, please refer to *Shell_User_Manual.pdf* included in the DPR-120 Release Package.

```
Help <topic> [...]
Exit
Open <Device ID>
List
Close
CLS
Run <DOS Command>
License add <key>
License list
License remove <key-index>
License save
License load
DPIN HPD <Operation>
DPIN Linkconfig show
DPIN Linkconfig <Lane_count> <Speed> <MST> <TPS3>
DPIN DPCD Read <Address> [Length]
DPIN DPCD Write <Address> <Data1> [Data2]
DPIN DPCD Save <Target-file> <Address> [Length]
DPIN DPCD Load <Source-file>
DPIN Status
DPIN Streams
SINK EDID Load <Source-file>
SINK EDID Save <Target-file>
```

```
DPMON Select <Stream Index>
DPMON Read <Data_ID>
DPMON Log Start <Data ID> <Target File>
DPMON Log Stop <Data ID>
CTS List
CTS Config load <config_file>
CTS Config save <config_file>
CTS Config show [conf entry]
CTS Config Link <Max-lanes> <Max-rate> <HPD Timeout>
CTS Config flags <'+'|'-'> <Flag1> [Flag2] [...]
CTS Config ta flags <'+'|'-'> <Flag1> [Flag2] [...]
CTS Config ready_event <Event>
CTS Config timestamp <BitRate> <Lanes> <ResolutionID>
CTS Config most_packed <ResID1> <ResID2> <ResID4>
CTS Config colorimetry <'+'|'-'> <CL_ID1> [CL_ID2] [...]
CTS Run <Test_Index>
Proceed
Pass
Fail
Abort
CTS Report DUT_Model <String>
CTS Report DUT_Revision <String>
CTS Report DUT_FW <String>
CTS Report DUT Serial <String>
CTS Report DUT Driver <String>
CTS Report Tester <String>
CTS Report Remarks <String>
CTS Report show
CTS Report save <Target_File>
```