AX5240

32 Bit DI with Interrupt, 40 Bit DIO
or
6 Channel Counter/Timer Board

User's Manual

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ESD Precautions

Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.

Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.

Wear a wrist grounding strap, available from most electronic component stores, when handling boards and components.

Unpacking

The AX5240 is packed in an anti-static bag. This board has components that are easily damaged by static electricity. Do not remove the anti-static wrapping until proper precautions have been taken. Safety instructions in front of this User's Manual describe anti-static precautions and procedures.

Inventory and Inspection

After unpacking the board, place it on a raised surface and carefully inspect the board for any damage that might have occurred during shipment. Ground the board and exercise extreme care to prevent damage to the board from static electricity.

Integrated circuits will sometimes come out of their sockets during shipment. Examine all integrated circuits, particularly the BIOS, processor and keyboard controller chip to ensure that they are firmly seated.

The AX5240 32 Bit DI with Interrupt, 40 Bit DIO or 6 Channel Counter/Timer Board package includes the following:

- **AX5240 Board**
- **AS59099 DAC Driver CD**
- **AX5240 Technical Manual**
- **AX5240 User's Manual**
- **Warranty Card**

Make sure that all of the items listed above are present.

What To Do If There Is A Problem

If there are damaged or missing parts, contact your supplier and/or dealer immediately. Do not attempt to apply power to the board if there is damage to any of its components.

Table of Contents

Chapter 1 Introduction

General Description

The AX5240 is a digital with/without interrupt or timing I/O board for IBM PC/XT/AT and compatible computers. The board uses a pair of the powerful Zilog Z8536 programmable digital I/O chips which make it programmable for 32-bit digital input with interrupt, 40-bit digital I/O or 6-channel counter/timer board.

The Z8536 may be programmed as 20 lines of digital I/O. Each line may be independently set for input or output and may be inverting or non-inverting. Once the digital I/O lines are programmed, writes and reads are on a byte wide basis to the three addresses for ports A, B and C. The digital I/O ports may also be programmed as a two-wire or three-wire handshaking interface port.

Up to three down counters may be set up independently or chained together internally. Each has an input, an output, a gate and a trigger. The trigger may be used externally or internally via software to load the count value from the hold register into the counter and initiate the count down. Outputs may be square wave, one shot or pulse at terminal count; all three modes are recyclable. Inputs are programmable for level or edge trigger, either high, low, rising or falling. Outputs may be inverting or non-inverting.

Each Z8536 may be programmed to accept 16 independent external interrupts, high, low, rising or falling edge, and output an interrupt to the PC. The output from the two Z8536s may be ANDed by onboard jumper so that any of 32 external events may cause a PC interrupt service routine to be executed.

All AX5240's I/O lines are built in a 50-pin connector. To ease and guide user in application, many programming examples on a diskette is included along with the AX5240 board. About more detailed information for programming the Z8536, user must refer to Zilog Z8536 manual.

Features

- **Fully programmable for combinations of up to**
  - **32 vector interrupt director**
  - **40 bits of bit setable digital I/O**
  - **Six 16-bit counters with In, Out, Gate and Trigger**
- **Pattern matching**
- **Inverting or non-inverting input and output**
- **Rising or falling edge or high or low level trigger/sense**
- **Two-wire or three-wire handshaking digital interface**
- **Programming examples included**

Specifications

- **Digital I/O**
  - **Z8536 Output High :** 2.4V min. @ -250µA
  - **Z8536 Output Low :** 0.5V max. @ 3.2mA
  - **Z8536 Input High :** 2.0V min., 7.3V max.
  - **Z8536 Input Low :** -0.3V min., 0.8V max.
  - **Z8536 Drive Capability :** 5 LSTTL loads
- **Interrupt Input**
  - **Type :** Positive edge triggered
  - **PC Bus IRQ :** IRQ 2, 3, 4, 5, 6, 7
  - **Enable Interrupt :** TTL "0"
  - **External Interrupt :** TTL positive trigger
- **Power Requirement**
  - **+5VDC :** 440mA typ.
    720mA max.
- **Physical/Environment**
  - **Dimensions :** 98mm X 104mm
  - **Weight :** 110g
  - **Operating Temperature Range :** 0EC to +55EC
  - **Storage Temperature Range :** -20EC to +70EC
  - **Relative Humidity :** 0 to 90%, non-condensing

Accessories Guide

- **AX754**

  24-channel opto-isolated D/I panel for signal connection and conditioning with the AX5240. Shipped with 3.3 feet (1 meter) cable and 50-pin connector. If used only 20 channels are available and if using interrupt ability only 16 channels are permitted.

- **AX755**

  8-channel electromechanical single-pole, double-throw(SPDT) and 16-channel opto-isolated digital I/P panel. Shipped with 3.3 feet (1 meter) cable and 50-pin connector. If used only 16 channels are available and permitted to interrupt only 4 channels of relay can be used.

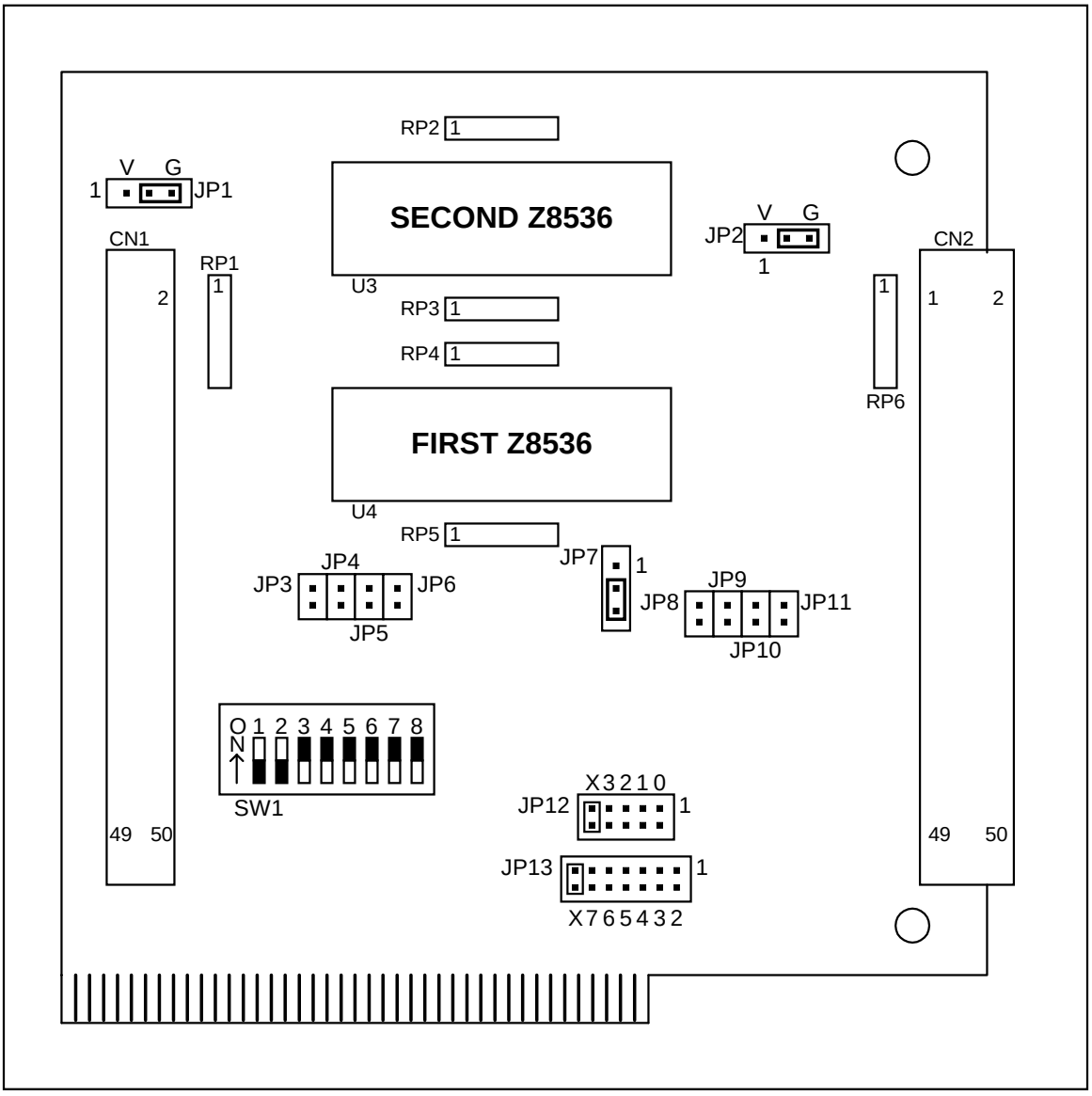
- **AX756**

  24-channel electromechanical single-pole, double-throw (SPDT) which can be driven by the AX5240. Shipped with 3.3 feet (1 meter) cable and 50-pin connector. If used only 20 channels are available.

C h a p t e r 2 Board Configuration and Installation

Component Locator Diagram

The following figure shows the component location of AX5240. All switch and jumper settings in this figure are the factory default settings.

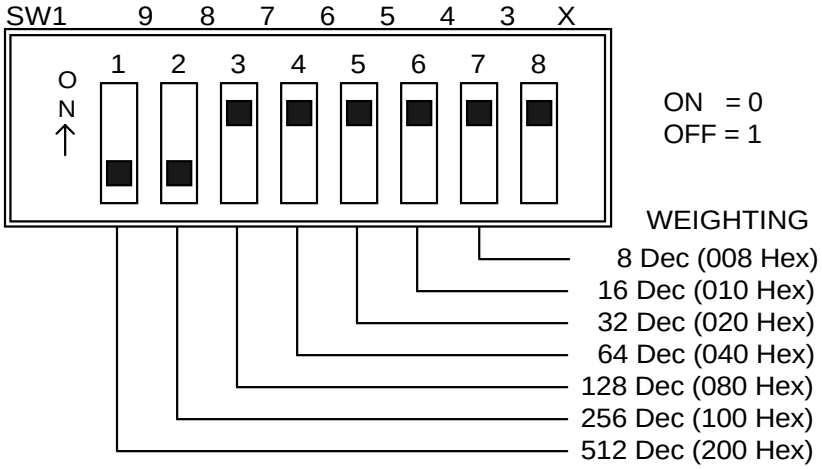


Base Address Switch

The AX5240 board occupies 8 consecutive locations in I/O address space. The first address or base address is selected via a 8-position DIP switch labeled SW1. If more than one boards are to be installed to one PC, each board must be given its own distinct I/O address or base address. No more than one board may use the same base address. When you are selecting the base address, it would be better if you check with *Appendix A* to avoid conflicting with other installed devices. In factory, the AX5240 base address is set for 300 Hex or 768 Dec.

To set to appropriate base address, switch the individual switches into the ON or OFF position. The following figure shows SW1 default setting, 300 Hex, where switches 1 and 2 are moved to the OFF position while leaving all other switches in the ON position. A table for the switch configuration is given in the following page.

Base Address Switch Setting



Each switch represents one address weight. The desired base address is determined by adding the weight of the switches flipped at OFF position. The base address calculation is as follows:

Base Address = 512 + 256 = 768 Dec
= 300 Hex

I/O Port Range (Hexadecimal)	DIP Switch Position							
	1	2	3	4	5	6	7	8
	A9	A8	A7	A6	A5	A4	A3	A2
200 e 207	1	0	0	0	0	0	0	X
208 e 20F	1	0	0	0	0	0	1	X
210 e 217	1	0	0	0	0	1	0	X
218 e 21F	1	0	0	0	0	1	1	X
220 e 227	1	0	0	0	1	0	0	X
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
300 e 307 **(*)**	1	1	0	0	0	0	0	X
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
3F0 e 3F7	1	1	1	1	1	1	0	X
3F8 e 3FF	1	1	1	1	1	1	1	X

NOTE *0 = ON, 1 = OFF, X = Don't care*
***(*)** : Factory default setting*

+12V or Ground Selection

Pins 2 and 4 at CN1 and CN2 50-pin connectors can be connected to +12V PC power or Ground by setting JP1 and JP2 jumpers, respectively. When the +12V is jumpered to the CN1 or CN2 connector, you may use the AX5240 for direct relay driving or input pull high voltage. The JP1 and JP2 jumper settings are listed in below table.

Jumper Configuration	Description
JP1 V G	Connect PC Ground to pins 2 and 4 of CN1 connector. This is also JP1 factory default setting. (*)
JP1 V G	Connect +12VDC PC power to pins 2 and 4 of CN1 connector. (**)
JP2 V G	Connect PC Ground to pins 2 and 4 of CN2 connector. This is also JP2 factory default setting. (*)
JP2 V G	Connect +12VDC PC power to pins 2 and 4 of CN2 connector. (**)

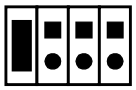
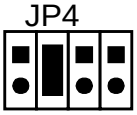
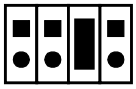
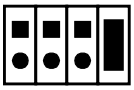
NOTE *(*) : Through the corresponding connector, the AX5240 is compatible with AX1416 and AX1424 solid-state module panels from AXIOMTEK.*

(**) : Through the corresponding connector, the AX5240 is compatible with AX754, AX755 and AX756 accessory boards from AXIOMTEK.

When the AX5240 is used with standard Opto-22 interface panel board, pins 2 and 3 of JP1/JP2 must be connected.

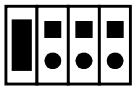
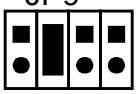
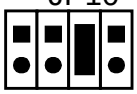
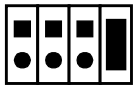
External Interrupt Enable, Clock and Interrupt Output Setting

JP3 through JP6 jumpers are used to set external interrupt input, second Z8536 interrupt output, 2.5MHz and 5MHz clock output for CN1 connector. The JP3 through JP6 jumper configurations are listed in the following table.

Jumper Configuration	Description
JP3 	Connect the external interrupt input signal at pin 15 of CN1 connector to internal interrupt ckt. If external interrupt source is selected (refer to *Interrupt Source Selection* section), this JP3 jumper must be connected.
JP4 	Connect second Z8536 interrupt output to pin 13 of CN1 connector.
JP5 	Connect the 2.5MHz clock output to pin 11 of CN1 connector.
 JP6	Connect the 5MHz clock output to pin 9 of CN1 connector.

In factory, all JP3 through JP6 jumpers are left open.

JP8 through JP11 jumpers are used to set external interrupt enable signal, first Z8536 interrupt output, 2.5MHz and 5MHz clock output for CN2 connector. The JP8 through JP11 jumper configurations are listed in the following table.

Jumper Configuration	Description
JP8 	Connect the external interrupt enable signal at pin 15 of CN2 connector to internal interrupt ckt. If external interrupt source is selected (refer to *Interrupt Source Selection* section), this JP8 jumper must be connected.
JP9 	Connect first Z8536 interrupt output to pin 13 of CN2 connector.
JP10 	Connect the 2.5MHz clock output to pin 11 of CN2 connector.
 JP11	Connect the 5MHz clock output to pin 9 of CN2 connector.

In factory, all JP8 through JP11 jumpers are left open.

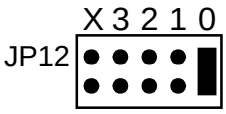
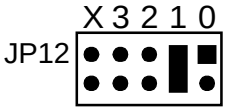
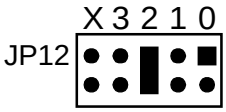
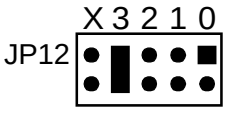
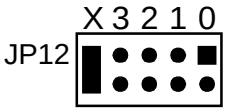
Independent/Chained Interrupt Selection

Interrupts for the two Z8536s may be independent or chained together by setting JP7 jumper. Each Z8536 may be programmed to accept 16 independent external interrupt lines in high, low, rising or falling edge, and output an interrupt to PC interrupt service routine. Or the 16 interrupt lines may be chained together as a set of 32 external interrupt lines by connecting pins 2 and 3 of JP7 jumper.

Jumper Configuration	Description
JP7 	Interrupts for the two Z8536s are independent, that is each Z8536 accepts 16 independent external interrupt lines.
JP7 	Interrupts are chained from first to second Z8536 as a set of 32 external interrupt lines. This is also JP7 factory default setting.

Interrupt Source Selection

By configuring JP12 jumper, you may have several choices of interrupt source for your PC. The following table lists all the possibly configurations of JP12.

Jumper Configuration	Description
	Select interrupt source from both Z8536 chips. When first and second Z8536 chips are chained, JP12 must be jumpered in position 0.
	Select interrupt output from first Z8536 chip.
	Select interrupt output from second Z8536 chip.
	Select external interrupt source. **(*)**
	Disable interrupt. This is JP12 factory default setting.

NOTE

(*) : *When external interrupt source is selected:*

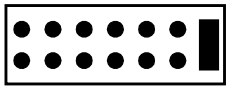
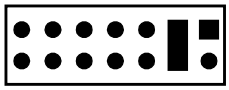
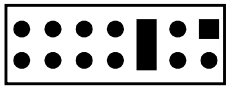
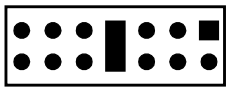
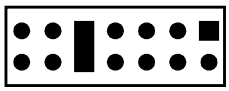
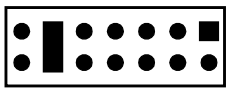
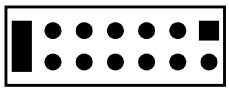
- *JP3 and JP8 must be installed.*
- *The external interrupt signal routed to the PC bus is determined by EX INT pin at CN1 and EX INTE pin at CN2.*

EX INTE	EX INT	Description
0	0 → 1	An interrupt generated
0	1 → 0	No interrupt generated
1	X	External Interrupt disable
1	X	External Interrupt disable

X : don't care

Interrupt Level Selection

The AX5240 provides interrupt handling capability for various applications. The signal from interrupt source can be led to any of the six PC interrupt request lines (IRQ level 2-7) by setting JP13 jumper. Refer to the following table and properly set JP13 if the AX5240 board uses interrupt.

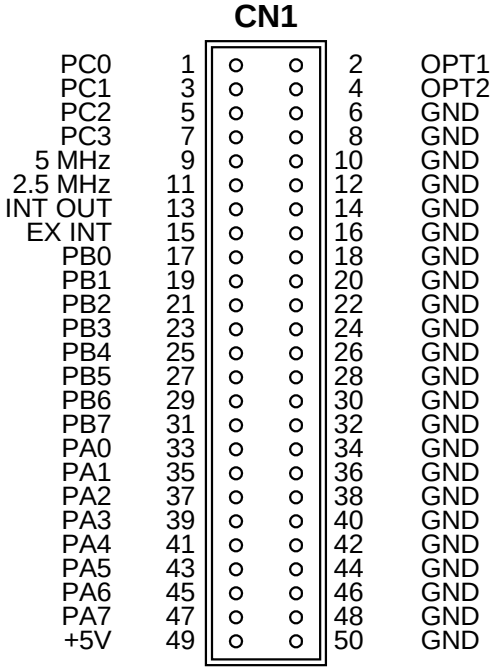
Jumper Configuration	Description
JP13 	Select IRQ 2.
JP13 	Select IRQ 3.
JP13 	Select IRQ 4.
JP13 	Select IRQ 5.
JP13 	Select IRQ 6.
JP13 	Select IRQ 7.
JP13 	If no interrupt is used, jumper the JP13 in position X. This is also JP13 factory default setting.

NOTE *It cannot be stated often enough to those unfamiliar with the Z8536.*
WHENEVER THE Z8536 IS POWERED ON OR RESET, ALL PINS ARE SET TO HIGH IMPEDANCE INPUT.

The implications of this fact is that if you have output devices such as solid state relays, they may be switched on whenever the computer is powered on or reset. To prevent unwanted switching and to drive all outputs to a known state after power on or reset, pull all pins either high or low through a 10K ohm resistor.

Connector Pin Assignment

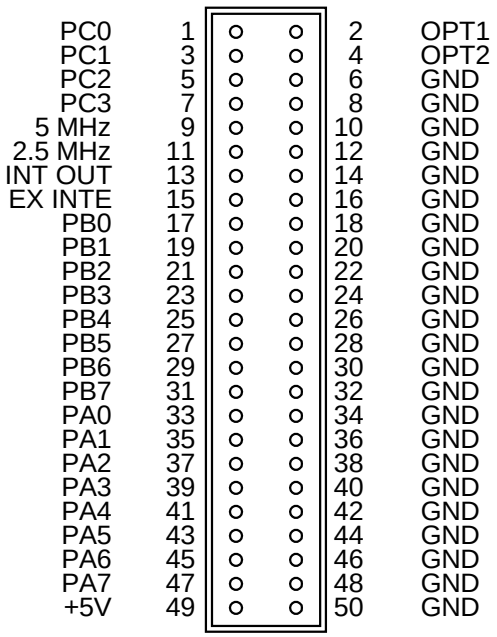
All AX5240's input and output signals are built in two standard 50-pin male mating connectors labeled CN1 and CN2. First Z8536 chip is brought to CN2 (accessible from the rear panel of the PC), while second Z8536 is brought to CN1. The connectors provides easy and direct cabling connections between the AX5240 and AXIOMTEK's accessory boards such as AX754, AX755 and AX756. The CN1 and CN2 pin assignments and description are given as follows:



CN1 connector pin assignments:

Pin Name	Description
PC0~PC3	Second Z8536's Port C four digital I/O lines.
5MHz	When JP6 jumper is installed, this pin is connected to 5MHz clock output.
2.5MHz	When JP5 jumper is installed, this pin is connected to 2.5MHz clock output.
INT OUT	When JP4 jumper is installed, this pin is connected to second Z8536 interrupt output.
EX INT	This is the external interrupt input pin.
PB0~PB7	Second Z8536's Port B eight digital I/O lines.
PA0~PA7	Second Z8536's Port A eight digital I/O lines.
+5V	+5VDC PC power.
OPT1, OPT2	By setting JP1 jumper (refer to *+12V or Ground Selection* section), these pins can be connected to +12V PC power or Ground.
GND	Ground.

CN2



CN2 connector pin assignments:

Pin Name	Description
PC0~PC3	First Z8536's Port C four digital I/O lines.
5MHz	When JP11 jumper is installed, this pin is connected to 5MHz clock output.
2.5MHz	When JP10 jumper is installed, this pin is connected to 2.5MHz clock output.
INT OUT	When JP9 jumper is installed, this pin is connected to first Z8536 interrupt output.
EX INTE	This is the external interrupt enable pin.
PB0~PB7	First Z8536's Port B eight digital I/O lines.
PA0~PA7	First Z8536's Port A eight digital I/O lines.
+5V	+5VDC PC power.
OPT1, OPT2	By setting JP2 jumper (refer to *+12V or Ground Selection* section), these pins can be connected to +12V PC power or Ground.
GND	Ground.

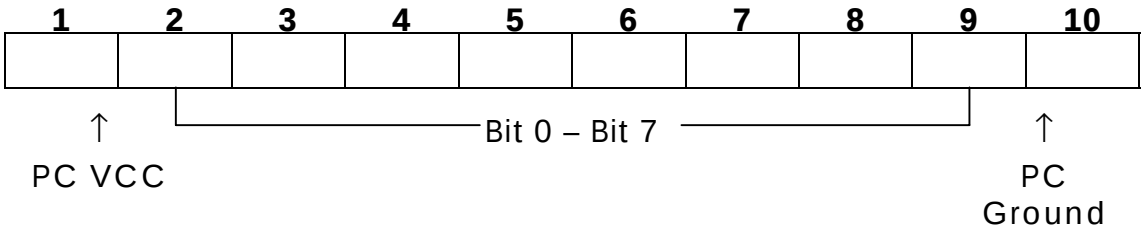
Pull High/Down Resistors

On the AX5240 board, there are reserved spaces for installing pull high/down resistors (resistor packs). Below table lists the DI/O lines and their corresponding resistor packs.

DI/O Lines	Resistor Rack
First Z8536	
PA0~PA7	RP4
PB0~PB7	RP5
PC0~PC3	RP6
Second Z8536	
PA0~PA7	RP2
PB0~PB7	RP3
PC0~PC3	RP1

When using interrupt, the resistor packs have to be installed to avoid unstable floating signals. The resistor values are suggested to be within 4.7KΩ~10KΩ and pull high.

The positions of resistor pack (RP1~RP6) are shown on location diagram. The pin definitions are illustrated as follows:



The RP1~RP6 are all the same as above figure.

Board Installation

The AX5240 board is shipped with protective electrostatic cover. When unpacking, touch the board electrostatically shielded packaging with the metal frame of your computer to discharge the accumulated static electricity prior to touching the board.

The following description summarizes the procedures for installing AX5240:

WARNING *TURN OFF the PC and all accessories connected to the PC whenever installing or removing any peripheral board including the AX5240 series board.*

Installation Procedure:

1. Turn off the PC and all accessories power.
2. Unplug all power cords and entire cables from PC's rear panel.
3. Remove the PC's cover (see your PC operation Guide if you are not skillful about it).
4. Find an unused expansion slot. Remove the blank expansion slot cover and save the screw for affixing retaining bracket.
5. Grab the upper edge of the AX5240 board. Align the AX5240 board's retaining bracket with the expansion slot rear panel, and straighten the board's gold finger with the expansion slot, crush the board into the slot.
6. Restore the screw to the expansion slot retaining bracket.
7. Replace the PC's cover and connect the cables you detached in step 2.
8. Turn on the PC and other peripheral devices power.

Chapter 3 Register Format and Description

The AX5240 occupies 8 consecutive addresses of PC I/O address space. The first address or base address is determined during installation by setting onboard DIP switch labeled SW1. The base address +0 through +3 access first Z8536's three data and one control registers. The base address +4 through +7 access second Z8536's three data and one control registers.

This chapter lists each AX5240 register in terms of address and function. Each register is easy to read and write to by using direct I/O instructions of whatever application languages. To write a control word or data to the 8-bit wide register, the individual bits must be set to 0 or 1 then combined to form a byte. An 8-bit data is read from the register and the individual bits are analyzed to determine which bits are 0 or 1.

AX5240 I/O Address Map

The registers and their functions are listed in the following table (R = Read, W = Write, Base = Base address).

Address	Function	Type
First Z8536		
Base +0	Port C digital input/output	R/W
Base +1	Port B digital input/output	R/W
Base +2	Port A digital input/output	R/W
Base +3	Control and status register	R/W
Second Z8536		
Base +4	Port C digital input/output	R/W
Base +5	Port B digital input/output	R/W
Base +6	Port A digital input/output	R/W
Base +7	Control and status register	R/W

More detailed information can be found in Zilog Z8536 manual.

Chapter 4 Programming

The diskette supplied contains many demo programs, in different kinds of programming language, listed in the following description. The main spirit of AX5240 lies on the programming of Z8536 which is given in more detailed at the technical manual of Z8536.

- **Microsoft Quick Basic**

USERVENT.ASM	Assembly part of ONUEVENT.BAS. Its major task is to do interrupt service routine.
ONUEVENT.BAS	Demo how to invoke interrupt process routine.

- **Microsoft C 6.00**

DEMO_DIO.C	Demo how to issue digital output and digital input.
DEMO1INT.C	Demo how to detect interrupt from Port A (8 bits) at CN2 connector.
DEMO2INT.C	Demo how to detect interrupt from Port A (8 bits) at CN1 connector.
INT16BIT.C	Demo how to detect interrupt from Port A and Port B at CN2.
INT32A.C	Demo how to detect interrupt from both Port A and Port B at CN1 and CN2.
INT32B.C	The same as INT32A.C but in different structure.

- **BASIC Language**

DIGITIN.BAS	Demo how to read digital input.
DIGITOUT.BAS	Demo how to write digital output.
COUNTER.BAS	Demo how to program the counter.
MATCHP.BAS	Demo how to detect a matched pattern.

- **TC**

  For Turbo C users, you have to modify the MSC demo programs.

- **Turbo Pascal**

  Users have to migrate to Pascal programs by the same I/O read and write sequence which apply to the MSC demo program.

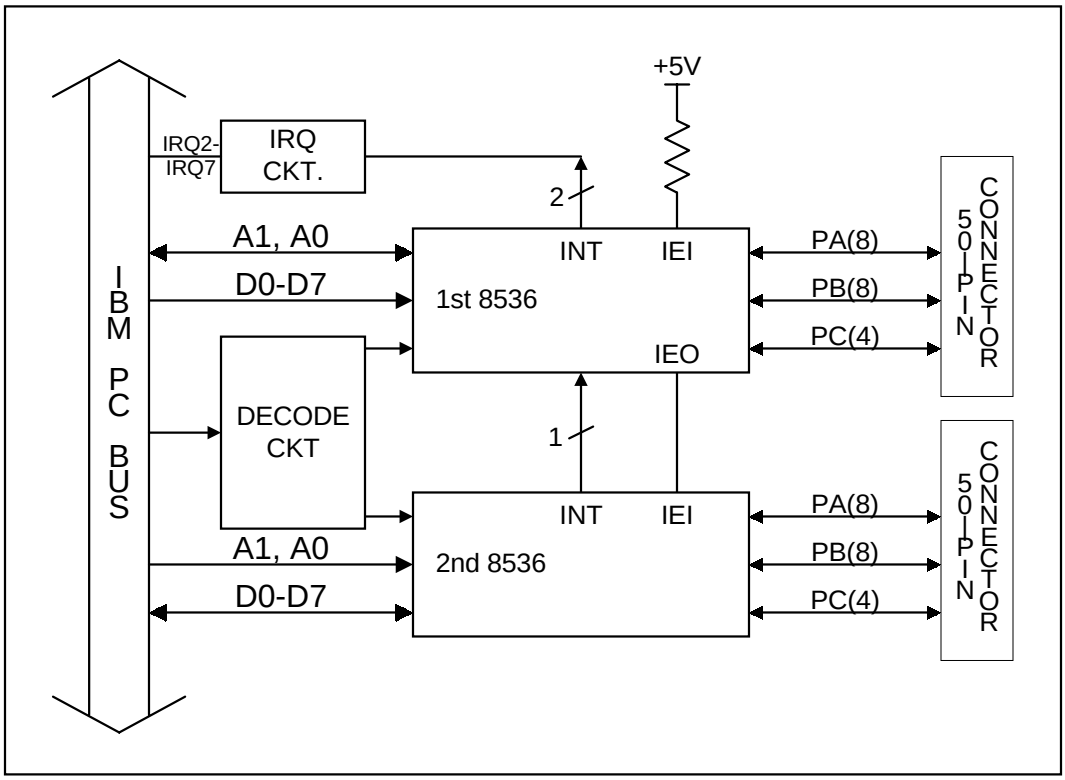
Appendix A PC I/O Port Mapping

I/O Port Address Range	Function
000 e 1FF	PC reserved
200 e 20F	Game controller (Joystick)
278 e 27F	Second parallel printer port (LPT2)
2E1	GPIB controller
2F8 e 2FF	Second serial port (COM2)
320 e 32F	Fixed disk (XT)
378 e 37F	Primary parallel printer port (LPT1)
380 e 38F	SDLC communication port
3B0 e 3BF	Monochrome adapter/printer
3C0 e 3CF	EGA, reserved
3D0 e 3DF	Color/graphics adapter
3F0 e 3F7	Floppy disk controller
3F8 e 3FF	Primary serial port (COM1)

Appendix B Summary of Interrupt Levels

Interrupt Level	Usage
NMI	Parity, AT Channel Check
IRQ0	Interval Timer 1, Counter 0 Out
IRQ1	Keyboard Controller
IRQ2	Reserved (XT) Cascade Interrupts from IRQ8 to IRQ15 (AT)
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Hard Disk (XT) Parallel Port #2 (AT)
IRQ6	Floppy Disk
IRQ7	Parallel Port #1
IRQ8	Real Time Clock (AT)
IRQ9	Re-directed to IRQ2 (AT)
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	Unassigned
IRQ13	Coprocessor Error
IRQ14	Hard Disk
IRQ15	Unassigned

Appendix C Block Diagram

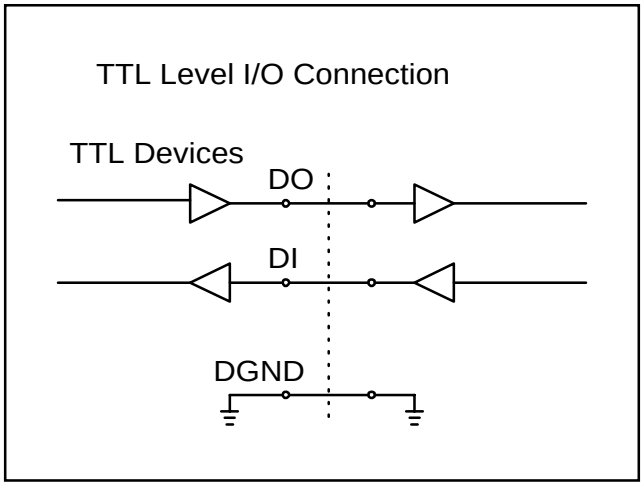


Appendix D Technical Reference

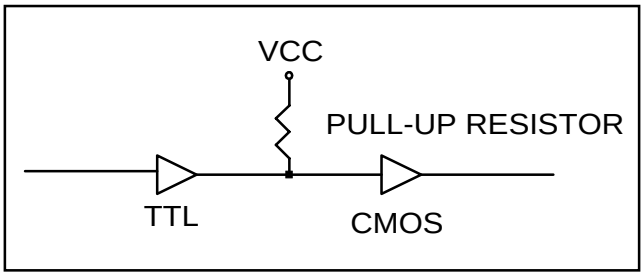
Digital Input and Output

Digital signals are used for detecting logical status or controlling devices. TTL level signals are usually developed by most DAS systems. Some application are given as follows:

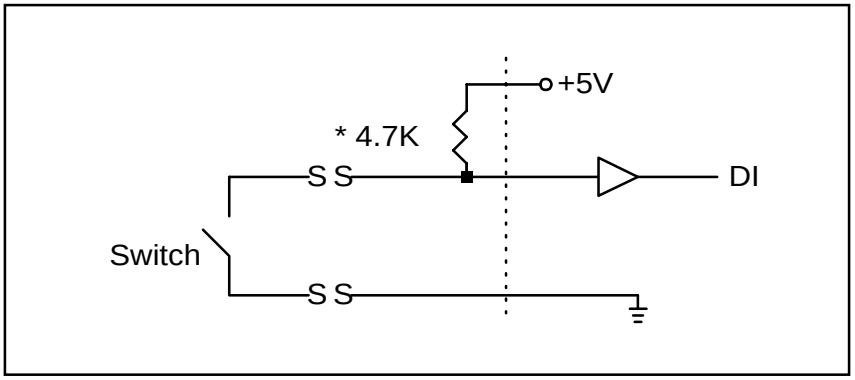
- **TTL or LSTTL Level I / O Connections**



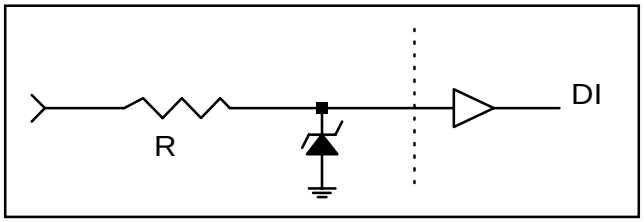
Connection with CMOS Device – Use a pull-up resistor if you wish to interface to CMOS devices. This will raise the logic high output level from its minimum TTL level of 2.4V to +5V suitable for CMOS interface.



Digital Input for Open/Short Switch Detection – A pull-up resistor must be connected, especially at long distance wiring, to ensure logic high input level.



Digital Input for Large Signal



Digital Output for Relay Driving - The D1 diode is added to protect the IC driver against the inductive "kickback" from the relay coil.