FPGA Advantage with LeonardoSpectrum Tutorial

Software Version 6.1

4 June 2003

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About This Manual

This manual is a printable Acrobat PDF version of the *FPGA Advantage with LeonardoSpectrum Tutorial.*

The screen shots and path name convention (/) are the same as those used in the Windows environment. The screen shots shown in the Windows environment will look different to the ones that will appear when using the tutorial with UNIX workstations. However, the design flow is the same for any configuration on all platforms.

FPGA Advantage Tutorial

Welcome to FPGA Advantage

This simple tutorial presents a complete design flow using a sample text design and Text HDL import, HDL generation, and simulation through to synthesis in approximately 30 minutes.

You should have installed at least one configuration of FPGA Advantage and obtained your evaluation or permanent licenses before starting this tutorial. Temporary evaluation licences can be obtained for FPGA Advantage from the FPGA Advantage website.

The design used in the *FPGA Advantage with LeonardoSpectrum Tutorial* is based on HDL code recovered using HDL2Graphics technology. You can choose to complete the tutorial by using either VHDL or Verilog languages.

Invoking on Windows

You can invoke your installed configuration of FPGA Advantage on Windows by double-clicking the shortcut which was created by the install program on your desktop. Alternatively, you can choose the same shortcut from the **FPGA Advantage 6.1** cascade of the **Programs** menu.

For example:

Start > **Programs > FPGA Advantage 6.1** > **FPGAdv with LS**

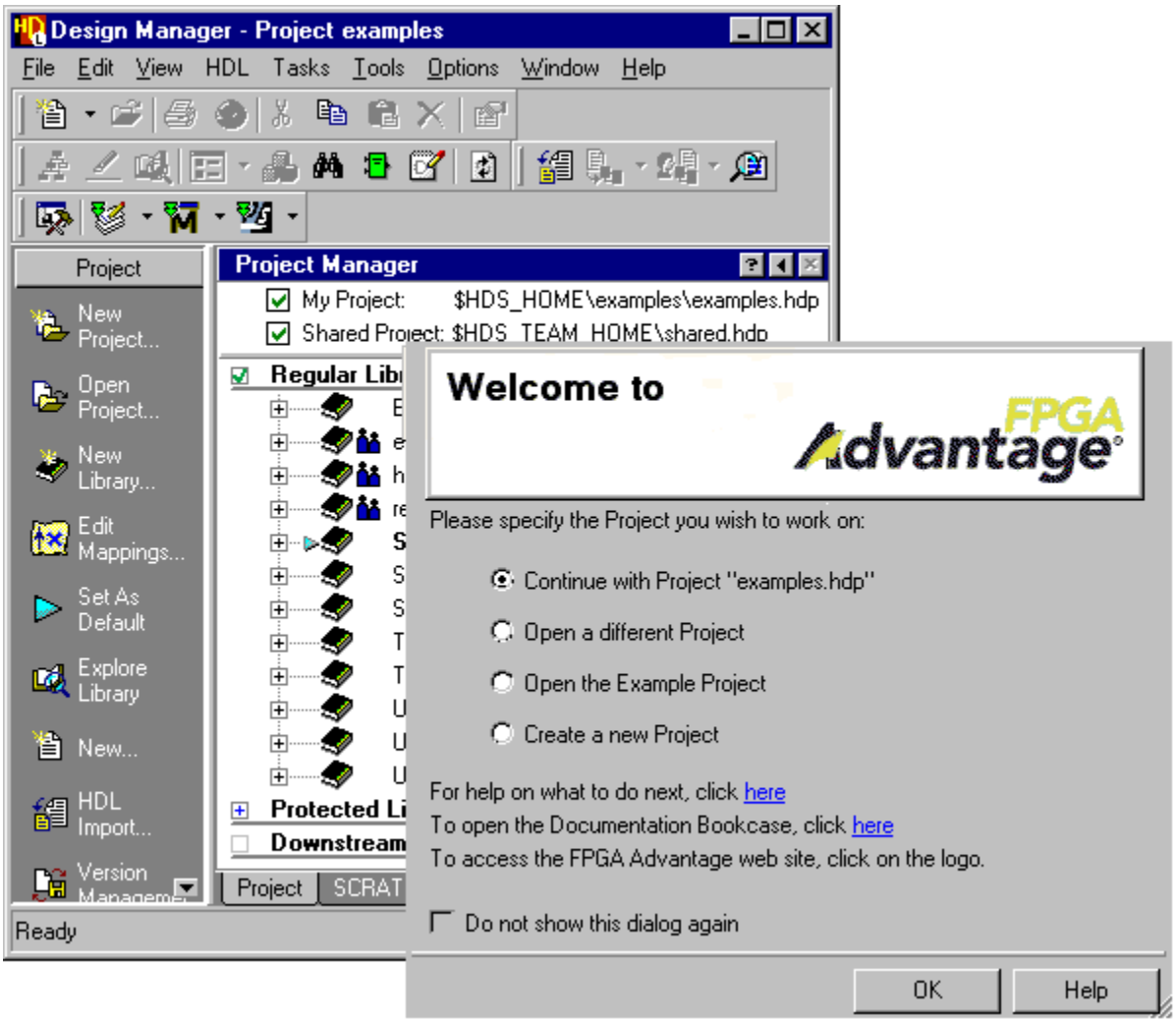
Invoking on UNIX or Linux

When you install FPGA Advantage on UNIX or Linux systems, invoke scripts are created for each configuration in the install program as shown in the table below. The scripts and corresponding shortcut links are located in the following subdirectory of your installation: *<install_dir>/Fpgadv/bin*

Configuration	Script
FPGA Advantage with LeonardoSpectrum	*fa_with_ls*
FPGA Advantage with Precision Synthesis	*fa_with_ps*
FPGA Advantage with LeonardoSpectrum and Precision Synthesis	*fa_with_ls* *fa_with_ps*
FPGA Advantage with Precision Physical Synthesis	*fa_with_pp*

Refer to the *FPGA Advantage Start Here Guide* to see a full list of configurations supported with FPGA Advantage 6.1.

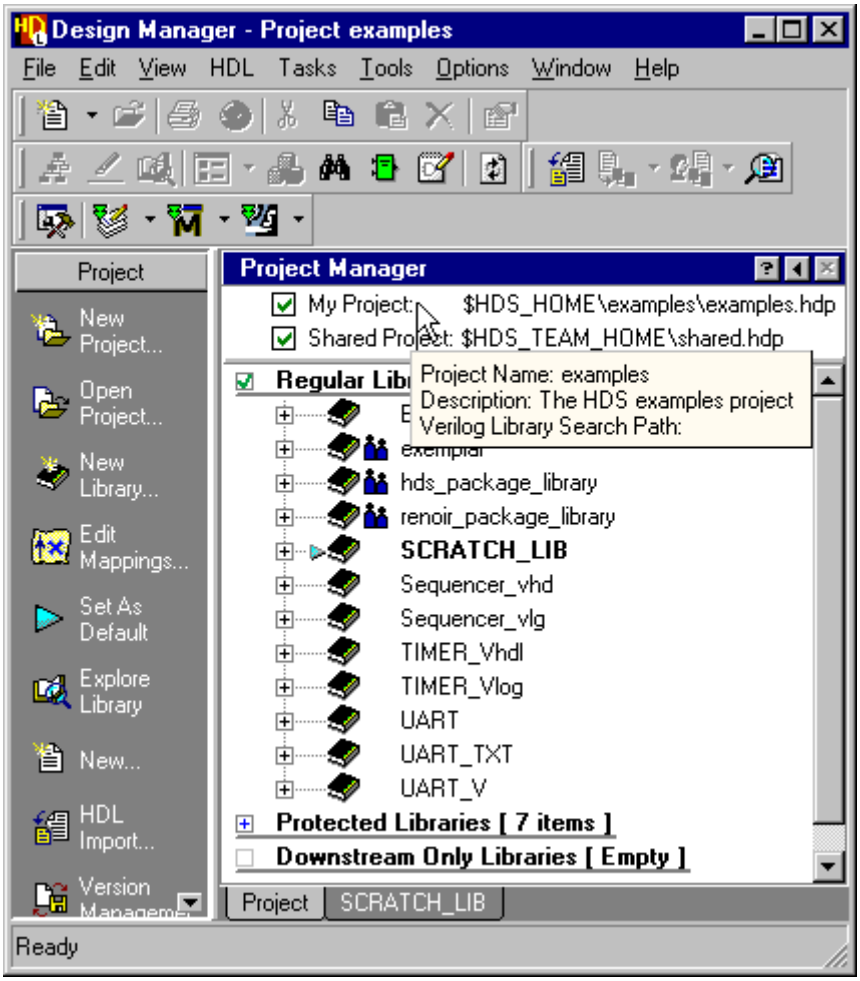
When FPGA Advantage is first invoked, the HDL Designer Series (HDS) Design Manager will be displayed showing the FPGA Advantage Welcome screen:



Click the **OK** button to remove the Welcome screen.

Exploring The Designs

The Design Manager is divided into two browsers. The first browser shows the **Project Manager** with several example designs shown in a list of **Regular Libraries.** The designs include a mixed language HDL text design named *UART_TXT*, a graphical VHDL design named *UART* and the corresponding graphical Verilog design named *UART_V*.



The details of the current user project, **My Project** is shown inside the tooltip in the screenshot above. By default, the examples directory appears as the current project when FPGA Advantage is first invoked.

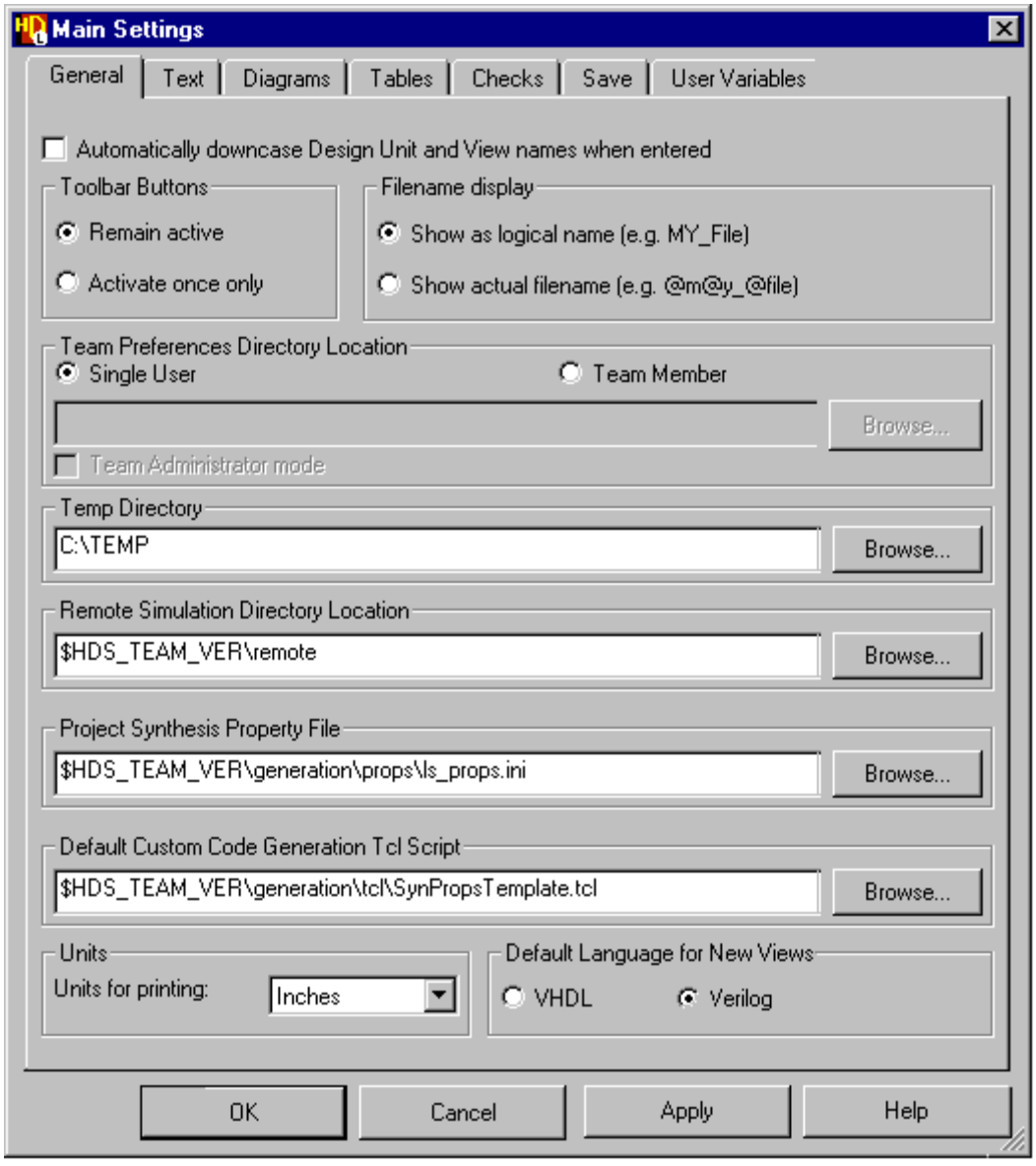
For example: `$HDS_HOME\examples\examples.hdp`

The second browser named **Project** lists the current active shortcuts you can use in the Project Manager. The remaining shortcuts become available when you open different windows in the Design Manager.

Protected Libraries: contain reusable design objects or standard packages which are not generated or recompiled.
Downstream Only Libraries: contain compiled data. For example from Model*Sim* and Precision Synthesis.

Set the Default Language

Choose **Main** from the **Options** menu to display the Main Settings dialog box. Select **Verilog** as the default language for all new diagrams. Click the Apply button to confirm your language choice and then OK to close the dialog box.

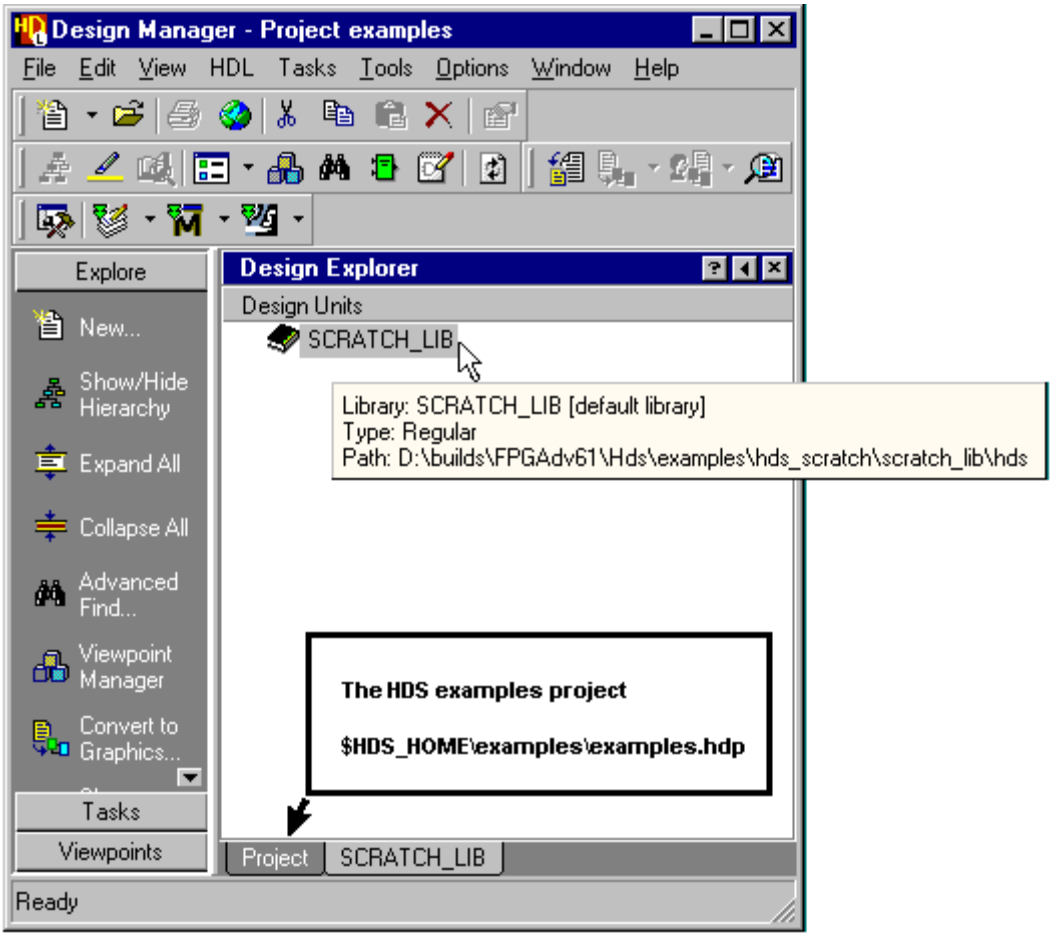


The *FPGA Advantage with LeonardoSpectrum Tutorial* can be completed using either Verilog or VHDL languages. For the purposes of this tutorial the Verilog language has been selected.

Open Library

Double-click the *SCRATCH_LIB* library shown in the list of **Regular Libraries** in the **Project Manager**.

The Design Explorer now shows the empty *SCRATCH_LIB* library.



The *SCRATCH_LIB* library will be used to import an example design using HDL Import.

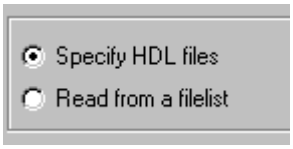
Notice the path shown inside the tooltip now shows the directory where FPGA Advantage is installed.

Import the Fibonacci Design

This tutorial uses a Fibonacci sequencer design which can be imported as either VHDL or Verilog code. The design is imported using the HDL Import Wizard which recovers the VHDL or Verilog code using HDL Import technology. The code is converted into HDS text views and displayed in the *SCRATCH_LIB* library in the Design Explorer.

Click the  button on the Design Manager toolbar to invoke the HDL Import Wizard. Alternatively, choose **HDL Import** from the **HDL** menu.

Select **Specify HDL files** in the first page of the HDL Import wizard:



This tutorial can be completed using either the VHDL or Verilog example code depending upon your language preference. The language will be determined automatically providing that the source code file extension is recognized in the general preferences.

Click the **Next** button to display the **Specify HDL Source Files** page of the **HDL Import** Wizard.

Select Source HDL Files

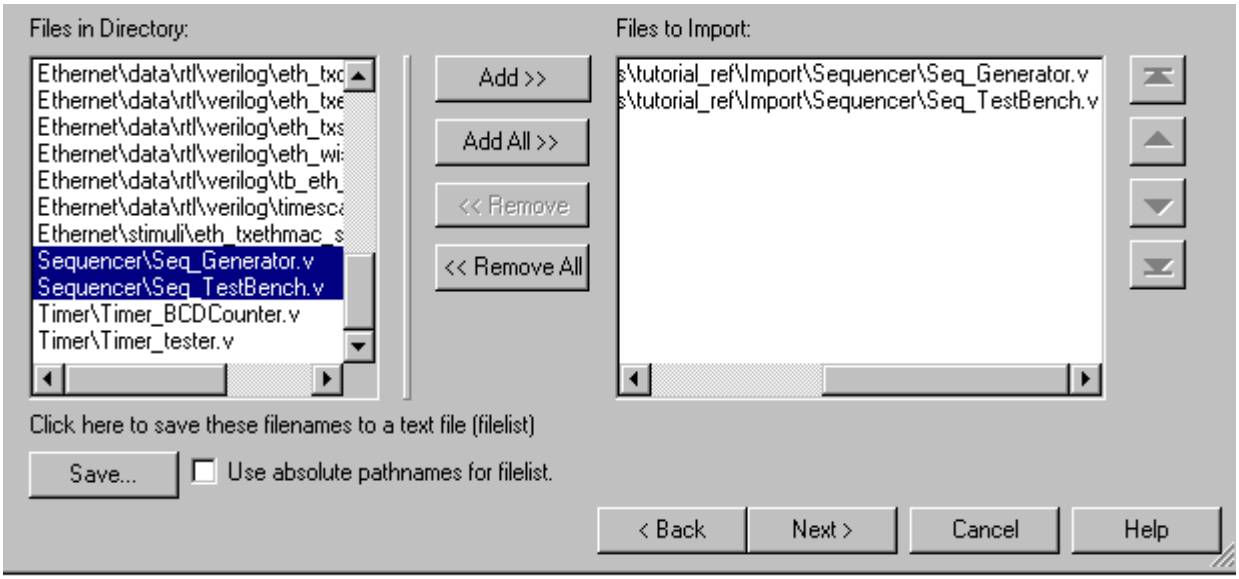
Use the **Browse** button to locate the Fibonacci sequencer source code in the examples sub-directory of your FPGA Advantage installation as shown in the **Directory** entry box below. For example, if FPGA Advantage has been installed in the directory D:\Builds\FPGAdv61, the pathname to locate all source HDL files would be:

```
D:\Builds\FPGAdv61\Hds\examples\tutorial_ref\Import
```

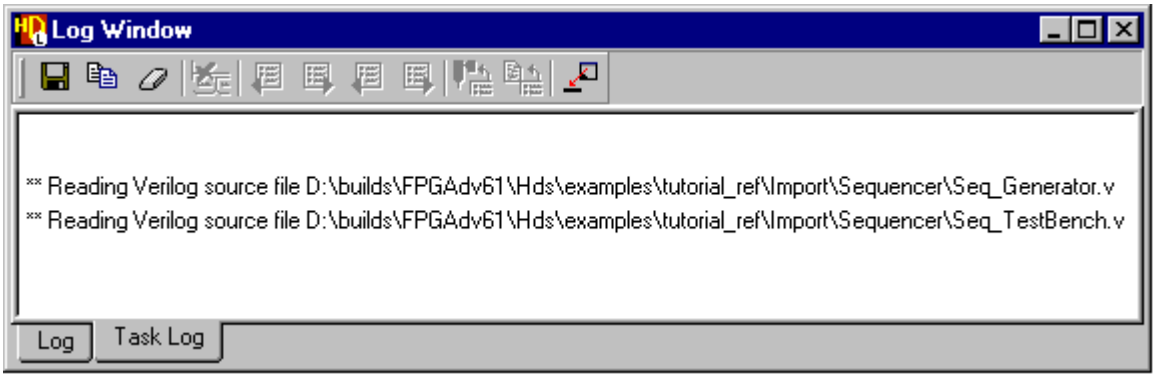
Use the **Files of type** pulldown to select either VHDL or Verilog files. For example, Verilog files are shown for the purposes of this tutorial:

Check the **Search Sub Directories** check box.

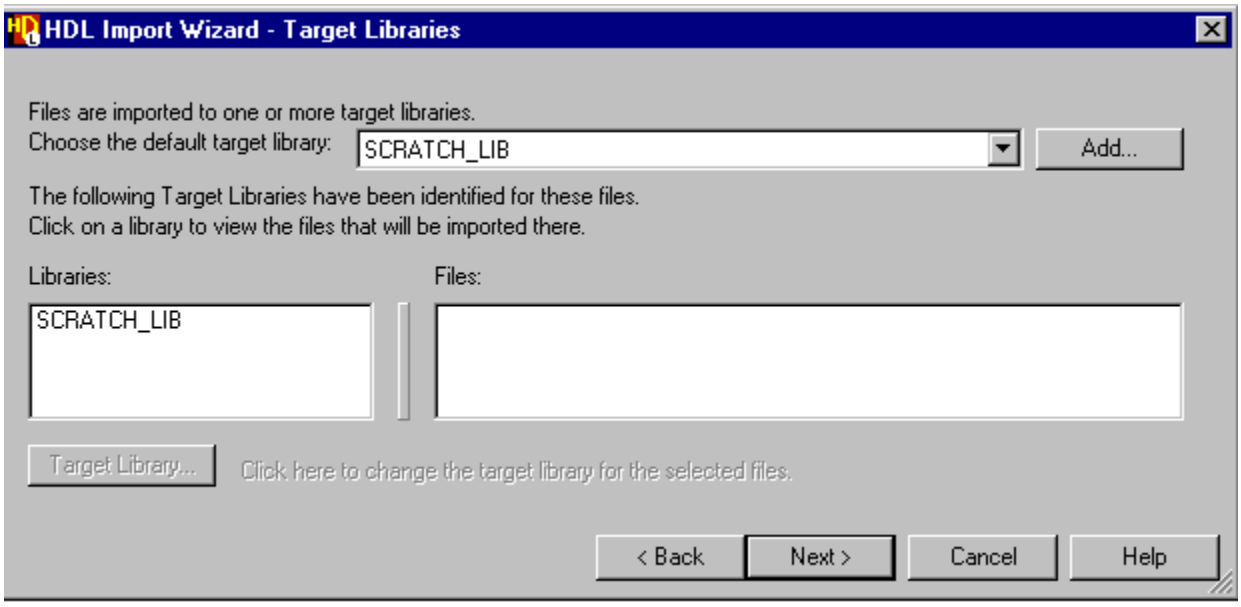
Select the *Sequencer\Seq_Generator* and the *Sequencer\Seq_TestBench* HDL files by using Ctrl + Left mouse button. Click Add >> to convert the files.



Click the **Next** button. You will now see the Log Window showing the Verilog source files for the Fibonacci design as they are read in:

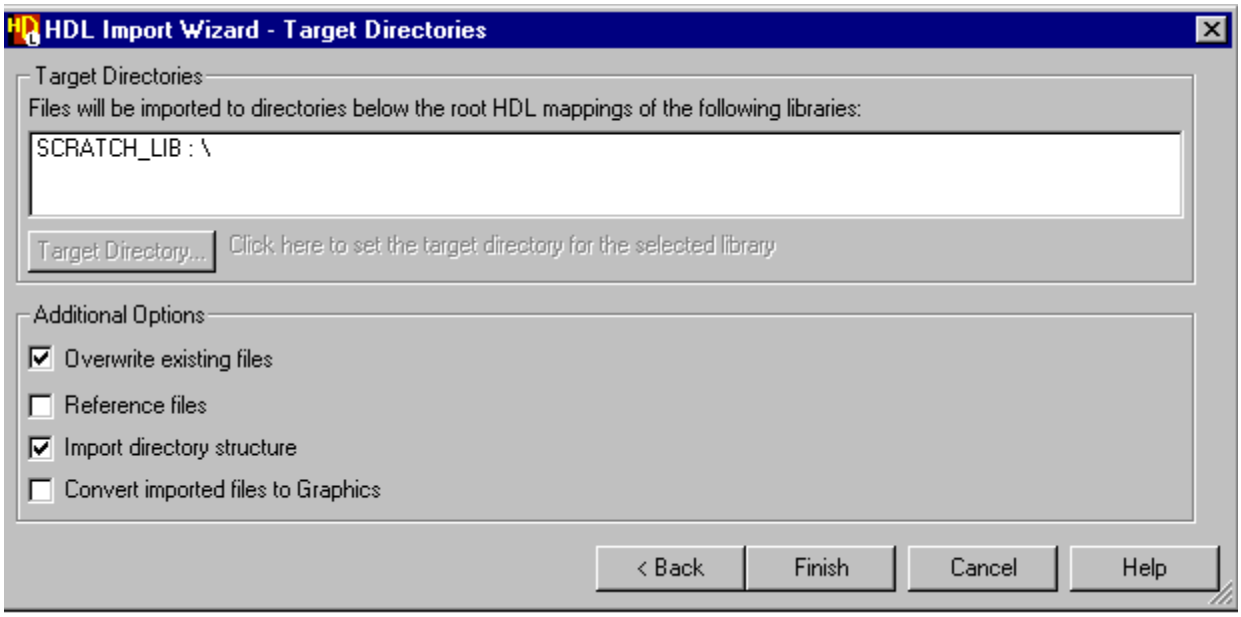


The HDL Import Wizard Target Libraries dialog box appears showing the *SCRATCH_LIB* library as the default target library.



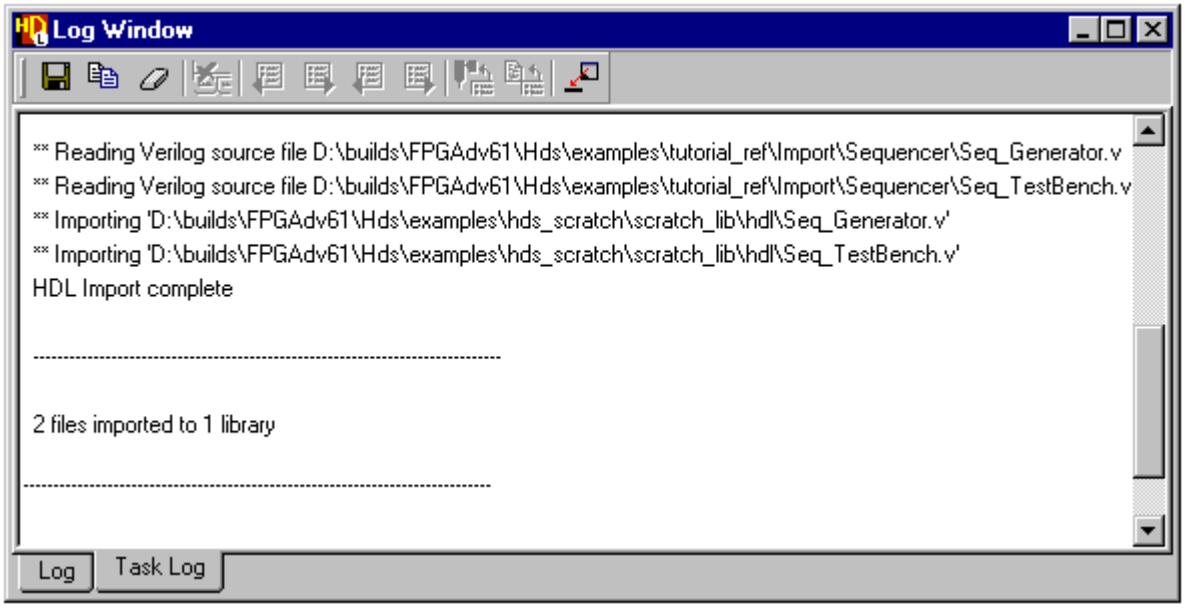
Click the **Next** button.

The HDL Import Wizard Target Directories dialog box appears showing where the imported files will appear below the root HDL mapping:



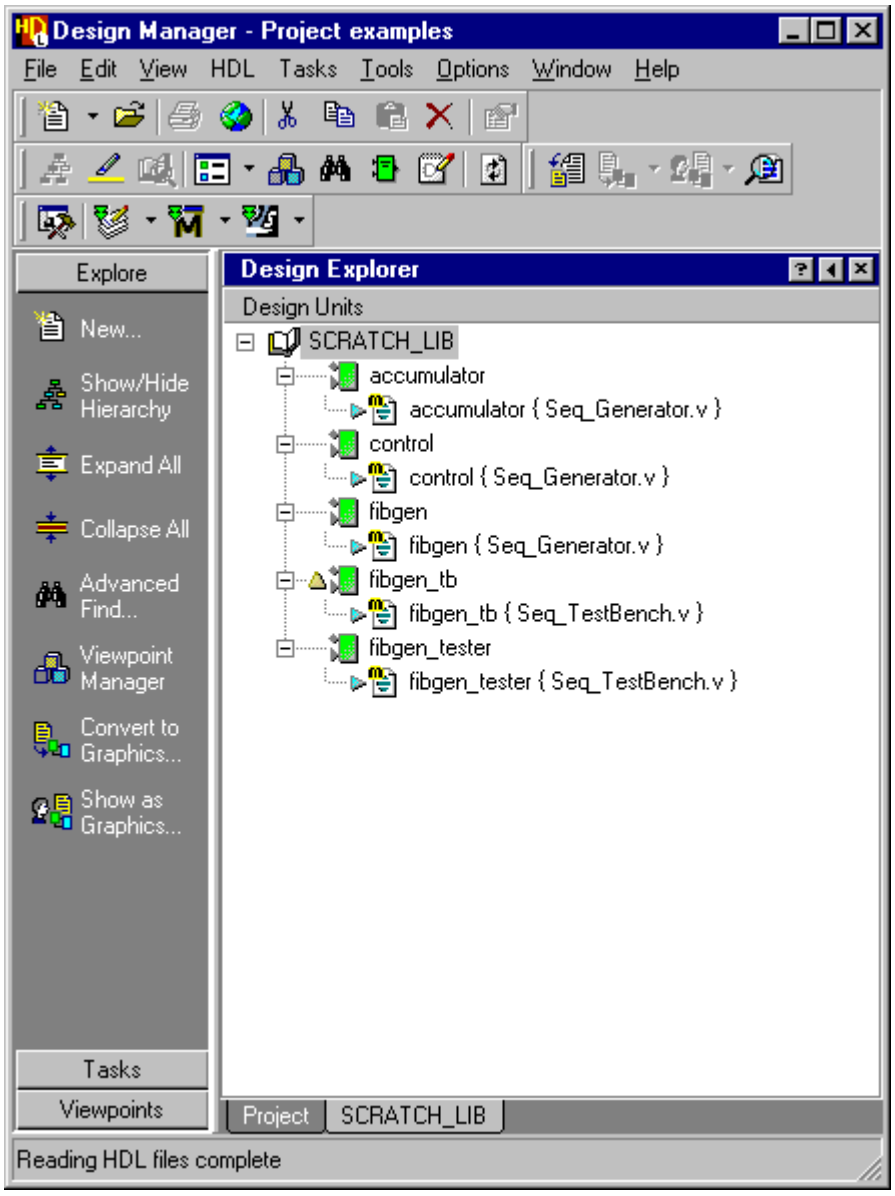
Click the **Finish** button.

The HDL Log Window will indicate that a hierarchy of designs is being automatically created for the Fibonacci design. The Log Window will show the following summary report:



Browsing the Fibonacci Design

Select the *SCRATCH_LIB* library in the Design Manager. Click the right mouse button and choose **Expand All** from the popup menu. The design units for the Fibonacci design should now be displayed in the Design Explorer as shown below:

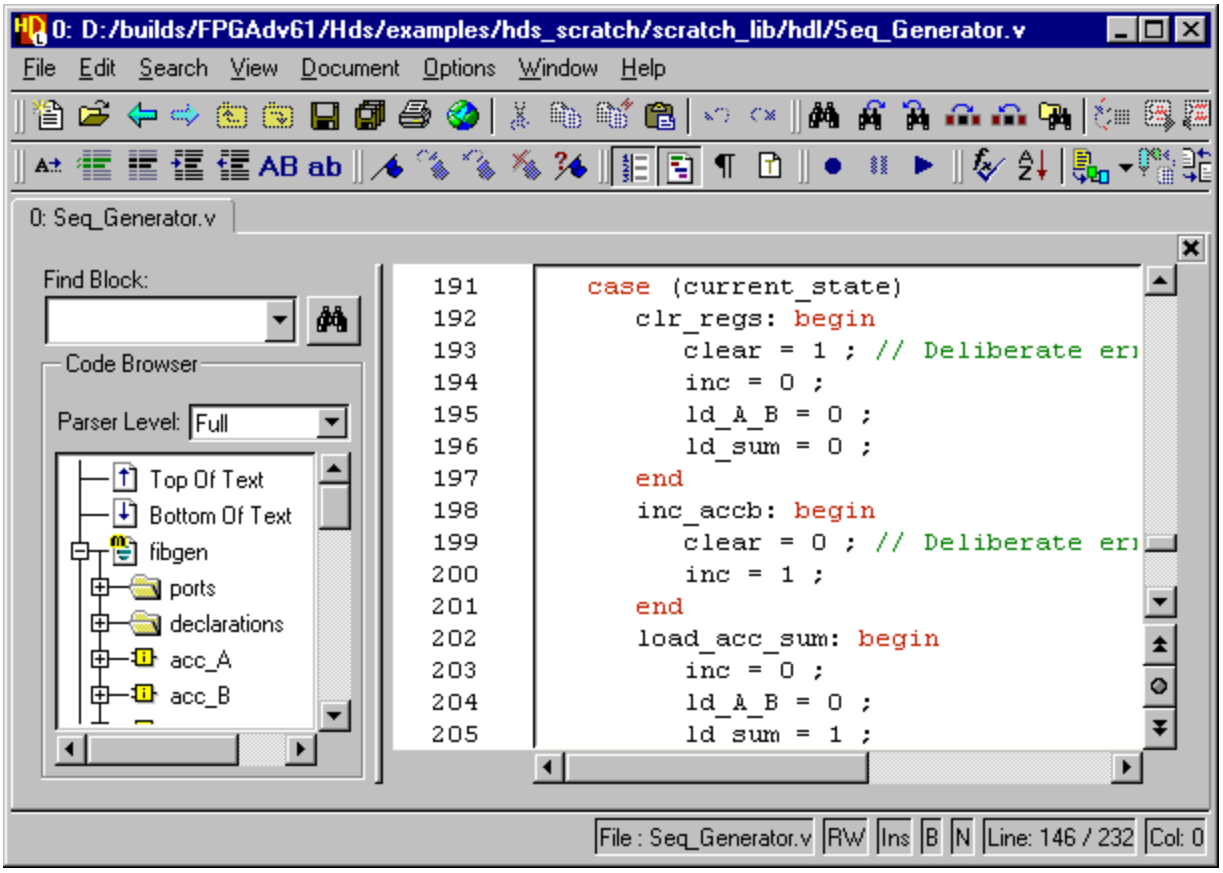


Examine the State Machine Text View

Double-click on the icon representing the *control* component design unit in the Design Explorer which will display the state machine shown in the DesignPad text editor.

Use the scroll bar to view the Verilog code and notice that there are two deliberate errors which have been added on the following lines:

193 clear = 1 ; // Deliberate error, signal is declared as clr
199 clear = 0 ; // Deliberate error, signal is declared as clr



The deliberate errors will appear on lines 195 and 200 in the VHDL version of the state machine code.

Close the text editor by choosing either **Close Window** from the **Window** menu or you can use the keyboard shortcut Ctrl + F4.

Correct the State Machine Errors

Select the component design unit icon for *fibgen_tb* which is displayed with a "top of design" marker in the HDS Design Manager.

Press the ModelS*im* Flow button on the Design Manager toolbar.

Notice that the HDS Log Window now displays a single error message. This represents the two deliberate errors shown in the previous topic.

When using the VHDL language a total of seven errors are displayed in the Log Window.

Make the Log Window active and double-click on the error message. DesignPad will now appear allowing you to edit the errors in the state machine source code.

Correct both of the errors by replacing the word *clear* with *clr* and delete all of the comment text after the semi-colon. Repeat this procedure for the second occurrence of the error.

The modified Verilog code should look similar to the example shown below:

```
clr_regs: begin
   clr = 1 ;
   inc = 0 ;
   ld_A_B = 0 ;
   ld_sum = 0 ;
end
inc_accb: begin
   clr = 0 ;
   inc = 1 ;
end
```

Click the button on the DesignPad toolbar to save the edited source file.

Close DesignPad by choosing either **Close Window** from the **Window** menu or you can use the keyboard shortcut Ctrl + F4.

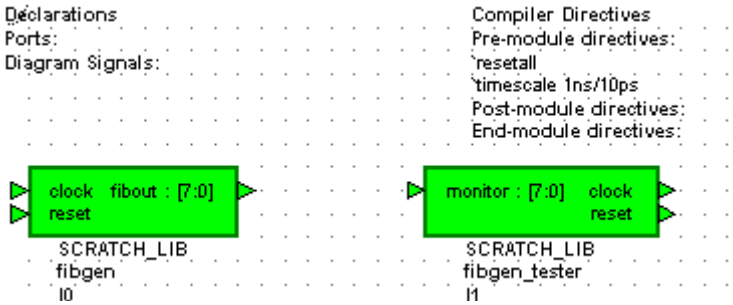
Close the Log Window.

Create Graphical Test Bench

From the Design Manager click the button and choose **Specified** from the pulldown menu. The File Creation Wizard appears prompting you to specify a file type. Double-click **Block Diagram** from the **File Types** list to open the diagram. Alternatively, select **Block Diagram** and click **Finish** on the dialog box.

An Untitled block diagram appears. Click the button on the block diagram toolbar to display the Component Browser showing the Fibonacci design.

From the Component Browser select the *fibgen* component, hold down the left mouse button and drag the component onto the block diagram. Repeat this procedure for the *fibgen_tester* component. The diagram should look similar to the one shown below:



Close the component browser.

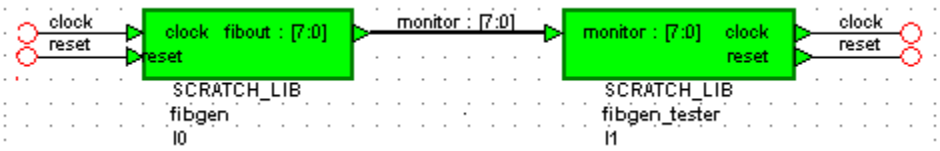
Select the *fibgen* component and use the right mouse button to choose **Add Signal Stubs** from the popup menu. The Add Signal Stubs dialog box appears prompting you to choose the type of ports that require signal stubs. Click OK to accept the default setting and notice that two signals, *clock* and *reset* are added to the diagram plus a bus named *fibout.*

Repeat this procedure for the *fibgen_tester* component. The WARNING messages which appear can be ignored. This is because the net *clock* and *reset* already exist and the port and net declarations differ. Click OK to acknowledge the warning message.

Note from the diagram that two further *clock* and *reset* signals have been added plus a second bus named *monitor.*

Select and delete the bus *fibout*. Drag and connect the bus *monitor* to the port *fibout.*

The finished diagram should look similar to the one shown below:



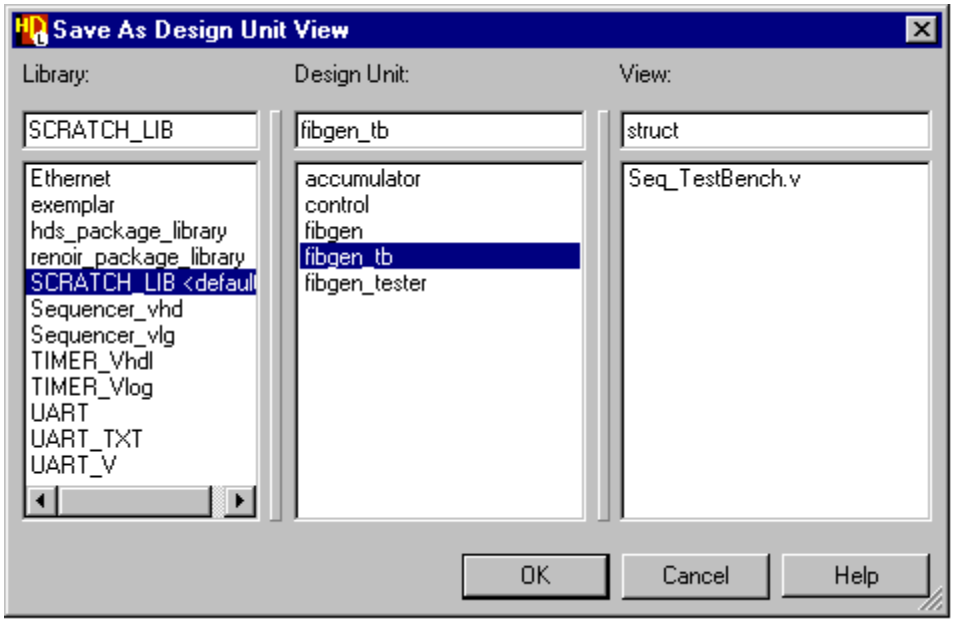
It is not necessary to explicitly connect the *clock* and *reset* signals between each port on the component and tester as these are implicitly connected by name.

Save the Test Bench

Use the button to save the test bench. The Save As Design Unit View dialog box is displayed which allows you to save a design unit into any currently mapped library. The columns allow you to specify the design unit name with its default view type.

The *SCRATCH_LIB* library appears by default (as shown).

Save the **Design Unit** name as *fibgen_tb*. The Save As Design Unit View dialog box should look the same as the example below:



Click the OK button to save the test bench.

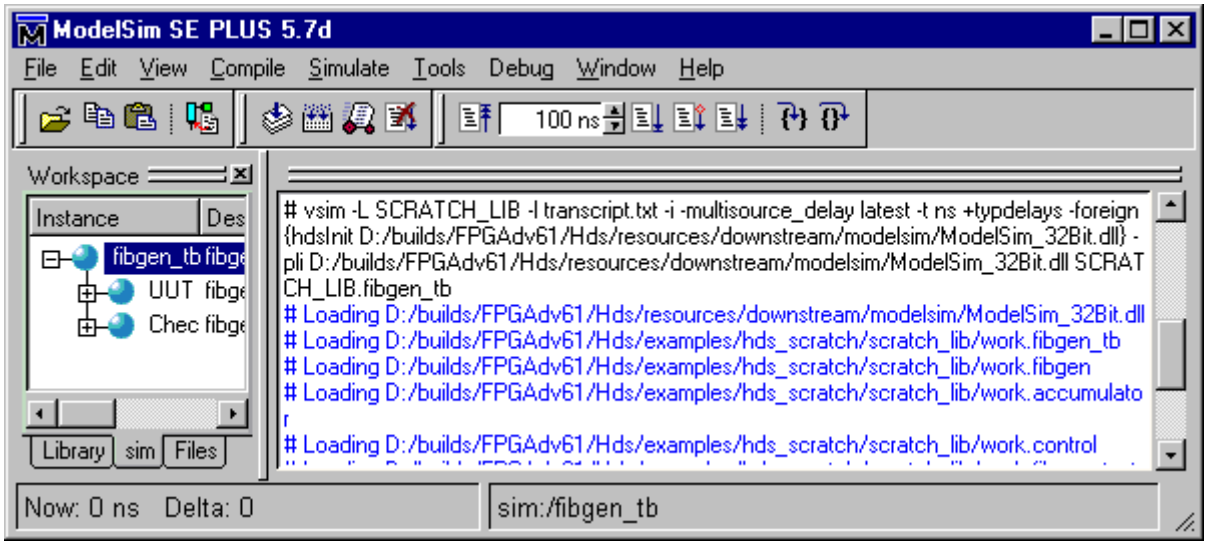
Simulate Your Design

Select the *struct* view below *fibgen_tb* from the Design Manager and choose **Set Default View** from the popup menu. This will define the graphical test bench view *struct* as the default view before simulating the design. A blue triangle now appears next to *struct* indicating that it is now the default view.

Select the *fibgen_tb* component and select the button from the toolbar which will set up and automatically generate and compile HDL for the hierarchy below the selected design unit. The Start Model*Sim* 5.5-5.7 dialog box will now appear.

Ensure that the **Enable Communication with HDS** option is set and click the OK button to confirm the dialog box.

If generation and compilation are completed successfully, the Model*Sim* simulator is invoked and the entire compiled design is loaded. Messages will now appear in the HDS Log Window confirming that the HDL has been compiled for all the HDS design units.



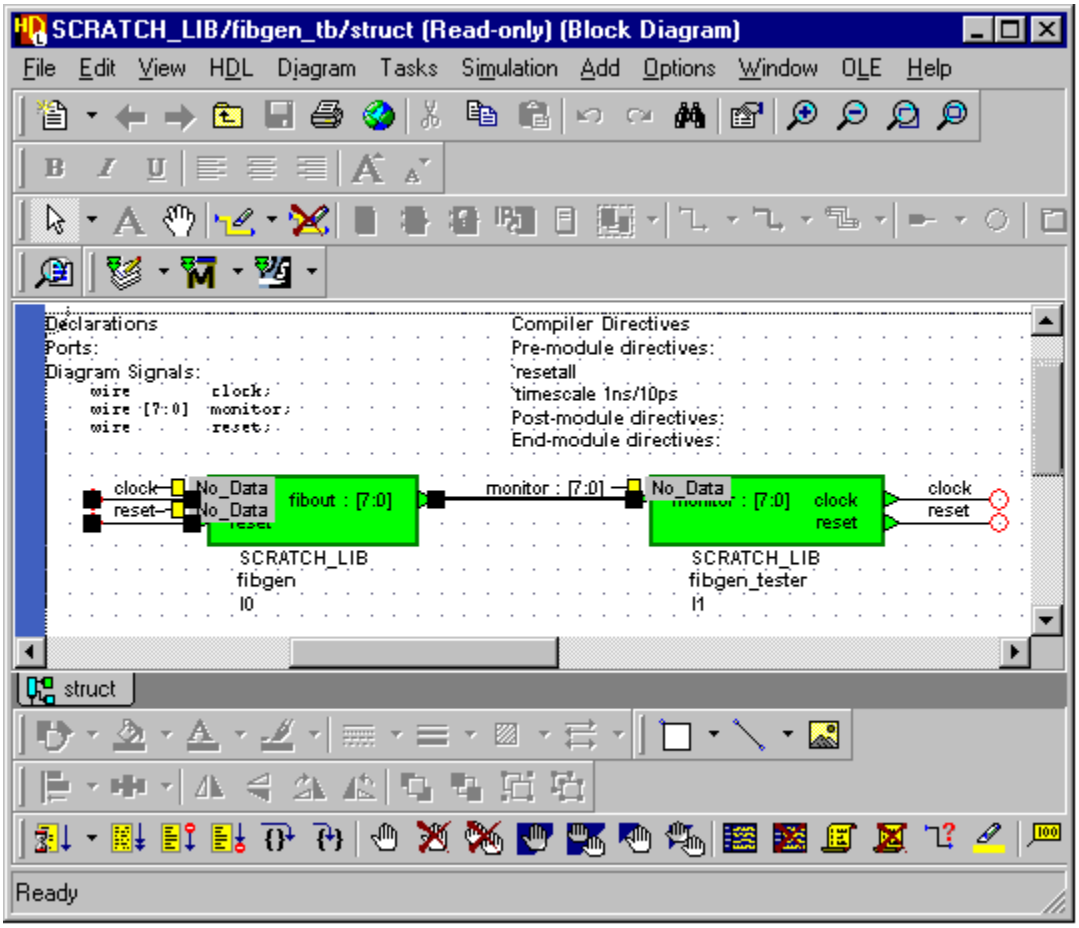
The progress of HDL generation and compilation are shown in the HDS Log Window. Notice that most design units are generated but all design units are compiled. If any compilation errors are detected when you compile a design, you can cross-reference from the HDS Log Window to the source graphics or generated HDL in the same way as for HDL generation errors.

Add Probes to the Test Bench

Make the *fibgen_tb* block diagram active.

You can select multiple signals by using Shift + Left mouse button or by dragging a box crossing the required signals.

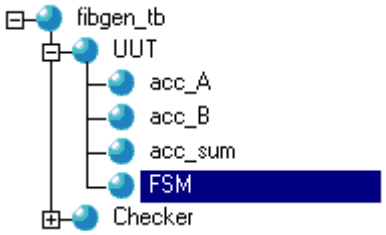
Select the two signals *clock* and *reset* and the bus *monitor* as shown in the diagram.



Notice that when the simulator is invoked there is an additional simulation toolbar displayed at the bottom of the HDS block diagram. Click the button to add simulation probes showing the current value of each signal.

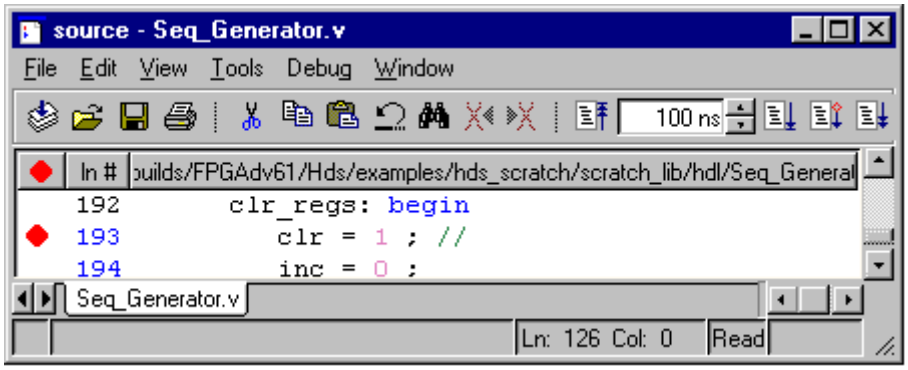
Add a Breakpoint

In the *fibgen_tb* block diagram view, choose **Structure** from the **View** cascade of the **Simulation** menu in the design browser. A window showing the *fibgen_tb* hierarchy will appear. Expand the hierarchy underneath *UUT* and select the *FSM: control* view.



The VHDL version of the *fibgen_tb* hierarchy is shown underneath *iO*:

In the *fibgen_tb* block diagram view, choose **Source** from the **View** cascade of the **Simulation** menu to open the state machine source window as shown below. Navigate to line 193 and use the left mouse button to add a breakpoint to the line. Alternatively, choose the right mouse button and select **Enable Breakpoint 193** from the popup menu. A red dot will be shown indicating that a breakpoint is now set on line 193.

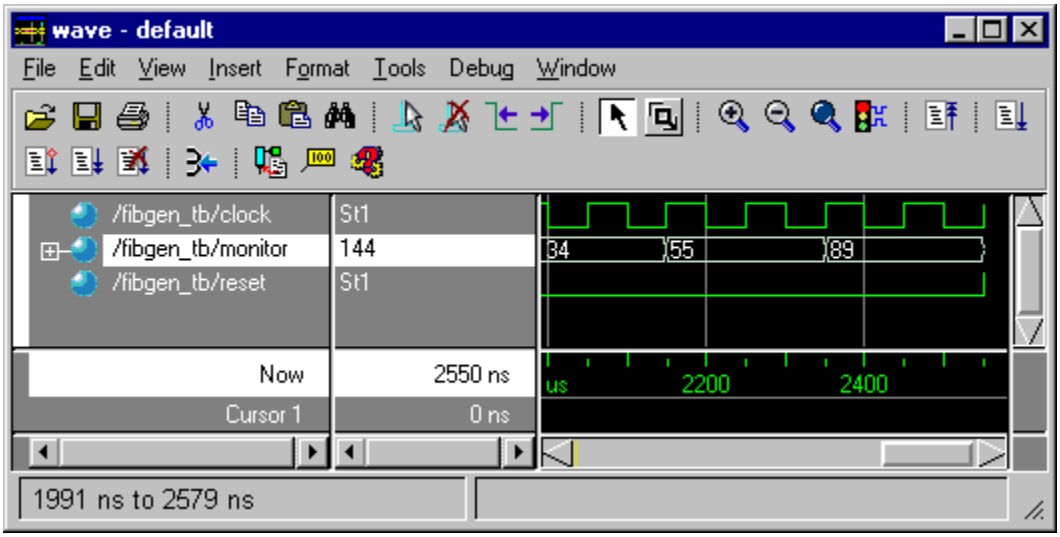


Line 195 is used to set the breakpoint when the VHDL language is used.

```
195     clr <= '1' ;
196     inc <= '0' ;
```

Run the Simulator

Make the *fibgen_tb* block diagram active and ensure that the bus *monitor* and the signals *clock* and *reset* are selected. Click the button to automatically open the Model*Sim* Wave window. Select the *fibgen_tb/monitor* bus as shown, and press the right mouse button and choose **Unsigned** for the **Radix** cascade of the popup menu.



In the *fibgen_tb* block diagram view click the pulldown next to the button and choose **run 100** from the popup menu to advance the simulation by 100 nanoseconds. Notice that the signal values are initialized in the simulation probes on the test bench block diagram.

Click the button to run the simulator until the next breakpoint. Notice that the waveform appears as the simulation advances. Notice that a blue arrow appears over the red dot in the *Seq__Generator.v* source window.

Finally, make sure that the *Seq__Generator.v* source window is active and remove the breakpoint by choosing **Remove Breakpoint 193** from the popup menu.

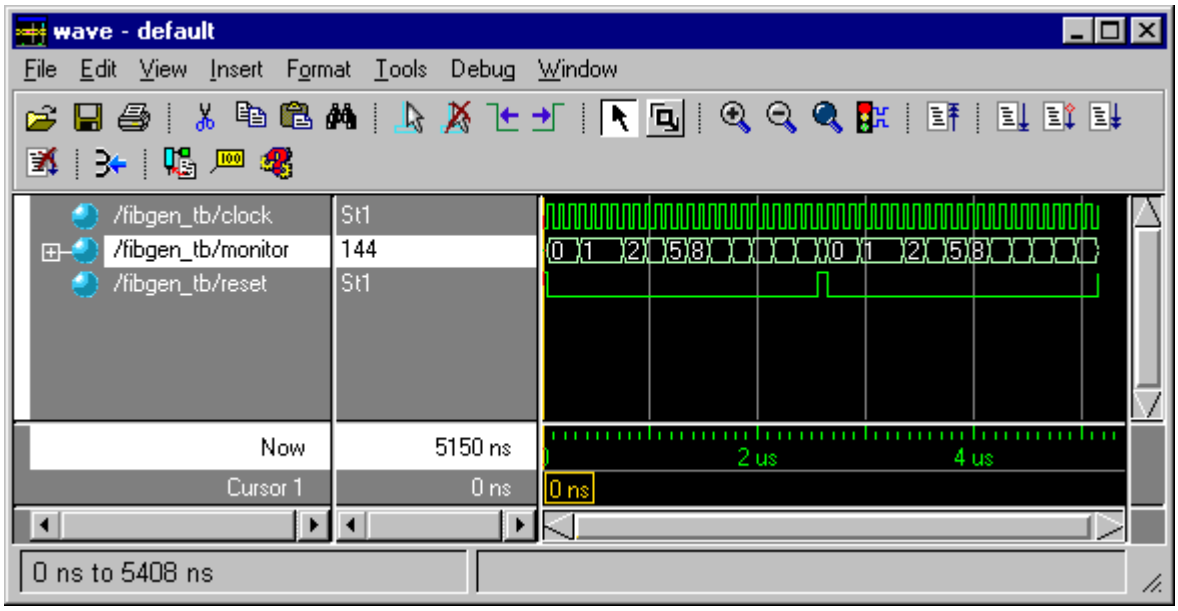
Alternatively, choose **Breakpoints** from the **Tools** menu. A dialog box will appear showing all breakpoints currently set. Select the breakpoint which appears on line 193 and press the **Delete** button. Click **OK** to close the dialog box.

Complete the Simulation

In the fibgen block diagram click the button adjacent to the button on the toolbar and select **Choose** from the popup menu. Another dialog will appear prompting you to enter a time interval to run the simulator. Enter 3000 into the entry box and click **OK** to run the simulator.

Alternatively, you can enter a time interval in the Model*Sim* window and then run the simulator.

Make the Model*Sim* Wave window active and choose **Zoom Full** from the **Zoom** cascade of the **View** menu. This will display the full simulation waveforms which should look similar to the picture below for a successfully verified design.

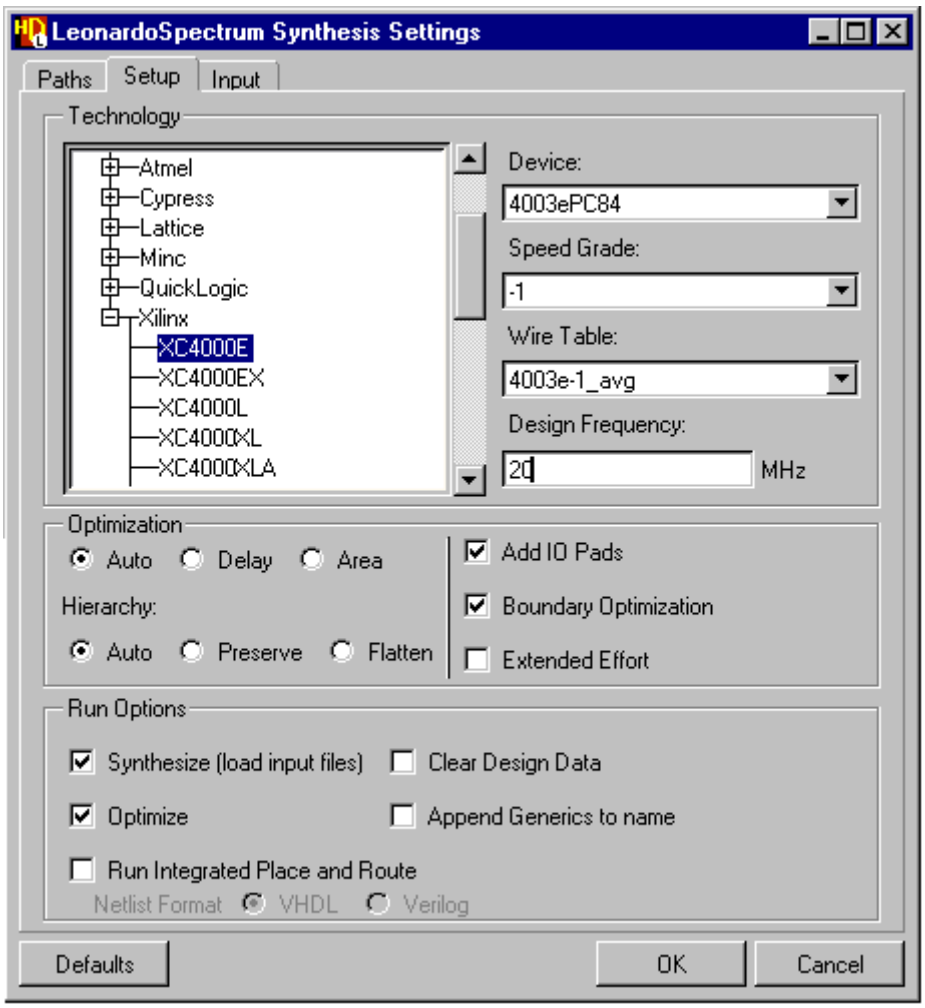


Simulation is now complete. Choose **Quit** from the Model*Sim* **File** menu to exit from the simulator. Click **Yes** to the exit message. Close the fibgen_tb block diagram.

Invoke LeonardoSpectrum

Select the *fibgen* component in the HDS Design Manager and then click on the button. The LeonardoSpectrum Invoke Settings dialog is displayed. Select the technology of your choice in the **Quick Setup** tab.

For example, choose FPGA and Xilinx XC4000E by using the ⊞ buttons to expand the list of FPGA technologies available.



You cannot synthesize a test bench, so you must select the top level design unit of the actual design you want to synthesize.

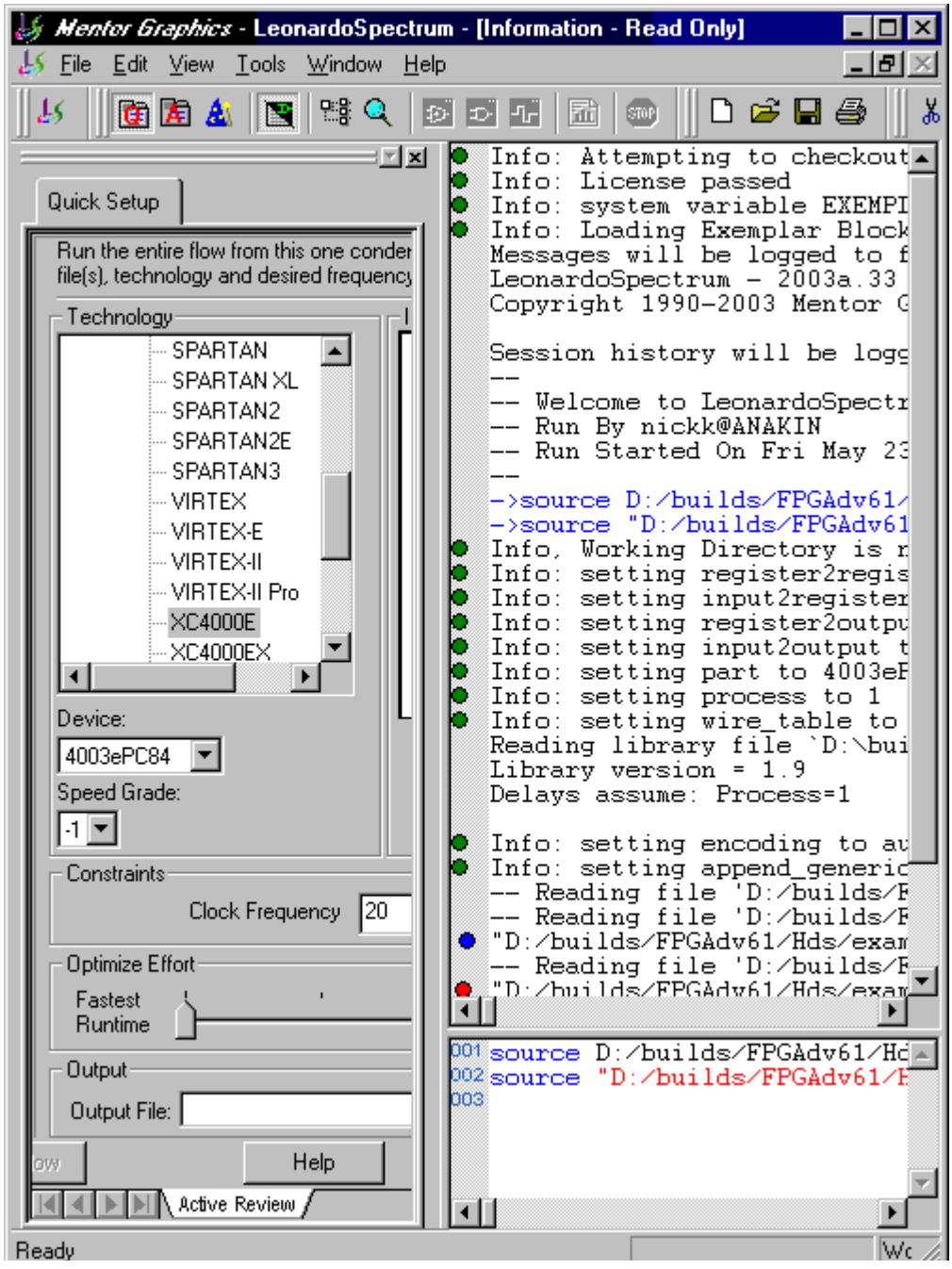
When you select a technology, default values are automatically entered in the **Device Speed Grade** and **Wire Table** fields (these may vary from the ones shown below). The remaining fields will be set by default. Enter the value **20** in the **Design Frequency** field and synthesize your design by clicking the **OK** button.

You are prompted to confirm the LeonardoSpectrum license.

You must choose a Level 2 license if you are using any of the *FPGA Advantage Personal* configurations. If you are using any of the *FPGA Advantage* configurations, select a Level 3 license. You can uncheck the **Run license selection next time** option if you want to run synthesis without prompting for the license level next time you invoke.

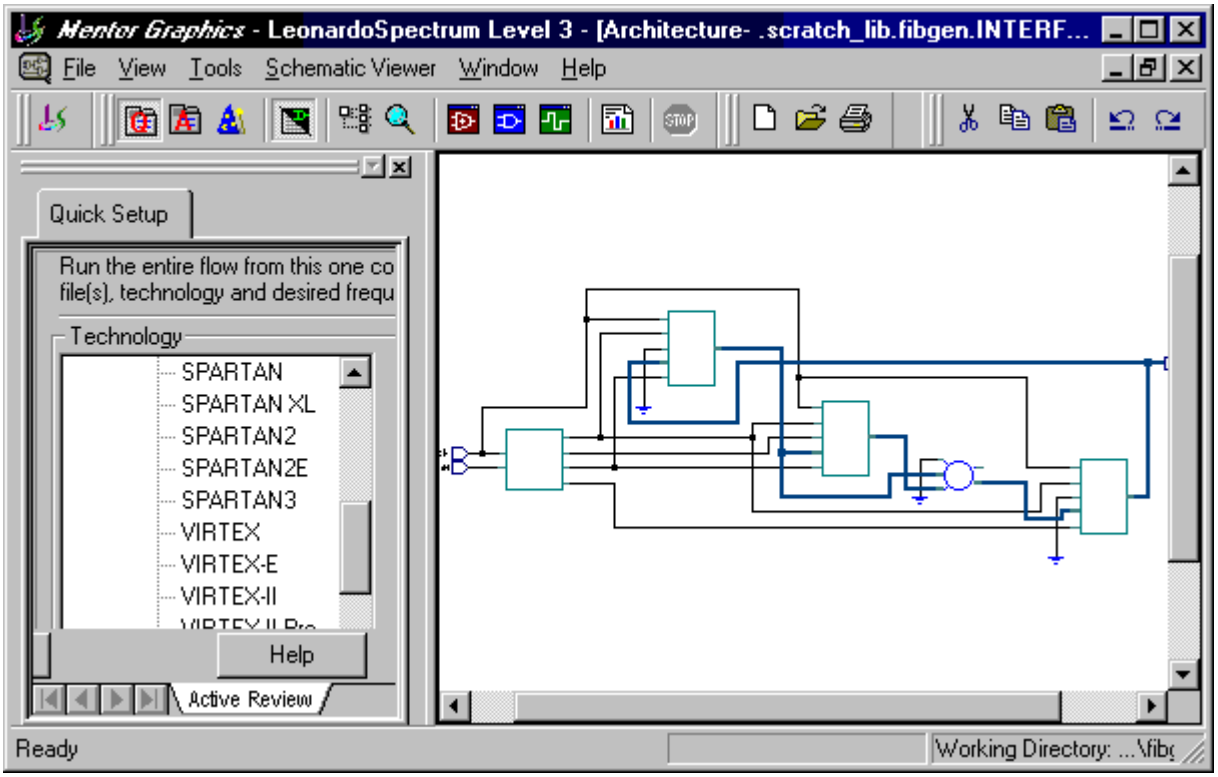
A Tip of the Day dialog box may appear. Click **OK** to clear the dialog box and LeonardoSpectrum is invoked on the entire design and the HDL files for your design are shown in the **Quick Setup** tab.

LeonardoSpectrum will optimize the design. Progress and completion messages will be displayed in the information window showing that the synthesis run has finished.



View the RTL Schematic

If you are using the Level 3 license for LeonardoSpectrum, you can display an RTL Schematic for your design by clicking the button. You can move around the schematic using the scroll bars and the diagram can be enlarged inside the browser by choosing **Zoom In** from the **Zoom** cascade of the **Schematic Viewer** pulldown menu.



You can cross-probe from the schematic to the corresponding object in an HDS source diagram. This is achieved by selecting an instance on the schematic and clicking the right mouse button. To view the HDS source diagram choose **Trace to HDL Designer** from the popup menu. The relevant HDS design unit view is displayed.

The Schematic Viewer is not available with a LeonardoSpectrum level 2 license. However, a license can be added if you obtain an additional license feature for LeonardoInsight.

Close the text editor windows and do the following:

Close the LeonardoSpectrum window by choosing **Exit** from the LeonardoSpectrum **File** menu, choosing **No** from the confirmation dialog box.

Close HDS by choosing **Exit** from the **File** menu in the Design Manager window and choosing **Yes** from the confirmation dialog box.

Further Information

You have now completed the FPGA Advantage *with LeonardoSpectrum Tutorial* and seen the complete design flow from importing HDL into HDS, through verification using the Model*Sim* simulator and used LeonardoSpectrum to synthesize a gate level netlist.

Each of these tools support a large range of features which cannot be illustrated in this simple tutorial. For more information, see the documentation which is available from the **Help** menu in each tool.

You can also access documentation from the **FPGA Advantage 6.1 > Bookcase** which can be opened on Windows platforms from the **Programs** cascade of the **Start** menu.

You can access this document on UNIX by opening the PDF document named *DocIndex.pdf* which can be found in the FPGA Advantage installation at: `<install_dir>/Doc/DocIndex.pdf.`

The **FPGA Advantage Bookcase** can also be accessed from the **Help** pulldown menu in the Design Manager on both Windows and UNIX by selecting **Help > FPGA Advantage Bookcase.**

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