PRELIMINARY

Video Platform User Manual

V2.0, Rev. 1.1 (5/25/2005)

1 Overview

This datasheet describes a compact configurable platform, capable of real time video processing, based on a board equipped with a FPGA. The board has been designed to meet the high demanding characteristics of real time video processing. This inexpensive and cost-effective platform can be easily used and configured for different types of algorithms and applications. It provides interfaces with a digital camera and with an output video peripheral for video display. It is also equipped with a standard bus connector to allow debug or stream data input/output or to attach expansion modules. In fig. 1 is presented the block diagram of the platform.

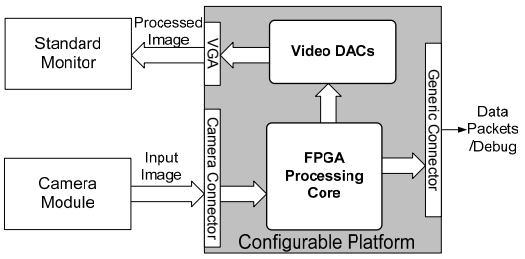

Figure 1: Block diagram of the platform.

2 Features

The developed board presents the following main features:

- Xilinx Spartan3 XC3S400 FPGA as the processing core with:
  - 400K system gates,
  - 288Kb of RAM in 16 blocks,
  - Sixteen 18-bit multipliers,
  - Fast carry look-ahead logic,
  - JTAG configuration or through Serial PROM;
- Xilinx XCF02S serial configuration flash PROM (On-board FPGA boot);
- Two 100-mil spaced, right angle DIP, expansion connectors:
  - "Camera Connector": 32-pin header providing 25 I/O pins, including two Global Clock inputs, supports several camera modules from Omnivision,
  - "Generic I/O Connector": 40-pin socket providing 37 I/O pins, including four GCLK inputs, supports several expansion modules provided by Diligent;
- VGA true color display port, with three 20MHz conversion rate video DACs;
- On-board user interface: eight LEDs, one 4-way slide switch, two push buttons;
- 50MHz HCMOS 3.3V oscillator;
- Three 3A power regulators (1.2 V, 2.5V and 3.3V) and one 1.5A, 5V power regulator.

3 Platform Description

The employed FPGA has sixteen embedded 18-bit multipliers, fast carry look-ahead logic and a total of 400K system gates. This gives the developer enough resources to perform video processing. The development can be performed by designing the circuits in VHDL, using the free ISE WebPACK software tool from Xilinx.

To provide the interface with a standard VGA monitor, this design employs three high speed video DACs capable of a conversion rate up to 30MHz. These devices generate the red (R), green (G), blue (B), analog color signals require for the VGA interface. Impedance adaptation is ensured using a triple video buffer.

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The board has been designed to be compatible with several expansion modules, like the provided by Digilent. The employed expansion connectors use standard 100mil spacing and can easily be found in common distributors. These connectors make available: I/O pins, one or more supply voltages and a reference ground signal.
Furthermore, as currently CMOS sensors are capable of relatively good image quality, the board was equipped with a connector capable of receiving several development camera modules from Omnivision. Since the development modules can be equipped with different image sensors, the voltage level applied to "Camera Connector" can be configured. With this platform it is provided a simple VHDL description of an image capture module with the corresponding camera register configuration module.
Table 1 presents a summary of all the signals routed on the Video Board. A more detailed description of these circuits can be found in the following sections. Figure 2 presents a simplified layout of the components in the Video Board, which has been implemented with a four layers; the two internal corresponding to power/ground planes.

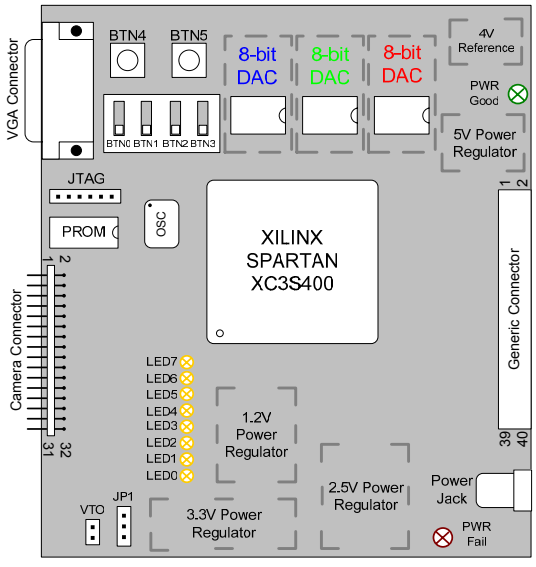

Figure 2: Simplified layout of the Video Board.

Power Supplies:

- V_{CCu} – Unregulated power supply voltage;
- V_{CCo} – 3.3V, routed on a PCB plane, employs a 3A PWM regulator, I/O supply voltage for the FPGA;
- V_{CCaux} – 2.5V auxiliary supply, required for the FPGA and for the camera expansion connector, also uses a 3A PWM regulator;
- V_{CCint} – 1.2V core supply, provides the supply voltage to the FPGA;
- V_{CC} – 5V provides power to the DACs or for the "Camera Connector", maximum of 1.5A;
- GND – System ground to all devices except the analog ground of the DACs.

Video Port:

- DR0-DR7 – Digital red data signal bus that connect to a DAC;
- DG0-DG7 – Digital green data signal bus that connect to a DAC;
- DB0-DB7 – Digital blue data signal bus that connect to a DAC;
- CLK_dac – Clock signal for the DACs;
- HS – Horizontal VGA synchronization;
- VS – Vertical VGA synchronization;
- RGB – Analog VGA color channels.

On-board Devices:

- LED0-LED7 – User controllable LEDs;
- BTN0-BTN3 – User controllable slide switch inputs;
- BTN4-BTN5 – User controllable push button inputs;
- Power Fail – Overvoltage condition LED;
- Power Good – Normal supply status LED;
- CLK – HCMOS oscillator connected to GCLK5;

Expansion Connectors:

- C01-C32 – Signals that connect the "Camera Connector" to the FPGA and to the power supplies;
- G04-G40 – Signal bus that connects the FPGA to the "Generic I/O Connector".
- VTO – Analog Video signal output;

Table 1: Video Board signal definitions.

4 VGA Display Port

The display port is based in three separate 8-bit DAC converters, TLC5602C, one per RGB channel. This DAC presents low power consumption and a maximum conversion rate of 20MHz. The signal conditioning for VGA port is performed using high speed video buffers with a 75Ω resistance in series with the output. The voltage level required for powering the DAC is generated using a TPS78601, an ultra low-noise, low-dropout linear regulator with a maximum output current of 1.5A. The FPGA pin assignments for the tree converters are presented in table 2, the **clock signal** for the all DACs is provided by the **FPGA pin 140**.

Table 2: FPGA pins for the video DACs.

Data Red		Data Green		Data Blue	
FPGA PIN	**Function**	**FPGA PIN**	**Function**	**FPGA PIN**	**Function**
106	DR0 (LSB)	116	DG0 (LSB)	126	DB0 (LSB)
107	DR1	117	DG1	128	DB1
108	DR2	119	DG2	130	DB2
109	DR3	120	DG3	131	DB3
111	DR4	122	DG4	132	DB4
113	DR5	123	DG5	133	DB5
114	DR6	124	DG6	135	DB6
115	DR7 (MSB)	125	DG7 (MSB)	137	DB7 (MSB)

Note: when using this video port please ensure that the clock input of video DACs is lower than 20MHz.

The three analog voltage level generated by these DACs (RGB), together with the *Horizontal Sync* (HS) and the *Vertical Sync* (HS) are connected to a PCB mounted, 15-pin sub-HD socket (standard VGA). Figure 3 describes the mapping of these pins in socket and table 3 summarizes the function of each pin.

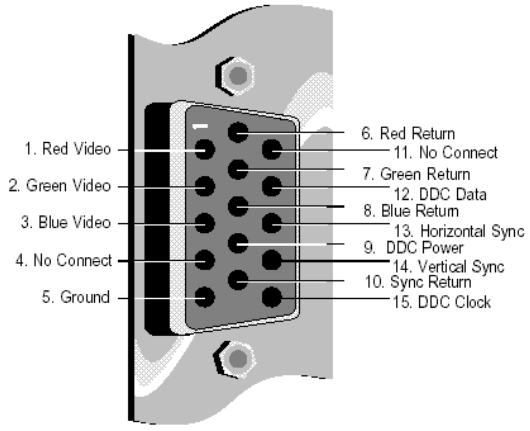

Figure 3: VGA socket pin description.

Table 3: VGA socket pin mapping.

FPGA PIN	Number	VGA
-	1	analog Red
-	2	analog Green
-	3	analog Blue
-	4	N. C.
-	5	Ground
-	6	Ground
-	7	Ground
-	8	Ground
-	9	N. C.
-	10	Ground
-	11	N. C.
-	12	N. C.
138	13	HS
139	14	VS
-	15	N. C.

To implement this video out interface, a VHDL module is provided with the board to generate the synchronization signals necessary for a standard VGA monitor. The adopted configuration uses a resolution of 640 x 480 and a refresh rate of 60Hz. The provided implementation uses a simple stage machine to generate the signals necessary to control the image display. The image to be visualized can be stored into a frame memory block or be provided directly by the processing modules. Figure 4 shows the temporal diagram of the VGA signals and Table 4 the necessary timings for the signals.

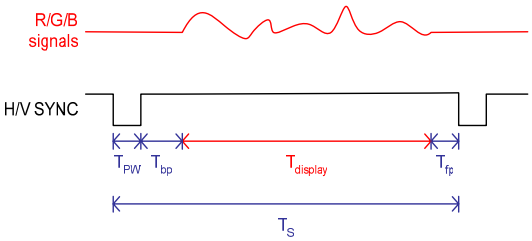

Figure 4: VGA timing diagram.

Table 4: VGA Timings.

Symbol	Parameter	VS	HS
T_S	Period	16.7 ms	32 µs
T_{disp}	Display time	15.36 ms	25.6 µs
T_{pw}	Sync pulse width	64 µs	3.84 µs
T_{fp}	Sync front porch	320 µs	640 ns
T_{bp}	Sync back porch	928 µs	1.92 µs

5 Oscillator

A 50MHz oscillator with a 3.3V maximum amplitude is used. This HCMOS SMD device presents an accuracy of 50ppm. The oscillator is connected to one GCLK FPGA pin (**P181**) and is located close to the FPGA. Oscillators for different frequencies can be employed by request. Using the DCMs (Digital Clock Managers) available in the Startan 3 FPGA other frequencies can also be synthesized.

6 Power Supply

This board requires a power supply with an output voltage within the range of 5V to 6V DC. The input voltage is monitored using a MAX4841, which provides overvoltage protection up to 28V. If the unregulated input voltage is above 5.8V the MAX4841 disables a FET transistor isolating the remaining circuit. The “PWR Fail” led indicates overvoltage condition. The DC power socket must be connected to a 2.1mm female center-positive plug and the supply must be capable of delivering at least 1A. The board generates a total of four voltage levels, 1.2V, 2.5V, 3.3V and 5V. In order to save power, all the supply voltages except the 5V are generated using a MAX1830/MAX1831 a low voltage PWM (Pulse Width Modulation), step-down regulator, which delivers a current of up to 3A with a peak efficiency of 94%. Some of these voltages, as well as the unregulated input are available through the expansion connectors.

To achieve a more efficient PDS (Power Distribution System) this board uses a four layer PCB with the inner layers dedicated to ground and power. Most of the power plane is at 3.3V but is divided into several islands, one for each DAC and more two for the other supply voltages required for the FPGA. The ground plane is also divided, but in a more simple manner. All the digital circuitry shares the same plane, only the analog part of the DACs has a separate ground.

All the I/O pin operate with 3.3V, but some of the FPGA banks can be connected to other voltage levels by request.

7 FPGA Configuration

The FPGA can be configured using a six pin JTAG header; fig. 5 shows the function of each pin in the connector. The header can be connected to a standard JTAG programming cable (Digilent JTAG3), the *Vcc* pin is connected to the 3.3V supply voltage.

It also employs the XCF02S serial configuration flash PROM to store FPGA configuration data. Using this design, the FPGA can automatically boot from the on-board PROM whenever the power is applied. The configuration of the PROM is also done through the JTAG header.

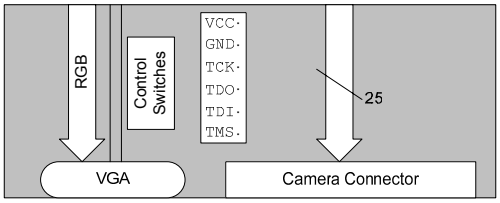

Figure 5: JTAG connector pin order.

8 On-board User Interface

The slide switches can be used to connect either V_{CCo} or GND to the FPGA pins.The slide switch in the OFF position pulls the FPGA pin to ground and in the ON will go high. The output of the push button is normally pulled to V_{CCo}, when pressed is pulled to ground. No active debounce circuit was employed in either interface.

The board also provides 8 LEDs as output circuits and those LEDs are driven directly from the FPGA pins. The LEDs are accessible through the pins presented in table 7 and are active high.

Table 6: FPGA pins for the slide switches and the push buttons.

FPGA PIN	Function	PIN num
156	BTN0	1
155	BTN1	2
154	BTN2	3
152	BTN3	4
150	BTN4	-
149	BTN5	-

Table 7: FPGA pins for the leds.

FPGA PIN	Function
19	LED0
18	LED1
16	LED2
15	LED3
13	LED4
12	LED5
11	LED6
10	LED7

9 Image Capture

The board is pin compatible several digital camera modules from Omnivision like the camera module based on the OV7620 CMOS image sensor or other modules with more recent sensors like the OV9650. All camera functions can be configured using a serial data transmission protocol, SCCB, which is a simplified version of the Philips I2C protocol. A VHDL implementation of this protocol is supplied, the desired register values are provided by a simple VHDL ROM like description. Considering a camera module with the OV9650 sensor, it can be programmed to capture frames in SXGA, VGA, QVGA and other specific formats or other programmed format. Frame synchronization is performed by detecting a high pulse in the vertical sync (VSYN) signal and a new line occurs with a low pulse on the horizontal reference (HREF) signal, moreover, the camera also provides the pixel clock (PCLK) signal. Figure 6 shows the temporal diagrams of those signals.

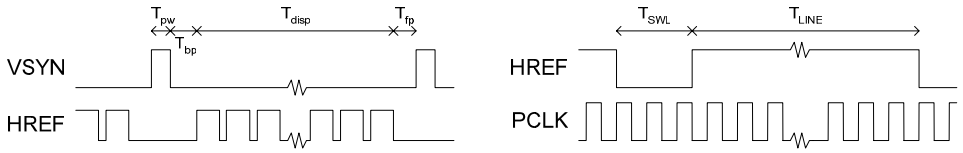

Figure 6: Camera module sync signals.

The pixels information is updated every falling edge of the PCLK signal, which means that pixel information can be read on the rising edge of PCLK, the VHDL description of this module is provided.

10 Expansion Connectors

This board provides two expansion connectors; both can provide supply power to an expansion module. The pin arrangement is not equal for the two connectors. As the ”Camera Connector” must receive data from a digital camera the pin arrangement must be the same than for the camera module. The power pins of this connector can be configured through JP1 to be 5V or 2.5V, depending on the camera module. Both connectors are close to the FPGA, thus these connectors will exhibit a small signal delay, and high data transfer rates.

Table 6 shows the pin mapping between the FPGA I/O and the ”Camera Connector”. There is also a two pin header that provides the analog output video signal, if the employed module provides this output. Table 7 shows the FPGA pins for the ”Generic I/O Connector” expansion slot.

All the available I/O signals from the FPGA can be seen in fig. 7, and the mapping of all the pins is shown in table 10.

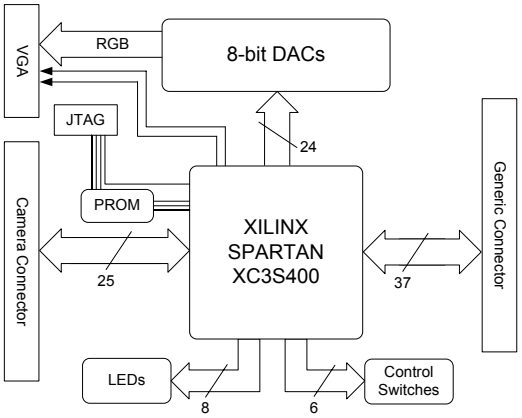

Figure 7: FPGA available I/O signals.

Table 8: FPGA pins for camera connector expansion slot.

FPGA PIN	Function	Number
178		C01
176		C02
180*		C03
182		C04
187		C05
185		C06
190		C07
189		C08
194		C09
191		C10
197		C11
196		C12
198		C13
199		C14
-	GND	C15
200		C16
-	GND	C17
183*		C18
184*		C19
-	Vccaux/Vcc **	C20
-	GND	C21
-	Vccaux/Vcc **	C22
203		C23
204		C24
205		C25
2		C26
3		C27
4		C28
5		C29
7		C30
-	GND	C31
-	VTO	C32

* GCLK pin

** Configured through JP1

Table 9: FPGA pins for the generic expansion slot.

FPGA PIN	Function	Number
-	GND	G01
-	Vccu	G02
-	Vcco	G03
52		G04
101		G05
102		G06
97		G07
100		G08
95		G09
96		G10
93		G11
94		G12
90		G13
92		G14
86		G15
87		G16
83		G17
85		G18
80*		G19
81		G20
78		G21
79*		G22
76*		G23
77*		G24
72		G25
74		G26
68		G27
71		G28
65		G29
67		G30
63		G31
64		G32
61		G33
62		G34
57		G35
58		G36
50		G37
48		G38
46		G39
48		G40

* GCLK pin

Table 10: Video Board FPGA pin assignment.

FPGA PIN	Number	FPGA PIN	Number	FPGA PIN	Number	FPGA PIN	Number
1	GND	53	GND	105	GND	157	GND
2	C26	54	GND	106	DR0 (LSB)	158	TDO
3	C27	55	GND	107	DR1	159	TCK
4	C28	56	GND	108	DR2	160	TMS
5	C29	57	G35	109	DR3	161	N. C.
6	Vcco	58	G36	110	Vcco	162	N. C.
7	C30	59	GND	111	DR4	163	GND
8	GND	60	Vcco	112	GND	164	Vcco
9	N. C.	61	G33	113	DR5	165	N. C.
10	LED7	62	G34	114	DR6	166	N. C.
11	LED6	63	G31	115	DR7 (MSB)	167	N. C.
12	LED5	64	G32	116	DG0 (LSB)	168	N. C.
13	LED4	65	G29	117	DG1	169	N. C.
14	GND	66	GND	118	GND	170	GND
15	LED3	67	G30	119	DG2	171	N. C.
16	LED2	68	G27	120	DG3	172	N. C.
17	Vccaux	69	Vccaux	121	Vccaux	173	Vccaux
18	LED1	70	Vccint	122	DG4	174	Vccint
19	LED0	71	G28	123	DG5	175	N. C.
20	N. C.	72	G25	124	DG6	176	C02
21	N. C.	73	Vcco	125	DG7 (MSB)	177	Vcco
22	N. C.	74	G26	126	DB0 (LSB)	178	C01
23	Vcco	75	GND	127	Vcco	179	GND
24	N. C.	76*	G23	128	DB1	180*	C03
25	GND	77*	G24	129	GND	181*	CLK
26	N. C.	78	G21	130	DB2	182	C04
27	N. C.	79*	G22	131	DB3	183*	C18
28	N. C.	80*	G19	132	DB4	184*	C19
29	N. C.	81	G20	133	DB5	185	C06
30	GND	82	GND	134	GND	186	GND
31	N. C.	83	G17	135	DB6	187	C05
32	Vcco	84	Vcco	136	Vcco	188	Vcco
33	N. C.	85	G18	137	DB7 (MSB)	189	C08
34	N. C.	86	G15	138	HS	190	C07
35	N. C.	87	G16	139	VS	191	C10
36	N. C.	88	Vccint	140	CLK_dac	192	Vccint
37	N. C.	89	Vccaux	141	N. C.	193	Vccaux
38	Vccaux	90	G13	142	Vccaux	194	C09
39	N. C.	91	GND	143	N. C.	195	GND
40	N. C.	92	G14	144	N. C.	196	C12
41	GND	93	G11	145	GND	197	C11
42	N. C.	94	G12	146	N. C.	198	C13
43	N. C.	95	G09	147	N. C.	199	C14
44	N. C.	96	G10	148	N. C.	200	C16
45	N. C.	97	G07	149	BTN5	201	Vcco
46	G39	98	Vcco	150	BTN4	202	GND
47	GND	99	GND	151	GND	203	C23
48	G38	100	G08	152	BTN3	204	C24
49	Vcco	101	G05	153	Vcco	205	C25
50	G37	102	G06	154	BTN2	206	GND
51	N. C.	103	DONE	155	BTN1	207	PROG_B
52	G04	104	CCLK	156	BTN0	208	TDI

* GCLK input