RAVEN USER'S MANUAL

Using OCDemon™ technology from Macraigor Systems LLC

This guide provides all the information you need to use the RAVEN interface to debug your target processor

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Unpacking your RAVEN

The RAVEN is shipped with the following:

- RAVEN
- Six foot IEEE-1284 male DB-25 to female DB-25 cable
- 5v International switching power supply
- One 18" target processor OCD cable (attached)

Specifications

Size	2.25 (w) x 3.75 (l) x .875 (d) inches excluding cables
Weight	.25 lb.
Power supply	5 volts DC, 2.0 amp
Parallel interface	IEEE 1284 compatible, B connector
OCD interface	Macraigor Systems LLC proprietary pin out OCD Clock speeds to 8 MHz.
Multiple Processors	Can handle scan chains with up to 255 devices (known and unknown)
Indicators	Power, Host Communication, Target Mode

Introduction

This guide describes all of the tasks necessary to connect your new RAVEN to your host computer system and your target under test. The steps needed actually depend on the host software you will be using.

What *exactly* is the RAVEN?

Many modern CPUs have one or another form of On Chip Debug (OCD). This may take the form of BDM (Background Debug Mode), JTAG (IEEE 1149.x), EJTAG (Extended JTAG), OnCE (On Chip Emulation), COP, or one of many others. All of these comprise an electrical/timing specification as well as a communication specification.

The Raven is a product that "translates" commands from a host software debugger into the appropriate OCD format and communicates with the target CPU under test. The Raven communicates with the host debugger via parallel port and can communicate with the target CPU in a wide variety of OCD formats including all of those previously mentioned as well as others. Because there are so many OCD formats, each with its own electrical characteristics and pin outs, the Raven varies in form by different OCD cables. The OCD cables are very similar to the mpDemon's "personality module", except that the Raven's OCD cables are not customer interchangeable.

The Raven's OCD cable comes out of one side of the product and varies by the pin type at the end of the cable, 14pin, 16pin and 20pin are a few of the variations. The circuitry of this cable modifies any necessary signals and presents to the target CPU the correct signals with the correct pin out. Although there are many types of OCD cables, they are 90% the same. The differences are simply in routing signals to a connector appropriate for the specific target.

What software is available for the RAVEN?

There are many software debuggers available (see the section on Installing Host Software) as well as various production line test applications such as flash eeprom programmers and general test routines, for the Raven. There is also a wide selection of third party software tools that work with Macraigor's hardware tools. Refer to our web site, www.macraigor.com, for more information on these software tools.

Features

The RAVEN offers the following features:

- LED status indicators
- IEEE 1284 Parallel Port
- Scan chains of up to 255 devices, all may be debugged
- Eighteen inch target OCD cable
- Auto sensing of target voltage
- Fully API compatible with the Wiggler and the mpDemon
- Small footprint – 2.25 x 3.75 inches

Hardware Issues

Power Supply

The RAVEN is powered by an international 5v output switching power supply. Macraigor Systems LLC recommends that the power supply obtain its ac from the same wall outlet as the target under test. Ideally, the host system is also powered also from the same outlet. This helps eliminate any chance of a "ground loop" forming and causing additional noise, or worse, in the system. There is no specific power on/off button on the Raven, **the means of disconnection from the mains power supply is the plug**.

In international markets, the Raven is shipped with an international power adapter, which is designed to work with a variety of power cords, depending on the type of outlet in each country. **You should use a nationally approved power supply cord with the international power adapter**.

JTAG Clock Rate

The rate at which the Raven clocks JTAG commands to the target is selected by a "speed" parameter sent to it by the host software. The following table relates Raven "speed" values to JTAG clock rates:

1	2	3	4	5	6	7	8
8Mhz	4Mhz	2Mhz	1Mhz	500Khz	125Khz	60Khz	30Khz

Hot Plugging

It is never a good idea to attach electronic devices together, or disconnect them, when power is applied unless they are specifically designed to "hot plug." No part of the RAVEN is designed for hot plugging. The target, host, and RAVEN should all be off while being connected.

OCD Cable

A different OCD cable is needed for each type of target. The OCD cable is responsible for ensuring the correct footprint for the target connector as well as the correct voltages for debug communication. Make sure the module is securely plugged into your target board, remembering to align pin 1 of the connector with the same for the cable. Only connect the cable when the RAVEN's power supply is not yet plugged in.

Parallel Cable

Both the quality and the length of parallel cables make a large difference as to the overall system performance. Macraigor recommends that only the supplied IEEE 1284 parallel cable is used with the Raven. Longer or inferior cables will most certainly introduce noise and other errors in data transfers.

Host Communications – Parallel Port

The host communicates with the RAVEN via the parallel port. Electrically, the RAVEN is IEEE 1284 compatible. It does not support daisy chaining. The best mode of communication is EPP; ECP mode is not recommended. EPP mode can typically be set in the CMOS BIOS setting of the host PC.

Setting up Raven

Follow these instructions to set up your RAVEN:

1. Plug your RAVEN into the PC parallel port using the IEEE1284 parallel cable supplied. If you have a parallel cable that is not IEEE1284 compliant or is longer than the one provided, it may not work properly.
2. The target board, the host system and the RAVEN should all be off prior to connecting the equipment.
3. Ensure you have set up your parallel port correctly. This should be done by entering the "BIOS Setup" mode when the PC first boots up. You may select ECP or EPP modes. EPP mode is preferred for maximum performance.
4. Check that no other software on your PC has access to the parallel port. An apparently inactive device driver can cause problems.
5. Connect the end of the OCD cable to the specified JTAG / BDM type connector on your target microprocessor based board. Be sure to align pin 1 of the cable with pin 1 of the connector on the board. Pin one is signified by the red line on the cable.
6. Install your debugging software. Be sure to configure the software to work with the RAVEN.

Installing Host Software

Macraigor Systems provides two free software tools, for use with its RAVEN. The first is an assembly level debugger called OCD Commander and the second is a version of GNU Tools (includes *unsupported* C++ compiler, GCC, source level debugger, GDB, linker and assembler). The GNU tools build is available for ARM7/9, MIPS32, MIPS64, PowerPC and XScale architectures. All applications can be downloaded from the Macraigor web site, www.macraigor.com. Macraigor Systems also has a flash programming application, a target access and flash access DLL available for sale from its web site.

If you are installing Macraigor Systems' software, simply follow the instructions during the install process.

NOTE: If you are installing your software debugger on an NT or NT based machine (i.e.: Windows NT, 2000, etc.) make sure you are logged on as ADMINSTRATOR and make sure you re-boot your machine after the install process.

In addition to Macraigor's own software tools, the RAVEN is often used with third party software. Companies with software debuggers which work with various target microprocessors include (but are not limited to):

- Accelerated Technology
- ARM Ltd. (Allant Software)
- CAD-UL
- Green Hills Software
- Metaware
- Metrowerks
- Microsoft
- QNX
- Red Hat
- Tasking (Altium)

Please refer to each third party to obtain their software debugging tools.

Trouble Shooting

Power light is not on.
Is the power supply plugged into the rear of the unit? Is the power supply plugged into an appropriate source of power?

Host computer cannot seem to communicate.
Make sure all the proper cables are connected (i.e.: parallel cable for IEEE-1284 connection, etc.).

- Parallel Port – verify that the port is enabled via the CMOS setup for your computer. Set the mode for ECP if available. Verify that you are connected to the port you are telling the software you are connected to (i.e.: LPT1, LPT2, etc.). Verify the use of an IEEE-1284 rated parallel port cable.

There is also a Raven software tester that can be downloaded from Macraigor's web site, www.macraigor.com. This software will test to see that the Raven can be reached from your host system. This application works with Raven's using JTAG; BDM is not supported.

NOTE: **The Raven is designed with no internal serviceable parts. If you have a problem with the product, please contact Macraigor Systems. Do not try to repair it yourself.**

Appendix A

Common OCD pin outs

NOTE: Macraigor Systems accepts NO responsibility for the accuracy of the following information. We strongly recommend that you use the OCD header specified by the semiconductor manufacturer. Please refer to the manufacturer's proper data book or reference design for information. *The pin outs given below may show a subset of the signals specified by the manufacturer.*

General Notes:

- Unless otherwise indicated, all headers are male dual-row Berg style connectors on 0.1 centers.
- We do not specify the use of pull ups or pull downs on any signals although they may be needed. Check with the chip manufacturer.
- TVcc pins should be the I/O ring voltage and that signal is used to determine the electrical characteristics of the other signals. If you must current limit this line, allow the probe at least 2 mA.
- Unless otherwise indicated, RESET\ is an open collector signal from the probe to the target. It should directly drive the target processor and not drive power on reset circuits or the like.
- Some target boards may use a non-standard connector or a connector that we identify for a different target.
- Place the header as close to the processor as possible, use short traces of approximately equal length on all clock and data signals.

Pin Specifications:

Pins are identified by number and type.

- o = output from target processor to OCD interface
- i = input to target processor from OCD interface
- p = power pin
- oc = open collector driven from OCD interface, either floating or actively held low
- nc = not connected, i.e.: not driven nor read by OCD interface
- k = key, pin is typically missing from the target board

"COP" pin out

Motorola PowerPC 6xx, 7xx, 8xxx
IBM 4xx
LSI SerialICE 2

TDO	**o**	**1**	**2**	**i**	QACK
TDI	**i**	**3**	**4**	**i**	TRST\
HALTED	**o**	**5**	**6**	**p**	TVcc
TCK	**i**	**7**	**8**	**nc**	
TMS	**i**	**9**	**10**	**nc**	
SRESET	**i**	**11**	**12**	**p**	GND
HRESET	**oc**	**13**	**14**	**nc**	
CKSTP_OUT	**o**	**15**	**16**	**p**	GND

"BDM" – Background Debug Mode

There are actually several BDM pinouts.

Motorola MPC8xx, MPC5xx

NOTE: It is vital that pins 1 and 6 properly reflect the status of the target processor immediately following RESET. Some processors have configurable pins (MPC8xx, etc.) that are specified by a reset configuration word at the time of reset. These pins must be set properly and must ALWAYS reflect the status of the processor correctly. Check the 'hardware reset configuration word' in the Motorola User's manual.

FRZ or VFLS0	**o**	**1**	**2**	**o**	SRESET
GND	**p**	**3**	**4**	**i**	DSCK
GND	**p**	**5**	**6**	**o**	FRZ or VFLS1
RESET\	**oc**	**7**	**8**	**i**	DSDI
TVcc	**p**	**9**	**10**	**o**	DSDO

Motorola CPU32 (*this version is obsolete and not recommended*)

GND	**p**	**1**	**2**	**i**	DSCK
GND	**p**	**3**	**4**	**o**	FRZ
RESET\	**oc**	**5**	**6**	**i**	DSDI
TVcc	**p**	**7**	**8**	**o**	DSDO

Motorola CPU16, CPU32

Note: Most probes are powered via TVcc, hence don't current limit.

DS	**o**	**1**	**2**	**o**	BERR
GND	**p**	**3**	**4**	**i**	DSCK
GND	**p**	**5**	**6**	**o**	FRZ
RESET\	**oc**	**7**	**8**	**i**	DSDI
TVcc	**p**	**9**	**10**	**o**	DSDO

"OnCE" – On Chip Emulation
Motorola DSP, M•CORE

TDI	**i**	**1**	**2**	**p**	GND
TDO	**o**	**3**	**4**	**p**	GND
TCK	**i**	**5**	**6**	**p**	GND
	nc	**7**	**8**	**nc**	
RESET\	**oc**	**9**	**10**	**i**	TMS
TVcc	**p**	**11**	**12**	**p**	GND
	nc	**13**	**14**	**i**	TRST\

ARM

There are two standard ARM pin outs, and older 14 pin specification and a newer 20 pin specification.

TVcc	**p**	**1**	**2**	**p**	GND
TRST\	**i**	**3**	**4**	**p**	GND
TDI	**i**	**5**	**6**	**p**	GND
TMS	**i**	**7**	**8**	**p**	GND
TCK	**i**	**9**	**10**	**p**	GND
TDO	**o**	**11**	**12**	**oc**	RESET\
TVcc	**p**	**13**	**14**	**p**	GND

OR

TVcc	**p**	**1**	**2**		nc
TRST\	**i**	**3**	**4**	**p**	GND
TDI	**i**	**5**	**6**	**p**	GND
TMS	**i**	**7**	**8**	**p**	GND
TCK	**i**	**9**	**10**	**p**	GND
	nc	**11**	**12**	**p**	GND
TDO	**o**	**13**	**14**	**p**	GND
RESET/	**oc**	**15**	**16**	**p**	GND
	nc	**17**	**18**	**p**	GND
	nc	**19**	**20**	**p**	GND

MIPS – EJTAG 2.5

There are many MIPS OCD headers in use. This is the one specified by MTI for EJTAG 2.5

TRST\	**i**	**1**	**2**	**p**	GND
TDI	**i**	**3**	**4**	**p**	GND
TDO	**o**	**5**	**6**	**p**	GND
TMS	**i**	**7**	**8**	**p**	GND
TCK	**i**	**9**	**10**	**p**	GND
RESET\	**oc**	**11**	**12**	**k**	key
DINT	**i**	**13**	**14**	**p**	TVcc

AMD – Athlon

These are the pins that Macraigor uses on the Athlon header.

TVcc	**p**	**1**	**2**	**i**	TCK
	nc	**3**	**4**	**i**	TMS
	nc	**5**	**6**	**nc**	
	nc	**7**	**8**	**i**	TDI
	nc	**9**	**10**	**i**	TRST\
GND	**p**	**11**	**12**	**o**	TDO
DBREQ	**i**	**13**	**14**	**o**	DBRDY
RESET\	**oc**	**15**	**16**	**i**	PLL_TEST