MVME3600/4600 Series
VME Processor Modules

Installation and Use

V36V46A/IH5

September 2001 Edition

Printed in the United States of America.

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution

Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.

Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

CE Notice (European Community)

Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

> EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class B
>
> EN55024 “Information technology equipment—Immunity characteristics—Limits and methods of measurement”

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC performance.

In accordance with European Community directives, a “Declaration of Conformity” has been made and is available on request. Please contact your sales representative.

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About This Manual

The *MVME3600/4600 Series VME Processor Modules Installation and Use* manual provides information to install and use your MVME3600 and MVME4600 Series VME Processor Modules.

The model numbers listed in the first table below are **compatible only with the MVME761 transition module**. The MVME712M references remain in this edition of the *Installation and Use* manual for use with the end of life model numbers listed in the next table.

Model Numbers	Description
MVME3604-5442, 5462A, 5472A	400 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and IEEE 1101 front panel for use with MVME761
MVME4604-5442, 5462A, 5472A	Dual 400 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and IEEE 1101 front panel for use with MVME761

The model numbers listed below are no longer orderable as of September 2001, but the information in this edition of the *Installation and Use* manual still applies.

EOL Model Numbers	Description
MVME3604-5342A, 5352, 5362, 5372	300 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and IEEE 1101 front panel for use with MVME761
MVME3604-6342, 6352, 6362, 6372	300 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and Scanbe front panel for use with MVME712M
MVME3604-5462, 5472	400 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and IEEE 1101 front panel for use with MVME761
MVME3604-6442, 6462, 6472	400 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and Scanbe front panel for use with MVME712M
MVME4604-5342A, 5352, 5362, 5372	Dual 300 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and IEEE 1101 front panel for use with MVME761
MVME4604-6342, 6352, 6362, 6372A	Dual 300 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and Scanbe front panel for use with MVME712M
MVME4604-5462, 5472	Dual 400 MHz MPC604, 64-512MB ECC DRAM, 9MB Flash, 512KB L2 cache, and IEEE 1101 front panel for use with MVME761

Summary of Changes

This is the fifth edition of the *Installation and Use* manual. It supersedes the August 2001 edition and incorporates the following updates.

Date	Description of Change
September 2001	Reflects the discontinuation of a cable that made it possible to install a 1GB double-board RAM201 mezzanine assembly on top of the processor/memory mezzanine. The orderable MVME3604 and MVME4604 model numbers, listed in *About This Manual*, are **not** compatible with the MVME712M transition module. The MVME712M transition module references remain in this manual for use with the end of life models.
August 2001	All data referring to the VME CSR Bit Set Register (VCSR_SET) and VME CSR Bit Clear Register (VCSR_CLR) has been deleted. These registers of the Universe II are unavailable for implementation as intended by the MVME materials and the Universe II User Manual.
March 2000	Reflects the speed increase of the processor from 300 MHz to 400 MHz. Engineering changes also reflected several voltage changes on key components from 5V to 3.3V (DRAMs, etc.). The change to 3.3V DRAM devices means that older 5V DRAM mezzanines cannot be used with this product and, in fact, will be disabled if they are attached to any one of these boards. Mezzanines that are no longer usable include assembly numbers 01-W3174F and 01-W3373F. If there are any question regarding these changes, the user is encouraged to check with the local Motorola Computer Group sales or sales support representative.
September 1999	Clarify which settings on I/O jumpers J9, J10, J15 and J16 applied to which transition module (MVME761 and MVME712). (See pages 1-11, 1-12, 1-13 and 1-14.)
July 1999	Clarify to which style I/O jumpers J15, J9 and J10 applied (see pages 1-11, 1-12 and 1-13.)
February 1999	Correct an error to Table B-4 on page B-6. The pin assignment information to pin numbers 18 and 19 were inverted. In addition, new templates were added, as well as corrections to certain cross-references.

Overview of Contents

Chapter 1, *Hardware Preparation and Installation*, provides startup information, hardware preparation and installation instructions for the MVME3600 and MVME4600 family of VME Processor Modules.

Chapter 2, *Operating Instructions*, supplies information on use of the MVME3600 and MVME4600 series family of VME Processor Modules in a system configuration.

Chapter 3, *Functional Description*, describes the MVME3600/4600 series VME Processor Modules on a block diagram level.

Chapter 4, *Connector Pin Assignments*, provides pin assignments for the interconnect signals on the MVME3600 and MVME4600 VME Processor Modules.

Chapter 5, *PPCBug Firmware*, describes the basics of PPCBug and its architecture, describes the monitor (interactive command portion of the firmware) in detail, and gives information on actually using the PPCBug debugger and the special commands.

Chapter 6, *CNFG and ENV Commands*, contains information about the **CNFG** and **ENV** commands. These two commands are used to change configuration information and command parameters interactively.

Appendix A, *Specifications*, lists the general specifications for the MVME3600 and MVME4600 VME Processor Modules.

Appendix B, *Serial Interconnections*, describes the serial communications interface on the MVME3600 and 4600 series VMEmodules.

Appendix C, *Troubleshooting CPU Boards*, provides simple troubleshooting tips for your MVME3600 and MVME4600 VME Processor Modules.

Appendix D, *Related Documentation*, lists all documentation related to the MVME3600 and MVME4600 series VMEmodules.

Comments and Suggestions

Motorola welcomes and appreciates your comments on its documentation. We want to know what you think about our manuals and how we can make them better. Mail comments to:

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

Unless otherwise specified, all address references are in hexadecimal. An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low. An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

$	dollar	specifies a hexadecimal number
&	ampersand	specifies a decimal number
%	percent	specifies a binary number

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

- A *byte* is eight bits, numbered 0 through 7, with bit 0 being the least significant.
- A *word* is 16 bits, numbered 0 through 15, with bit 0 being the least significant.
- A *longword* is 32 bits, numbered 0 through 31, with bit 0 being the least significant.

The terms *control bit*, *status bit*, *true*, and *false* are used extensively in this document. The term *control bit* is used to describe a bit in a register that can be set and cleared under software control. The term *true* is used to indicate that a bit is in the state that enables the function it controls. The term *false* is used to indicate that the bit is in the state that disables the function it controls. In all tables, the terms *0* and *1* are used to describe the

actual value that should be written to the bit, or the value that it yields when read. The term *status bit* is used to describe a bit in a register that reflects a specific condition. The status bit can be read by software to determine operational or exception conditions.

Hardware Preparation and Installation

1

Introduction

This chapter provides startup information, hardware preparation and installation instructions for the MVME3600 and MVME4600 family of VME Processor Modules. Installation instructions are also provided for the MVME712M and MVME761 transition modules, which mate with the MVME3600 and 4600 base boards. Peripheral board install instructions are also provided for the PMC module, the DRAM memory module and the processor/memory mezzanine module. Required jumper settings for various component and base boards are included where necessary.

Note The MVME712M transition module references remain in this edition of the *Installation and Use* manual for use with the end of life model numbers listed in the front matter of this manual.

The MVME 3600/4600 series boards are double-high, two-slot configurations equipped with single or twin (4600 only) PowerPC® microprocessors. All versions are also supplied with 512KB of L2 cache (level 2 secondary cache memory).

Both MVME 3600 and 4600 families have two parallel rear I/O options: one configuration is compatible with MVME712M transition modules, while the other uses MVME761 transition modules. The logic design is the same for both versions. In either case, all 3600 and 4600 VMEmodules consists of a base board plus:

- A single or twin PowerPC 604™ processor/memory module with L2 cache
- An optional ECC DRAM module (RAM201) for memory
- An optional PCI mezzanine card (PMC) module for additional versatility
- An optional PMC carrier board for additional PCI expansion

Both base boards, RAM201 modules, PMC modules, and PMC carrier boards are identical. Only the processor/memory mezzanine is unique to the MVME4600 series. The block diagram in Figure 1-1 illustrates the architecture of the MVME3600 series base board and Figure 1-2 illustrates the architecture of the MVME4600.

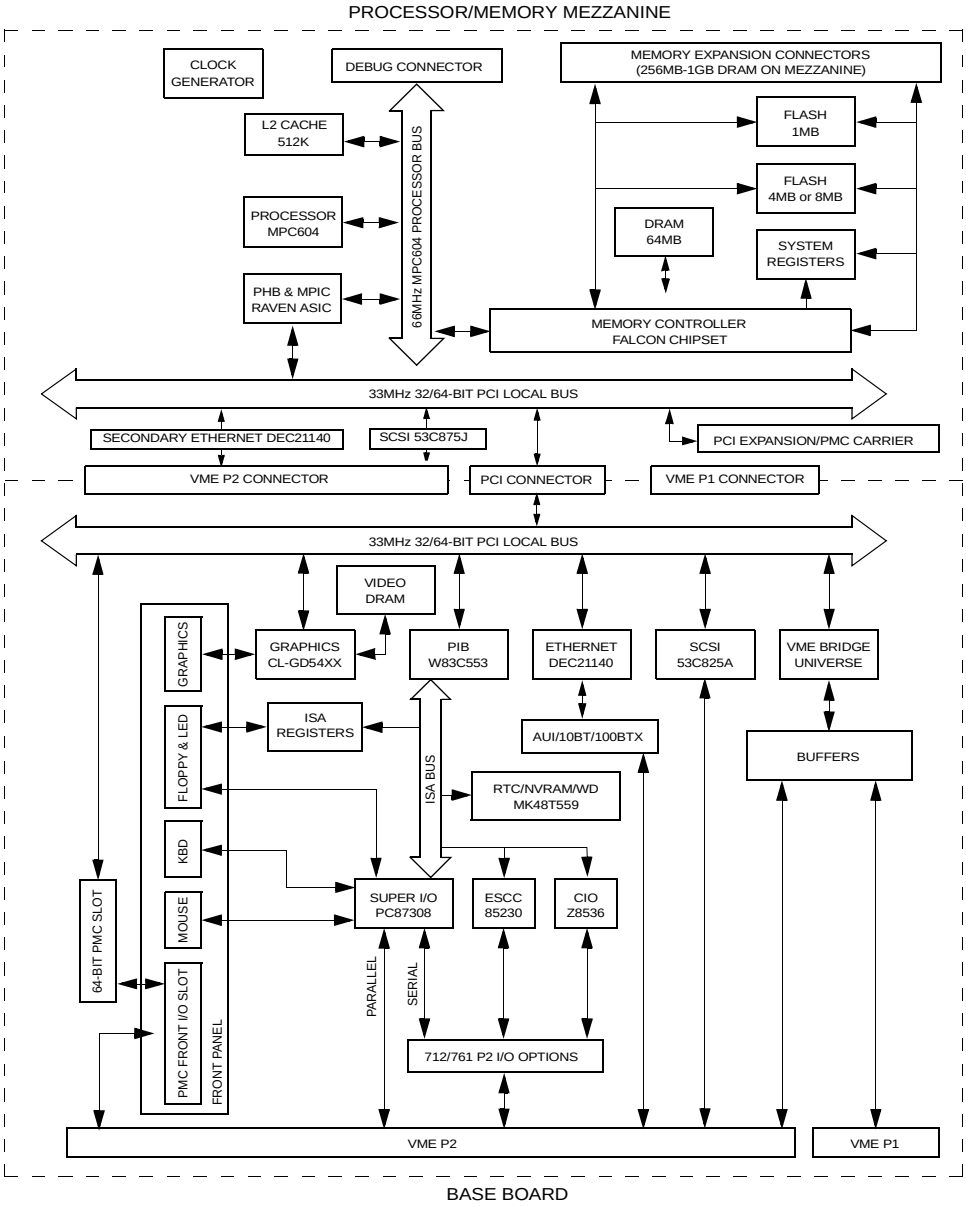


Figure 1-1. MVME3600 Series System Block Diagram

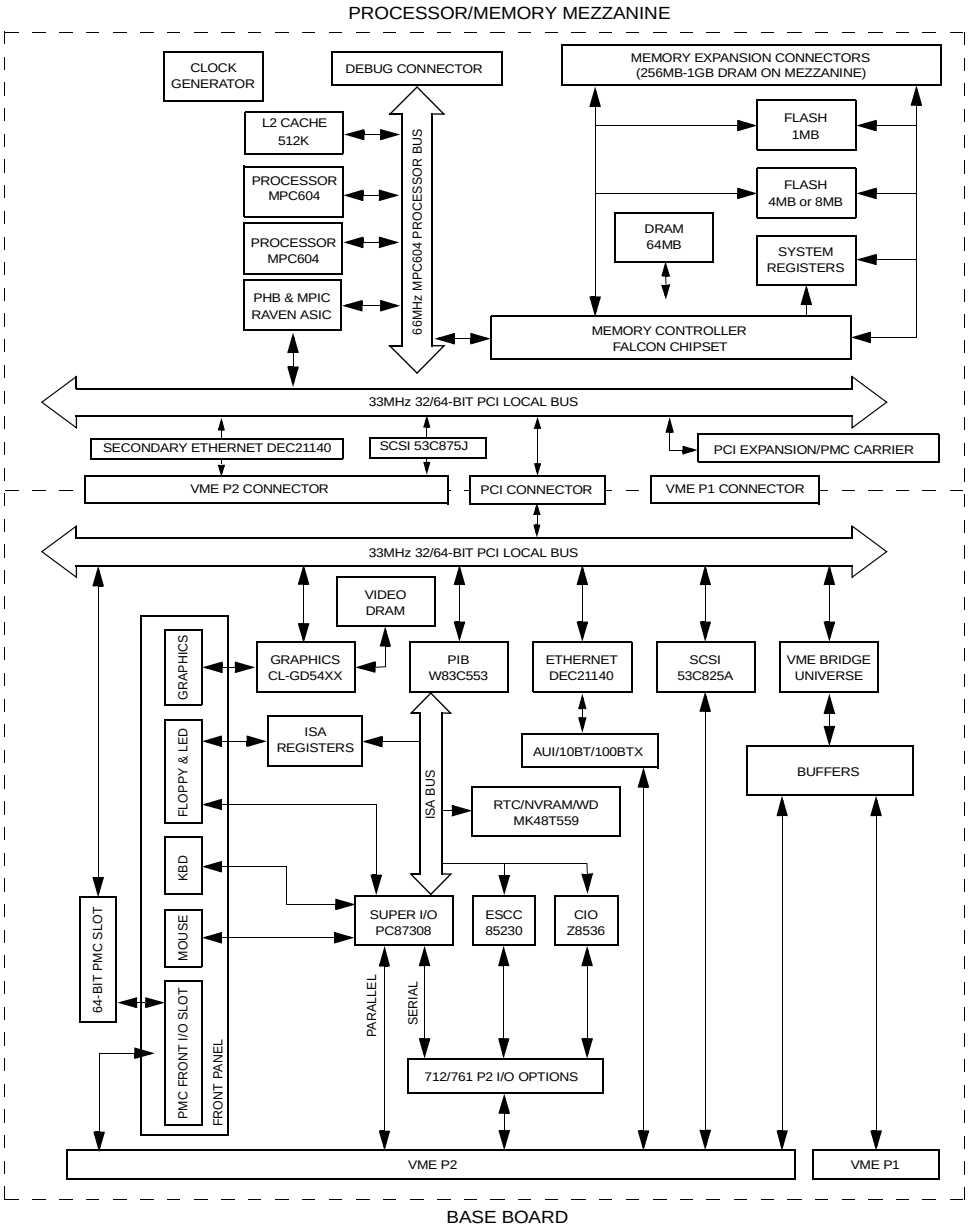


Figure 1-2. MVME4600 Series System Block Diagram

Equipment Required

To complete an MVME3600 or 4600 series system, you need the following equipment:

- ❏ VME system enclosure
- ❏ System console terminal
- ❏ Operating system (and/or application software)
- ❏ Disk drives (and/or other I/O) and controllers
- ❏ Transition module (MVME712M or MVME761) and connecting cables

MVME 3600 and 4600 series VMEmodules are factory-configured for I/O handling via either MVME712M or MVME761 transition modules.

Overview of Startup Procedure

The following table lists the things you will need to do before you can use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter, including all Caution and Warning notes, before you begin.

Table 1-1. Startup Overview

What you need to do...	Refer to...
Unpack the hardware.	*Unpacking Instructions* on page 1-6
Configure the hardware by setting jumpers on the boards and transition modules.	*MVME3600/4600 Series VMEmodule Preparation* on page 1-7 and *MVME712M Transition Module Preparation* on page 1-20 or *MVME761 Transition Module Preparation* on page 1-31
Ensure mezzanine boards are properly installed.	*Hardware Installation* on page 1-43, PMC Module; Processor/ Memory Mezzanine; RAM201 Memory Mezzanine; PMC Carrier Board
Install the MVME3600 or 4600 series VMEmodule in the chassis.	*MVME3600 and 4600 Series VMEmodule Install* on page 1-54, MVME3600/4600 Series VMEmodule

Table 1-1. Startup Overview

What you need to do...	Refer to...
Install the transition module in the chassis.	*MVME712M Transition Module* on page 1-56 or *MVME761 Transition Module* on page 1-59
Connect a console terminal.	*System Considerations* on page 1-62, MVME4600 Series VMEmodule
Connect any other equipment you will be using.	Chapter 4, *Connector Pin Assignments*
	For more information on optional devices and equipment, refer to the documentation provided with the equipment.
Power up the system.	*Applying Power* on page 2-1
	Appendix C, *Troubleshooting CPU Boards*
Note that the firmware initializes the board.	*Using the Debugger* on page 5-3
	You may also wish to obtain the *PPCBug Firmware Package User's Manual*, listed in Appendix D, *Related Documentation*.
Initialize the system clock.	Chapter 6, *CNFG and ENV Commands*
Examine and/or change environmental parameters.	Chapter 6, *CNFG and ENV Commands*
Program the board as needed for your applications.	*MVME3600/4600 Series VME Processor Module Programmer's Reference Guide*, listed in Appendix D, *Related Documentation*.

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Hardware Configuration

To produce the desired configuration and ensure proper operation of the MVME3600 or 4600 series VMEmodule, you may need to carry out certain hardware modifications before installing the module.

The MVME3600 and 4600 series VMEmodule provides software control over most options: by setting bits in control registers after installing the module in a system, you can modify its configuration. (The MVME3600/4600 series control registers are described in Chapter 3, *Functional Description*, and/or in the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide*, as listed in Appendix D, *Related Documentation*.)

Some options, however, are not software-programmable. Such options are controlled through manual installation or removal of header jumpers or interface modules on the MVME3600 and 4600 series VMEmodule or the associated transition module.

MVME3600/4600 Series VMEmodule Preparation

Figure 1-3 and Figure 1-4 illustrate the placement of the switches, jumper headers, connectors, and LED indicators on the base board and the processor/memory mezzanine respectively. Manually configurable items on the base board or processor/memory mezzanine are listed below.

On the base board:

- Remote status and control (J1)
- System controller selection (J5)
- Serial Port 3 transmit clock configuration (J15)

- Serial Port 4 transmit clock receiver buffer control (J9)
- Serial Port 4 receive clock configuration (J10)
- Serial Port 4 transmit clock configuration (J16)

On the processor/memory mezzanine:

- Firmware boot block protection (J1)
- Flash bank selection (J2)
- Secondary SCSI transfer rate (J13)

In conjunction with the serial port settings on the base board, serial ports on the associated MVME712M or MVME761 transition module are also manually configurable. For a discussion of the configurable items on the transition module, refer to *MVME712M Transition Module Preparation*, *MVME761 Transition Module Preparation*, or to the respective user's manuals for the transition modules (listed in Appendix D, *Related Documentation*) as necessary.

The MVME3600/4600 series VMEmodule is factory tested and shipped with the configurations described in the following sections. The MVME3600/4600 family's required and factory-installed debug monitor, PPCBug, operates with those factory settings.

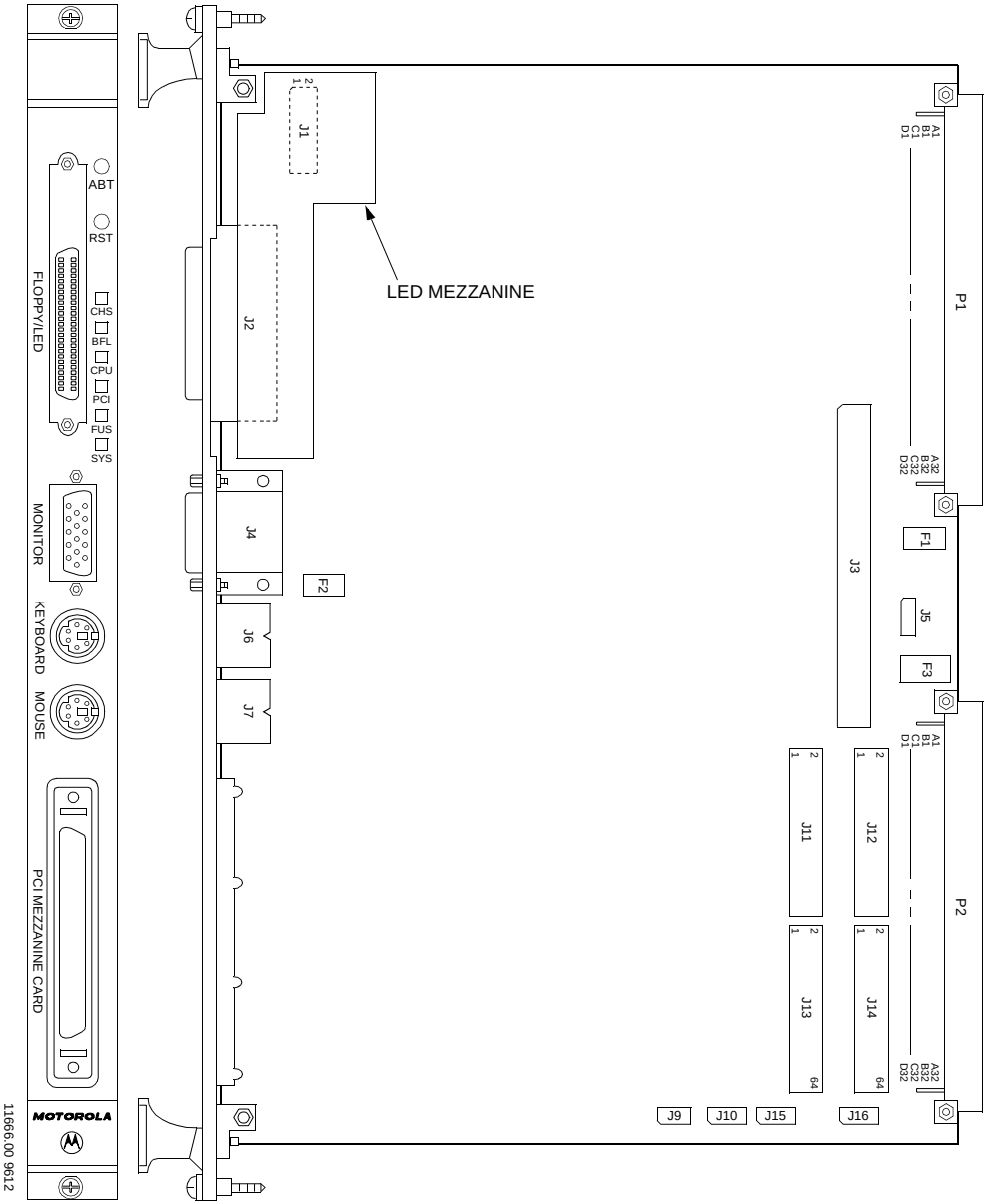


Figure 1-3. Base Board Switches, Headers, Connectors, Fuses, LEDs

Remote Status and Control (J1)

The MVME3600 and 4600 series front panel LEDs and switches are mounted on a removable mezzanine board. Removing the LED mezzanine makes the mezzanine connector (J1, a keyed double-row 14-pin connector on the base board) available for service as a remote status and control connector. In this application, J1 can be connected to a user-supplied external cable to carry the Reset and Abort signals and the LED lines to a control panel located apart from the MVME3600 or 4600 series VMEmodule. Maximum cable length is 15 feet.

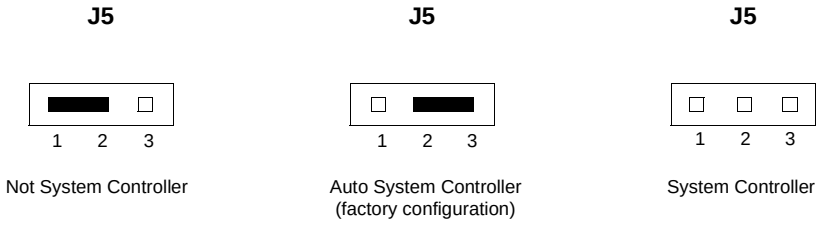
Table 4-1 on page 4-3 lists the pin numbers and signal mnemonics for J1.

System Controller Selection (J5)

The MVME3600 and 4600 series VMEmodule is factory-configured as an autoselective VMEbus system controller by a jumper placed across pins 2 and 3 of jumper header J5, located on the base board.

In the “automatic” system controller mode, the MVME3600 and 4600 series VMEmodule determines by its position in the backplane whether it should become the system controller. If the board is in the first slot from the left, it configures itself as the system controller. While the MVME3600 or 4600 is functioning as the system controller, the SCON LED is lit.

With J5 empty, the MVME3600 and 4600 functions as the system controller at all times. If the board is not to be the system controller under any circumstances, place the jumper on J5 pins 1 and 2.



Serial Port 3 Transmit Clock Configuration (J15)

In synchronous serial communications using the MVME761 transition module, you can configure Serial Port 3 on the MVME3600 and 4600 series VMEmodule to use the clock signals provided by the TxC signal line. On *MVME761-compatible* versions of the base board, header J15 configures port 3 to either drive or receive TxC. The factory configuration has port 3 set to receive TxC. J15 remains open on MVME712M-compatible versions.

To complete the configuration of Serial Port 3, you must set J2 on the MVME761 transition module (Serial Port 3 clock configuration) as well.

Figure 1-9 and Figure 1-10 (for the MVME712M) and Figure 1-16 and Figure 1-18 (for the MVME761) diagram the overall jumper settings required on the MVME3600 or 4600 and the transition module for a Serial Port 3 DCE or DTE configuration. Refer also to Table 1-2 below.

For additional details on the configuration of the MVME761 headers, refer to *MVME761 Transition Module* on page 1-59 or to the user's manual for the module (listed in Appendix D, *Related Documentation*).

NOTE: MVME761-compatible versions only. Leave J15 open on MVME712M I/O versions.

Table 1-2. MVME712/761 Jumper Settings

Jumper	For 712 I/O	For 761 I/O
J9	1-2	OPEN
J10	2-3	OPEN
J15	OPEN	2-3
J16	2-3	2-3

Serial Port 4 Transmit Clock Receiver Buffer Control (J9)

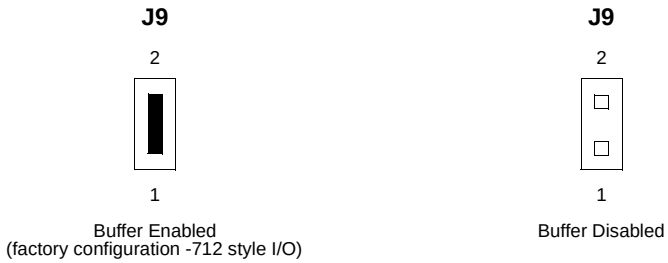
As described here and in other sections, a complete configuration of Serial Port 4 requires that you set the following jumper headers on the MVME3600 or 4600 series VMEmodule or the transition module:

- J10 (Serial Port 4 receive clock configuration) on *MVME712M-compatible* versions of the base board
- J16 (Serial Port 4 transmit clock configuration), both versions
- J9 (Serial Port 4 transmit clock receiver buffer control) on *MVME712M-compatible* versions of the base board
- J15 on the MVME712M transition module or J3 on the MVME761 (Serial Port 4 clock configuration)

A transmit clock receiver buffer (controlled by header J9) is associated with Serial Port 4. Installing a jumper on J9 enables the buffer. Removing the jumper disables the buffer. The factory configuration has the Serial Port 4 buffer enabled.

J9 remains open on MVME761-compatible versions. On MVME712M-compatible versions, J9 is set in tandem with J16 to configure the Serial Port 4 transmit clock. If one deviates from the factory configuration, so must the other. Figure 1-11 and Figure 1-12 (for the MVME712M) and Figure 1-17 and Figure 1-19 (for the MVME761) diagram the overall jumper settings required on the MVME3600/4600 and transition module for a Serial Port 4 DCE or DTE configuration.

For additional details on the configuration of those headers, refer to the *MVME712M Transition Module* or *MVME761 Transition Module* sections or to the user's manual for the transition module you are using (listed in Appendix D, *Related Documentation*).



Serial Port 4 Receive Clock Configuration (J10)

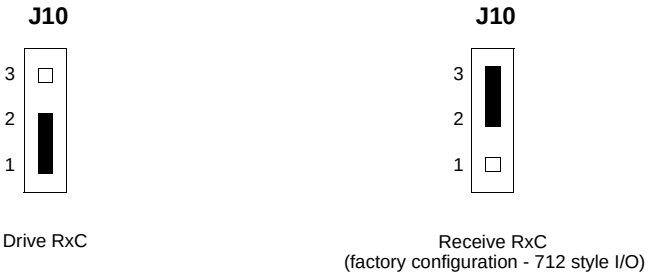
In synchronous serial communications, you can configure Serial Port 4 on the MVME3600/4600 series VMEmodules to use the clock signals provided by the RxC signal line. On *MVME712M-compatible* versions of the base board, header J10 configures port 4 to either drive or receive RxC. The factory configuration has port 4 set to receive RxC. J10 remains open on MVME761-compatible versions.

To complete the configuration of Serial Port 4, you must set the following configuration headers as well:

- J16 (Serial Port 4 transmit clock configuration)
- J9 (Serial Port 4 transmit clock receiver buffer control)
- J15 on the MVME712M transition module or J3 on the MVME761 transition module (Serial Port 4 clock configuration)

Figure 1-11 and Figure 1-12 (for the MVME712M) and Figure 1-17 and Figure 1-19 (for the MVME761) diagram the overall jumper settings required on the MVME3600 or 4600 and transition module for a Serial Port 4 DCE or DTE configuration.

For additional details on the configuration of those headers, refer to the *MVME712M Transition Module* or *MVME761 Transition Module* sections or to the user's manual for the transition module you are using (listed in Appendix D, *Related Documentation*).



Serial Port 4 Transmit Clock Configuration (J16)

In synchronous serial communications, you can configure Serial Port 4 on the MVME4600 series VMEmodule to use the clock signals provided by the TxC signal line. Header J16, located on the base board, configures port 4 to either drive or receive TxC. The factory configuration has port 4 set to receive TxC.

To complete the configuration of Serial Port 4, you must set the following configuration headers as well:

- J10 (Serial Port 4 receive clock configuration)
- J9 (Serial Port 4 transmit clock receiver buffer control)
- J15 on the MVME712M transition module or J3 on the MVME761 transition module (Serial Port 4 clock configuration)

Figure 1-11 and Figure 1-12 (for the MVME712M) and Figure 1-17 and Figure 1-19 (for the MVME761) diagram the overall jumper settings required on the MVME3600/4600 and transition module for a Serial Port 4 DCE or DTE configuration.

For additional details on the configuration of those headers, refer to the *MVME712M Transition Module* or *MVME761 Transition Module* sections or to the user's manual for the transition module you are using (listed in Appendix D, *Related Documentation*).

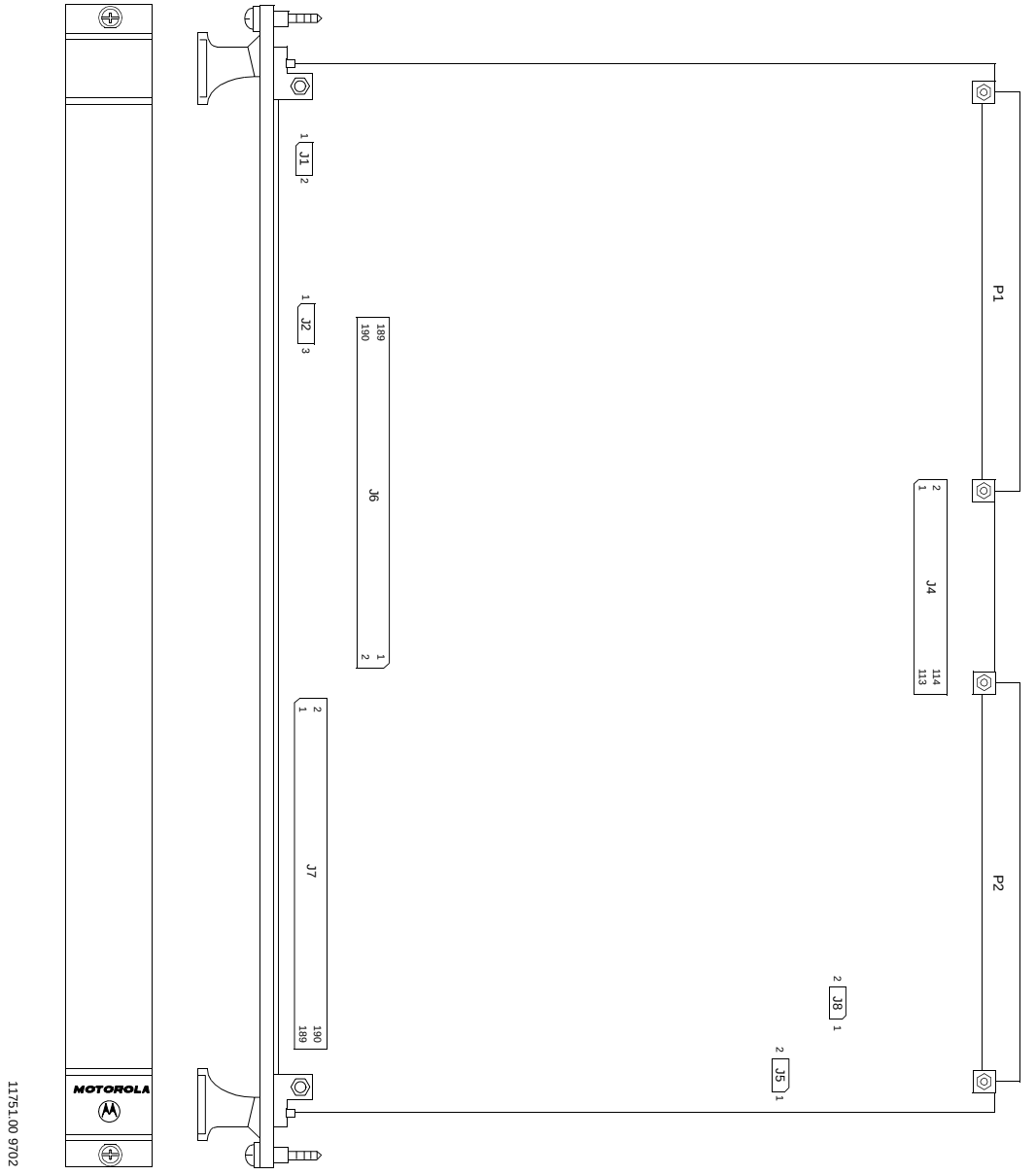


Figure 1-4. Processor/Memory Mezzanine Headers and Connectors

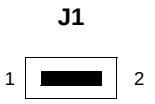
Firmware Boot Block Protection (J1)

Flash memory on the MVME3600 and 4600 series VMEmodules are organized in either one or two banks, each bank either 16 or 64 bits wide.

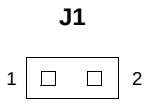
Flash bank A consists of 4MB or 8MB of firmware resident on soldered-in devices on the processor/memory mezzanine. Flash bank B contains 1MB of firmware located in sockets on the processor/memory mezzanine. Both banks contain the on-board firmware, PPCBug.

The first 16KB of Flash bank A contain the boot block portion of the firmware. Header J1 provides write protection for the boot block.

Installing a jumper across header J1 pins 1 and 2 protects the boot block portion of Flash bank A against overwriting. Removing the jumper permits reprogramming of the boot block area along with the rest of Flash memory. The factory configuration uses no jumper on J1, so that Flash bank A is reprogrammable in its entirety.



Boot Block Write-Protected



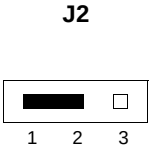
Boot Block Write-Enabled
(factory configuration)

Flash Bank Selection (J2)

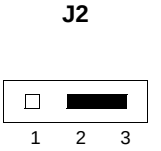
The MVME3600/4600 series processor/memory mezzanine has provision for 1MB of 16-bit Flash memory for the on-board firmware (or for customer-specific applications). In addition, it accommodates 4MB or 8MB of 64-bit Flash memory specifically for customer use.

The Flash memory is organized in either one or two banks, each bank either 16 or 64 bits wide. Both banks contain the on-board firmware, PPCBug.

To enable Flash bank A (4MB or 8MB of firmware resident on soldered-in devices on the processor/memory mezzanine), place a jumper across header J2 pins 1 and 2. To enable Flash bank B (1MB of firmware located in sockets on the processor/memory mezzanine), place a jumper across header J2 pins 2 and 3. The factory configuration uses Flash bank A.



Flash Bank A Enabled (4MB/8MB, Soldered)
(factory configuration)



Flash Bank B Enabled (1MB, Sockets)

Secondary SCSI Transfer Rate (J8)

In addition to the primary SCSI interface on the base board, an optional, secondary 16-bit SCSI interface is available on the PM604 processor/memory mezzanine. The secondary SCSI interface features “Ultra SCSI” (Fast-20) technology, permitting a data transfer rate of up to 40MB/s if the equipment supports it.

If that high a transfer rate is not desirable in your application, you can select a “Fast SCSI” speed of 20MB/s by installing a jumper across header J8 pins 1 and 2. Placing a jumper on J8 sets the GPIO1_MASTER line on the secondary SCSI controller chip low, and prevents the operating system from negotiating for “Ultra” speed on secondary SCSI devices.

The factory configuration uses no jumper on J8, so that an “Ultra” transfer rate is the default for secondary SCSI.

GPIO1_MASTER Line Low

GPIO1_MASTER Line High
(factory configuration)

MVME712M Transition Module Preparation

The MVME712M transition module (Figure 1-5 on page 1-22) and P2 adapter board are used in conjunction with certain models of the MVME3600 series VMEmodule.

The features of the MVME712M include:

- A parallel printer port
- An Ethernet interface supporting AUI connections
- Four EIA-232-D multiprotocol serial ports
- An SCSI interface (via P2 adapter) for connection to both internal and external devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Provision for modem connection
- Yellow LED for Ethernet transceiver power (DS1); green LED for SCSI terminator power (DS2)

The features of the three-row P2 adapter board (part number 01-W3496B01A) supplied with the MVME712M for three-row backplanes include:

- A 50-pin connector for SCSI cabling to the MVME712M and/or to other SCSI devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Fused SCSI terminator power developed from the +5V DC present at connector P2
- A 64-pin DIN connector to interface the EIA-232-D, parallel, SCSI, and Ethernet signals to the MVME712M

For installations in VME64 backplanes, you may wish to use the five-row P2 adapter and cable (model MVME761P2, part number 01-W3199F01A) supplied with the MVME761 transition module. Although the

MVME712M itself does not support the additional I/O capability on rows D and Z of the MVME4600's five-row P2 connector, those signals remain available for user-specific applications. To gain access to the 16-bit SCSI and PMC I/O present on rows D and Z when the MVME3600 or 4600 is installed in a VME64 backplane, use the five-row P2 adapter.

Serial Ports 1-4 DCE/DTE Configuration

Serial ports 1 through 4 are configurable as modems (DCE) for connection to terminals, or as terminals (DTE) for connection to modems. The MVME712M is shipped with the serial ports configured for DTE operation. Serial port DCE/DTE configuration is accomplished by positioning jumpers on one of two headers per port. The following table lists the serial ports with their corresponding jumper headers.

Table 1-3. MVME712M Port/Jumper Correspondence

Serial Port	Board Connector	Panel Connector	Jumper Header
Port 1	J7	SERIAL PORT 1/ CONSOLE	J1/J11
Port 2	J8	SERIAL PORT 2/ TTY	J16/J17
Port 3	J9	SERIAL PORT 3	J13/J14
Port 4	J10	SERIAL PORT 4	J18/J19

Figure 1-7 on page 1-24 through Figure 1-12 on page 1-29 show the MVME3600/4600 series VMEmodule and MVME712M transition module with interconnections and jumper settings for DCE/DTE configuration on each serial port.

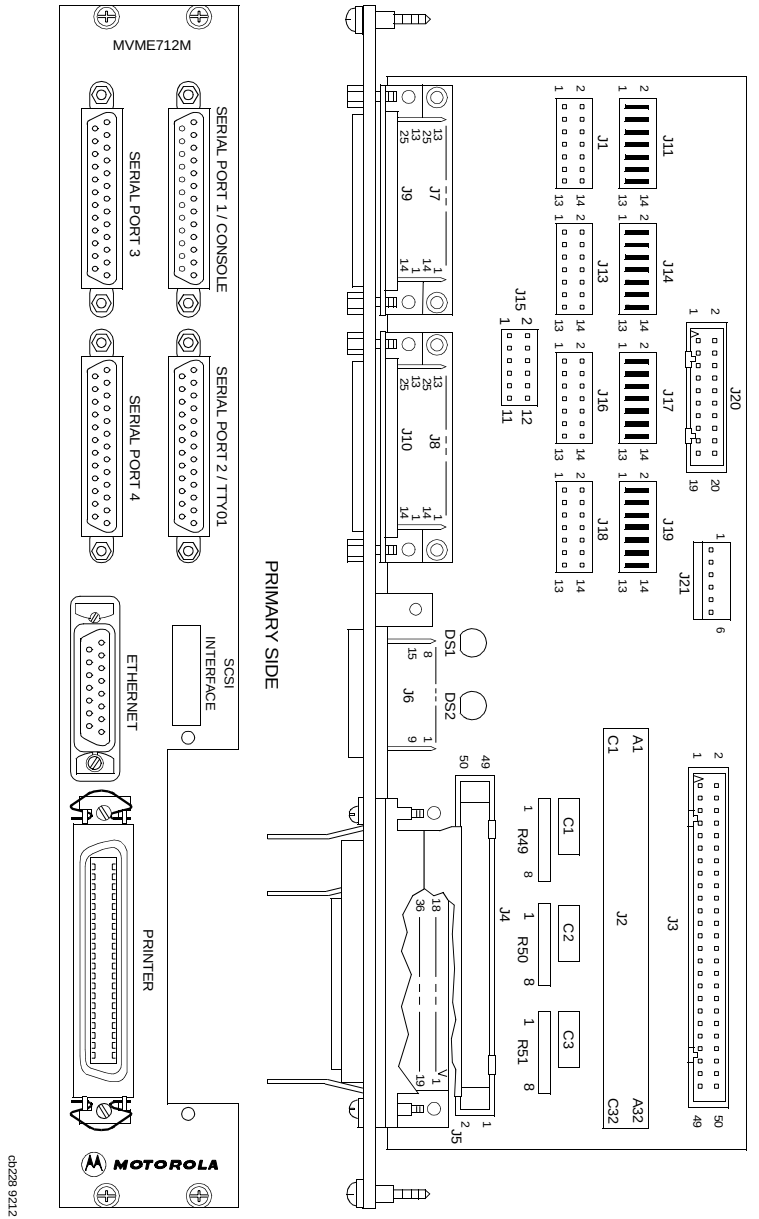


Figure 1-5. MVME712M Connector and Header Locations

Serial Port 4 Clock Configuration

Port 4 can be configured via J15 (Figure 1-6) to use the TrxC4 and RtxC4 signal lines. Part of the configuration is done with headers J9, J10, and J16 on the MVME3600/4600 (Figure 1-11 and Figure 1-12).

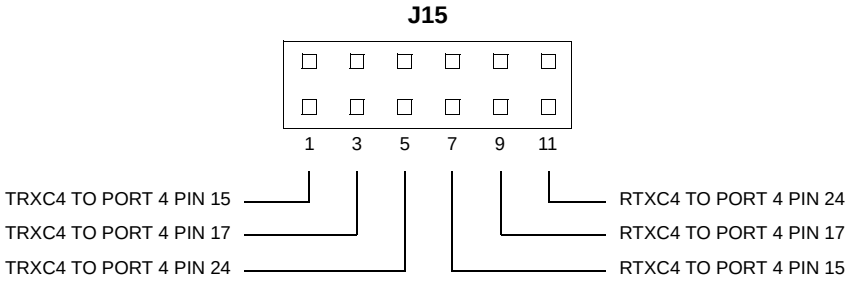


Figure 1-6. J15 Clock Line Configuration

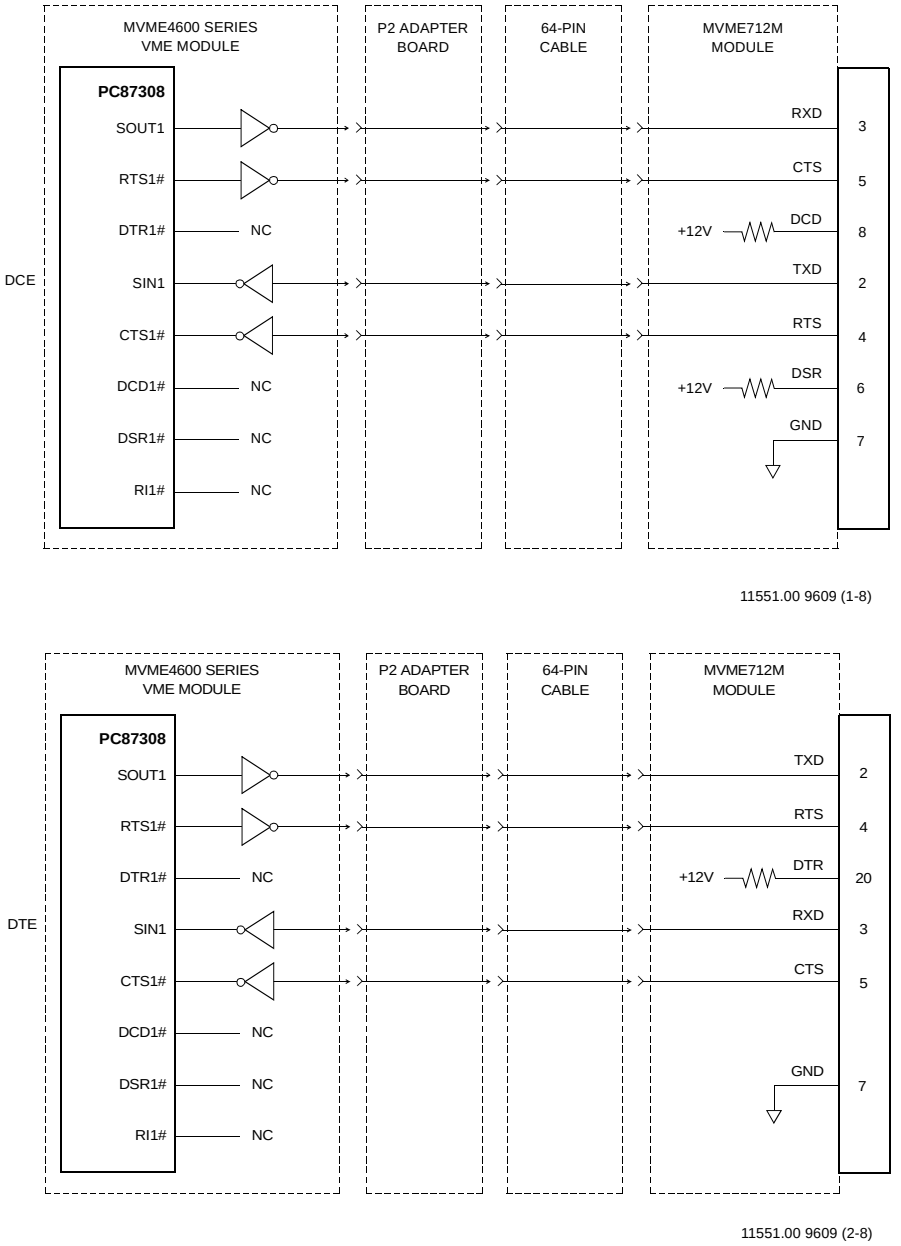


Figure 1-7. MVME712M Serial Port 1 DCE/DTE Configuration

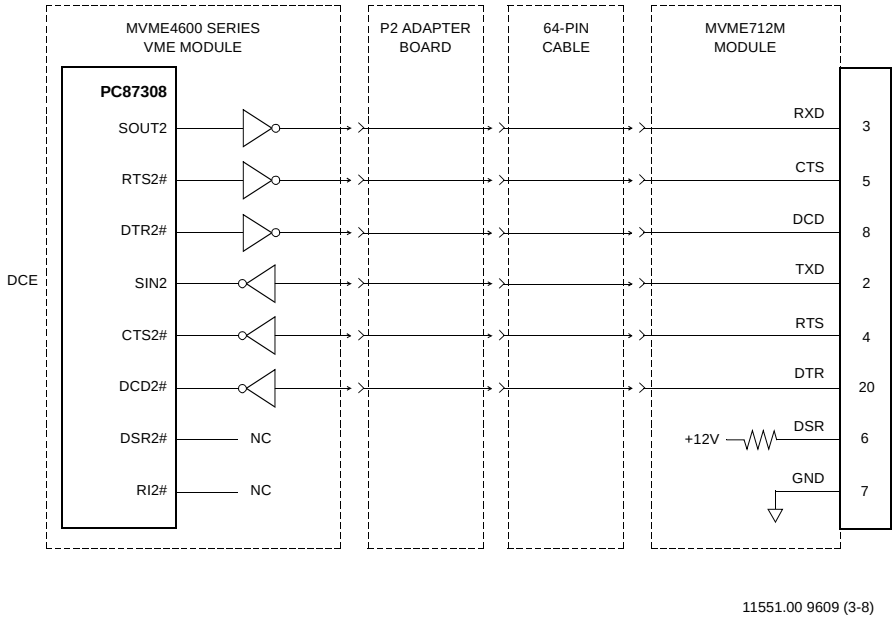


Figure 1-8. MVME712M Serial Port 2 DCE/DTE Configuration

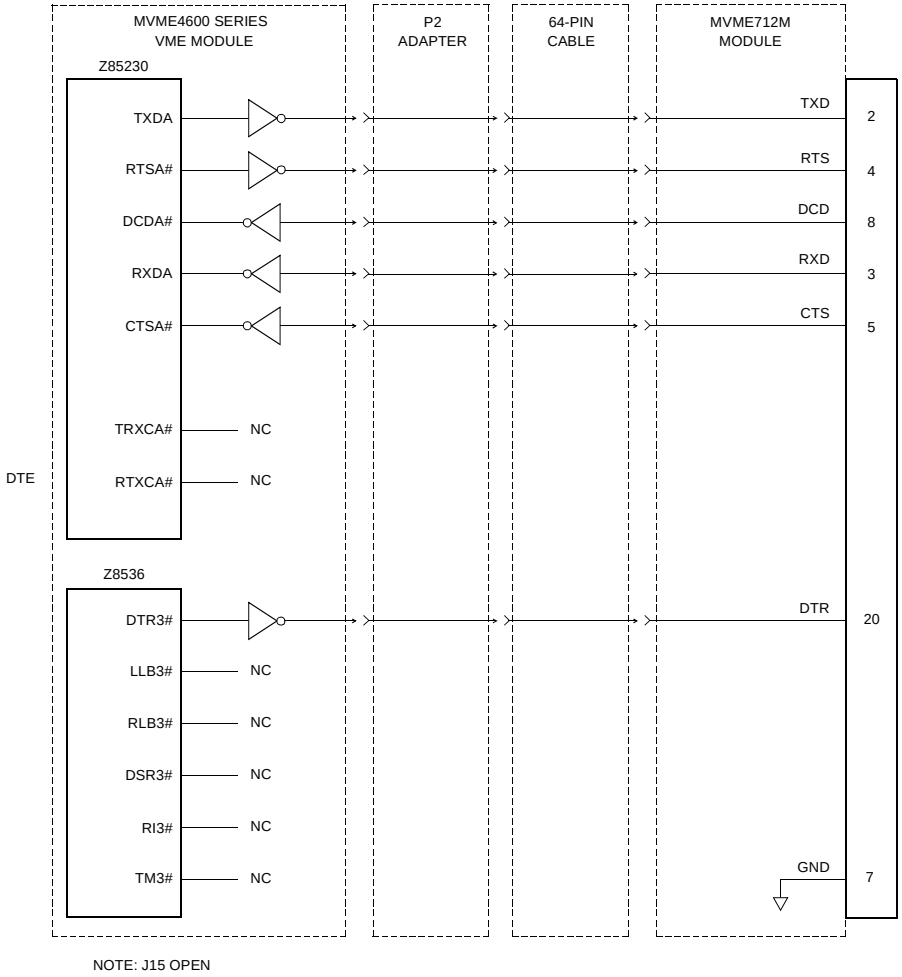


Figure 1-10. MVME712M Serial Port 3 DTE Configuration

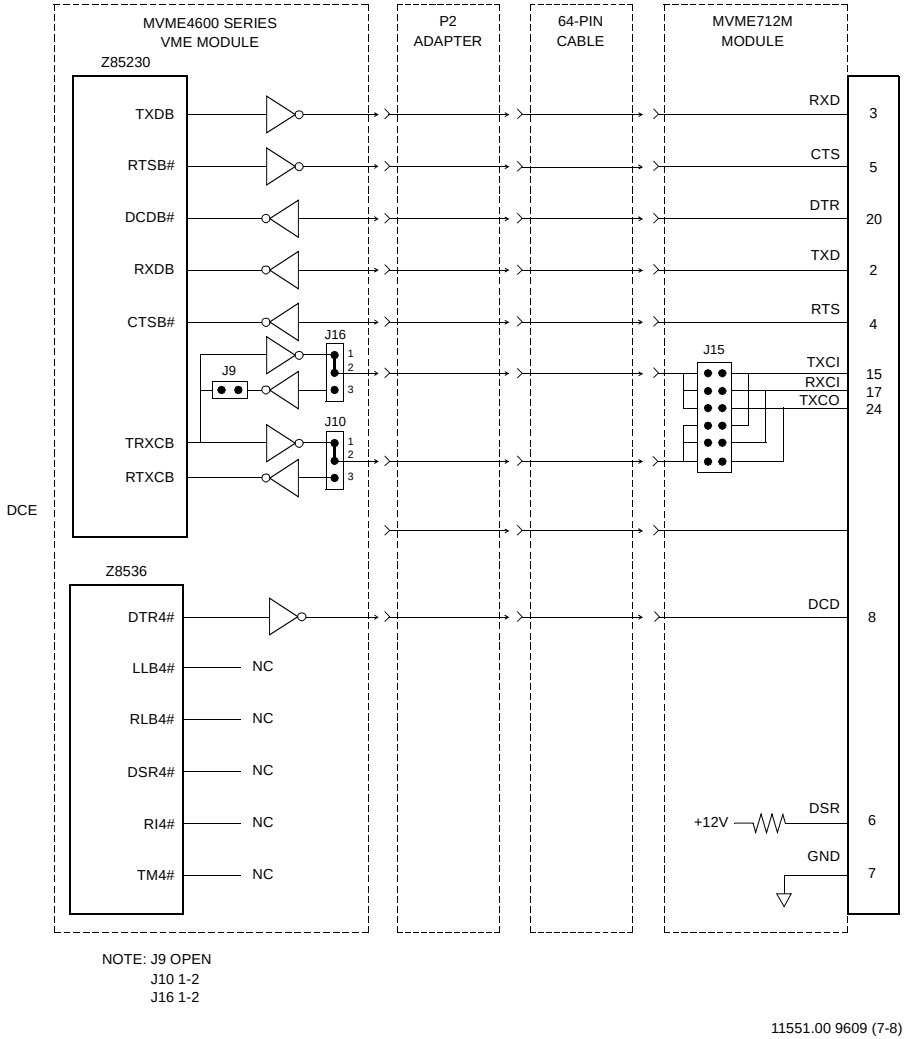


Figure 1-11. MVME712M Serial Port 4 DCE Configuration

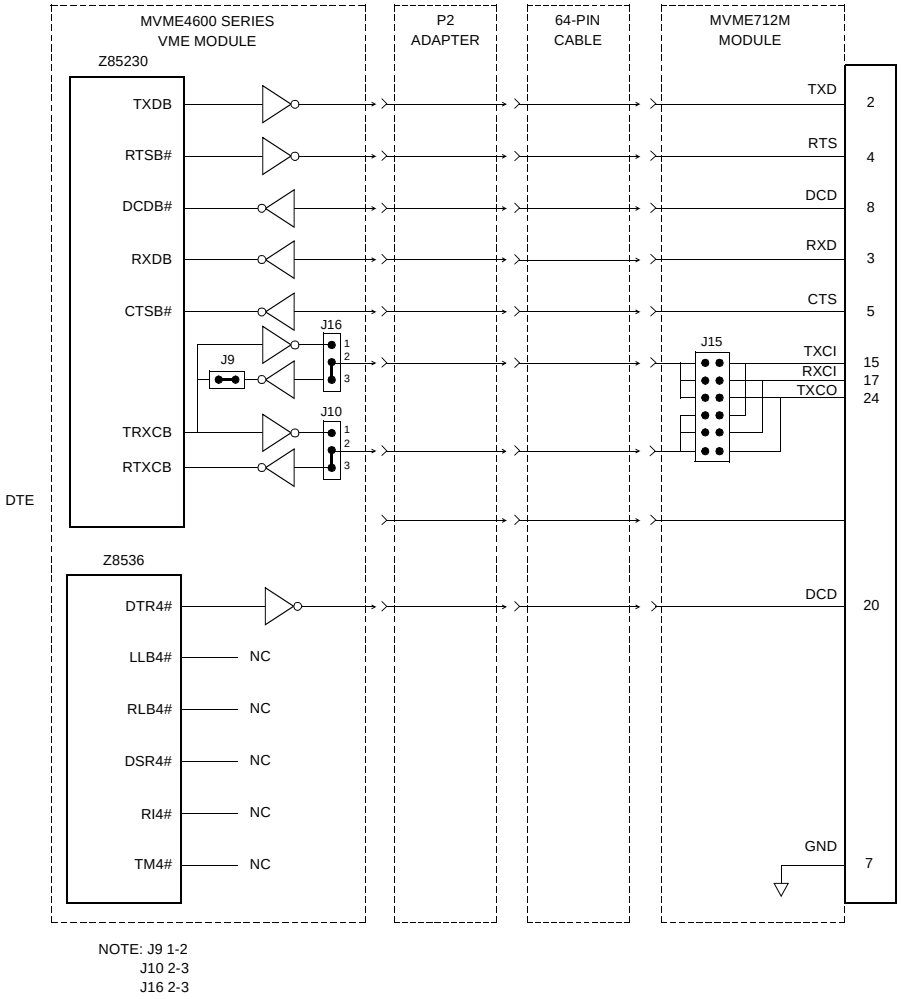


Figure 1-12. MVME712M Serial Port 4 DTE Configuration

P2 Adapter Preparation

In its factory configuration, the MVME712M transition module uses a three-row P2 adapter to transfer synchronous/asynchronous serial, parallel, and Ethernet signals to and from the MVME3600 and 4600 series VMEmodule base board. A 50-pin male connector (J3) on the P2 adapter carries 8-bit SCSI signals from the MVME3600 and 4600.

Preparation of the three-row P2 adapter for the MVME712M consists of removing or installing the SCSI terminating resistors, R1-R3. Figure 1-13 illustrates the location of the resistors, the connectors, and SCSI terminator power fuse F1. For further information on the preparation of the transition module and the P2 adapter, refer to the user's manual for the MVME712M (listed in Appendix D, *Related Documentation*) as necessary.

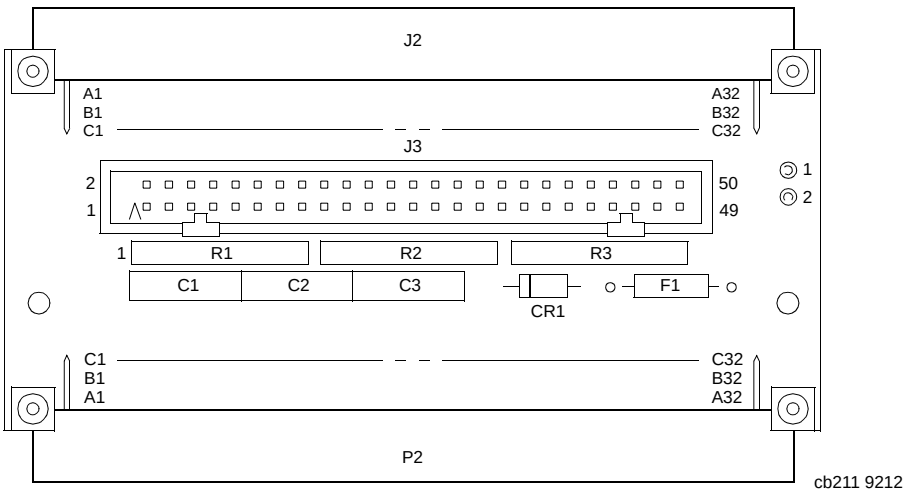


Figure 1-13. MVME712M Three-Row P2 Adapter

If you plan to connect the MVME712M to a VME64 backplane with a five-row P2 adapter (part number 01-W3199F01A), refer to the *P2 Adapter Preparation* segment of *MVME761 Transition Module Preparation* on page 1-31 for guidelines on preparing the adapter.

MVME761 Transition Module Preparation

The MVME761 transition module (Figure 1-14) and P2 adapter board are used in conjunction with the certain models of the MVME3600 and 4600 series VMEmodules.

The features of the MVME761 include:

- A parallel printer port (IEEE 1284-I compliant)
- An Ethernet interface supporting 10BaseT/100BaseTX connections
- Two EIA-232-D asynchronous serial ports (identified as COM1 and COM2 on the front panel)
- Two synchronous/asynchronous serial ports (SERIAL 3 and SERIAL 4 on the front panel), configurable for EIA-232-D, EIA-530, V.35, or X.21 protocols
- Two 60-pin Serial Interface Module (SIM) connectors, used on configuring serial ports 3 and 4

Both three-row and five-row P2 adapter boards are available for the MVME761. Their features include:

- A 50-pin (three-row adapter) or 68-pin (five-row adapter) connector for cabling to SCSI devices
- Jumper-selectable active SCSI terminating resistors
- Fused SCSI terminator power developed from the +5V DC present at connector P2
- A 64-pin 3M connector to the MVME761

Use the MVME761's three-row P2 adapter board in three-row VME backplanes. Use the five-row adapter in VME64 backplanes, which are equipped with five-row P2 connectors.

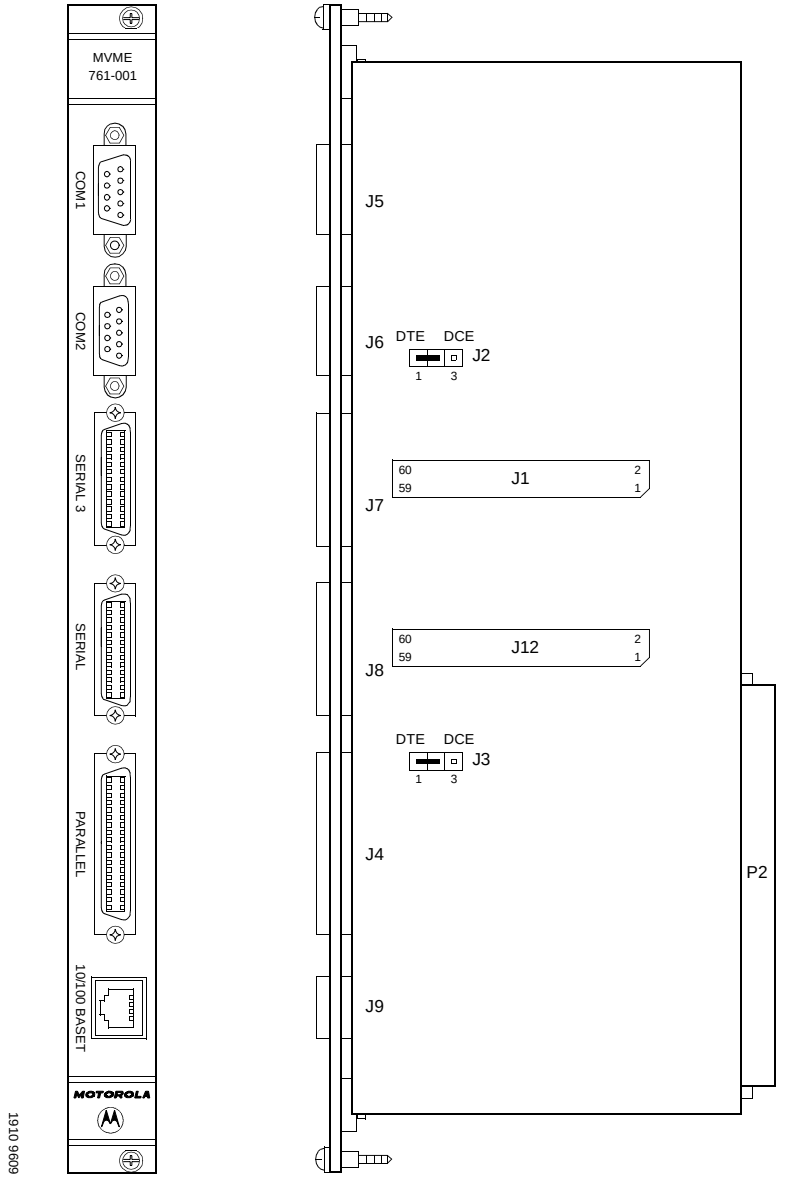


Figure 1-14. MVME761 Connector and Header Locations

Serial Ports 1 and 2

On MVME761-compatible models of the MVME3600/4600 series VMEmodule, the asynchronous serial ports (Serial Ports 1 and 2) are configured permanently as data circuit-terminating equipment (DCE). The port configuration is illustrated in Figure 1-15 on page 1-35.

Serial Ports 3 and 4

The synchronous serial ports, Serial Port 3 and Serial Port 4, are configurable through a combination of serial interface module (SIM) selection and jumper settings. The following table lists the SIM connectors and jumper headers corresponding to each of the synchronous serial ports.

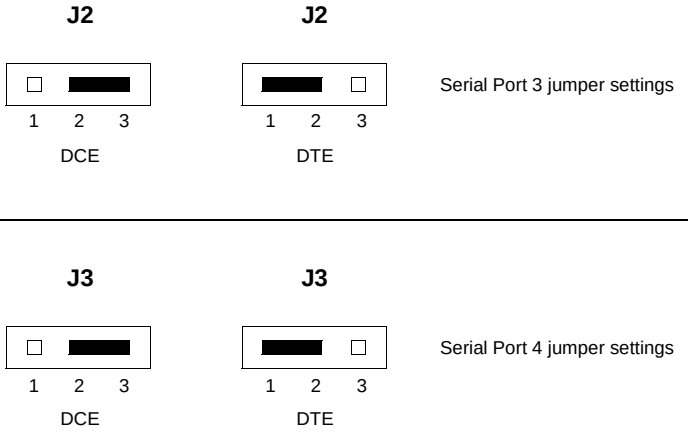
Synchronous Port	Board Connector	SIM Connector	Jumper Header
Port 3	J7	J1	J2
Port 4	J8	J12	J3

Port 3 is routed to board connector J7. Port 4 is available at board connector J8. Eight serial interface modules are available:

- EIA-232-D (DCE and DTE)
- EIA-530 (DCE and DTE)
- V.35 (DCE and DTE)
- X.21 (DCE and DTE)

You can configure Serial Ports 3 and 4 for any of the above serial protocols by installing the appropriate serial interface module and setting the corresponding jumper. SIMs can be ordered separately as required.

Headers J2 and J3 are used to configure Serial Port 3 and Serial Port 4, respectively, in tandem with SIM selection. With the jumper in position 1-2, the port is configured as a DTE. With the jumper in position 2-3, the port is configured as a DCE. *The jumper setting of the port should match the configuration of the corresponding SIM module.*



When installing the SIM modules, note that the headers are keyed for proper orientation.

For further information on the preparation of the transition module, refer to the user's manual for the MVME761 (listed in Appendix D, *Related Documentation*) as necessary.

The next five figures illustrate the MVME3600/4600 series VMEmodule and MVME761 transition module with the interconnections and jumper settings for DCE/DTE configuration on each serial port.

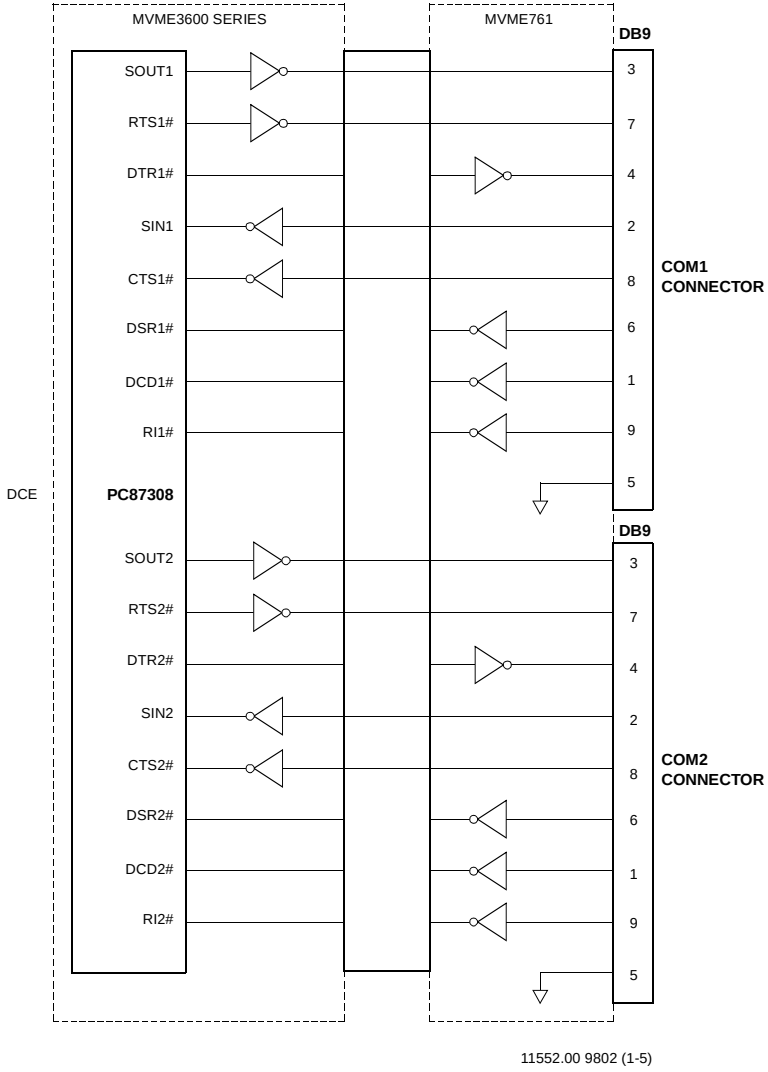


Figure 1-15. MVME761 Serial Ports 1 and 2 (DCE Only)

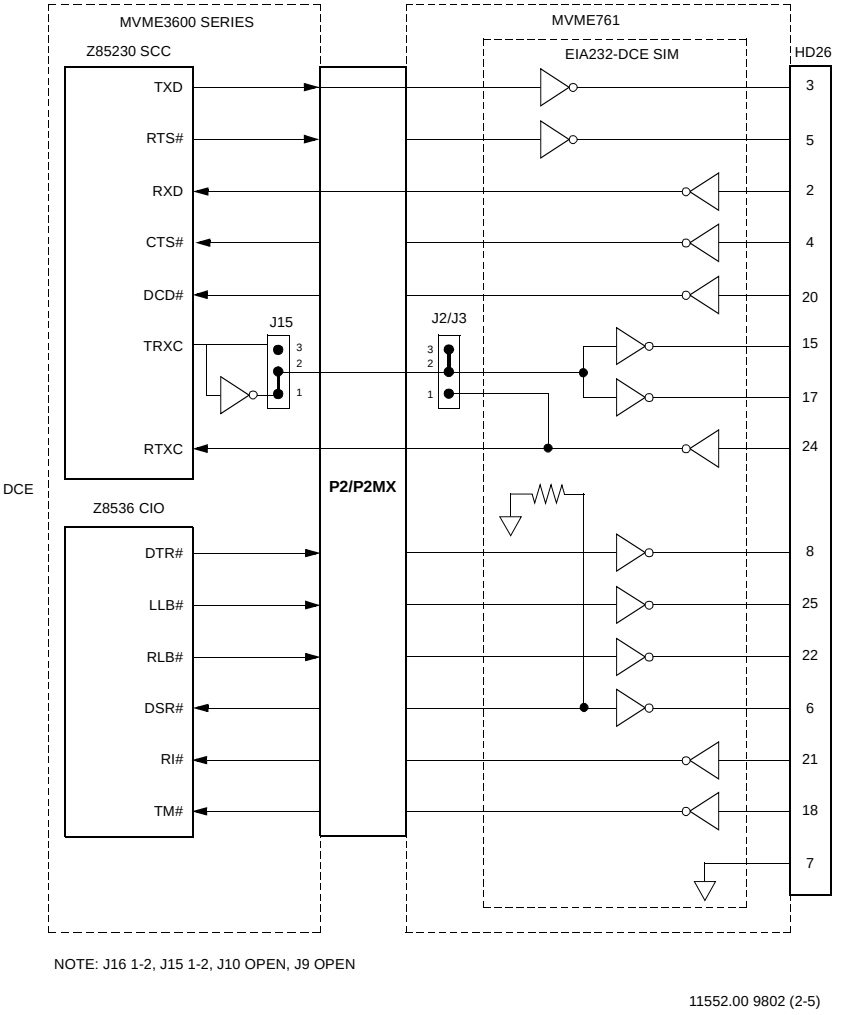


Figure 1-16. MVME761 Serial Port 3 DCE Configuration

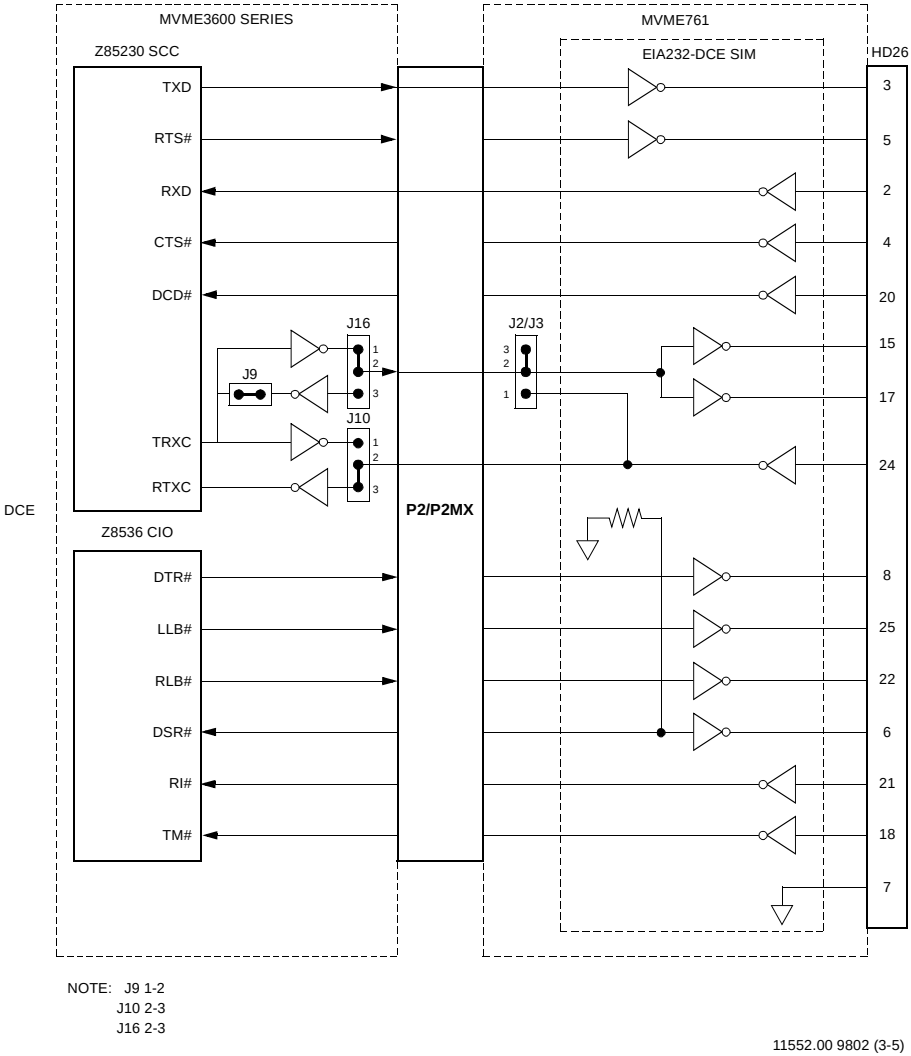


Figure 1-17. MVME761 Serial Port 4 DCE Configuration

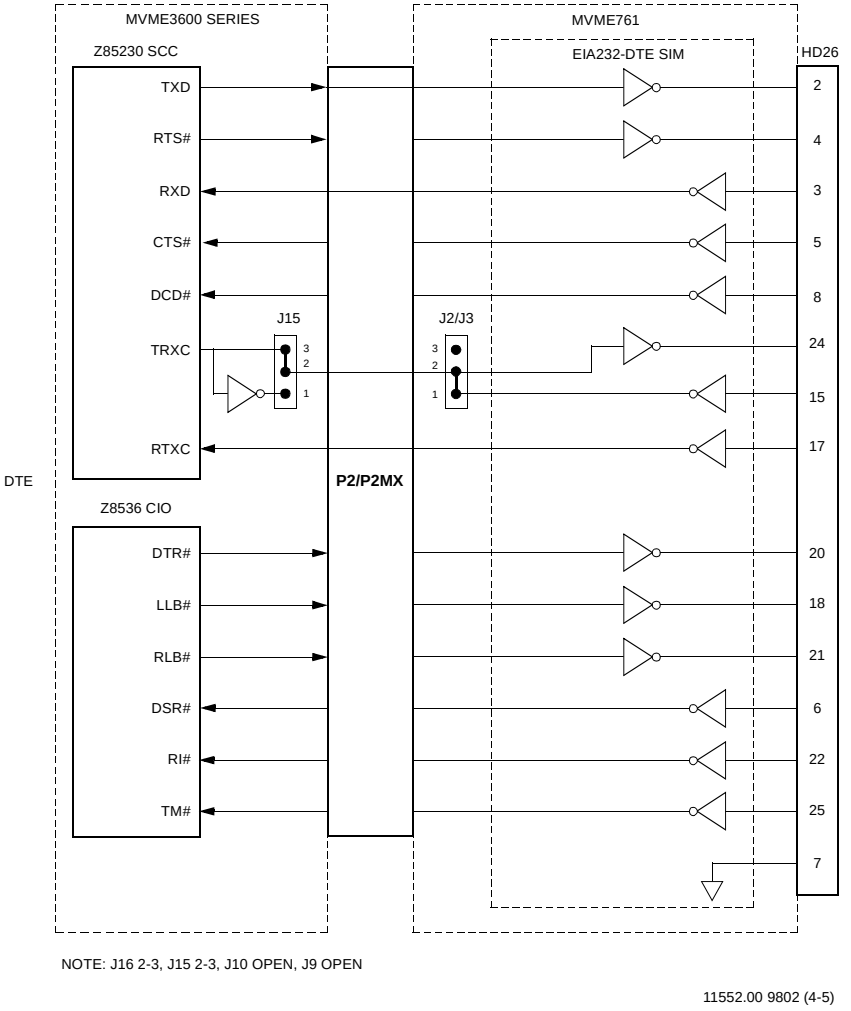


Figure 1-18. MVME761 Serial Port 3 DTE Configuration

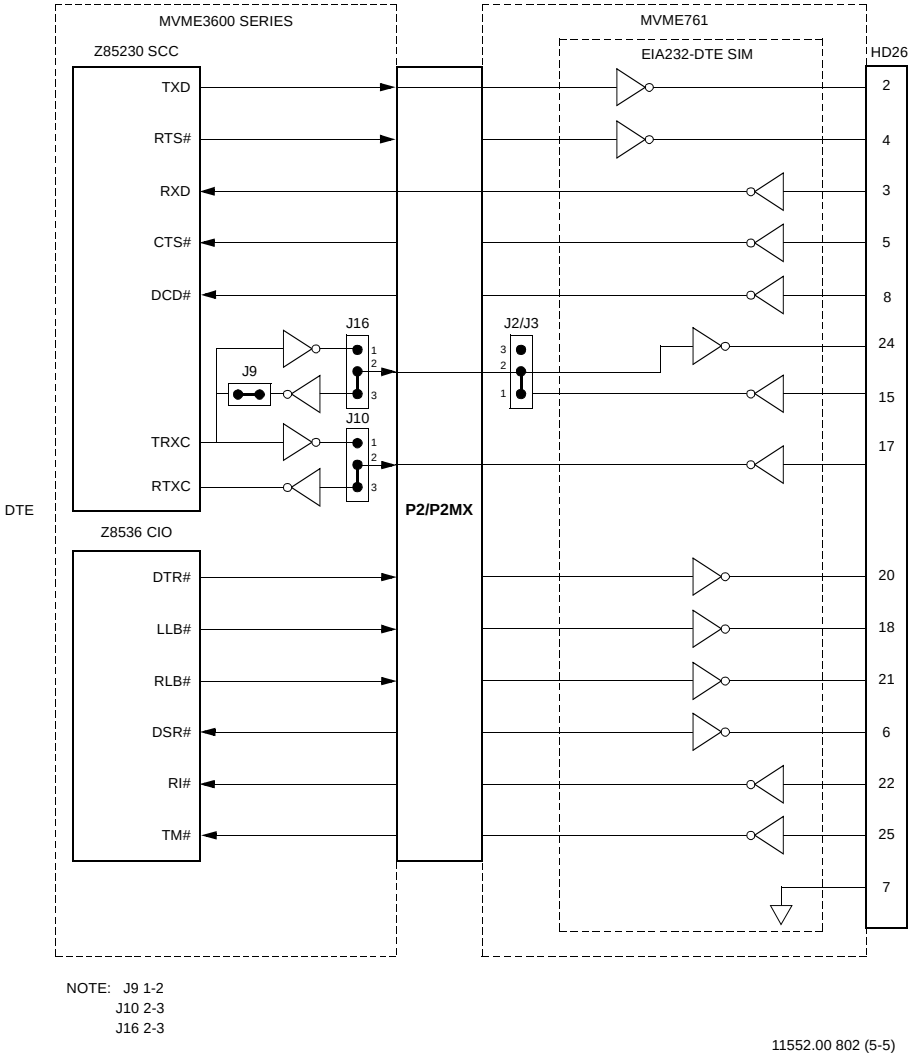


Figure 1-19. MVME761 Serial Port 4 DTE Configuration

P2 Adapter Preparation

The MVME761 transition module uses a three-row (model MVME761-001) or five-row (model MVME761-011) P2 adapter to transfer serial, parallel, and Ethernet signals to and from the MVME3600 and 4600 series VMEmodule base board.

Three-Row Adapter

On the three-row P2 adapter, a 50-pin male connector (J2) also carries 8-bit SCSI signals from the MVME3600 and 4600 base board. (To run external SCSI devices, you may install an optional front panel extension, MVME761EXT, next to the MVME761. The panel extension supplies both 8- and 16-bit SCSI.)

Preparation of a three-row P2 adapter for the MVME761 consists of installing a jumper on header J1 to enable the SCSI terminating resistors if necessary. Figure 1-20 illustrates the location of the jumper header and connectors on the MVME761's three-row P2 adapter.

For basic preparation of the five-row P2 adapter, refer to the next section.

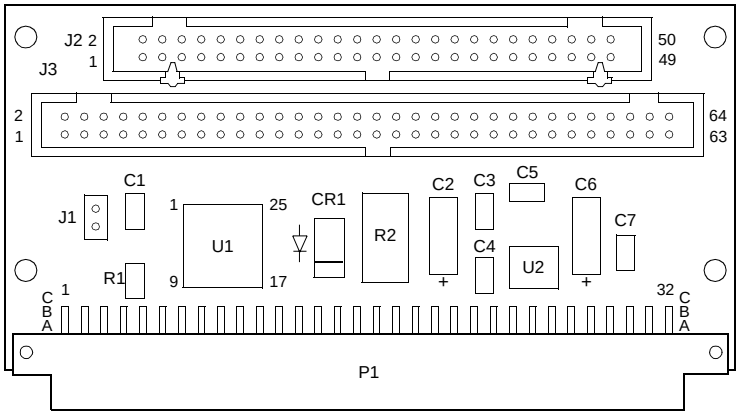


Figure 1-20. MVME761 Three-Row P2 Adapter

Five-Row Adapter

On the five-row adapter for the MVME761, a 68-pin female connector (J1) carries 16-bit SCSI signals from the MVME3600 or 4600 base board. (To run external SCSI devices, you may install an optional front panel extension, MVME761EXT, next to the MVME761. The panel extension supplies both 8- and 16-bit SCSI.) In addition, the five-row P2 adapter also supports PMC I/O via connector J3.

Preparation of a five-row P2 adapter for the MVME761 consists of installing a jumper on header J5 to enable the SCSI terminating resistors if necessary. Figure 1-21 illustrates the location of the jumper header, the connectors, and SCSI terminator power fuse (polyswitch) R4.

For further information on the preparation of the transition module and the P2 adapter, refer to the user's manual for the MVME761 (listed in Appendix D, *Related Documentation*) as necessary.

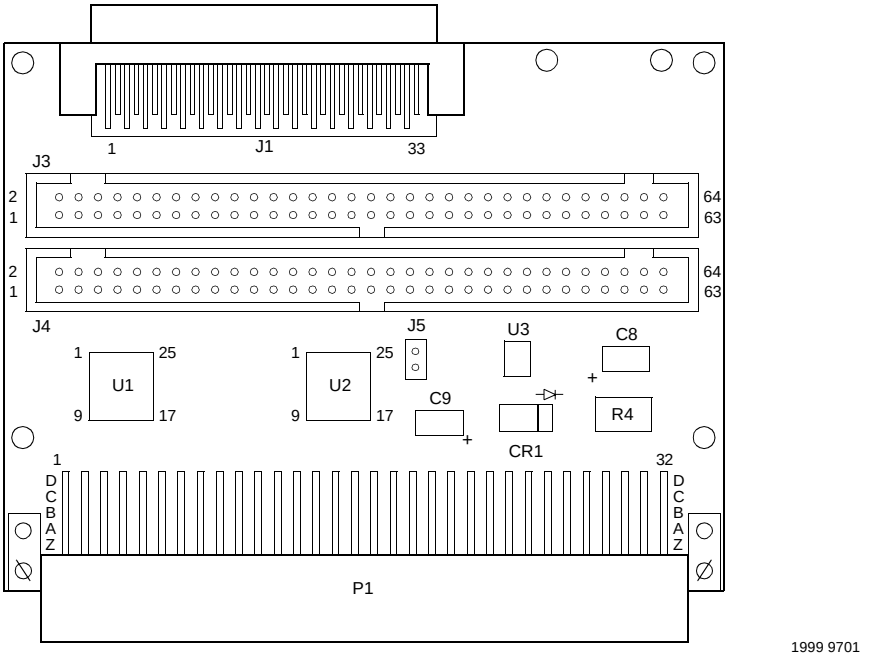


Figure 1-21. MVME761 Five-Row P2 Adapter

Hardware Installation

The following sections discuss the placement of mezzanine cards on the base board, the installation of the complete MVME3600 or 4600 series VMEmodule assembly and transition module into a VME chassis, and the system considerations relevant to the installation. Before installing the MVME3600 or 4600, ensure that the serial ports and all header jumpers are configured as desired.

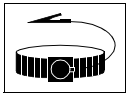
In most cases, the mezzanine cards—the twin-processor PM604 processor/memory mezzanine, RAM201 ECC DRAM module, the optional PCI mezzanine (if applicable), and the optional carrier board for additional PCI expansion (if applicable)—are already in place on the base board. The user-configurable jumpers are accessible with the mezzanines installed. Should it be necessary to install mezzanines on the base board, refer to the following sections for a brief description of the installation procedure.

Caution

Mixing of MVME3600/4600 series processor/memory and base modules with MVME1600 series base and processor/memory modules is *not* supported. Motorola cannot predict or guarantee the performance of any such mixture of modules.

ESD Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.

PMC Module

PCI mezzanine card (PMC) modules mount on top of the base board, below the processor/memory mezzanine. To install a PMC module, refer to Figure 1-22 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodule card cage.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. If the MVME3600 or 4600 series VMEmodule is presently installed in a system, carefully remove the module from its VMEbus card slot.
4. Lay the module flat, with connectors P1 and P2 facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

5. Remove the PMC carrier board (if installed), the RAM201 memory mezzanine, and the PM604 processor/memory mezzanine from the base board. To do so, reverse the installation procedures described in the applicable sections.

6. Remove the PCI filler from the front panel.

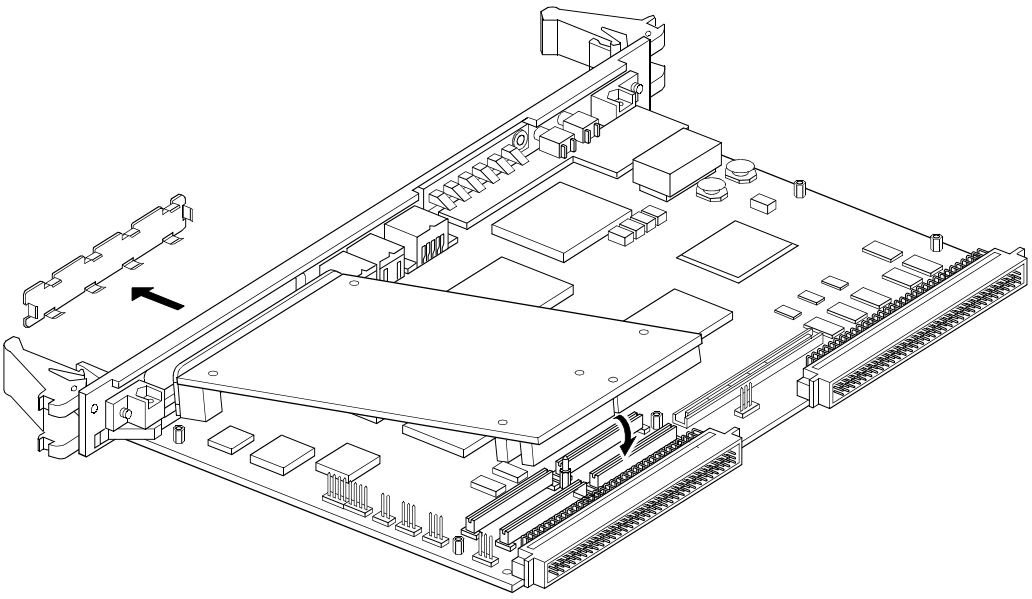


Figure 1-22. PMC Module Placement on Base Board

7. Slide the edge connector of the PMC module into the front panel opening from behind and place the PMC module on top of the base board. The four connectors on the underside of the PMC module should then connect smoothly with the corresponding connectors (J11/12/13/14) on the base board. Be sure the 5V keying pin at the rear of the base board (between the four PMC connectors) fits through the hole in the PMC module.

8. Insert the short Phillips screws through the underside of the base board, into the standoffs at the corners of the PMC module. (Some modules take a screw at each corner; others require only two screws at the forward corners). Tighten the screws.

9. Reinstall the processor/memory mezzanine, the RAM201 memory mezzanine, and the PMC carrier board (if previously installed) on the base board. To do so, carry out the installation procedures described in the applicable sections.
10. Reinstall the MVME3600 or 4600 series assembly in its proper card slot. Be sure the module is well seated in the backplane connectors. Do not damage or bend connector pins.
11. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

Processor/Memory Mezzanine

Processor/memory mezzanine boards mount on top of the base board, above the PMC module (if installed). To upgrade or install a mezzanine, refer to Figure 1-23 on page 1-48 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodule card cage.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the MVME3600 or 4600 series module from its VMEbus card slot and lay it flat, with connectors P1 and P2 facing you.

Caution Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. Remove the PMC carrier board (if installed) and the RAM201 memory mezzanine from the processor/memory mezzanine. To do so, reverse the installation procedures described in the applicable sections.
5. Remove the four standoffs and the two short Phillips screws that secure the processor/memory mezzanine to the base board. Separate the mezzanine from the base board.
6. Place the new processor/memory mezzanine on top of the base board. The connector on the underside of the processor/memory mezzanine should connect smoothly with the corresponding connector J3 (located between P1 and P2) on the base board.
7. Reinstall the four standoffs and the two short Phillips screws that secure the processor/memory mezzanine to the base board.
8. Reinstall the RAM201 memory mezzanine and the PMC carrier board (if previously installed) on the processor/ memory mezzanine. To do so, carry out the installation procedures described in the applicable sections.
9. Reinstall the MVME3600 or 4600 series assembly in its proper card slot. Be sure the module is well seated in the backplane connectors. Do not damage or bend connector pins.
10. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

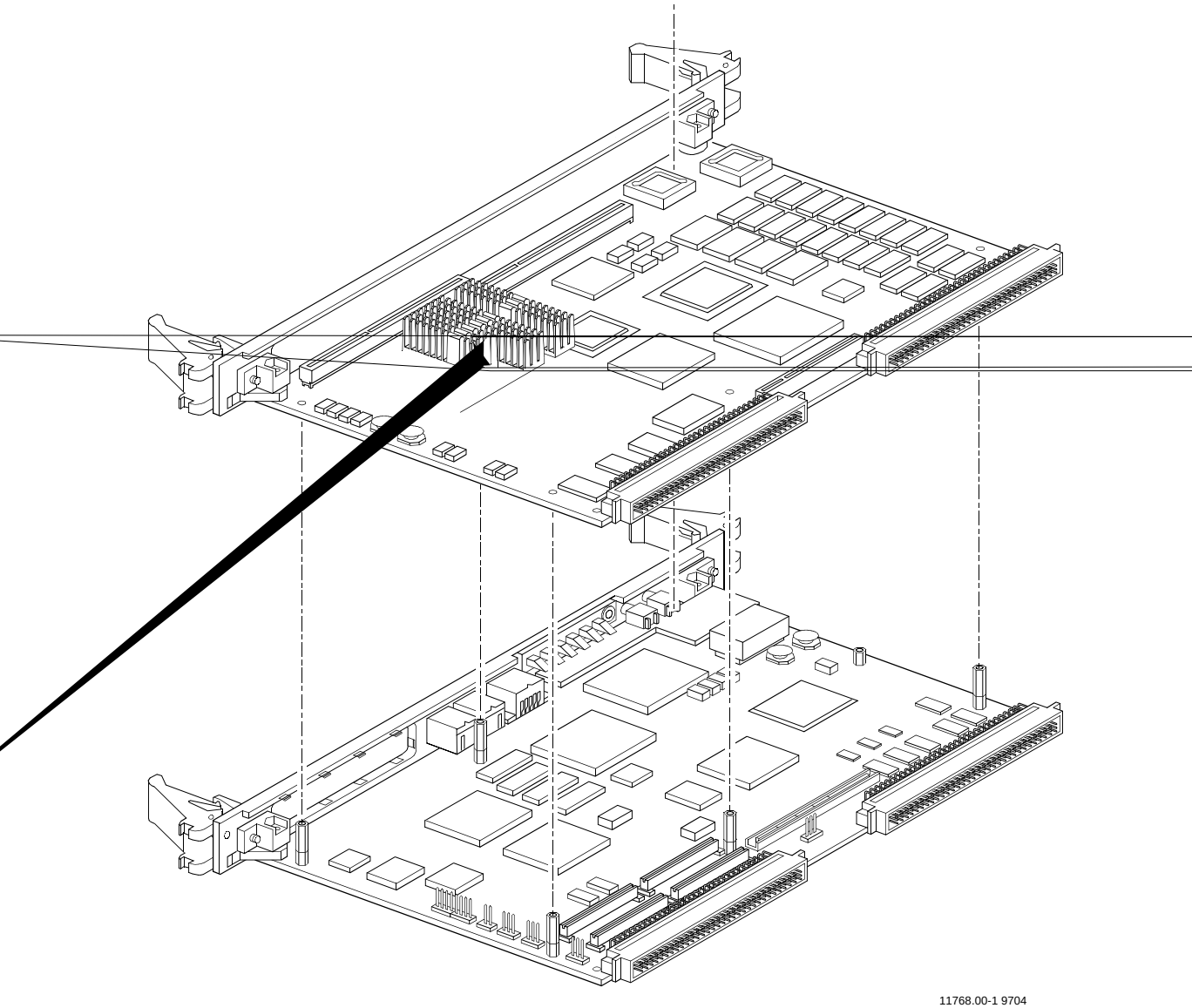


Figure 1-23. Processor/Memory Mezzanine Placement on Base Board

RAM201 Memory Mezzanine

The RAM201 DRAM mezzanine mounts on top of the processor/memory mezzanine. To upgrade or install a 256MB through 1GB RAM201 memory mezzanine, refer to Figure 1-24 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. If the VMEmodule is presently installed in a system, carefully remove the module from its VMEbus card slot.
4. Lay the module flat, with connectors P1 and P2 facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

5. Remove the PMC carrier board (if installed) from the processor/memory mezzanine attached to the base board. To do so, reverse the installation procedure described in the applicable section.

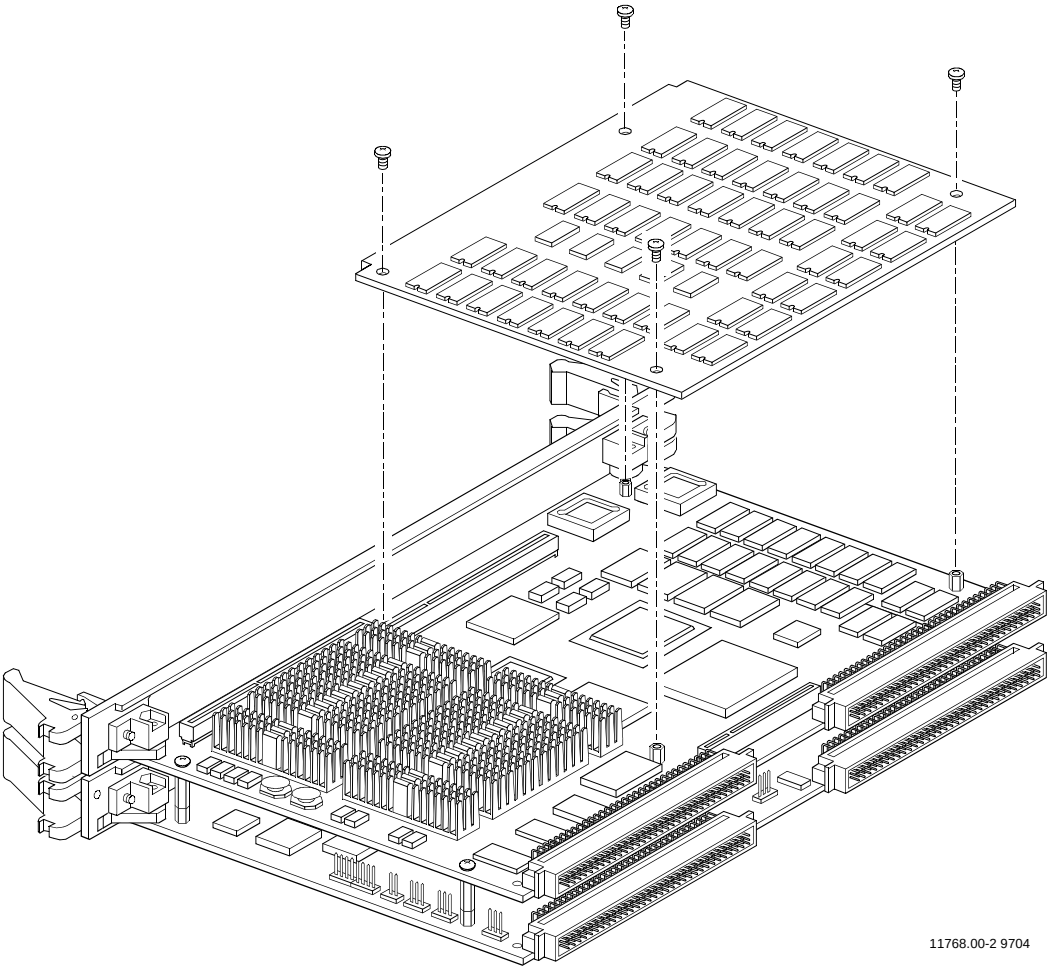


Figure 1-24. RAM201 Memory Mezzanine Placement

6. Remove the four short Phillips screws that secure the RAM201 to the standoffs on the processor/memory mezzanine.
7. Separate the RAM201 from the processor/memory mezzanine.

8. Place the new RAM201 module on top of the processor/ memory mezzanine. Connector J1 on the underside of the RAM201 should connect smoothly with the corresponding connector J6 on the processor/memory mezzanine.
9. Insert the four short Phillips screws through the holes at the corners of the RAM201, into the standoffs on the processor/ memory mezzanine. Tighten the screws.
10. Reinstall the PMC carrier board (if previously installed) on the processor/memory mezzanine. To do so, carry out the installation procedure described in the applicable section.
11. Reinstall the VMEmodule assembly in its proper card slot. Be sure the module is well seated in the backplane connectors. Do not damage or bend connector pins.
12. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

PMC Carrier Board

PCI mezzanine card (PMC) carrier boards mount above the processor/memory mezzanine and (if installed) PMC module on the MVME4600 series base board. To install a PMC carrier board for additional PCI expansion, refer to Figure 1-25 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution Inserting or removing modules with power applied may result in damage to module components.

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the VMEmodule from its VMEbus card slot and lay it flat, with connectors P1 and P2 facing you.

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. If PMC modules are to be installed on the carrier board, install the modules at this point. Be sure the 5V keying pin aligns with the appropriate hole on the PMC board.

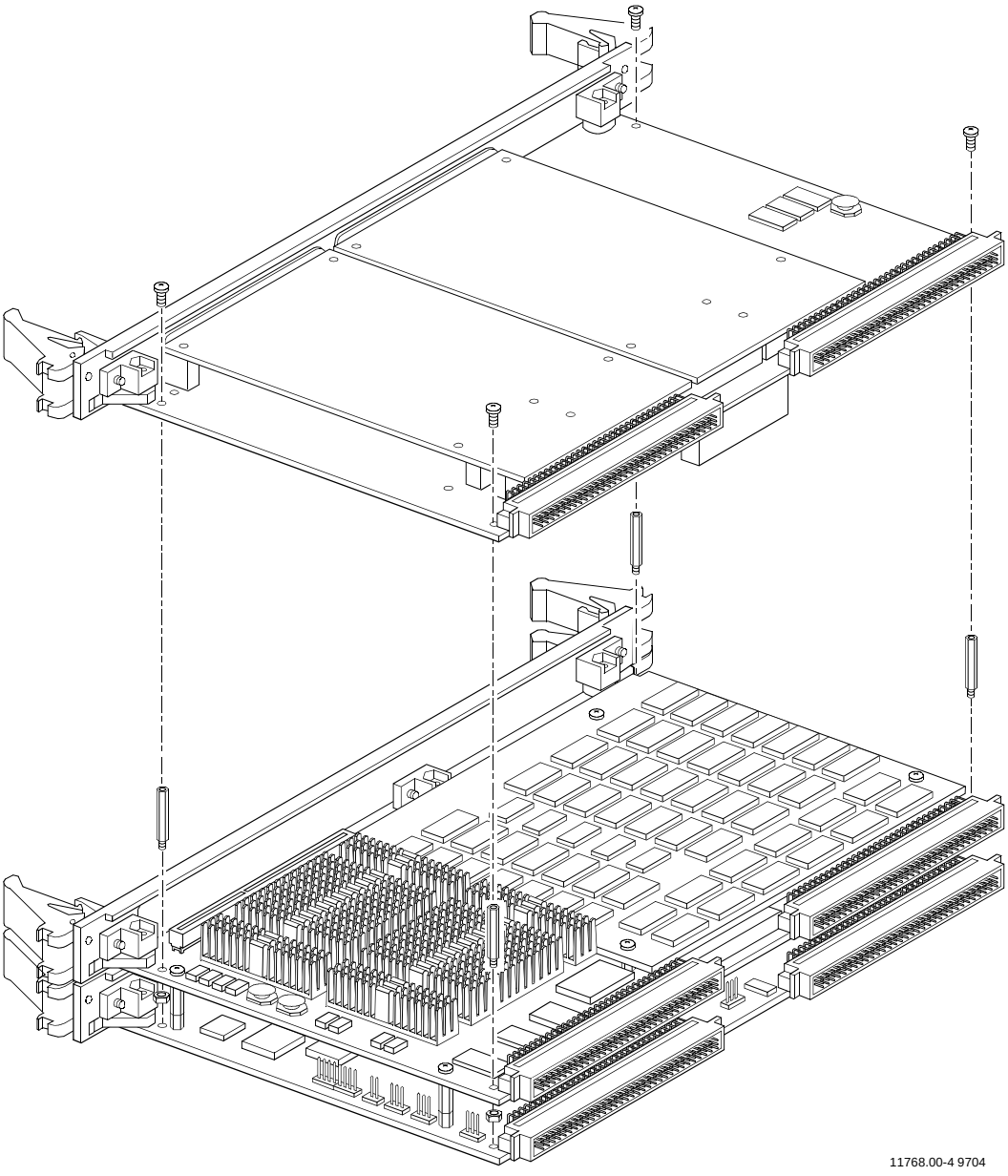


Figure 1-25. PMC Carrier Board Placement

5. Insert the mezzanine-to-carrier-board standoffs through the holes at the corners of the processor/memory mezzanine. Thread the nuts supplied with the kit onto the standoff tips. Tighten the nuts with a box-end wrench or a pair of needlenose pliers.
6. Place the PMC carrier board on top of the processor/ memory mezzanine. The connector on the underside of the carrier board should connect smoothly with the corresponding connector J4 on the processor/memory mezzanine.
7. Insert the four short Phillips screws through the holes at the corners of the carrier board, into the standoffs on the processor/memory mezzanine. Tighten the screws.

Note These screws have two different head diameters. Those with the narrower heads are intended for installation in the corners next to VMEbus connectors P1 and P2.

8. Reinstall the VMEmodule assembly in its proper card slot. Be sure the module is well seated in the backplane connectors. Do not damage or bend connector pins.
9. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

MVME3600 and 4600 Series VMEmodule Install

With mezzanine board(s) installed and headers properly configured, proceed as follows to install the VMEmodule assembly in the VME chassis:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system.

Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the filler panel(s) from the card slot(s) where you are going to install the VMEmodule. (You may need to shift other modules in the chassis to allow space for the VME4600, which has a double-wide front panel.)
   - If you intend to use the VMEmodule as system controller, it must occupy the left-most card slot (slot 1). The system controller must be in slot 1 to correctly initiate the bus-grant daisy-chain and to ensure proper operation of the IACK daisy-chain driver.
   - If you do not intend to use the VMEmodule as system controller, it can occupy any unused double-height card slot.
4. Slide the VMEmodule into the selected card slots. Be sure the module is well seated in the P1 and P2 connectors on the backplane. Do not damage or bend connector pins.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

5. Secure the VMEmodule in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
6. On the chassis backplane, remove the INTERRUPT ACKNOWLEDGE (IACK) and BUS GRANT (BG) jumpers from the header for the card slots occupied by the VMEmodule.

Note Some VME backplanes (for example, those used in Motorola "Modular Chassis" systems) have an auto-jumpering feature for automatic propagation of the IACK and BG signals. Step 6 does not apply to such backplane designs.

7. If necessary, install an MVME712M or MVME761 transition module and cable it to the VMEmodule as described in the following sections of this document.
8. Replace the chassis or system cover(s), cable peripherals to the panel connectors as appropriate, reconnect the system to the AC or DC power source, and turn the equipment power on.

MVME712M Transition Module

This section applies to MVME712M-compatible models of the MVME3600 and 4600 series VMEmodule. With the VMEmodule installed, refer to Figure 1-26 and proceed as follows to install an MVME712M transition module:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution Inserting or removing modules with power applied may result in damage to module components.

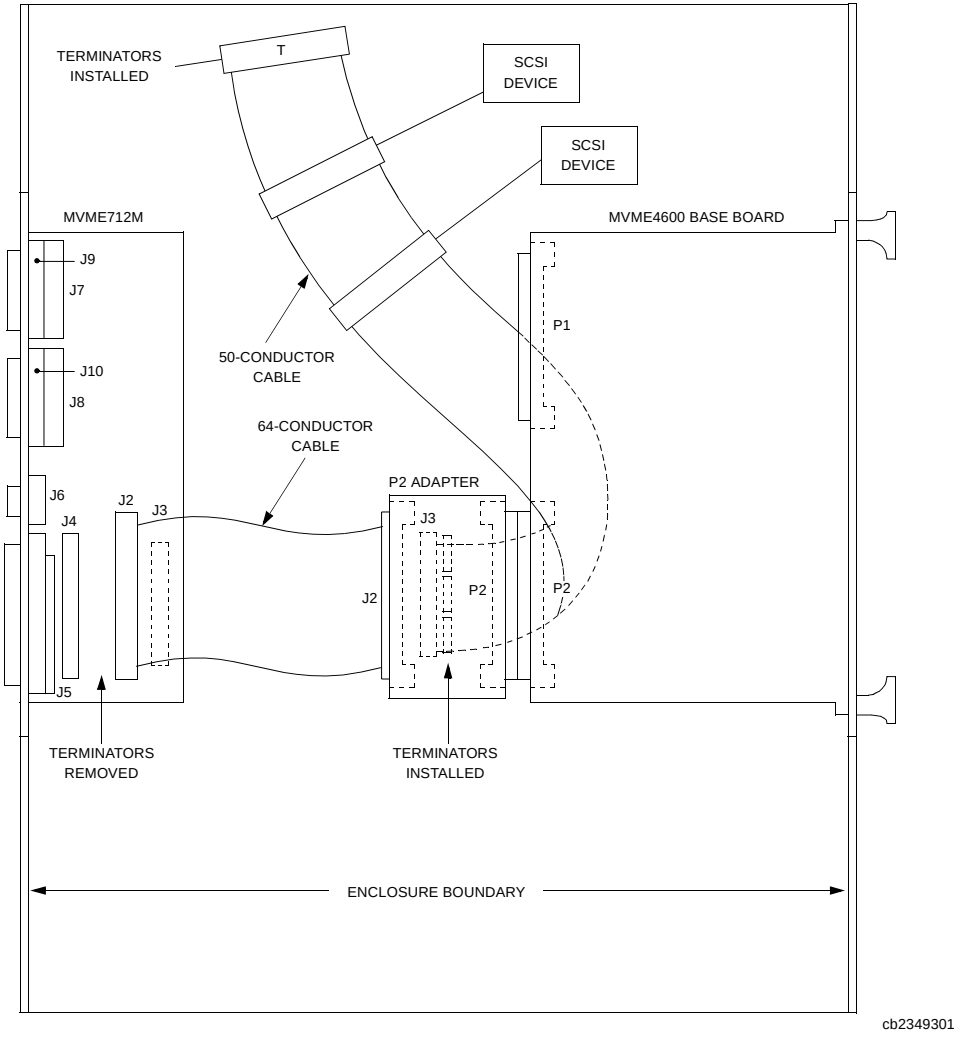


Figure 1-26. MVME712M/MVME4600 Cable Connections

Caution

Connecting MVME761-compatible (for example,VME4604-5*xxx*) models to MVME712M transition modules will damage module components.

Warning Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the filler panel(s) from the appropriate card slot(s) at the front or rear of the chassis. (You may need to shift other modules in the chassis to allow space for the MVME712M, which has a double-wide front panel.)
4. Attach the P2 adapter board to the P2 backplane connector at the slot occupied by the VMEmodule.
5. Route the 64-conductor cable furnished with the MVME712M from J2 on the P2 adapter board to J2 on the transition module. Be sure to orient cable pin 1 with connector pin 1.

Caution Avoid touching areas of integrated circuitry; static discharge can damage these circuits

6. Secure the MVME712M in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
7. Referring to the user's manual for the MVME712M (listed in Appendix D, *Related Documentation*), route the 50-conductor cable to the internal or external SCSI devices as appropriate to your system configuration. Be sure to orient cable pin 1 with connector pin 1.

Note The SCSI cabling can be configured in a number of ways to accommodate various device and system configurations. Figure 1-26 on page 1-57 shows a possible configuration for use with internal SCSI devices. For more detailed information on installing the P2 adapter board and the MVME712M transition module, refer to the user's manual (listed in Appendix D, *Related Documentation*).

8. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

Note Not all peripheral cables are provided with the MVME712M; you may need to fabricate or purchase certain cables. (To minimize radiation, Motorola recommends shielded cable for peripheral connections where possible.)

MVME761 Transition Module

This section applies to MVME761-compatible models of the MVME3600 or 4600 series VMEmodule. With the appropriate VMEmodule installed, refer to Figure 1-14 on page 1-32 and proceed as follows to install an MVME761 transition module:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution Inserting or removing modules with power applied may result in damage to module components.

Caution Connecting MVME712M-compatible (for example, MVME4604-6*xxx*) models of the VMEmodule to MVME761 transition modules will damage module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the filler panel(s) from the appropriate card slot(s) at the front or rear of the chassis. (You may need to shift other modules in the chassis to allow space for the cabling to the MVME761.)
4. Attach the P2 adapter board to the P2 backplane connector at the slot occupied by the VMEmodule.

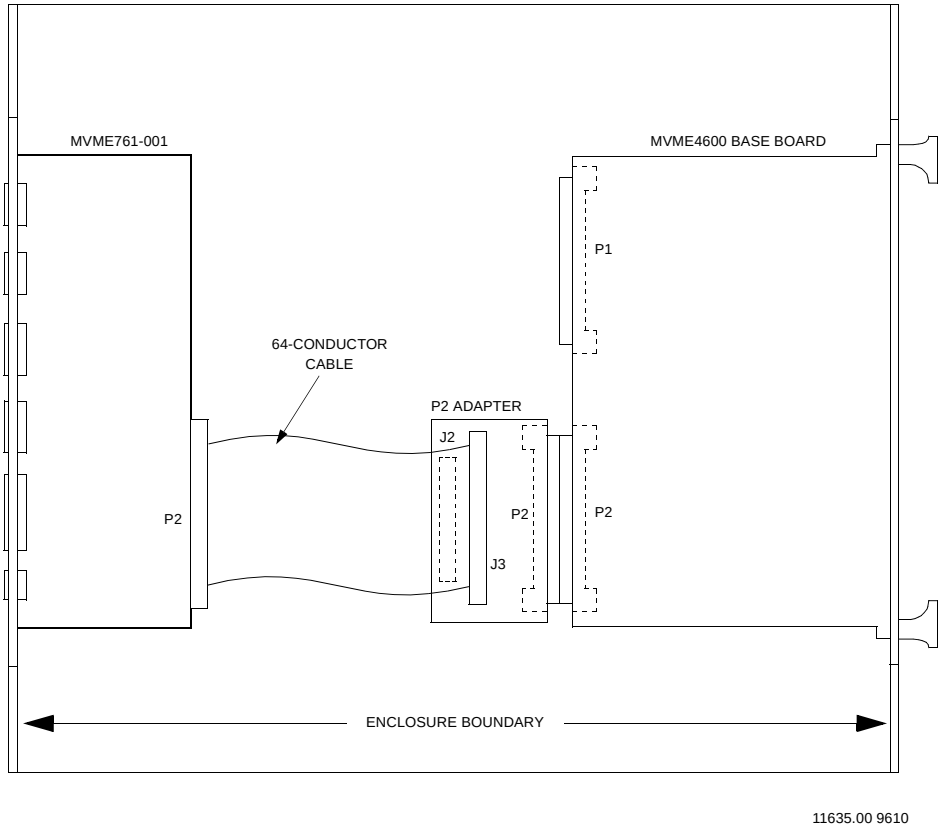


Figure 1-27. MVME761/VMEmodule Cable Connections

5. Route the 64-conductor cable furnished with the MVME761 from J3 on the P2 adapter board to P2 on the transition module. Be sure to orient cable pin 1 with connector pin 1.

Caution Avoid touching areas of integrated circuitry; static discharge can damage these circuits

6. Secure the MVME761 in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.

Note The cabling can be configured in a number of ways to accommodate various device and system configurations. Figure 1-27 on page 1-60 shows one possible configuration. For more detailed information on installing the P2 adapter board and the MVME761 transition module, refer to the user's manual (listed in Appendix D, *Related Documentation*).

7. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

Note Not all peripheral cables are provided with the MVME761; you may need to fabricate or purchase certain cables. (To minimize radiation, Motorola recommends shielded cable for peripheral connections where possible.)

System Considerations

The MVME3600 and 4600 series VMEmodule draws power from VMEbus backplane connectors P1 and P2. P2 is also used for the upper 16 bits of data in 32-bit transfers, and for the upper eight address lines in extended addressing mode. The VMEmodule may not function properly without its main board connected to VMEbus backplane connectors P1 and P2.

Whether the MVME3600 or 4600 operates as a VMEbus master or as a VMEbus slave, it is configured for 32 bits of address and 32 bits of data (A32/D32). However, it handles A16 or A24 devices in the address ranges indicated in Chapter 2, *Operating Instructions*. D8 and/or D16 devices in the system must be handled by the PowerPC processor software. Refer to the memory maps in Chapter 2, *Operating Instructions*.

The MVME3600 and 4600 series VMEmodule contains shared onboard DRAM (and, optionally, secondary cache memory) whose base address is software-selectable. Both the onboard processor and offboard VMEbus devices see this local DRAM at base physical address $00000000, as programmed by the firmware. This may be changed via software to any other base address. Refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* for more information.

If the VMEmodule tries to access offboard resources in a nonexistent location and is not system controller, and if the system does not have a global bus timeout, the VMEmodule waits forever for the VMEbus cycle to complete. This will cause the system to lock up. There is only one situation in which the system might lack this global bus timeout: when the VMEmodule is not the system controller and there is no global bus timeout elsewhere in the system.

Multiple VMEmodules may be installed in a single VME chassis. In general, hardware multiprocessor features are supported.

Other MPUs on the VMEbus can interrupt, disable, communicate with, and determine the operational status of the processor(s). One register of the GCSR (global control/status register) set includes four bits that function as

location monitors to allow one MVME series processor to broadcast a signal to any other MVME series processors. All eight registers are accessible from any local processor as well as from the VMEbus.

The VMEmodule draws +5V DC, +12V DC, and –12V DC power from the VMEbus backplane through connectors P1 and P2. The 3.3V DC and 2.5V DC power is derived on-board from the +5V DC.

VMEmodule

The VMEmodule furnishes +12V DC and (in MVME761 I/O mode) –12V DC power to the transition module through polyswitches (resettable fuses) F3 and F1 respectively. These voltage sources power the serial port drivers and any LAN transceivers connected to the transition module. Fused +5V DC power is supplied to the base board's keyboard and mouse connectors through polyswitch F2 and to the 14-pin combined LED-mezzanine/remote-reset connector, J1. The FUS LED (DS5) on the MVME4600 front panel illuminates when all three voltages are available.

In MVME712M I/O mode, the VMEmodule supplies SCSI terminator power through a 1A fuse (F1) located on the P2 adapter board. If the fuse is blown, the SCSI device(s) may function erratically or not at all. With the P2 adapter board cabled to a transition module and with an SCSI bus connected to the transition module, the green SCSI LED on the module illuminates when SCSI terminator power is available. If the SCSI LED on the transition module flickers during SCSI bus operation, check fuse F1 on the P2 adapter board.

Note Because any device on the SCSI bus can provide the TERMPWR signal, and because the VMEmodule FUS LED monitors the status of several voltages, the LED does not directly indicate the condition of any single fuse. If the FUS LED flickers or goes out, check all the fuses (polyswitches).

In MVME761 I/O mode, the VMEmodule supplies SCSI terminator power through a polyswitch (resettable fuse) located on the P2 adapter board.

If the optional secondary SCSI interface is present on the processor/memory mezzanine, it may require termination at the VMEmodule end of the SCSI chain. Should that be the case, the P2 adapter for the processor/memory mezzanine supplies the termination point. Use adapter model MVME3600P2-*xx*1, or 4600P2-*xx*1 for single-ended SCSI configurations. Use adapter model MVME3600P2-*xx*2, or 4600P2-*xx*2 for differential SCSI configurations.

The VMEmodule supplies a SPEAKER_OUT signal to the 14-pin combined LED-mezzanine/remote-reset connector on the base board, J1. When J1 is used as a remote reset connector with the LED mezzanine removed, the SPEAKER_OUT signal can be cabled to an external speaker. For the pin assignments of J1, refer to Table 4-1 on page 4-3.

The standard serial console port on the VMEmodule (COM1, accessible through the transition module) serves as the firmware console port. The firmware console should be set up as follows:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

9600 baud is the power-up default for serial ports on MVME series boards. After power-up you can reconfigure the baud rate if you wish, using the PPCBug **PF** (Port Format) command via the command line interface. Whatever the baud rate, some type of hardware handshaking — either XON/OFF or via the RTS/CTS line — is desirable if the system supports it.

Operating Instructions 2

Introduction

This chapter supplies information on use of the MVME3600 and 4600 series family of VME Processor Modules in a system configuration. Here you will find the power-up procedure and descriptions of the switches and LEDs, memory maps, and software initialization.

Applying Power

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. Applying power (as well as resetting the system) triggers the MPU, hardware, and firmware initialization process. The firmware initializes the devices on the VMEmodule in preparation for booting the operating system.

The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system.

The following flowchart shows the basic initialization process that takes place during PowerPC system startup.

For further information on the firmware, refer to Chapter 5, *PPCBug Firmware*; to Appendix C, *Troubleshooting CPU Boards*; or to the *PPCBug Firmware Package User's Manual*, as referenced in Appendix D, *Related Documentation*.

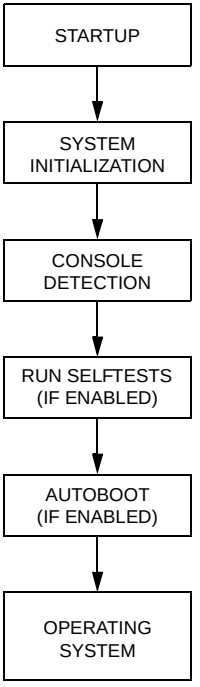


Figure 2-1. PowerPC Firmware System Startup

The MVME3600 and 4600 series front panel has ABORT and RESET switches and six LED (light-emitting diode) status indicators (CHS, BFL, CPU, PCI, FUS, SYS). The switches and LEDs are mounted on an LED mezzanine board that plugs into the base board.

ABORT Switch (S1)

When activated by software, the ABORT switch can generate an interrupt signal from the base board to the processor at a user-programmable level. The interrupt is normally used to abort program execution and return control to the debugger firmware located in the VMEmodule PROM and Flash memory. The interrupt signal reaches the processor module via ISA bus interrupt line IRQ8*. The signal is also available at pin PB7 of the Z8536 CIO device, which handles various status signals, serial I/O lines, and counters.

The interrupter connected to the ABORT switch is an edge-sensitive circuit, filtered to remove switch bounce.

RESET Switch (S2)

The RESET switch resets all onboard devices; it also drives a SYSRESET* signal if the VMEmodule is the system controller.

The Universe ASIC includes both a global and a local reset driver. When the Universe operates as the VMEbus system controller, the reset driver provides a global system reset by asserting the VMEbus signal SYSRESET*. A SYSRESET* signal may be generated by the RESET switch, a power-up reset, a watchdog timeout, or by a control bit in the Miscellaneous Control Register (MISC_CTL) in the Universe ASIC. SYSRESET* remains asserted for at least 200 ms, as required by the VMEbus specification.

Similarly, the Universe ASIC supplies an input signal and a control bit to initiate a local reset operation. By setting a control bit, software can maintain a board in a reset state, disabling a faulty board from participating in normal system operation. The local reset driver is enabled even when the Universe ASIC is not system controller. Local resets may be generated by the RESET switch, a power-up reset, a watchdog timeout, a VMEbus SYSRESET*, or a control bit in the MISC_CTL register.

2

Front Panel Indicators (DS1 – DS6)

There are six LEDs on the MVME3600 and 4600 front panel: CHS, BFL, CPU, PCI, FUS, and SYS.

- CHS (DS1, yellow). Checkstop; driven by the MPC status lines on the VMEmodule. Lights when a halt condition from the processor is detected.
- BFL (DS2, yellow). Board Failure; lights when the BRDFAIL* signal line is active.
- CPU (DS3, green). CPU activity; lights when the DBB* (Data Bus Busy) signal line on the processor bus is active.
- PCI (DS4, green). PCI activity; lights when the IRDY* (Initiator Ready) signal line on the PCI bus is active. This indicates that the PCI mezzanine (if installed) is active.
- FUS (DS5, green). Fuse OK; lights when +5V DC, +12V DC, and –12V DC power is available from the base board to the transition module and remote devices.

Note Because the FUS LED monitors the status of several voltages on the VMEmodule, it does not directly indicate the condition of any single fuse. If the LED flickers or goes out, check all the fuses (polyswitches).

- SYS (DS6, green). System Controller; lights when the Universe ASIC in the VMEmodule is the VMEbus system controller.

Memory Maps

There are three points of view for memory maps:

- The mapping of all resources as viewed by the processor (MPU bus memory map)
- The mapping of onboard resources as viewed by PCI local bus masters (PCI bus memory map)
- The mapping of onboard resources as viewed by VMEbus masters (VMEbus memory map)

The following sections give a general description of the VMEmodule memory organization from the above three points of view. Detailed memory maps can be found in the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

Processor Memory Map

The processor memory map configuration is under the control of the Raven bridge controller ASIC and the Falcon memory controller chip set. The Raven and Falcon devices adjust system mapping to suit a given application via programmable map decoder registers. At system power-up or reset, a default processor memory map takes over.

Default Processor Memory Map

The default processor memory map that is valid at power-up or reset remains in effect until reprogrammed for specific applications. Table 2-1 defines the entire default map ($00000000 to $FFFFFFFF). Table 2-2 on page 2-10 further defines the map for the local I/O devices (accessible through the PCI/ISA I/O Space).

Table 2-1. Processor Default View of the Memory Map

Processor Address		Size	Definition	Notes
Start	End			
00000000	7FFFFFFF	2GB	Not Mapped	
80000000	8001FFFF	128KB	PCI/ISA I/O Space	1
80020000	FEF7FFFF	2GB-16MB-640KB	Not Mapped	
FEF80000	FEF8FFFF	64KB	Falcon Registers	
FEF90000	FEFEFFFF	384KB	Not Mapped	
FEFF0000	FEFFFFFF	64KB	Raven Registers	
FF000000	FFEFFFFF	15MB	Not Mapped	
FFF00000	FFFFFFFF	1MB	ROM/Flash Bank A or Bank B	2

Notes

1. Default map for PCI/ISA I/O space. Allows software to determine whether the system is MPC105-based or Falcon/Raven-based by examining either the PHB Device ID or the CPU Type register.
2. The first 1MB of ROM/Flash bank A (soldered 4MB or 8MB ROM/Flash) appears in this range after a reset if the **rom_b_rv** control bit in the Falcon's ROM B Base/Size register is cleared. If the **rom_b_rv** control bit is set, this address range maps to ROM/Flash bank B (socketed 1MB ROM/Flash).

For detailed processor memory maps, including suggested CHRP- and PREP-compatible memory maps, refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

PCI Local Bus Memory Map

The PCI memory map is controlled by the Raven MPU/PCI bus bridge controller ASIC and by the Universe PCI/VME bus bridge ASIC. The Raven and Universe devices adjust system mapping to suit a given application via programmable map decoder registers.

No default PCI memory map exists. Resetting the system turns the PCI map decoders off, and they must be reprogrammed in software for the intended application.

For detailed PCI memory maps, including suggested CHRP- and PREP-compatible memory maps, refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

VMEbus Memory Map

The VMEbus is programmable. Like other parts of the VMEmodule memory map, the mapping of local resources as viewed by VMEbus masters varies among applications.

The Universe PCI/VME bus bridge ASIC includes a user-programmable map decoder for the VMEbus-to-local-bus interface. The address translation capabilities of the Universe enable the processor to access any range of addresses on the VMEbus.

Recommendations for VMEbus mapping, including suggested CHRP- and PREP-compatible memory maps, can be found in the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*). The following figure shows the overall mapping approach from the standpoint of a VMEbus master.

2

Programming Considerations

Good programming practice dictates that only one MPU at a time have control of the control registers in the VMEmodule. Of particular note are:

- Registers that modify the address map
- Registers that require two cycles to access
- VMEbus interrupt request registers

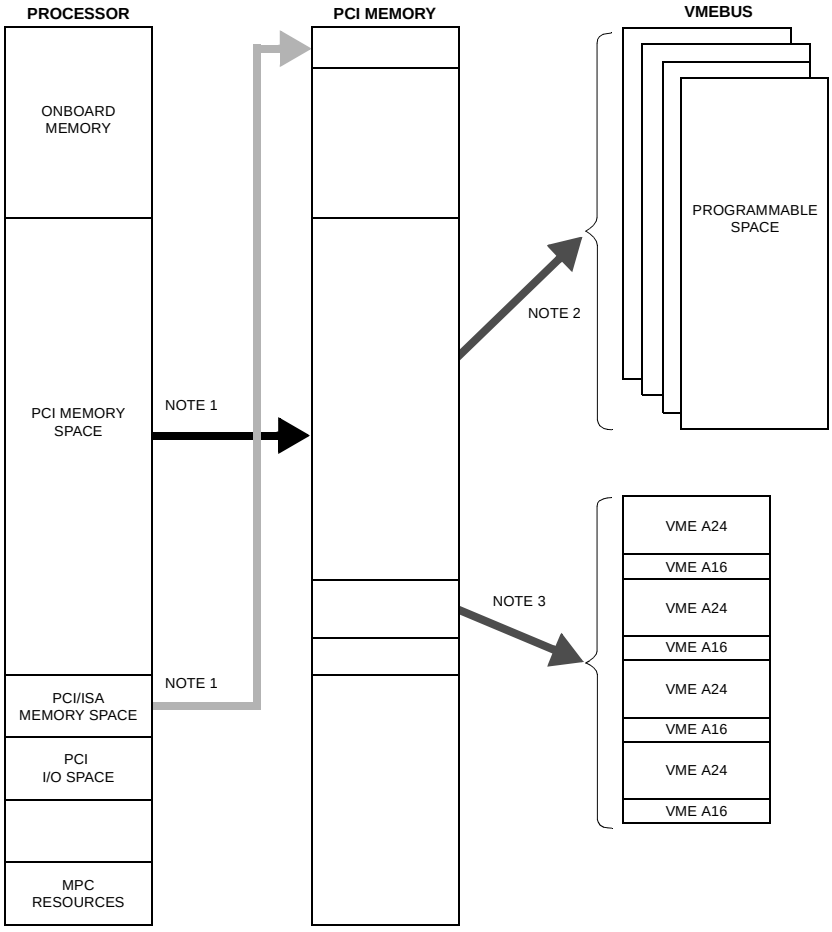


Figure 2-2. VMEbus Master Mapping

PCI Arbitration

There are seven potential PCI bus masters on the MVME3600 and 4600 series VMEmodule:

- Raven ASIC (MPU/PCI bus bridge controller)
- Winbond W83C553 PIB (PCI/ISA bus bridge controller)
- DEC21140 Ethernet controller
- SYM53C825A SCSI controller
- Universe ASIC (PCI/VME bus bridge controller)
- PMC Slot 1 (PCI mezzanine card)
- PMC Slot 2 (PCI expansion)

The Winbond W83C553 PIB device supplies the PCI arbitration support for these seven types of devices. The PIB supports flexible arbitration modes of fixed priority, rotating priority, and mixed priority, as appropriate in a given application. For details on PCI arbitration, refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

The arbitration assignments for the VMEmodule are shown in the following table.

Table 2-2. PCI Arbitration Assignments

PCI Bus Request	PCI Master(s)
PIB (Internal)	PIB
CPU	Secondary Ethernet Secondary SCSI Raven ASIC
Request 0	PMC Slot 2 (PCIX)
Request 1	PMC Slot 1
Request 2	Ethernet
Request 3	SCSI
Request 4	VMEbus (Universe ASIC)

Interrupt Handling

The Raven ASIC, which controls PHB (PCI Host Bridge) MPU/local bus interface functions on the VMEmodule, performs interrupt handling as well. Sources of interrupts may be any of the following:

- The Raven ASIC itself (timer interrupts or transfer error interrupts)
- The processor (processor self-interrupts)
- The Falcon chip set (memory error interrupts)
- The PCI bus (interrupts from PCI devices)
- The ISA bus (interrupts from ISA devices)

The following figure illustrates interrupt architecture on the MVME3600/4600. For details on interrupt handling, refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

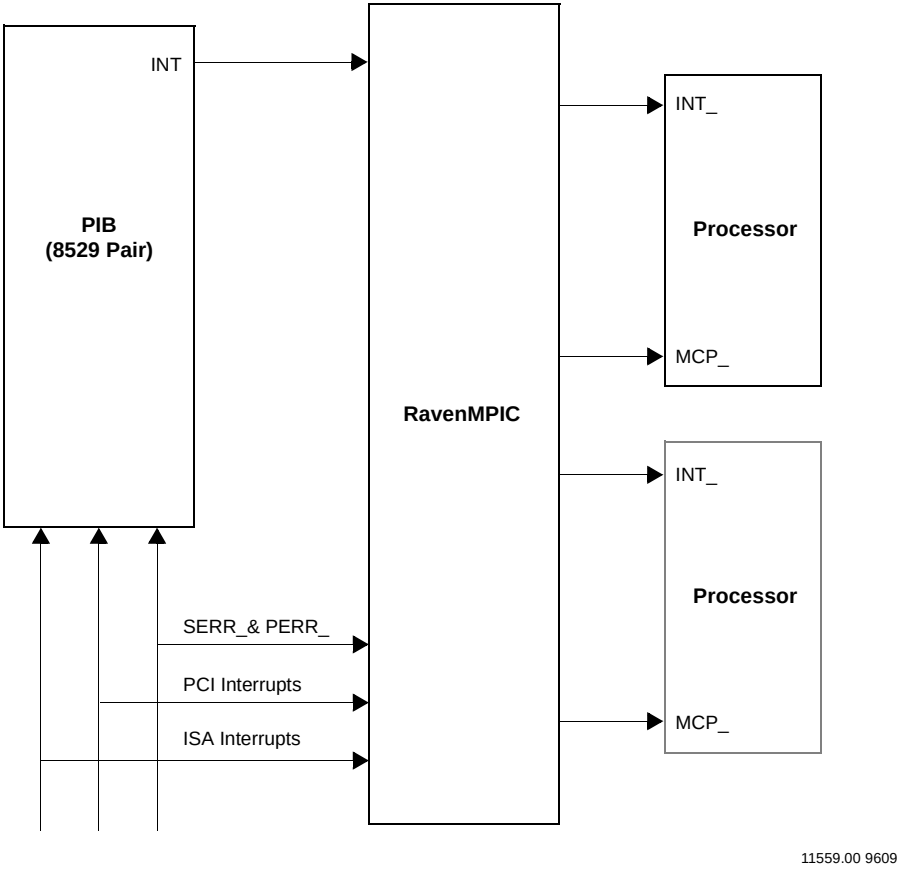


Figure 2-3. MVME3600/4600 Series VMEmodule Interrupt Architecture

DMA Channels

The PIB supports seven DMA channels. Channels 0 through 3 support 8-bit DMA devices. Channels 5 through 7 are dedicated to 16-bit DMA devices. The channels are allocated as follows:

Table 2-3. IBC DMA Channel Assignments

IBC Priority	IBC Label	Controller	DMA Assignment
1	Channel 0	DMA1	Serial Port 3 Receiver (Z85230 Port A Rx)
2	Channel 1		Serial Port 3 Transmitter (Z85230 Port A Tx)
3	Channel 2		Floppy Drive Controller
4	Channel 3		Parallel Port
5	Channel 4	DMA2	Not available — Cascaded from DMA1
6	Channel 5		Serial Port 4 Receiver (Z85230 Port B Rx)
7	Channel 6		Serial Port 4 Transmitter (Z85230 Port B Tx)
8	Channel 7		Not Used

Sources of Reset

The MVME3600 and 4600 series SBC has eight potential sources of reset:

1. Power-on reset
2. RESET switch (resets the VMEbus when the VMEmodule is system controller)
3. Watchdog timer Reset function controlled by the SGS-Thomson M48T59/M48T559 timekeeper device (resets the VMEbus when the VMEmodule is system controller)
4. ALT_RST* function controlled by the Port 92 register in the PIB (resets the VMEbus when the VMEmodule is the system controller)

5. PCI/ISA I/O Reset function controlled by the Clock Divisor register in the PIB
6. The VMEbus SYSRESET* signal
7. VMEbus Reset sources from the Universe ASIC (PCI/VME bus bridge controller): the System Software reset and Local Software reset

The following table shows which devices are affected by the various types of resets. For details on using resets, refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

Table 2-4. Classes of Reset and Effectiveness

Device Affected / Reset Source	Processor	Raven ASIC	Falcon Chip Set	PCI Devices	ISA Devices	VMEbus (as system controller
Power-On reset	√	√	√	√	√	√
Reset switch	√	√	√	√	√	√
Watchdog reset	√	√	√	√	√	√
VME SYSRESET*signal	√	√	√	√	√	√
VME System SW reset	√	√	√	√	√	√
VME Local SW reset	√	√	√	√	√	
Hot reset (Port 92)	√	√	√	√	√	
PCI/ISA reset				√	√	

Endian Issues

The MVME3600 and 4600 series SBC supports both little-endian (for example, Windows NT) and big-endian (for example, AIX) software. The PowerPC processor and the VMEbus are inherently big-endian, while the PCI bus is inherently little-endian. The following sections summarize how the VMEmodule handles software and hardware differences in big- and

little-endian operations. For further details on endian considerations, refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

Processor/Memory Domain

The MPC604 processor can operate in both big-endian and little-endian mode. However, it always treats the external processor/memory bus as big-endian by performing *address rearrangement and reordering* when running in little-endian mode. The MPC registers in the Raven MPU/PCI bus bridge controller ASIC and the Falcon memory controller chip set, as well as DRAM, ROM/Flash, and system registers, always appear as big-endian.

Role of the Raven ASIC

Because the PCI bus is little-endian, the Raven performs byte swapping in both directions (from PCI to memory and from the processor to PCI) to maintain address invariance while programmed to operate in big-endian mode with the processor and the memory subsystem.

In little-endian mode, the Raven *reverse-rearranges* the address for PCI-bound accesses and *rearranges* the address for memory-bound accesses (from PCI). In this case, no byte swapping is done.

PCI Domain

The PCI bus is inherently little-endian. All devices connected directly to the PCI bus operate in little-endian mode, regardless of the mode of operation in the processor's domain.

PCI and SCSI

SCSI is byte-stream-oriented; the byte having the lowest address in memory is the first one to be transferred regardless of the endian mode. Since the Raven ASIC maintains address invariance in both little-endian and big-endian modes, no endian issues should arise for SCSI data. Big-endian software must still take the byte-swapping effect into account when accessing the registers of the PCI/SCSI device, however.

PCI and Ethernet

Ethernet is also byte-stream-oriented; the byte having the lowest address in memory is the first one to be transferred regardless of the endian mode. Since the Raven maintains address invariance in both little-endian and big-endian mode, no endian issues should arise for Ethernet data. Big-endian software must still take the byte-swapping effect into account when accessing the registers of the PCI/Ethernet device, however.

Role of the Universe ASIC

Because the PCI bus is little-endian while the VMEbus is big-endian, the Universe PCI/VME bus bridge ASIC performs byte swapping in both directions (from PCI to VMEbus and from VMEbus to PCI) to maintain address invariance, regardless of the mode of operation in the processor's domain.

VMEbus Domain

The VMEbus is inherently big-endian. All devices connected directly to the VMEbus must operate in big-endian mode, regardless of the mode of operation in the processor's domain.

In big-endian mode, byte-swapping is performed first by the Universe ASIC and then by the Raven. The result is transparent to big-endian software (a desirable effect).

In little-endian mode, however, software must take the byte-swapping effect of the Universe ASIC and the address *reverse-rearranging* effect of the Raven into account.

For further details on endian considerations, refer to the *MVME3600/4600 Series VME Processor Module Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*).

Functional Description 3

Introduction

This chapter describes the MVME3600/4600 series VME Processor Modules on a block diagram level. The *General Description* provides an overview of the MVME3600/4600 series VMEmodule, followed by a detailed description of several blocks of circuitry. Figure 3-1 on page 3-5 shows a block diagram of the overall board architecture.

Detailed descriptions of other MVME3600 and 4600 blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *MVME3600/4600 Programmer's Reference Guide* (listed in Appendix D, *Related Documentation*). Refer to it for a functional description of the MVME3600 and 4600 series VMEmodules in greater depth.

Features

The following table summarizes the characteristics of the MVME3600 and 4600 series VMEmodule.

Table 3-1. Features of the MVME3600 and 4600 Series VMEmodules

Feature	Description
Microprocessor	PowerPC 604 processor
ECC DRAM	64MB–1GB (divided between processor/memory mezzanine and RAM201 memory module)
L2 cache memory	512KB on processor/memory mezzanine
Flash Memory	Two 32-pin PLCC sockets (1MB 16-bit Flash) and two banks (4MB or 8MB 64-bit Flash) on processor/memory mezzanine
Real-time clock	8KB NVRAM with RTC and battery backup (SGS-Thomson M48T59/M48T559) on base board
Switches	RESET and ABORT
Status LEDs	Six: CHS, BFL, CPU, PCI, FUS, and SYS

Table 3-1. Features of the MVME3600 and 4600 Series VMEmodules

Feature	Description
Tick timers	Four programmable 16-bit timers (one in S82378ZB ISA bridge; three in Z8536 CIO device) Four programmable 32-bit timers in Raven PCI-MPU bridge
Watchdog timer	Provided in SGS-Thomson M48T59
Interrupts	Software interrupt handling via Raven (PCI-MPU bridge) and Winbond (PCI-ISA bridge) controllers
VME I/O	VMEbus P2 connector
Serial I/O	MVME712M-compatible models: three async ports, one sync/async port via P2 and transition module
	MVME761-compatible models: two async ports, two sync/async ports via P2 and transition module
Parallel I/O	MVME712M-compatible models: Centronics parallel port (PC87308 SIO) via P2 and transition module
	MVME761-compatible models: IEEE 1284 bidirectional parallel port (PC87308 SIO) via P2 and transition module
SCSI I/O	MVME712M-compatible models: 8-bit/16-bit single-ended fast SCSI-2 interface (SYM53C825A) via base board P2 and transition module
	MVME761-compatible models: 8-bit/16-bit single-ended fast SCSI-2 interface (SYM53C825A) via base board P2
Secondary SCSI	All models: optional secondary 8- or 16-bit ultra SCSI via processor mezzanine P2
Ethernet I/O	MVME712M-compatible models: AUI connections via base board P2 and transition module
	MVME761-compatible models: 10BaseT/100BaseTX connections via base board P2 and transition module
Secondary Ethernet	All models: optional secondary 10/100Mb/s Ethernet via processor mezzanine P2
PCI interface	One IEEE P1386.1 PCI Mezzanine Card (PMC) slot; one 114-pin Mictor connector for additional PMC carrier board
Keyboard/mouse interface	Support for keyboard and mouse input (PC87308 SIO) via front panel connectors
Graphics port	Super VGA high-resolution color graphics (Cirrus Logic CL-GD5446 graphics accelerator) via front panel connector

Table 3-1. Features of the MVME3600 and 4600 Series VMEmodules

Feature	Description
Floppy disk controller	Support for floppy disk drive (PC87308 SIO) via front panel connector
VMEbus interface	VMEbus system controller functions
	VMEbus-to-local-bus interface (A24/A32, D8/D16/D32/block transfer [D8/D16/D32/D64])
	Local-bus-to-VMEbus interface (A16/A24/A32, D8/D16/D32)
	VMEbus interrupter
	VMEbus interrupt handler
	Global control/status register for interprocessor communications
	DMA for fast local memory/VMEbus transfers (A16/A24/A32, D16/D32/D64)

General Description

The MVME3600 and 4600 are VME processor modules equipped with one or two Motorola PowerPC 604 or IBM PowerPC 604 (Mach5) microprocessors. A 512KB L2 cache (level 2 secondary cache memory) is available on all versions.

As shown in the *Features* section, the MVME3600 and 4600 series VMEmodules offer many standard features desirable in a computer system—such as synchronous and asynchronous serial ports, parallel port, boot ROM and DRAM, SCSI, Ethernet, support for an external disk drive, and keyboard, mouse, and graphics support—in a two-slot VME package. Its flexible mezzanine architecture allows relatively easy upgrades in memory and functionality.

A key feature of the MVME3600 and 4600 series families is the PCI (Peripheral Component Interconnect) bus. In addition to the on-board local bus peripherals, the PCI bus supports an industry-standard mezzanine interface, IEEE P1386.1 PMC (PCI Mezzanine Card). PMC modules offer a variety of possibilities for I/O expansion through FDDI (Fiber Distributed Data Interface), ATM (Asynchronous Transfer Mode),

graphics, Ethernet, or SCSI ports. The base board supports PMC front panel I/O. There is also provision for additional expansion via a PMC carrier board.

Block Diagram

Figure 3-1 diagrams the overall architecture of the MVME4600 series VMEmodule. The MVME3600 series module is identical to the 4600 with the exception that it has a single, rather than a dual, processor.

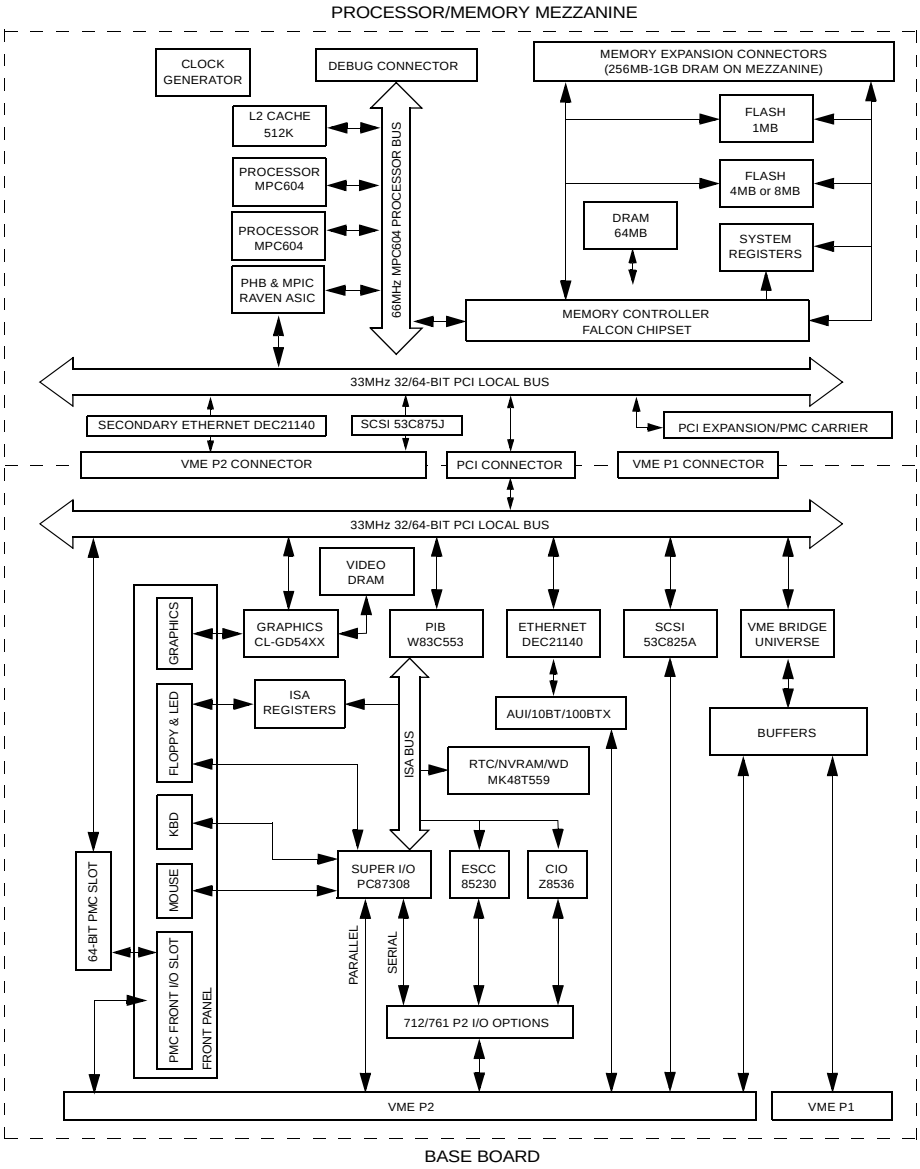


Figure 3-1. MVME4600 Series System Block Diagram

Graphics Interface

The MVME3600 and 4600 series VMEmodules have a Super VGA (Video Graphics Array) color graphics interface implemented with a Cirrus Logic CL-GD5446 graphics accelerator. The CL-GD5446 supports pixel clock rates of up to 135 MHz. Its internal palette DAC is configurable for industry-standard 16- or 256-color VGA modes. The DAC is also extensible to high- and true-color modes of 32 thousand or 16.7 million colors.

Depending on the color selection and bits-per-pixel mode, the CL-GD5446 device supports resolutions of up to 1280 x 1024. 2MB of video buffer memory (in the form of four 256K x 16, 40-pin SOJ, 60ns DRAM chips) are available to the CL-GD5446.

The VGA port routes the graphics data to an industry-standard 3-row DB-15 connector on the front panel of the base board (as illustrated in Figure 1-3 on page 1-9).

Refer to Chapter 6, *CNFG and ENV Commands* for the pin assignments of the front panel VGA connector. Refer to Cirrus Logic's CL-GD5446 *Technical Reference Manual* for detailed programming information.

SCSI Interface

The MVME3600 and 4600 series VMEmodules support mass storage subsystems through the industry-standard SCSI bus. These subsystems may include hard and floppy disk drives, streaming tape drives, and other mass storage devices. The SCSI interface is implemented using the Symbios 53C825A SCSI I/O controller at a clock speed of 40 MHz. The SCSI I/O controller connects directly to the PCI local bus.

MVME712M-compatible versions of the MVME3600 and 4600 series VMEmodules route the SCSI lines through the P2 connector to the MVME712M transition module (as illustrated in Figure 1-26 on page 1-57). The SCSI control lines have filter networks to minimize the effects of VMEbus signal noise at P2.

In the MVME761 case, the SCSI lines are routed through the P2 connector up to connector J2 on the P2 adapter board (as illustrated in Figure 1-27 on page 1-60). The MVME761 itself has no SCSI support, but you can run SCSI devices by installing an optional front panel extension, MVME761EXT, next to the MVME761. The panel extension supplies both 8- and 16-bit SCSI.

The SCSI bus is 16 bits wide in systems that support the VME64 extension (that is, those equipped with 5-row, 160-pin VME backplane connectors). The SCSI bus is 8 bits wide in VME systems that do not support the extension. Refer to the MVME712M *User's Manual* for the pin assignments of the SCSI connectors used on the transition module. Refer to the Symbios 53C825A data manual for detailed programming information.

SCSI Termination

The individual configuring the system must ensure that the SCSI bus is properly terminated at both ends.

In MVME712M I/O mode, the base board uses the sockets provided for SCSI bus terminators on the three-row P2 adapter board supplied with the MVME712M. If the SCSI bus ends at the adapter board, termination resistors must be installed there. +5V DC power to the SCSI bus TERMPWR signal and termination resistors is supplied through a fuse located on the adapter board.

If a five-row P2 adapter is furnished for the MVME712M, it is identical to the five-row adapter (part number 01-W3199F01A) used with the MVME761.

In MVME761 I/O mode, the three- or five-row P2 adapter board used with the MVME761 has a jumper to enable/disable SCSI bus terminators. +5V DC power for SCSI termination is supplied through a polyswitch located on the adapter board.

Secondary SCSI Interface

In addition to the primary SCSI interface on the base board, an optional, secondary 16-bit SCSI interface is available on the PM604 or PM760 processor/memory mezzanine. If present, the secondary SCSI is implemented with a Symbios 53C875 SCSI I/O controller at an external clock speed of 40 MHz. The 53C875 device includes a clock doubler.

The secondary SCSI interface lines are routed through rows A and C of the P2 connector on the processor/memory mezzanine. A P2 adapter board is necessary to transfer the signals from the P2 connector to an SCSI connector. If the interface requires termination at the VMEmodule end of the SCSI chain, the P2 adapter also supplies the termination point.

Two types of P2 adapter boards are available for the secondary SCSI interface on the processor/memory mezzanine:

- For single-ended SCSI configurations requiring termination at the VMEmodule, use adapter model MVME4600P2-001 (part number 01-W3203F03A).
- For differential SCSI configurations, use adapter model MVME4600P2-002 (part number 01-W3203F04A).

For details on programming the secondary SCSI interface, refer to the Symbios 53C875 data manual.

Ethernet Interface

The MVME3600 and 4600 series VMEmodules use Intel's DEC21140 PCI Fast Ethernet LAN controller to implement an Ethernet interface that supports both AUI (via MVME712M) and 10BaseT/100BaseTX (via MVME761) connections. The balanced differential transceiver lines are coupled via on-board transformers.

The MVME3600 and 4600 series VMEmodules route its AUI and 10BaseT/100BaseTX lines through the P2 connector to the transition module (as illustrated in Figure 1-26 and Figure 1-27). The MVME712M front panel has an industry-standard DB-15 connector for an AUI connection. The MVME761 supports 10BaseT/100BaseTX connections.

Every VMEmodule is assigned an Ethernet station address. The address is $08003E2*xxxxx*, where *xxxxx* is the unique 5-nibble number assigned to the board (that is, every board has a different value for *xxxxx*).

Each VMEmodule displays its Ethernet station address on a label attached to the base board in the PMC connector keepout area just behind the front panel. In addition, the six bytes including the Ethernet station address are stored in an SROM device separate from the DEC Ethernet controller. That is, the value 08003E2*xxxxx* is stored in SROM. At an offset of $1F2C, the upper four bytes (08003E2*x*) can be read. At an offset of $1F30, the lower two bytes (*xxxx*) can be read. The VMEmodule firmware has the capability to retrieve or set the Ethernet station address via the **CNFG** command.

Note The unique Ethernet address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable.

If the data in SROM is lost, use the number on the label in the PMC connector keepout area to restore it.

For the pin assignments of the transition module AUI or 10BaseT/100BaseTX connector, refer to Chapter 4, *Connector Pin Assignments*. For detailed programming information, refer to the BBRAM/TOD Clock memory map description in the *MVME3600/4600 Series Programmer's Reference Guide*.

Secondary Ethernet Interface

In addition to the primary Ethernet interface on the base board, an optional, secondary 10BaseT/100BaseTX Ethernet interface is available on the PM604 or PM760 processor/memory module. If present, the secondary Ethernet is implemented with an additional DEC21140 PCI Fast Ethernet LAN controller.

The secondary Ethernet interface lines are routed through rows A and C of the P2 connector on the processor/memory module. A P2 adapter board (model MVME4600P2-001 or MVME4600P2-002) is necessary to

transfer the signals from the P2 connector to an Ethernet connector. For details on programming the secondary Ethernet interface, refer to the DEC21140 data manual.

PCI Mezzanine Interface

A key feature of the MVME3600 and 4600 series families is the PCI (Peripheral Component Interconnect) bus. In addition to the on-board local bus devices (SCSI, Ethernet, graphics, etc.), the PCI bus supports an industry-standard mezzanine interface, IEEE P1386.1 PMC (PCI Mezzanine Card).

PMC modules offer a variety of possibilities for I/O expansion through FDDI (Fiber Distributed Data Interface), ATM (Asynchronous Transfer Mode), graphics, Ethernet, or SCSI ports. The base board supports PMC front panel and rear P2 I/O. There is also provision for stacking a PMC carrier board on the base board/processor mezzanine assembly for additional expansion.

The MVME3600 and 4600 series VMEmodules support one PMC slot. Four 64-pin connectors on the base board (J11, J12, J13, and J14) interface with 32-bit IEEE P1386.1 PMC-compatible mezzanines to add any desirable function. The PCI Mezzanine Card slot has the following characteristics:

Mezzanine Type	PMC (PCI Mezzanine Card)
Mezzanine Size	S1B: Single width, standard depth (75 mm x 150 mm) with front panel
PMC Connectors	J11 and J12 (32/64-Bit PCI with front and rear I/O)
Signaling Voltage	V_{io} = 5.0Vdc

The PMC carrier board connector (J4) is a 114-pin Mictor connector located on the processor/memory mezzanine.

Refer to Chapter 4, *Connector Pin Assignments* for the pin assignments of the PMC connectors. For detailed programming information, refer to the PCI bus descriptions in the *MVME3600/4600 Series Programmer's Reference Guide* and to the user documentation for the PMC modules you intend to use.

VMEbus Interface

The VMEbus interface is implemented with the CA91C042 “Universe” ASIC. The Universe chip interfaces the 32/64-bit PCI local bus to the VMEbus.

The Universe ASIC provides:

- The PCI-bus-to-VMEbus interface
- The VMEbus-to-PCI-bus interface
- The DMA controller functions of the local VMEbus

The Universe chip includes Universe Control and Status Registers (UCSRs) for interprocessor communications. It can provide the VMEbus system controller functions as well. For detailed programming information, refer to the *Universe User’s Manual* and to the discussions in the *MVME3600/4600 Series Programmer's Reference Guide*.

ISA Super I/O Device (ISASIO)

The MVME3600 and 4600 series VMEmodules use a PC87308 ISASIO chip from National Semiconductor to implement certain segments of the P2 and front-panel I/O:

- Two asynchronous serial ports (COM1 and COM2) via P2 and transition module
- Parallel port via P2 and transition module:
  - Centronics printer port in MVME712M-compatible models
  - IEEE1284 bidirectional parallel port in MVME761-compatible models
- Floppy disk drive support via drive/power connector J2
- Keyboard and mouse interface via circular DIN connectors J6 and J7

Asynchronous Serial Ports

The two asynchronous ports provided by the ISASIO device employ TTL-level signals that are buffered through EIA-232-D drivers and receivers and routed to the P2 connector.

Hardware initializes the two serial ports as COM1 and COM2 with ISA I/O base addresses of $3F8 and $2F8 respectively. This default configuration also assigns COM1 to PIB (PCI/ISA Bridge Controller) interrupt request line IRQ4 and COM2 to IRQ3. You can change the default configuration by reprogramming the ISASIO device. For detailed programming information, refer to the PCI and ISA bus discussions in the *MVME3600/4600 Series Programmer's Reference Guide* and to the vendor documentation for the ISASIO device.

Parallel Port

The parallel port is a Centronics printer interface in MVME712M-compatible models, and a full IEEE-1284 bidirectional parallel port in MVME761-compatible models. Both versions are implemented with the ISASIO device. All parallel I/O interface signals are routed to P2 through series damping resistors.

Hardware initializes the parallel port as PPT1 with an ISA IO base address of $3BC. This default configuration also assigns the parallel port to PIB (PCI/ISA Bridge Controller) interrupt request line IRQ7. You can change the default configuration by reprogramming the ISASIO device. For detailed programming information, refer to the PCI and ISA bus discussions in the *MVME3600/4600 Series Programmer's Reference Guide* and to the vendor documentation for the ISASIO device.

Disk Drive Controller

The ISASIO device incorporates a PS/2-compatible low- and high-density disk drive controller for use with an optional external disk drive (model XRFLOPPY2-F, part number 01-W3200F01B). The drive interfaces with the ISASIO controller via base board connector J2, which relays both power and control signals.

The ISASIO disk drive controller is compatible with the DP8473, 765A, and N82077 devices commonly used to implement floppy disk controllers. Software written for those devices may be used without change to operate the ISASIO controller. The ISASIO device may be used to support any of the following devices:

- 3½-inch 1.44MB floppy disk drive
- 5¼-inch 1.2MB floppy disk drive
- Standard 250kbps to 2Mbps tape drive system

In addition to the disk drive control signals, a set of 16 lines is available to drive an external LED array.

Keyboard and Mouse Interface

The National Semiconductor PC87308 ISASIO chip used to implement certain segments of the P2 and front-panel I/O provides ROM-based keyboard and mouse interface control. The front panel of the MVME4600 series base board has two 6-pin circular DIN connectors for the keyboard and mouse connections.

PCI-ISA Bridge (PIB) Controller

The MVME3600 and 4600 series VMEmodules use a Winbond W83C553 bridge controller to supply the interface between the PCI local bus and the ISA system I/O bus (diagrammed in Figure 1-1 on page 1-3).

The PIB controller provides the following functions:

- PCI bus arbitration for:
  - ISA (Industry Standard Architecture) bus DMA
  - The PHB (PCI Host Bridge) MPU/local bus interface function, implemented by the Raven ASIC
  - All on-board PCI devices
  - The PMC (PCI Mezzanine Card) slot
- ISA (Industry Standard Architecture) bus arbitration for DMA devices
- ISA interrupt mapping for four PCI interrupts
- Interrupt controller functionality to support 14 ISA interrupts
- Edge/level control for ISA interrupts
- Seven independently programmable DMA channels
- One 16-bit timer
- Three interval counters/timers

Accesses to the configuration space for the PIB (PCI/ISA Bridge) controller are performed by way of the CONADD and CONDAT (Configuration Address and Data) registers in the Raven bridge controller ASIC. The registers are located at offsets $CF8 and $CFC, respectively, from the PCI I/O base address.

Real-Time Clock/NVRAM/Timer Function

The MVME3600 and 4600 series VMEmodule employs an SGS-Thomson surface-mount M48T59 or M48T559 RAM and clock chip to provide 8KB of non-volatile static RAM, a real-time clock, and a watchdog timer function. This chip supplies a clock, oscillator, crystal, power failure detection, memory write protection, 8KB of NVRAM, and a battery in a package consisting of two parts:

- A 28-pin 330mil SO device containing the real-time clock, the oscillator, power failure detection circuitry, timer logic, 8KB of static RAM, and gold-plated sockets for a battery
- A SNAPHAT® battery housing a crystal along with the battery

The SNAPHAT battery package is mounted on top of the M48T59/M48T559 device. The battery housing is keyed to prevent reverse insertion.

The clock furnishes seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. Corrections for 28-, 29- (leap year), and 30-day months are made automatically. The clock generates no interrupts. Although the M48T59/M48T559 is an 8-bit device, it supports 16- and 32-bit accesses as well as 8-bit accesses from the ISA bus. Refer to the *MVME3600/4600 Series Programmer's Reference Guide* and to the M48T59 and M48T559 data sheet for detailed programming and battery life information.

Programmable Timers

Among the resources available to the local processor are a number of programmable timers. Timers are incorporated into the PIB controller and the Z8536 CIO device (diagrammed in Figure 1-1 and Figure 3-1). They can be programmed to generate periodic interrupts to the processor.

Interval Timers

The PCI-ISA Bridge controller has three built-in counters that are equivalent to those found in an 82C54 programmable interval timer. The counters are grouped into one timer unit, Timer 1, in the PIB controller. Each counter output has a specific function:

- Counter 0 is associated with interrupt request line IRQ0. It can be used for system timing functions, such as a timer interrupt for a time-of-day function.
- Counter 1 generates a refresh request signal for ISA memory. This timer is not used in the MVME4600 series.

- Counter 2 provides the tone for the speaker output function on the PIB controller (the SPEAKER_OUT signal which can be cabled to an external speaker via the remote reset connector).

The interval timers use the OSC clock input as their clock source. The MVME4600 series VMEmodule drives the OSC pin with a 14.31818 MHz clock source.

16-Bit Timers

Four 16-bit timers are available on the MVME4600 series. The PIB controller supplies one 16-bit timer; the Z8536 CIO device provides the other three. For information on programming these timers, refer to the data sheets for the W83C553 PIB controller and the Z8536 CIO device.

Serial Communications Interface

The MVME4600 series VMEmodule uses a Zilog Z85230 ESCC (Enhanced Serial Communications Controller) to implement the two serial communications interfaces, which are routed through P2. The Z85230 supports synchronous (SDLC/HDLC) and asynchronous protocols. The MVME4600 series hardware supports asynchronous serial baud rates of 110B/s to 38.4KB/s.

Each interface supports the CTS, DCD, RTS, and DTR control signals as well as the TxD and RxD transmit/receive data signals, and TxC/RxC synchronous clock signals. Since not all modem control lines are available in the Z85230, a Z8536 CIO is used to provide the missing modem lines.

A PAL device performs decoding of register accesses and pseudo interrupt acknowledge cycles for the Z85230 and the Z8536 in ISA I/O space. The PIB controller supplies DMA support for the Z85230.

The Z85230 receives a 10 MHz clock input. The Z85230 supplies an interrupt vector during pseudo interrupt acknowledge cycles. The vector is modified within the Z85230 according to the interrupt source. Interrupt request levels are programmed via the PIB controller. Refer to the Z85230 data sheet and to the *MVME3600/4600 Series Programmer's Reference Guide* for further information.

Z8536 CIO Device

The Z8536 CIO device complements the Z85230 ESCC by supplying modem control lines not provided by the Z85230 ESCC. In addition, the Z8536 CIO device has three independent 16-bit counters/ timers. The Z8536 receives a 5 MHz clock input.

Base Module Feature Register

The Base Module Feature Register contains the details of the MVME3600/4600 series VMEmodule's configuration. It is an 8-bit read-only register located on the base board at ISA I/O address $0802.

Base Module Feature Register — Offset $0802								
BIT	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
FIELD	Not Used	SCCP*	PMC2P*	PMC1P*	VMEP*	GFXP*	LANP*	SCSIP*
OPER		R	R	R	R	R	R	R
RESET		N/A	1	N/A	N/A	N/A	N/A	N/A

SCCP* Z85230 ESCC present. If set, there is no on-board synchronous serial support (the ESCC is not present). If cleared, the Z85230 ESCC is installed and there is on-board support for synchronous serial communication.

PMC2P* PMC/PMCIX slot 2 present. If set, no PCI mezzanine card (or PCI expansion device) is installed in PMC slot 2. If cleared, PMC/PMCIX slot 2 contains a PCI mezzanine card (or PCI expansion device).

PMC1P* PMC slot 1 present. If set, no PCI mezzanine card is installed in PMC slot 1. If cleared, PMC slot 1 contains a PCI mezzanine card.

VMEP* VMEbus present. If set, there is no VMEbus interface. If cleared, the VMEbus interface is supported.

GFXP* Graphics present. If set, no graphics interface is installed. If cleared, on-board graphics are available.

LANP* Ethernet present. If set, no Ethernet transceiver interface is installed. If cleared, there is on-board Ethernet support.

SCSIP* SCSI present. If set, there is no on-board SCSI interface. If cleared, on-board SCSI is supported.

P2 Signal Multiplexing

Due to the limited supply of available pins in the P2 backplane connectors of MVME3600 and 4600 series models that are configured for MVME761 I/O mode, certain signals are multiplexed through VMEbus connector P2 for additional I/O capacity.

The signals affected are synchronous I/O control signals that pass between the base board and the MVME761 transition module. The multiplexing is a hardware function that is entirely transparent to software.

Four signals are involved in the P2 multiplexing function: MXDO, MXDI, MXCLK, and MXSYNC*.

MXDO is a time-multiplexed data output line from the main board and MXDI is a time-multiplexed line from the MVME761 module. MXCLK is a 10 MHz bit clock for the MXDO and MXDI data lines. MXSYNC* is asserted for one bit time at time slot 15 (refer to the following table) by the base board. The MVME761 transition module uses MXSYNC* to synchronize with the base board.

A 16-to-1 multiplexing scheme is used with MXCLK's 10 MHz bit rate. Sixteen time slots are defined and allocated as follows:

Table 3-2. P2 Multiplexing Sequence

MXDO (From Base Board)		MXDI (From MVME761)	
Time Slot	**Signal Name**	**Time Slot**	**Signal Name**
0	RTS3	0	CTS3
1	DTR3	1	DSR3/MID1
2	LLB3/MODSEL	2	DCD3
3	RLB3	3	TM3/MID0
4	RTS4	4	RI3

Table 3-2. P2 Multiplexing Sequence (Continued)

MXDO (From Base Board)		MXDI (From MVME761)	
Time Slot	**Signal Name**	**Time Slot**	**Signal Name**
5	DTR4	5	CTS4
6	LLB4	6	DSR4/MID3
7	RLB4	7	DCD4
8	IDREQ*	8	TM4/MID2
9	DTR1	9	RI4
10	DTR2	10	RI1
11	Reserved	11	DSR1
12	Reserved	12	DCD1
13	Reserved	13	RI2
14	Reserved	14	DSR2
15	Reserved	15	DCD2

ABORT Switch (S1)

The ABORT switch is located on the LED mezzanine. When activated by software, the ABORT switch can generate an interrupt signal from the base board to the processor. The interrupt is normally used to abort program execution and return control to the debugger firmware located in the MVME4600 series VMEmodule's PROM and Flash memory. The interrupt signal reaches the processor module via ISA bus interrupt line IRQ8*. The signal is also available at pin PB7 of the Z8536 CIO device, which handles various status signals, serial I/O lines, and counters.

The interrupter connected to the ABORT switch is an edge-sensitive circuit, filtered to remove switch bounce.

RESET Switch (S2)

The RESET switch is located on the LED mezzanine. The RESET switch resets all onboard devices; it also drives a SYSRESET* signal if the MVME3600 and 4600 series VMEmodule is the system controller.

Front Panel Indicators (DS1 – DS6)

There are six LEDs on the MVME3600 and 4600 front panel: CHS, BFL, CPU, PCI, FUS, and SYS.

- CHS (DS1, yellow). Checkstop; driven by the MPC604 or MCP760 status lines on the VMEmodule. Lights when a halt condition from the processor is detected.
- BFL (DS2, yellow). Board Failure; lights when the BRDFAIL* signal line is active.
- CPU (DS3, green). CPU activity; lights when the DBB* (Data Bus Busy) signal line on the processor bus is active.
- PCI (DS4, green). PCI activity; lights when the IRDY* (Initiator Ready) signal line on the PCI bus is active. This indicates that the PCI mezzanine or carrier board (if installed) is active.
- FUS (DS5, green). Fuse OK; lights when +5Vdc, +12Vdc, and –12Vdc power is available from the base board to the transition module and remote devices.

Note Because the FUS LED monitors the status of several voltages on the VMEmodule, it does not directly indicate the condition of any single fuse. If the LED flickers or goes out, check all the fuses (polyswitches).

- SYS (DS6, green). System Controller; lights when the Universe ASIC in the VMEmodule is the VMEbus system controller.

Polyswitches (Resettable Fuses)

The MVME3600 and 4600 series VMEmodule draws fused +5V DC, +12V DC, and –12V DC power from the VMEbus backplane through connectors P1 and P2. The 3.3V DC and core processor voltage power is supplied by the on-board +5V DC. The following table lists the fuses with the voltages they protect.

Table 3-3. Fuse Assignments

Fuse	Voltage
R28	–12V DC (used on MVME761 versions)
R30	+5V DC
R34	+12V DC

I/O Power

The MVME3600 and 4600 series VMEmodule furnishes +12V DC and (in MVME761 I/O mode) –12V DC power to the transition module through polyswitches (resettable fuses) F3 and F1 respectively. These voltage sources power the serial port drivers and any LAN transceivers connected to the transition module. Fused +5V DC power is supplied to the base board's keyboard and mouse connectors through polyswitch F2 and to the 14-pin combined LED-mezzanine/remote-reset connector, J1. The FUS LED (DS5) on the MVME3600 and 4600 front panel illuminates when all three voltages are available.

In MVME712M I/O mode, the yellow DS1 LED on the MVME712M also signals the availability of +12V DC LAN power, indicating in turn that polyswitch F3 is good. If the Ethernet transceiver fails to operate, check polyswitch F3.

In MVME712M I/O mode, the MVME3600 and 4600 series VMEmodule supplies SCSI terminator power through a 1A fuse (F1) located on the P2 adapter board. If the fuse is blown, the SCSI device(s) may function erratically or not at all. With the P2 adapter board cabled to a transition module and with an SCSI bus connected to the transition module, the green

SCSI LED on the module illuminates when SCSI terminator power is available. If the SCSI LED on the transition module flickers during SCSI bus operation, check fuse F1 on the P2 adapter board.

Note Because any device on the SCSI bus can provide TERMPWR, and because the FUS LED monitors the status of several voltages, the LED does not directly indicate the condition of any single fuse. If the LED flickers or goes out, check all the fuses (polyswitches).

In MVME761 I/O mode, the MVME3600 and 4600 series VMEmodule supplies SCSI terminator power through a polyswitch (resettable fuse) located on the P2 adapter board.

Speaker Control

The base board supplies a SPEAKER_OUT signal to the 14-pin combined LED-mezzanine/remote-reset connector, J1. When J1 is used as a remote reset connector with the LED mezzanine removed, the SPEAKER_OUT signal can be cabled to an external speaker to obtain a beep tone. For the pin assignments of J1, refer to Table 4-1.

Processor for PM604

The MVME3600 and 4600 series VMEmodules have either one or two PowerPC 604 processor chips with 64MB to 1GB of ECC DRAM, 512KB of level 2 cache (L2 cache), and up to 9MB of Flash memory. The L2 cache, Flash memory, and 64MB of ECC DRAM reside on the processor/memory mezzanine (PM604). Additional ECC DRAM, for a total of up to 1GB overall, is located on the RAM201 memory mezzanine.

The PowerPC 604 is a 64-bit processor with 32KB (16KB data cache and 16KB instruction cache), or 64KB (32KB data cache and 32KB instruction cache) on-chip cache.

The Raven bridge controller ASIC provides the bridge between the PowerPC microprocessor bus and the PCI local bus. Electrically, the Raven chip is a 64-bit PCI connection. Four programmable map decoders in each direction provide flexible addressing between the PowerPC microprocessor bus and the PCI local bus.

Flash Memory

The processor/memory mezzanine has 1MB of 16-bit Flash memory in two 8-bit sockets, primarily for storage of the boot firmware. It also accommodates 4MB of additional 64-bit Flash memory in two banks for customer-specific requirements.

The on-board monitor/debugger, PPCBug, resides in the Flash chips. The PPCBug firmware provides functionality for:

- Booting and resetting the system
- Initializing a request
- Displaying and modifying configuration variables
- Running self-tests and diagnostics
- Updating firmware ROM

A jumper header (J2) tells the Falcon chip set where in memory to fetch the board reset vector. Depending on the configuration of J2, resets execute either from Flash memory bank A (64-bit Flash) or from bank B (16-bit Flash).

In normal operation, the Flash devices are in “read-only” mode, their contents are predefined, and they are protected against inadvertent writes arising from power outages. However, for programming purposes, programming voltage is always supplied to the devices and the Flash contents may be modified by executing the proper program command sequence. Refer to the third-party data sheet and/or to the *PPCBug Firmware Package User’s Manual* for further device-specific information on modifying Flash contents.

RAM201 Memory Module

The RAM201 is the ECC DRAM memory mezzanine module that (together with a processor/memory mezzanine, an LED mezzanine and an optional PMC module) plugs into the base board to make a complete MVME4600 series VMEmodule. See Figure 1-23.

RAM201 modules of 64, 128, 256, or 512MB are available for memory expansion. The ECC DRAM is controlled by the Falcon memory controller chip set. The Falcon ASICs perform two-way interleaving, with double-bit error detection and single-bit error correction.

MVME712M Transition Module

The MVME712M transition module (Figure 1-5 on page 1-22) and P2 adapter board are used in conjunction with certain models of the MVME3600 and 4600 series VMEmodules.

The features of the MVME712M include:

- A parallel printer port
- An Ethernet interface supporting AUI connections
- Four EIA-232-D multiprotocol serial ports
- An SCSI interface (via P2 adapter) for connection to both internal and external devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Provision for modem connection
- Green LED for SCSI terminator power; yellow LED for Ethernet transceiver power

The features of the P2 adapter board include:

- A 50-pin connector for SCSI cabling to the MVME712M and/or to other SCSI devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Fused SCSI terminator power developed from the +5V DC present at connector P2
- A 64-pin DIN connector to interface the EIA-232-D, parallel, SCSI, and Ethernet signals to the MVME712M

MVME761 Transition Module

The MVME761 transition module (Figure 1-14 on page 1-32) and P2 adapter board are used in conjunction with certain models of the MVME3600 and 4600 series VMEmodules.

The features of the MVME761 include:

- A parallel printer port (IEEE 1284-I compliant)
- An Ethernet interface supporting 10BaseT/100BaseTX connections
- Two EIA-232-D asynchronous serial ports (identified as COM1 and COM2 on the front panel)
- Two synchronous serial ports (SERIAL 3 and SERIAL 4 on the front panel), configurable for EIA-232-D, EIA-530, V.35, or X.21 protocols
- Two 60-pin Serial Interface Module (SIM) connectors

Serial Interface Modules

The synchronous serial ports on the MVME761 are configurable via serial interface modules (SIMs), used in conjunction with the appropriate jumper settings on the transition module and base board. The SIMs are small plug-in printed circuit boards which contain all the circuitry needed to convert

a TTL-level port to the standard voltage levels needed by various industry-standard serial interfaces, such as EIA-232, EIA-530, etc. SIMs are available for the following configurations:

Table 3-4. SIM Type Identification

Model Number	Module Type
SIM232DCE	EIA-232 DCE
SIM232DTE	EIA-232 DTE
SIM530DCE	EIA-530 DCE
SIM530DTE	EIA-530 DTE
SIMV35DCE	V.35 DCE
SIMV35DTE	V.35 DTE
SIMX21DCE	X.21 DCE
SIMX21DTE	X.21 DTE

For additional information about the serial interface modules, refer to the MVME761 *User's Manual* (listed in Appendix D, *Related Documentation*) as necessary.

Connector Pin Assignments

4

MVME3600 and 4600 Series VMEmodule Connectors

This chapter summarizes the pin assignments for the following groups of interconnect signals for MVME3600 and 4600 series VMEmodules:

- Connectors with pin assignments common to MVME712M- as well as MVME761-compatible versions of the board

Connector
LED Mezzanine Connector J1 on page 4-3
Floppy/LED Connector J2 on page 4-4
Processor/Memory Mezzanine Connector J3 on page 4-5
PMC Carrier Board Connector J4 on page 4-8
Graphics Connector J4 on page 4-104
DRAM Mezzanine Connector J6 on page 4-11
Debug Connector J7 on page 4-14
Keyboard and Mouse Connectors J6, J7 on page 4-18
PMC Module Connectors on page 4-18
VMEbus Connector P1 on page 4-21
PM604 P1 Connector on page 4-22
PM604 P2 Connector on page 4-24

- Connectors with pin assignments specific to MVME712M-compatible versions of the board

Connector
VMEbus Connector P2 on page 4-25
SCSI Connector on page 4-27
Serial Ports 1-4 on page 4-28
Parallel Connector on page 4-29
Ethernet AUI Connector on page 4-30

- Connectors with pin assignments specific to MVME761-compatible versions of the board

Connector
VMEbus Connector P2 on page 4-31
Serial Ports 1 and 2 on page 4-33
Serial Ports 3 and 4 on page 4-33
Parallel Connector on page 4-35
Ethernet 10BaseT/100BaseTX Connector on page 4-36

The following tables furnish pin assignments only. For detailed descriptions of the various interconnect signals, consult the support information documentation package for the MVME3600 and 4600 series VMEmodule or the support information sections of the transition module documentation as necessary.

Common Connectors

The following tables describe connectors used with the same pin assignments by MVME712M- as well as MVME761-compatible versions of the base board.

LED Mezzanine Connector J1

A 14-pin connector (J1 on the base board) supplies the interface between the base board and the LED mezzanine module. On the base board, this connector is a 2x7 header. On the LED mezzanine, it is a 2x7 surface-mount socket strip.

Removing the LED mezzanine makes the mezzanine connector available for service as a remote status and control connector. In this application, J1 can be connected to a user-supplied external cable to carry the Reset and Abort signals and the LED lines to a control panel located apart from the VMEmodule. Maximum cable length is 15 feet. The pin assignments are as follows:

Table 4-1. LED Mezzanine Connector

1	GND	RESETSW*	2
3	No Connection	ABORTSW*	4
5	PCILED*	FAILLED*	6
7	LANLED*	STATLED*	8
9	FUSELED*	RUNLED*	10
11	SBSYLED*	SCONLED*	12
13	+5V	SPKR	14

Floppy/LED Connector J2

A 50-pin high-density connector (J2 on the base board) supplies the interface between the base board and an optional external floppy disk drive. In addition to the disk drive control signals, a set of 16 lines is available to drive an external LED array. The pin assignments are listed in the following table.

Table 4-2. Floppy/LED Connector

1	+5VF	+5VF	2
3	LEDDISP0	LEDDISP1	4
5	LEDDISP2	LEDDISP3	6
7	LEDDISP4	LEDDISP5	8
9	LEDDISP6	LEDDISP7	10
11	LEDDISP8	LEDDISP9	12
13	LEDDISP10	LEDDISP11	14
15	LEDDISP12	LEDDISP13	16
17	LEDDISP14	LEDDISP15	18
19	LEDBLNK	F_DENSEL	20
21	GND	F_MSEN0	22
23	GND	F_INDEX*	24
25	GND	F_MTR0*	26
27	GND	F_DR1*	28
29	GND	F_DR0*	30
31	GND	F_MTR1*	32
33	GND	F_DIR*	34
35	GND	F_STEP*	36
37	GND	F_WDATA*	38
39	GND	F_WGATE*	40
41	GND	F_TRK0*	42

Table 4-2. Floppy/LED Connector (Continued)

43	GND	F_WP*	44
45	GND	F_RDATA*	46
47	GND	F_HDSEL*	48
49	GND	F_DSKCHG*	50

Processor/Memory Mezzanine Connector J3

A 152-pin connector (J3 on the base board) supplies the interface between the base board and the processor/memory mezzanine module. The pin assignments are listed in the following table.

Table 4-3. Processor/Memory Mezzanine Connector

1	PCICLK1		PCICLK2	2
3	PCICLK3		PCICLK4	4
5	GND		GND	6
7	CKSTOP*		CPULED*	8
9	IBCINT*		ABORT*	10
11	LANINT*		VME2PCIINT*	12
13	SCSIINT*		GRINT*	14
15	PMCIRQ*		KBIRQ	16
17	MOUSEIRQ		COM1IRQ	18
19	COM2IRQ	GND	PARPTIRQ	20
21	CIO_IRQ*		SCC_IRQ*	22
23	FLPYIRQ*		IRQ_B*	24
25	SMI*		SRESET*	26
27	NMI		LBRESET*	28
29	TBEN		PURESET*	30
31	TCK		TDO1	32
33	TDI1		TMS	34
35	PMCP*		TRST*	36
37	PMCREQ*		PMCGNT*	38

Table 4-3. Processor/Memory Mezzanine Connector

39	ISA_MSTR*		FLSHREQ*	40
41	SD7		FLSHACK*	42
43	SD6		Reserved	44
45	SD5		RAMCFG*	46
47	SD4		CPUCNFG*	48
49	SD3		X_IOR*	50
51	SD2		X_IOW*	52
53	SD1		SA1	54
55	SD0		SA0	56
57	–12V	+5V	+12V	58
59	SERR*		PERR*	60
61	SDONE		LOCK*	62
63	SBO*		DEVSEL*	64
65	GND		GND	66
67	IRDY*		TRDY*	68
69	FRAME*		STOP*	70
71	GND		GND	72
73	PCIGNT*		ACK64*	74
75	PCIREQ*		REQ64*	76
77	Reserved		PAR	78
79	CBE0*		CBE1*	80
81	CBE2*		CBE3*	82
83	AD0		AD1	84
85	AD2		AD3	86
87	AD4		AD5	88
89	AD6		AD7	90
91	AD8		AD9	92
93	AD10		AD11	94
95	AD12	GND	AD13	96
97	AD14		AD15	98

Table 4-3. Processor/Memory Mezzanine Connector

99	AD16		AD17	100
101	AD18		AD19	102
103	AD20		AD21	104
105	AD22		AD23	106
107	AD24		AD25	108
109	AD26		AD27	110
111	AD28		AD29	112
113	AD30		AD31	114
115	PCI_RESV5		PAR64	116
117	CBE4*		CBE5*	118
119	CBE6*		CBE7*	120
121	AD32		AD33	122
123	AD34		AD35	124
125	AD36		AD37	126
127	AD38		AD39	128
129	AD40		AD41	130
131	AD42		AD43	132
133	AD44	+3.3V	AD45	134
135	AD46		AD47	136
137	AD48		AD49	138
139	AD50		AD51	140
141	AD52		AD53	142
143	AD54		AD55	144
145	AD56		AD57	146
147	AD58		AD59	148
149	AD60		AD61	150
151	AD62		AD63	152

PMC Carrier Board Connector J4

The MVME3600 and 4600 series VMEmodule has provision for stacking a PMC carrier board onto the processor/memory mezzanine for additional PCI expansion. A 114-pin connector (J4 on the processor/memory mezzanine) supplies the interface between the VMEmodule and the carrier board. The pin assignments are listed in the following table.

Table 4-4. PMC Carrier Board Connector

1	+3.3V		+3.3V	2
3	PCICLK3		PMCINTA*	4
5	GND		PMCINTB*	6
7	PURESET*		PMCINTC*	8
9	HRESET*		PMCINTD*	10
11	PMC2DO		PHYTDO	12
13	TMS		TCK	14
15	TRST*		PMC2P*	16
17	PMC2GNT*		PMC2REQ*	18
19	+12V	GND	–12V	20
21	PERR*		SERR*	22
23	LOCK*		SDONE	24
25	DEVSEL*		SBO*	26
27	GND		GND	28
29	TRDY*		IRDY*	30
31	STOP*		FRAME*	32
33	GND		GND	34
35	ACK64*		Reserved	36
37	REQ64*		Reserved	38
39	PAR		PCIRST*	40
41	CBE1*		CBE0*	42
43	CBE3*		CBE2*	44
45	AD1		AD0	46

Table 4-4. PMC Carrier Board Connector (Continued)

47	AD3		AD2	48
49	AD5		AD4	50
51	AD7		AD6	52
53	AD9		AD8	54
55	AD11		AD10	56
57	AD13	+5V	AD12	58
59	AD15		AD14	60
61	AD17		AD16	62
63	AD19		AD18	64
65	AD21		AD20	66
67	AD23		AD22	68
69	AD25		AD24	70
71	AD27		AD26	72
73	AD29		AD28	74
75	AD31		AD30	76
77	PAR64		Reserved	78
79	CBE5*		CBE4*	80
81	CBE7*		CBE6*	82
83	AD33		AD32	84
85	AD35		AD34	86
87	AD37		AD36	88
89	AD39		AD39	90
91	AD41		AD40	92
93	AD43		AD42	94
95	AD45	GND	AD44	96
97	AD47		AD46	98
99	AD49		AD48	100
101	AD51		AD50	102
103	AD53		AD52	104
105	AD55		AD54	106

Table 4-4. PMC Carrier Board Connector (Continued)

107	AD57		AD56	108
109	AD59		AD58	110
111	AD61		AD60	112
113	AD63		AD62	114

Graphics Connector J4

The base board has a DB-15 graphics connector located on the front panel. The pin assignments for the graphics connector are listed in the following table.

Table 4-5. Graphics Connector

1	GIRED
2	GIGREEN
3	GIBLUE
4	GIP2
5	GND
6	GND
7	GND
8	GND
9	No Connection
10	GND
11	GIP0
12	GIP1
13	GIHSYNC
14	GIVSYNC
15	GIP3

DRAM Mezzanine Connector J6

A 190-pin connector (J6 on the processor/memory mezzanine) supplies the interface between the processor bus (MPU bus) and the RAM201 DRAM mezzanine. The pin assignments are listed in the following table.

Table 4-6. DRAM Mezzanine Connector

1	A_RAS*		A_CAS*	2
3	B_RAS*		B_CAS*	4
5	C_RAS*		C_CAS*	6
7	D_RAS*		D_CAS*	8
9	OEL*		OEU*	10
11	WEL*		WEU*	12
13	ROMACS*		ROMBCS*	14
15	RAMAEN		RAMBEN	16
17	RAMCEN		EN5VPWR	18
19	RAL0	GND	RAL1	20
21	RAL2		RAL3	22
23	RAL4		RAL5	24
25	RAL6		RAL7	26
27	RAL8		RAL9	28
29	RAL10		RAL11	30
31	RAL12		RAU0	32
33	RAU1		RAU2	34
35	RAU3		RAU4	36
37	RAU5		RAU6	38
39	RAU7		RAU8	40
41	RAU9		RAU10	42
43	RAU11		RAU12	44
45	RDL0		RDL1	46
47	RDL2		RDL3	48
49	RDL4		RDL5	50

Table 4-6. DRAM Mezzanine Connector (Continued)

51	RDL6		RDL7	52
53	RDL8		RDL9	54
55	RDL10		RDL11	56
57	RDL12	+5V	RDL13	58
59	RDL14		RDL15	60
61	RDL16		RDL17	62
63	RDL18		RDL19	64
65	RDL20		RDL21	66
67	RDL22		RDL23	68
69	RDL24		RDL25	70
71	RDL26		RDL27	72
73	RDL28		RDL29	74
75	RDL30		RDL31	76
77	RDL32		RDL33	78
79	RDL34		RDL35	80
81	RDL36		RDL37	82
83	RDL38		RDL39	84
85	RDL40		RDL41	86
87	RDL42		RDL43	88
89	RDL44		RDL45	90
91	RDL46		RDL47	92
93	RDL48		RDL49	94
95	RDL50	GND	RDL51	96
97	RDL52		RDL53	98
99	RDL54		RDL55	100
101	RDL56		RDL57	102
103	RDL58		RDL59	104
105	RDL60		RDL61	106
107	RDL62		RDL63	108
109	CDL0		CDL1	110

Table 4-6. DRAM Mezzanine Connector (Continued)

111	CDL2		CDL3	112
113	CDL4		CDL5	114
115	CDL6		CDL7	116
117	No Connection		No Connection	118
119	RDU0		RDU1	120
121	RDU2		RDU3	122
123	RDU4		RDU5	124
125	RDU6		RDU7	126
127	RDU8		RDU9	128
129	RDU10		RDU11	130
131	RDU12		RDU13	132
133	RDU14	+3.3V	RDU15	134
135	RDU16		RDU17	136
137	RDU18		RDU19	138
139	RDU20		RDU21	140
141	RDU22		RDU23	142
143	RDU24		RDU25	144
145	RDU26		RDU27	146
147	RDU28		RDU39	148
149	RDU30		RDU31	150
151	RDU32		RDU33	152
153	RDU34		RDU35	154
155	RDU36		RDU37	156
157	RDU38		RDU39	158
159	RDU40		RDU41	160
161	RDU42		RDU43	162
163	RDU44		RDU45	164
165	RDU46		RDU47	166
167	RDU48		RDU49	168
169	RDU50		RDU51	170

Table 4-6. DRAM Mezzanine Connector (Continued)

171	RDU52	GND	RDU53	172
173	RDU54		RDU55	174
175	RDU56		RDU57	176
177	RDU58		RDU59	178
179	RDU60		RDU61	180
181	RDU62		RDU63	182
183	CDU0		CDU1	184
185	CDU2		CDU3	186
187	CDU4		CDU5	188
189	CDU6		CDU7	190

Debug Connector J7

A 190-pin connector (J7 on the processor/memory mezzanine) provides access to the processor bus (MPU bus) and some bridge/memory controller signals. It can be used for debugging purposes. The pin assignments are listed in the following table.

Table 4-7. Debug Connector

1	PA0		PA1	2
3	PA2		PA3	4
5	PA4		PA5	6
7	PA6		PA7	8
9	PA8		PA9	10
11	PA10		PA11	12
13	PA12		PA13	14
15	PA14		PA15	16
17	PA16		PA17	18
19	PA18	GND	PA19	20
21	PA20		PA21	22
23	PA22		PA23	24

Table 4-7. Debug Connector (Continued)

25	PA24		PA25	26
27	PA26		PA27	28
29	PA28		PA29	30
31	PA30		PA31	32
33	PA_PAR0		PA_PAR1	34
35	PA_PAR2		PA_PAR3	36
37	APE*		RSRV*	38
39	PD0		PD1	40
41	PD2		PD3	42
43	PD4		PD5	44
45	PD6		PD7	46
47	PD8		PD9	48
49	PD10		PD11	50
51	PD12		PD13	52
53	PD14		PD15	54
55	PD16		PD17	56
57	PD18	+5V	PD19	58
59	PA20		PD21	60
61	PD22		PD23	62
63	PD24		PD25	64
65	PD26		PD27	66
67	PD28		PD29	68
69	PD30		PD31	70
71	PD32		PD33	72
73	PD34		PD35	74
75	PD36		PD37	76
77	PD38		PD39	78
79	PD40		PD41	80
81	PD42		PD43	82
83	PD44		PD45	84

Table 4-7. Debug Connector (Continued)

85	PD46		PD47	86
87	PD48		PD49	88
89	PA50		PD51	90
91	PD52		PD53	92
93	PD54		PD55	94
95	PD56	GND	PD57	96
97	PD58		PD59	98
99	PD60		PD61	100
101	PD62		PD63	102
103	PDPAR0		PDPAR1	104
105	PDPAR2		PDPAR3	106
107	PDPAR4		PDPAR5	108
109	PDPAR6		PDPAR7	110
111	No Connection		No Connection	112
113	DPE*		DBDIS*	114
115	TT0		TSIZ0	116
117	TT1		TSIZ1	118
119	TT2		TSIZ2	120
121	TT3		TC0	122
123	TT4		TC1	124
125	CI*		TC2	126
127	WT*		CSE0	128
129	GLOBAL*		CSE1	130
131	SHARED*		DBWO*	132
133	AACK*	+3.3V	TS*	134
135	ARTY*		XATS*	136
137	DRTY*		TBST*	138
139	TA*		No Connection	140
141	TEA*		No Connection	142
143	No Connection		DBG*	144

Table 4-7. Debug Connector (Continued)

145	No Connection		DBB*	146
147	No Connection		ABB*	148
149	TCLK_OUT		CPUGNT*	150
151	L2PRSNT0*		CPUREQ*	152
153	L2ADSC*		IBCINT*	154
155	L2BAA*		MCHK*	156
157	L2DIRTYI*		SMI*	158
159	L2DIRTYO*		CKSTPI*	160
161	L2DOE*		CKSTPO*	162
163	L2DWE1*		HALTED (N/C)	164
165	L2HIT*		TLBISYNC*	166
167	L2TALE		TBEN	168
169	L2TALOE*		SUSPEND*	170
171	L2TOE*	GND	DRVMOD0	172
173	L2TWE*		DRVMOD1 (N/C	174
175	L2TV		NAPRUN (N/C	176
177	L2PRSNT1*		QREQ*	178
179	SRESET*		QACK*	180
181	HRESET*		CPUTDO	182
183	GND		CPUTDI	184
185	CPUCLK1		CPUTCK	186
187	CPUCLK2		CPUTMS	188
189	CPUCLK3		CPUTRST*	190

Keyboard and Mouse Connectors J6, J7

The base board has two 6-pin circular DIN connectors located on the front panel for the keyboard (J6) and mouse (J7). The pin assignments for those connectors are listed in the following two tables.

Table 4-8. Keyboard Connector

1	K_DATA
2	Termination
3	GND
4	+5VF
5	K_CLK
6	Termination

Table 4-9. Mouse Connector

1	M_DATA
2	Termination
3	GND
4	+5VF
5	M_CLK
6	Termination

PMC Module Connectors

Four 64-pin connectors (J11/12/13/14 on the base board) supply the interface between the MVME3600 and 4600 series VMEmodules and an optional PCI mezzanine card (PMC) module. The pin assignments are listed in the tables on the next two pages.

Table 4-10. PMC Module Connectors

	J11				J12		
1	TCK	–12V	2	1	+12V	TRST*	2
3	GND	PMCINTA*	4	3	TMS	TDO	4
5	PMCINTB*	PMCINTC*	6	5	PMC2TDO	GND	6
7	PMC1P*	+5V	8	7	GND	Not Used	8
9	PMCINTD*	Not Used	10	9	Not Used	Not Used	10
11	GND	Not Used	12	11	Pull-up	+3.3V	12
13	PCICLK4	GND	14	13	PCIRST*	Pull-down	14
15	GND	PMC1GNT*	16	15	+3.3V	Pull-down	16
17	PMC1REQ*	+5V	18	17	Not Used	GND	18
19	+5V	AD31	20	19	AD30	AD29	20
21	AD28	AD27	22	21	GND	AD26	22
23	AD25	GND	24	23	AD24	+3.3V	24
25	GND	CBE3*	26	25	IDSEL	AD23	26
27	AD22	AD21	28	27	+3.3V	AD20	28
29	AD19	+5V	30	29	AD18	GND	30
31	+5V	AD17	32	31	AD16	CBE2*	32
33	FRAME*	GND	34	33	GND	Not Used	34
35	GND	IRDY*	36	35	TRDY*	+3.3V	36
37	DEVSEL*	+5V	38	37	GND	STOP*	38
39	GND	LOCK*	40	39	PERR*	GND	40
41	SDONE*	SBO*	42	41	+3.3V	SERR*	42
43	PAR	GND	44	43	CBE1*	GND	44
45	+5V	AD15	46	45	AD14	AD13	46
47	AD12	AD11	48	47	GND	AD10	48
49	AD09	+5V	50	49	AD08	+3.3V	50
51	GND	CBE0*	52	51	AD07	Not Used	52
53	AD06	AD05	54	53	+3.3V	Not Used	54
55	AD04	GND	56	55	Not Used	GND	56

Table 4-10. PMC Module Connectors (Continued)

57	+5V	AD03	58	57	Not Used	Not Used	58
59	AD02	AD01	60	59	GND	Not Used	60
61	AD00	+5V	62	61	ACK64*	+3.3V	62
63	GND	REQ64*	64	63	GND	Not Used	64

Table 4-11. PMC Module Connectors (Continued)

	J13				J14		
1	Not Used	GND	2	1	PMCIO0	PMCIO1	2
3	GND	CBE7*	4	3	PMCIO2	PMCIO3	4
5	CBE6*	CBE5*	6	5	PMCIO4	PMCIO5	6
7	CBE4*	GND	8	7	PMCIO6	PMCIO7	8
9	+5V	PAR64	10	9	PMCIO8	PMCIO9	10
11	AD63	AD62	12	11	PMCIO10	PMCIO11	12
13	AD61	GND	14	13	PMCIO12	PMCIO13	14
15	GND	AD60	16	15	PMCIO14	PMCIO15	16
17	AD59	AD58	18	17	PMCIO16	PMCIO17	18
19	AD57	GND	20	19	PMCIO18	PMCIO19	20
21	+5V	AD56	22	21	PMCIO20	PMCIO21	22
23	AD55	AD54	24	23	PMCIO22	PMCIO23	24
25	AD53	GND	26	25	PMCIO24	PMCIO25	26
27	GND	AD52	28	27	PMCIO26	PMCIO27	28
29	AD51	AD50	30	29	PMCIO28	PMCIO29	30
31	AD49	GND	32	31	PMCIO30	PMCIO31	32
33	GND	AD48	34	33	Not Used	Not Used	34
35	AD47	AD46	36	35	Not Used	Not Used	36
37	AD45	GND	38	37	Not Used	Not Used	38
39	+5V	AD44	40	39	Not Used	Not Used	40
41	AD43	AD42	42	41	Not Used	Not Used	42
43	AD41	GND	44	43	Not Used	Not Used	44
45	GND	AD40	46	45	Not Used	Not Used	46
47	AD39	AD38	48	47	Not Used	Not Used	48

Table 4-11. PMC Module Connectors (Continued)

49	AD37	GND	50	49	Not Used	Not Used	50
51	GND	AD36	52	51	Not Used	Not Used	52
53	AD35	AD34	54	53	Not Used	Not Used	54
55	AD33	GND	56	55	Not Used	Not Used	56
57	+5V	AD32	58	57	Not Used	Not Used	58
59	Not Used	Not Used	60	59	Not Used	Not Used	60
61	Not Used	GND	62	61	Not Used	Not Used	62
63	GND	Not Used	64	63	Not Used	Not Used	64

VMEbus Connector P1

Two 160-pin connectors (P1 and P2) supply the interface between the base board and the VMEbus. P1 provides power and VME signals for 24-bit addressing and 16-bit data. Its pin assignments are set by the VMEbus specification. They are listed in Table 4-12.

Table 4-12. VMEbus Connector P1

	Row Z	Row A	Row B	Row C	Row D	
1	Not Used	VD0	VBBSY*	VD8	Not Used	1
2	GND	VD1	VBCLR*	VD9	GND	2
3	Not Used	VD2	VACFAIL*	VD10	Not Used	3
4	GND	VD3	VBGIN0*	VD11	Not Used	4
5	Not Used	VD4	VBGOUT0*	VD12	Not Used	5
6	GND	VD5	VBGIN1*	VD13	Not Used	6
7	Not Used	VD6	VBGOUT1*	VD14	Not Used	7
8	GND	VD7	VBGIN2*	VD15	Not Used	8
9	Not Used	GND	VBGOUT2*	GND	VMEGAP*	9
10	GND	VSYSCLK	VBGIN3*	VSYSFAIL*	VMEGA0*	10
11	Not Used	GND	VBGOUT3*	VBERR*	VMEGA1*	11
12	GND	VDS1*	VBR0*	VSYSRESET*	Not Used	12
13	Not Used	VDS0*	VBR1*	VLWORD	VMEGA2*	13
14	GND	VWRITE*	VBR2*	VAM5	Not Used	14
15	Not Used	GND	VBR3*	VA23	VMEGA3*	15

Table 4-12. VMEbus Connector P1 (Continued)

16	GND	VDTACK*	VAM0	VA22	Not Used	16
17	Not Used	GND	VAM1	VA21	VMEGA4*	17
18	GND	VAS*	VAM2	VA20	Not Used	18
19	Not Used	GND	VAM3	VA19	Not Used	19
20	GND	VIACK*	GND	VA18	Not Used	20
21	Not Used	VIACKIN*	VSERCLK	VA17	Not Used	21
22	GND	VIACKOUT*	VSERDAT	VA16	Not Used	22
23	Not Used	VAM4	GND	VA15	Not Used	23
24	GND	VA7	VIRQ7*	VA14	Not Used	24
25	Not Used	VA6	VIRQ6*	VA13	Not Used	25
26	GND	VA5	VIRQ5*	VA12	Not Used	26
27	Not Used	VA4	VIRQ4*	VA11	Not Used	27
28	GND	VA3	VIRQ3*	VA10	Not Used	28
29	Not Used	VA2	VIRQ2*	VA9	Not Used	29
30	GND	VA1	VIRQ1*	VA8	Not Used	30
31	Not Used	–12V	+5VSTDBY	+12V	GND	31
32	GND	+5V	+5V	+5V	Not Used	32

PM604 P1 Connector

The P1 connector provides daisy chain connections for the IACKIN#/IACKOUT# and the BG[0:3]IN#/BG[0:3]OUT# signals. P1 also supplies additional +5V power to the board. The pin assignments for P1 are as follows:

Table 4-13. P1 Connector Pin Assignments

	Row A	Row B	Row C	
1				1
2				2
3				3
4		BG0IN#		4
5		BG0OUT#		5
6		BG1IN#		6

Table 4-13. P1 Connector Pin Assignments (Continued)

7		BG1OUT#		7
8		BG2IN#		8
9	GND	BG2OUT#	GND	9
10		BG3IN#		10
11	GND	BG3OUT#		11
12				12
13				13
14				14
15	GND			15
16				16
17	GND			17
18				18
19	GND			19
20		GND		20
21	IACKIN#			21
22	IACKOUT#			22
23		GND		23
24				24
25				25
26				26
27				27
28				28
29				29
30				30
31	–12V		+12V	31
32	+5V	+5V	+5V	32

PM604 P2 Connector

Row A and Row B of the P2 connector are used to route the optional SCSI interface signals for rear-I/O. The pin assignments for P2 are as follows:

Table 4-14. P2 Connector Pin Assignments

	Row A	Row B	Row C	
1	SDB0#	+5V	SDBDIR0	1
2	SDB1#	GND	SDBDIR1	2
3	SDB2#		SDBDIR2	3
4	SDB3#		SDBDIR3	4
5	SDB4#		SDBDIR4	5
6	SDB5#		SDBDIR5	6
7	SDB6#		SDBDIR6	7
8	SDB7#		SDBDIR7	8
9	SDB8#		SDBDIR8	9
10	SDB9#		SDBDIR9	10
11	SDB10#		SDBDIR10	11
12	SDB11#	GND	SDBDIR11	12
13	SDB12#	+5V	SDBDIR12	13
14	SDB13#		SDBDIR13	14
15	SDB14#		SDBDIR14	15
16	SDB15#		SDBDIR15	16
17	SDBP0#		SDBPDIR	17
18	SDBP1#		SSELDIR	18
19	SIO#		SRSTDIR	19
20	SREQ#		SBSYDIR	20
21	SCD#		SIGS	21
22	SSEL#	GND	STGS	22
23	SMSG#		SDIFFSENSE	23
24	SRST#			24
25	SACK#			25
26	SBSY#			26
27	SATN#			27

Table 4-14. P2 Connector Pin Assignments (Continued)

28				28
29	ID0		ENR-	29
30	ID1		ENR+	30
31	ID2	GND	ENT-	31
32	ID3	+5V	ENT+	32

MVME712M-Compatible Versions

The following tables summarize the pin assignments of connectors that are specific to MVME3600 and 4600 series VMEmodules configured for use with MVME712M transition modules.

VMEbus Connector P2

Two 160-pin connectors (P1 and P2) supply the interface between the base board and the VMEbus. P1 provides power and VME signals for 24-bit addressing and 16-bit data. Its pin assignments are set by the VMEbus specification. P2 rows A, C, Z, and D provide power and interface signals to the MVME712M transition module. P2 row B supplies the MVME3600 and 4600 series VMEmodules with power, with the upper eight VMEbus address lines, and with an additional 16 VMEbus data lines. The pin assignments for P2 are listed in Table 4-15.

Table 4-15. VMEbus Connector P2 (MVME712M I/O Mode)

	Row Z	Row A	Row B	Row C	Row D	
1	SDB8*	SDB0*	+5V	C–	PMCIO0	1
2	GND	SDB1*	GND	C+	PMCIO1	2
3	SDB9*	SDB2*	RETRY*	T–	PMCIO2	3
4	GND	SDB3*	VA24	T+	PMCIO3	4
5	SDB10*	SDB4*	VA25	R–	PMCIO4	5
6	GND	SDB5*	VA26	R+	PMCIO5	6
7	SDB11*	SDB6*	VA27	+12VF	PMCIO6	7
8	GND	SDB7*	VA28	PR_STB*	PMCIO7	8
9	SDB12*	SDBP0	VA29	PR_DATA0	PMCIO8	9
10	GND	SATN*	VA30	PR_DATA1	PMCIO9	10
11	SDB13*	SBSY*	VA31	PR_DATA2	PMCIO10	11
12	GND	SACK*	GND	PR_DATA3	PMCIO11	12
13	SDB14*	SRST*	+5V	PR_DATA4	PMCIO12	13
14	GND	SMSG*	VD16	PR_DATA5	PMCIO13	14
15	SDB15*	SSEL*	VD17	PR_DATA6	PMCIO14	15
16	GND	SCD*	VD18	PR_DATA7	PMCIO15	16
17	SDBP1	SREQ*	VD19	PR_ACK*	PMCIO16	17
18	GND	SIO*	VD20	PR_BUSY	PMCIO17	18
19	Not Used	TxD3	VD21	PR_PE	PMCIO18	19
20	GND	RxD3	VD22	PR_SLCT	PMCIO19	20
21	Not Used	RTS3	VD23	PR_INIT*	PMCIO20	21
22	GND	CTS3	GND	PR_ERR*	PMCIO21	22
23	Not Used	DTR3	VD24	TxD1	PMCIO22	23
24	GND	DCD3	VD25	RxD1	PMCIO23	24
25	Not Used	TxD4	VD26	RTS1	PMCIO24	25
26	GND	RxD4	VD27	CTS1	PMCIO25	26
27	Not Used	RTS4	VD28	TxD2	PMCIO26	27
28	GND	TRxC4	VD29	RxD2	PMCIO27	28
29	PMCIO30	CTS4	VD30	RTS2	PMCIO28	29
30	GND	DTR4	VD31	CTS2	PMCIO29	30
31	PMCIO31	DCD4	GND	DTR2	GND	31
32	GND	RTxC4	+5V	DCD2	Not Used	32

SCSI Connector

The SCSI connector for the MVME3600 and 4600 series is a 50-pin connector located on the front panel of the MVME712M transition module. The pin assignments for the SCSI connector are listed in Table 4-16.

Table 4-16. SCSI Connector (MVME712M)

1	GND	DB00*	26
2	GND	DB01*	27
3	GND	DB02*	28
4	GND	DB03*	29
5	GND	DB04*	30
6	GND	DB05*	31
7	GND	DB06*	32
8	GND	DB07*	33
9	GND	DBP*	34
10	GND	GND	35
11	GND	GND	36
12	GND	GND	37
13	Reserved	TERMPWR	38
14	GND	GND	39
15	GND	GND	40
16	GND	ATN*	41
17	GND	GND	42
18	GND	BSY*	43
19	GND	ACK*	44
20	GND	RST*	45
21	GND	MSG*	46
22	GND	SEL*	47
23	GND	D/C*	48
24	GND	REQ*	49
25	GND	O/I*	50

Serial Ports 1-4

For the MVME3600 and 4600 series VMEmodule, the interface for asynchronous ports 1 and 2 and for synchronous/asynchronous ports 3 and 4 is implemented with four EIA-232-D DB-25 connectors (J7-J10) located on the front panel of the MVME712M transition module. The pin assignments for serial ports 1-4 on the MVME712M are listed in the following table (*n* = 1-4).

Table 4-17. Serial Connections–Ports 1-4 (MVME712M)

1	No Connection
2	ETXD*n*
3	ERXD*n*
4	ERTS*n*
5	ECTS*n*
6	EDSR*n*
7	GND
8	EDCD*n*
9	No Connection
10	No Connection
11	No Connection
12	No Connection
13	No Connection
14	No Connection
15	ERTXC (*Port 4 only*)
16	No Connection
17	ERRXC (*Port 4 only*)
18	No Connection
19	No Connection
20	EDTR*n*
21	No Connection
22	No Connection
23	No Connection
24	ETTXC (*Port 4 only*)
25	No Connection

Parallel Connector

Both versions of the base board provide parallel I/O connections. For MVME712M-compatible base boards, the parallel interface is implemented with a 36-pin Centronics-type socket connector located on the MVME712M transition module. The pin assignments are listed in the following table.

Table 4-18. Parallel I/O Connector (MVME712M)

1	PRSTB*	GND	19
2	PRD0	GND	20
3	PRD1	GND	21
4	PRD2	GND	22
5	PRD3	GND	23
6	PRD4	GND	24
7	PRD5	GND	25
8	PRD6	GND	26
9	PRD7	GND	27
10	PRACK*	GND	28
11	PRBSY	GND	29
12	PRPE	GND	30
13	PRSEL	INPRIME*	31
14	No Connection	PRFAULT*	32
15	No Connection	No Connection	33
16	GND	No Connection	34
17	No Connection	No Connection	35
18	No Connection	No Connection	36

Ethernet AUI Connector

The MVME3600 and 4600 series VMEmodule provides both AUI and 10BaseT/100BaseTX LAN connections. For MVME712M-compatible base boards, the LAN interface is an AUI connection implemented with a DB15 connector (J6) located on the MVME712M transition module. The pin assignments are listed in the following table.

Table 4-19. Ethernet AUI Connector (MVME712M)

1	GND
2	C+
3	T+
4	GND
5	R+
6	GND
7	No Connection
8	No Connection
9	C–
10	T–
11	No Connection
12	R–
13	+12VF
14	No Connection
15	No Connection

Note The +12VF supplied at pin 13 is fused on the base board.

MVME761-Compatible Versions

The following tables summarize the pin assignments of connectors that are specific to MVME3600 and 4600 series VMEmodules configured for use with MVME761 transition modules.

VMEbus Connector P2

Two 160-pin connectors (P1 and P2) supply the interface between the base board and the VMEbus. P1 provides power and VME signals for 24-bit addressing and 16-bit data. Its pin assignments are set by the VMEbus specification. P2 rows A, C, Z, and D provide power and interface signals to the MVME761 transition module. P2 row B supplies the MVME4600 with power, with the upper eight VMEbus address lines, and with an additional 16 VMEbus data lines. The pin assignments for P2 are listed in the following table.

Table 4-20. VMEbus Connector P2 (MVME761 I/O Mode)

	Row Z	Row A	Row B	Row C	Row D	
1	SDB8*	SDB0*	+5V	RD– (10/100)	PMCIO0	1
2	GND	SDB1*	GND	RD+ (10/100)	PMCIO1	2
3	SDB9*	SDB2*	RETRY*	TD– (10/100)	PMCIO2	3
4	GND	SDB3*	VA24	TD+ (10/100)	PMCIO3	4
5	SDB10*	SDB4*	VA25	Not Used	PMCIO4	5
6	GND	SDB5*	VA26	Not Used	PMCIO5	6
7	SDB11*	SDB6*	VA27	+12VF	PMCIO6	7
8	GND	SDB7*	VA28	PR_STB*	PMCIO7	8
9	SDB12*	SDBP0	VA29	PR_DATA0	PMCIO8	9
10	GND	SATN*	VA30	PR_DATA1	PMCIO9	10
11	SDB13*	SBSY*	VA31	PR_DATA2	PMCIO10	11
12	GND	SACK*	GND	PR_DATA3	PMCIO11	12
13	SDB14*	SRST*	+5V	PR_DATA4	PMCIO12	13
14	GND	SMSG*	VD16	PR_DATA5	PMCIO13	14
15	SDB15*	SSEL*	VD17	PR_DATA6	PMCIO14	15
16	GND	SCD*	VD18	PR_DATA7	PMCIO15	16
17	SDBP1	SREQ*	VD19	PR_ACK*	PMCIO16	17

Table 4-20. VMEbus Connector P2 (MVME761 I/O Mode) (Continued)

18	GND	SIO*	VD20	PR_BUSY	PMCIO17	18
19	Not Used	AFD*	VD21	PR_PE	PMCIO18	19
20	GND	SLIN*	VD22	PR_SLCT	PMCIO19	20
21	Not Used	TxD3	VD23	PR_INIT*	PMCIO20	21
22	GND	RxD3	GND	PR_ERR*	PMCIO21	22
23	Not Used	RTxC3	VD24	TxD1	PMCIO22	23
24	GND	TRxC3	VD25	RxD1	PMCIO23	24
25	Not Used	TxD3	VD26	RTS1	PMCIO24	25
26	GND	RxD3	VD27	CTS1	PMCIO25	26
27	Not Used	RTxC4	VD28	TxD2	PMCIO26	27
28	GND	TRxC4	VD29	RxD2	PMCIO27	28
29	PMCIO30	Not Used	VD30	RTS2	PMCIO28	29
30	GND	–12VF	VD31	CTS2	PMCIO29	30
31	PMCIO31	MSYNC*	GND	MD0	GND	31
32	GND	MCLK	+5V	MD1	VPC	32

Serial Ports 1 and 2

The MVME3600 and 4600 series VMEmodule provides both asynchronous (ports 1 and 2) and synchronous/asynchronous (ports 3 and 4) serial connections. For the MVME761-compatible versions of the base board, the asynchronous interface is implemented with a pair of DB-9 connectors (COM1 and COM2) located on the MVME761 transition module. The pin assignments are listed in the following table (*n* = 1 or 2).

Table 4-21. Serial Connections—Ports 1 and 2 (MVME761)

1	SP*n*DCD
2	SP*n*RxD
3	SP*n*TxD
4	SP*n*DTR
5	GND
6	SP*n*DSR
7	SP*n*RTS
8	SP*n*CTS
9	SP*n*RI

Serial Ports 3 and 4

For MVME761-compatible versions of the base board, the synchronous/asynchronous interface for ports 3 and 4 is implemented with a pair of HD-26 connectors (J7 and J8) located on the front panel of the transition module. The pin assignments for serial ports 3 and 4 are listed in the following table (*n* = 3 or 4).

Table 4-22. Serial Connections—Ports 3 and 4 (MVME761)

1	No Connection
2	TXD*n*
3	RXD*n*
4	RTS*n*
5	CTS*n*
6	DSR*n*

Table 4-22. Serial Connections—Ports 3 and 4 (MVME761)

7	GND
8	DCD*n*
9	SP*n*_P9
10	SP*n*_P10
11	SP*n*_P11
12	SP*n*_P12
13	SP*n*_P13
14	SP*n*_P14
15	TXCI*n*
16	SP*n*_P16
17	RXCI*n*
18	LLB*n*
19	SP*n*_P19
20	DTR*n*
21	RLB*n*
22	RI*n*
23	SP*n*_P23
24	TXCO*n*
25	TM*n*
26	No Connection

Parallel Connector

Both versions of the base board provide parallel I/O connections. For MVME761-compatible models, the parallel interface is implemented with an IEEE P1284 36-pin connector (J10) located on the MVME761 transition module. The pin assignments are listed in the following table.

Table 4-23. Parallel I/O Connector (MVME761)

1	PRBSY	GND	19
2	PRSEL	GND	20
3	PRACK*	GND	21
4	PRFAULT*	GND	22
5	PRPE	GND	23
6	PRD0	GND	24
7	PRD1	GND	25
8	PRD2	GND	26
9	PRD3	GND	27
10	PRD4	GND	28
11	PRD5	GND	29
12	PRD6	GND	30
13	PRD7	GND	31
14	INPRIME*	GND	32
15	PRSTB*	GND	33
16	SELIN*	GND	34
17	AUTOFD*	GND	35
18	Pull-up	No Connection	36

Ethernet 10BaseT/100BaseTX Connector

The MVME3600 and 4600 series VMEmodule provides both AUI and 10BaseT/100BaseTX LAN connections. For MVME761-compatible base boards, the LAN interface is a 10BaseT/100BaseTX connection implemented with a standard RJ-45 socket located on the MVME761 transition module. The pin assignments are listed in the following table.

Table 4-24. Ethernet 10BaseT/100BaseTX Connector (MVME761)

1	TD+
2	TD–
3	RD+
4	No Connection
5	No Connection
6	RD–
7	No Connection
8	No Connection

For detailed descriptions of the various interconnect signals, consult the support information documentation package for the MVME4600 series VMEmodule or the support information sections of the transition module documentation as necessary.

PPCBug Firmware 5

Overview

The PowerPC debugger, PPCBug, is a versatile tool for evaluating and debugging systems built around Motorola PowerPC microcomputers. Its primary uses are to test and initialize the system hardware, determine the hardware configuration, and boot the operating system. Facilities are also available for loading and executing user programs under complete operator control for system evaluation.

The PowerPC debugger provides a high degree of functionality and user friendliness, and yet stresses portability and ease of maintenance. It achieves good portability and comprehensibility because it was written entirely in the C programming language, except where necessary to use assembler functions.

PPCBug includes commands for display and modification of memory, breakpoint and tracing capabilities, a powerful assembler and disassembler useful for patching programs, and a “self-test at power-up” feature which verifies the integrity of the main CPU board. Various PPCBug routines that handle I/O, data conversion, and string functions are available to user programs through the System Call handler. PPCBug consists of three parts:

- A command-driven user-interactive software debugger. It is hereafter referred to as “the debugger” or “PPCBug.”
- A set of command-driven diagnostics, which is hereafter referred to as “the diagnostics.”
- A user interface which accepts commands from the system console terminal.

When using PPCBug, you operate from within either the debugger directory or the diagnostic directory. The debugger prompt (`PPC1-Bug` or `PPC1-Diag`) tells you the current directory.

Because PPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. When you enter a command, PPCBug executes the command and the prompt reappears. However, if you enter a command that causes execution of user target code (for example, **GO**), then control may or may not return to PPCBug, depending on the outcome of the user program. The flow of control in PPCBug is described in the *PPCBug Firmware Package User's Manual*, listed in Appendix D, *Related Documentation*.

PPCBug is similar to previous Motorola firmware debugging packages (for example, MVME147Bug, MVME167Bug, MVME187Bug), with differences due to microprocessor architectures. These are primarily reflected in the instruction mnemonics, register displays, addressing modes of the assembler/disassembler, and the passing of arguments to the system calls.

Memory Requirements

PPCBug requires a total of 768KB of read/write memory (that is, DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB ($04000000) of read/write memory will place the PPCBug memory page at locations $03F80000 to $03FFFFFF.

Implementation

PPCBug is written largely in the C programming language, providing benefits of portability and maintainability. Where necessary, assembly language has been used in the form of separately compiled program modules containing only assembler code. No mixed-language modules are used.

Physically, PPCBug is contained in two socketed 32-pin PLCC Flash devices that together provide 1MB of storage. The executable code is checksummed at every power-on or reset firmware entry, and the result (which includes a precalculated checksum contained in the Flash devices), is verified against the expected checksum.

Using the Debugger

PPCBug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `PPC1-Bug` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `PPC1-Diag` prompt appears on the screen, the debugger is ready to accept diagnostic commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the Return or Enter key. This allows you to correct entry errors, if necessary, with the control characters described in the *PPCBug Firmware Package User's Manual*.

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example **GO**) then control may or may not return to the debugger, depending on what the user program does. For example, if a breakpoint has been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine RETURN (described in the *PPCBug Firmware Package User's Manual*). For more about this, refer to the **GD**, **GO**, and **GT** command descriptions in the *PPCBug Firmware Package User's Manual*.

A debugger command is made up of the following parts:

- The command name, either uppercase or lowercase (for example, **MD** or **md**).
- Any required arguments, as specified by command.
- At least one space before the first argument. Precede all other arguments with either a space or comma.
- One or more options. Precede an option or a string of options with a semicolon (**;**). If no option is entered, the command's default option conditions are used.

Debugger Commands

The individual debugger commands are listed in the following table. The commands are described in detail in the *PPCBug Firmware Package User's Manual.*

Note You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax for a particular command by entering **HE** and the command mnemonic, as listed below.

Table 5-1. Debugger Commands

Command	Description
AS	One Line Assembler
BC	Block of Memory Compare
BF	Block of Memory Fill
BI	Block of Memory Initialize
BM	Block of Memory Move
BR	Breakpoint Insert
NOBR	Breakpoint Delete
BS	Block of Memory Search
BV	Block of Memory Verify
CM	Concurrent Mode
NOCM	No Concurrent Mode
CNFG	Configure Board Information Block
CS	Checksum
CSAR	PCI Configuration Space READ Access
CSAW	PCI Configuration Space WRITE Access
DC	Data Conversion
DMA	Block of Memory Move
DS	One Line Disassembler
DU	Dump S-Records

Table 5-1. Debugger Commands (Continued)

Command	Description
ECHO	Echo String
ENV	Set Environment
FORK	Fork Idle MPU at Address
FORKWR	Fork Idle MPU with Registers
GD	Go Direct (Ignore Breakpoints)
GEVBOOT	Global Environment Variable Boot
GEVDEL	Global Environment Variable Delete
GEVDUMP	Global Environment Variable(s) Dump
GEVEDIT	Global Environment Variable Edit
GEVINIT	Global Environment Variable Initialization
GEVSHOW	Global Environment Variable(s) Display
GN	Go to Next Instruction
GO	Go Execute User Program
GT	Go to Temporary Breakpoint
HE	Help
IDLE	Idle Master MPU
IOC	I/O Control for Disk
IOI	I/O Inquiry
IOP	I/O Physical (Direct Disk Access)
IOT	I/O Teach for Configuring Disk Controller
IRD	Idle MPU Register Display
IRM	Idle MPU Register Modify
IRS	Idle MPU Register Set
LO	Load S-Records from Host
MA	Macro Define/Display
NOMA	Macro Delete
MAE	Macro Edit
MAL	Enable Macro Listing
NOMAL	Disable Macro Listing

Table 5-1. Debugger Commands (Continued)

Command	Description
MAR	Load Macros
MAW	Save Macros
MD, MDS	Memory Display
MENU	System Menu
MM	Memory Modify
MMD	Memory Map Diagnostic
MS	Memory Set
MW	Memory Write
NAB	Automatic Network Boot
NAP	Nap MPU
NBH	Network Boot Operating System, Halt
NBO	Network Boot Operating System
NIOC	Network I/O Control
NIOP	Network I/O Physical
NIOT	Network I/O Teach (Configuration)
NPING	Network Ping
OF	Offset Registers Display/Modify
PA	Printer Attach
NOPA	Printer Detach
PBOOT	Bootstrap Operating System
PF	Port Format
NOPF	Port Detach
PFLASH	Program Flash Memory
PS	Put RTC into Power Save Mode
RB	ROMboot Enable
NORB	ROMboot Disable
RD	Register Display
REMOTE	Remote
RESET	Cold/Warm Reset

Table 5-1. Debugger Commands (Continued)

Command	Description
RL	Read Loop
RM	Register Modify
RS	Register Set
RUN	MPU Execution/Status
SD	Switch Directories
SET	Set Time and Date
SROM	SROM Examine/Modify
SYM	Symbol Table Attach
NOSYM	Symbol Table Detach
SYMS	Symbol Table Display/Search
T	Trace
TA	Terminal Attach
TIME	Display Time and Date
TM	Transparent Mode
TT	Trace to Temporary Breakpoint
VE	Verify S-Records Against Memory
VER	Revision/Version Display
WL	Write Loop

Caution Although a command to allow the erasing and reprogramming of Flash memory is available to you, keep in mind that reprogramming any portion of Flash memory will erase everything currently contained in Flash, including the PPC1Bug debugger.

Note Flash banks A and B both contain the PPCBug debugger.

Diagnostic Tests

The individual diagnostic test sets are listed in the following table. The diagnostics are described in the *PPCBug Diagnostics Manual*.

Table 5-2. Diagnostic Test Groups

Test Set	Description	Applicability
DEC21x40	DEC 21x40 Ethernet Controller Chip Tests	All boards
Falcon	Falcon ECC Memory Controller Tests	All boards *
ISABRDGE	PCI/ISA Bridge Tests	All boards
KBD8730x	PC8730x Keyboard/Mouse Tests	All boards
L2CACHE	Level 2 Cache Tests	All boards with L2 cache
MPIC	Multiprocessor Interrupt Controller Tests	All boards *
NCR	NCR 53C825/53C810 SCSI-2 I/O Processor Tests	All boards
NVRAM	Nonvolatile RAM tests	All boards
PAR8730x	PC8730x Parallel Port Test	All boards
PCIBUS	Generic PCI/PMC Slot Test	All boards
RAM	Random Access Memory Tests	All boards
Raven	Raven PCI Bridge Tests	All boards *
RTC	Real-Time Clock Tests	All boards
SCC	Serial Communications Controller Tests	All boards
UART	PC16550 (or PC87308) UART Tests	All boards
Universe	VMEbus to PCI Interface ASIC Tests	All boards *
VGA543x	Video Graphics Tests	All MVME3600/4600 boards; not applicable to MVME2600 series boards
Z8536	Z8536 Counter/Timer Tests	All boards

Notes

1. Some diagnostics depend on restart defaults that are set up only in a particular restart mode. Refer to the documentation on a particular diagnostic for the correct mode.

2. Test Sets marked with an asterisk (*) are not available on PPCBug Release 3.1 and earlier.

CNFG and ENV Commands

6

Overview

You can use the factory-installed debug monitor, PPCBug, to modify certain parameters contained in the PowerPC board's Non-Volatile RAM (NVRAM), also known as Battery Backed-up RAM (BBRAM).

- The Board Information Block in NVRAM contains various elements relating to the operating parameters of the hardware itself. Use the PPCBug command **CNFG** to change those parameters.
- Use the PPCBug command **ENV** to change configurable PPCBug parameters in NVRAM.

The **CNFG** and **ENV** commands are both described in the *PPCBug Firmware Package User's Manual* (listed in Appendix D, *Related Documentation*). Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **CNFG** and **ENV** that is specific to the debugger, along with the PPCBug parameters that can be configured with the **ENV** command.

CNFG – Configure Board Information Block

Use this command to display and configure the Board Information Block, which is resident within the NVRAM. The board information block contains various elements that correspond to specific operational parameters of the PowerPC board. The board structure for the PowerPC board is as shown in the following example for an MVME4600:

```
Board (PWA) Serial Number     = “MOT001673590   ”
Board Identifier              = “MVME4600       ”
Artwork (PWA) Identifier      = “01-w3170F02A   ”
MPU Clock Speed               = “167            ”
Bus Clock Speed               = “067            ”
Ethernet Address              = 08003E20C983
Local SCSI Identifier         = “07”
System Serial Number          = “1463725        ”
System Identifier             = “Motorola MVME4600”
License Identifier            = “12345678 “
```

The parameters that are quoted are left-justified character (ASCII) strings padded with space characters, and the quotes (“) are displayed to indicate the size of the string. Parameters that are not quoted are considered data strings, and data strings are right-justified. The data strings are padded with zeroes if the length is not met.

The Board Information Block is factory-configured before shipment. There is no need to modify block parameters unless the NVRAM is corrupted.

Refer to the *Programmer’s Reference Guide* (listed in Appendix D, *Related Documentation*) for the actual location and other information about the Board Information Block.

Refer to the *PPCBug Firmware Package User's Manual* (listed in Appendix D, *Related Documentation*) for a description of **CNFG** and examples.

ENV – Set Environment

Use the **ENV** command to view and/or configure interactively all PPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PPCBug Firmware Package User's Manual* for a description of the use of **ENV**. Additional information on registers in the Universe ASIC that affect these parameters can be found in the *Programmer's Reference Guide* for your PowerPC board.

Listed and described below are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

Configuring the PPCBug Parameters

The parameters that can be configured using **ENV** are:

```
Bug or System environment [B/S] = B?
```

B Bug is the mode where no system type of support is displayed. However, system-related items are still available. (Default)

S System is the standard mode of operation, and is the default mode if NVRAM should fail. System mode is defined in the *PPCBug Firmware Package User's Manual*.

```
Field Service Menu Enable [Y/N] = N?
```

Y Display the field service menu.

N Do not display the field service menu.(Default)

```
Remote Start Method Switch [G/M/B/N] = B?
```

The Remote Start Method Switch is used when the MVME2600/ MVME3600/MVME4600 is cross-loaded from another VME-based CPU, to start execution of the cross-loaded program.

G Use the Global Control and Status Register on the Universe chip to pass and start execution of the cross-loaded program. (*Not applicable to MVME4600 boards*.)

M Use the Multiprocessor Control Register (MPCR) in shared RAM to pass and start execution of the cross-loaded program.

B Use both the GCSR and the MPCR methods to pass and start execution of the cross-loaded program. (Default)

N Do not use any Remote Start Method.

```
Probe System for Supported I/O Controllers [Y/N] = N?
```

Y Accesses will be made to the appropriate system buses (for example, VMEbus, local MPU bus) to determine the presence of supported controllers. (Default)

N Accesses will not be made to the VMEbus to determine the presence of supported controllers.

```
Auto-Initialize of NVRAM Header Enable [Y/N] = Y?
```

Y NVRAM (PReP partition) header space will be initialized automatically during board initialization, but only if the PREP partition fails a sanity check. (Default)

N NVRAM header space will not be initialized automatically during board initialization.

```
Network PReP-Boot Mode Enable [Y/N] = N?
```

Y Enable PReP-style network booting (same boot image from a network interface as from a mass storage device).

N Do not enable PReP-style network booting. (Default)

```
Negate VMEbus SYSFAIL* Always [Y/N] = N?
```

Y Negate the VMEbus SYSFAIL* signal during board initialization.

N Negate the VMEbus SYSFAIL* signal after successful completion or entrance into the bug command monitor. (Default)

```
Local SCSI Bus Reset on Debugger Startup [Y/N] = N?
```

Y Local SCSI bus is reset on debugger setup.

N Local SCSI bus is not reset on debugger setup. Default)

```
Local SCSI Bus Negotiations Type [A/S/N] = A?
```

A Asynchronous SCSI bus negotiation. (Default)

S Synchronous SCSI bus negotiation.

N None.

```
Local SCSI Data Bus Width [W/N] = N?
```

W Wide SCSI (16-bit bus).

N Narrow SCSI (8-bit bus). (Default)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Enable [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* global environment variable (GEV).

N Do not give boot priority to devices listed in the *fw-boot-path* GEV. (Default)

Note When enabled, the GEV (Global Environment Variable) boot takes priority over all other boots, including Autoboot and Network Boot.


```
NVRAM Bootlist (GEV.fw-boot-path) Boot at power-up only [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* GEV at power-up reset only.

N Give power-up boot priority to devices listed in the *fw-boot-path* GEV at any reset. (Default)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Abort Delay = 5?
```

The time in seconds that a boot from the NVRAM boot list will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the <**Break**> key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Auto Boot Enable [Y/N] = N?
```

Y The Autoboot function is enabled.

N The Autoboot function is disabled.(Default)

```
Auto Boot at power-up only [Y/N] = N?
```

Y Autoboot is attempted at power-up reset only.

N Autoboot is attempted at any reset.(Default)

```
Auto Boot Scan Enable [Y/N] = Y?
```

Y If Autoboot is enabled, the Autoboot process attempts to boot from devices specified in the scan list (for example, FDISK/CDROM/TAPE/HDISK). (Default)

N If Autoboot is enabled, the Autoboot process uses the Controller LUN and Device LUN to boot.

```
Auto Boot Scan Device Type List = FDISK/CDROM/TAPE/HDISK?
```

The listing of boot devices displayed if the Autoboot Scan option is enabled. If you modify the list, follow the format shown above (uppercase letters, using forward slash as separator).

```
Auto Boot Controller LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Auto Boot Device LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape devices currently supported by PPCBug. (Default = $00)

```
Auto Boot Partition Number = 00?
```

Which disk "partition" is to be booted, as specified in the PowerPC Reference Platform (PRP) specification. If set to zero, the firmware will search the partitions in order (1, 2, 3, 4) until it finds the first "bootable" partition. That is then the partition that will be booted. Other acceptable values are 1, 2, 3, or 4. In these four cases, the partition specified will be booted without searching.

```
Auto Boot Abort Delay = 7?
```

The time in seconds that the Autoboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the <**Break**> key. The time value is from 0-255 seconds. (Default = 7 seconds)

```
Auto Boot Default String [NULL for an empty string] =?
```

You may specify a string (filename) which is passed on to the code being booted. The maximum length of this string is 16 characters. (Default = null string)


```
ROM Boot Enable [Y/N] = N?
```

Y The ROMboot function is enabled.

N The ROMboot function is disabled. (Default)

```
ROM Boot at power-up only [Y/N] = Y?
```

Y ROMboot is attempted at power-up only. (Default)

N ROMboot is attempted at any reset.

```
ROM Boot Enable search of VMEbus [Y/N] = N?
```

Y VMEbus address space, in addition to the usual areas of memory, will be searched for a ROMboot module.

N VMEbus address space will not be accessed by ROMboot. (Default)

```
ROM Boot Abort Delay = 5?
```

The time in seconds that the ROMboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the <**Break**> key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
ROM Boot Direct Starting Address = FFF00000?
```

The first location tested when PPCBug searches for a ROMboot module. (Default = $FFF00000)

```
ROM Boot Direct Ending Address = FFFFFFFC?
```

The last location tested when PPCBug searches for a ROMboot module. (Default = $FFFFFFFC)

```
Network Auto Boot Enable [Y/N] = N?
```

Y	The Network Auto Boot (NETboot) function is enabled.
N	The NETboot function is disabled. (Default)

```
Network Auto Boot at power-up only [Y/N] = N?
```

Y	NETboot is attempted at power-up reset only.
N	NETboot is attempted at any reset. (Default)

```
Network Auto Boot Controller LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Device LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Abort Delay = 5?
```

The time in seconds that the NETboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the <**Break**> key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Network Auto Boot Configuration Parameters Offset (NVRAM) =
00001000?
```

The address where the network interface configuration parameters are to be saved/retained in NVRAM; these parameters are the necessary parameters to perform an unattended network boot. A typical offset might be $1000, but this value is application-specific.
(Default = $00001000)

If you use the **NIOT** debugger command, these parameters need to be saved somewhere in the offset range $00000000 through $00000FFF. The **NIOT** parameters do not exceed 128 bytes in size. The setting of this **ENV** pointer determines their location. If you have used the same space for your own program information or commands, they will be overwritten and lost.

You can relocate the network interface configuration parameters in this space by using the **ENV** command to change the Network Auto Boot Configuration Parameters offset from its default of $00001000 to the value you need to be clear of your data within NVRAM.


```
Memory Size Enable [Y/N] = Y?
```

Y	Memory will be sized for Self Test diagnostics. (Default)
N	Memory will not be sized for Self Test diagnostics.

```
Memory Size Starting Address = 00000000?
```

The default Starting Address is $00000000.

```
Memory Size Ending Address = 02000000?
```

The default Ending Address is the calculated size of local memory. If the memory start is changed from $00000000, this value will also need to be adjusted.

```
DRAM Speed in NANO Seconds = 60?
```

The default setting for this parameter will vary depending on the speed of the DRAM memory parts installed on the board. The default is set to the slowest speed found on the available banks of DRAM memory.

```
ROM First Access Length (0 - 31) = 10?
```

This is the value programmed into the MPC105 “ROMFAL” field (Memory Control Configuration Register 8: bits 23-27) to indicate the number of clock cycles used in accessing the ROM. The lowest allowable ROMFAL setting is $00; the highest allowable is $1F. The value to enter depends on processor speed. The default value varies according to the system’s bus clock speed.

Note ROM First Access Length is not applicable to the MVME2600/3600/4600. PPCBUG ignores the configured value.


```
ROM Next Access Length (0 - 15) = 0?
```

The value programmed into the MPC105 “ROMNAL” field (Memory Control Configuration Register 8: bits 28-31) to represent wait states in access time for nibble (or burst) mode ROM accesses. The lowest allowable ROMNAL setting is $0; the highest allowable is $F. The value to enter depends on processor speed. The default value varies according to the system’s bus clock speed.

Note ROM Next Access Length is not applicable to the MVME2600/MVME3600/MVME4600. PPCBUG ignores the configured value

```
DRAM Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O	DRAM parity is enabled upon detection. (Default)
A	DRAM parity is always enabled.
N	DRAM parity is never enabled.

Note This parameter also applies to enabling ECC for DRAM.

```
L2 Cache Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O L2 Cache parity is enabled upon detection. (Default)

A L2 Cache parity is always enabled.

N L2 Cache parity is never enabled.

```
PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?
```

Initializes the PIRQx (PCI Interrupts) route control registers in the IBC (PCI/ISA bus bridge controller). The **ENV** parameter is a 32-bit value that is divided by 4 to yield the values for route control registers PIRQ0/1/2/3. The default is determined by system type. For details on PCI/ISA interrupt assignments and for suggested values to enter for this parameter, refer to the *8259 Interrupts* section in the *MVME3600/4600 Series Programmer's Reference Guide*.

Configuring the VMEbus Interface

ENV asks the following series of questions to set up the VMEbus interface for MVME2600/MVME3600/MVME4600 series VMEmodules. To perform this configuration, you should have a working knowledge of the Universe ASIC as described in the *Programmer's Reference Guide*.

```
VME3PCI Master Master Enable [Y/N] = Y?
```

Y Set up and enable the VMEbus Interface (Default)

N Do not set up or enable the VMEbus Interface.

```
PCI Slave Image 0 Control = 00000000?
```

The configured value is written into the LSI0_CTL register of the Universe chip.

```
PCI Slave Image 0 Base Address Register = 00000000?
```

The configured value is written into the LSI0_BS register of the Universe chip.

```
PCI Slave Image 0 Bound Address Register = 00000000?
```

The configured value is written into the LSI0_BD register of the Universe chip.

```
PCI Slave Image 0 Translation Offset = 00000000?
```

The configured value is written into the LSI0_TO register of the Universe chip.

```
PCI Slave Image 1 Control = C0820000?
```

The configured value is written into the LSI1_CTL register of the Universe chip.

```
PCI Slave Image 1 Base Address Register = 01000000?
```

The configured value is written into the LSI1_BS register of the Universe chip.

```
PCI Slave Image 1 Bound Address Register = 20000000?
```

The configured value is written into the LSI1_BD register of the Universe chip.

```
PCI Slave Image 1 Translation Offset = 00000000?
```

The configured value is written into the LSI1_TO register of the Universe chip.

```
PCI Slave Image 2 Control = C0410000?
```

The configured value is written into the LSI2_CTL register of the Universe chip.

```
PCI Slave Image 2 Base Address Register = 20000000?
```

The configured value is written into the LSI2_BS register of the Universe chip.

```
PCI Slave Image 2 Bound Address Register = 22000000?
```

The configured value is written into the LSI2_BD register of the Universe chip.

```
PCI Slave Image 2 Translation Offset = D0000000?
```

The configured value is written into the LSI2_TO register of the Universe chip.

```
PCI Slave Image 3 Control = C0400000?
```

The configured value is written into the LSI3_CTL register of the Universe chip.

```
PCI Slave Image 3 Base Address Register = 2FFF0000?
```

The configured value is written into the LSI3_BS register of the Universe chip.

```
PCI Slave Image 3 Bound Address Register = 30000000?
```

The configured value is written into the LSI3_BD register of the Universe chip.


```
PCI Slave Image 3 Translation Offset = D0000000?
```

The configured value is written into the LSI3_TO register of the Universe chip.

```
VMEbus Slave Image 0 Control = E0F20000?
```

The configured value is written into the VSI0_CTL register of the Universe chip.

```
VMEbus Slave Image 0 Base Address Register = 00000000?
```

The configured value is written into the VSI0_BS register of the Universe chip.

```
VMEbus Slave Image 0 Bound Address Register = (Local DRAM Size)?
```

The configured value is written into the VSI0_BD register of the Universe chip. The value is the same as the Local Memory Found number already displayed.

```
VMEbus Slave Image 0 Translation Offset = 80000000?
```

The configured value is written into the VSI0_TO register of the Universe chip.

```
VMEbus Slave Image 1 Control = 00000000?
```

The configured value is written into the VSI1_CTL register of the Universe chip.

```
VMEbus Slave Image 1 Base Address Register = 00000000?
```

The configured value is written into the VSI1_BS register of the Universe chip.

```
VMEbus Slave Image 1 Bound Address Register = 00000000?
```

The configured value is written into the VSI1_BD register of the Universe chip.

```
VMEbus Slave Image 1 Translation Offset = 00000000?
```

The configured value is written into the VSI1_TO register of the Universe chip.

```
VMEbus Slave Image 2 Control = 00000000?
```

The configured value is written into the VSI2_CTL register of the Universe chip.

```
VMEbus Slave Image 2 Base Address Register = 00000000?
```

The configured value is written into the VSI2_BS register of the Universe chip.

```
VMEbus Slave Image 2 Bound Address Register = 00000000?
```

The configured value is written into the VSI2_BD register of the Universe chip.

```
VMEbus Slave Image 2 Translation Offset = 00000000?
```

The configured value is written into the VSI2_TO register of the Universe chip.

```
VMEbus Slave Image 3 Control = 00000000?
```

The configured value is written into the VSI3_CTL register of the Universe chip.

```
VMEbus Slave Image 3 Base Address Register = 00000000?
```

The configured value is written into the VSI3_BS register of the Universe chip.

```
VMEbus Slave Image 3 Bound Address Register = 00000000?
```

The configured value is written into the VSI3_BD register of the Universe chip.

```
VMEbus Slave Image 3 Translation Offset = 00000000?
```

The configured value is written into the VSI3_TO register of the Universe chip.

```
PCI Miscellaneous Register = 10000000?
```

The configured value is written into the LMISC register of the Universe chip.

```
Special PCI Slave Image Register = 00000000?
```

The configured value is written into the SLSI register of the Universe chip.


```
Master Control Register = 80C00000?
```

The configured value is written into the MAST_CTL register of the Universe chip.

```
Miscellaneous Control Register = 52060000?
```

The configured value is written into the MISC_CTL register of the Universe chip.

```
User AM Codes = 00000000?
```

The configured value is written into the USER_AM register of the Universe chip.

Specifications

Table A-1 lists the general specifications for MVME3600 and 4600 series VMEmodules. Subsequent sections detail cooling requirements and FCC compliance.

A complete functional description of the MVME3600/4600 series VMEmodules appears in Chapter 3, *Functional Description*. Specifications for the optional PCI mezzanines can be found in the documentation for those modules.

Table A-1. MVME3600/4600 Series Specifications

Characteristics	Specifications
Power requirements (Excluding transition module, keyboard, mouse)	+5V DC (±5%), 12 A typ., 15 A max. (with two MPC604 processors) +12V DC (±5%), 100 mA typ., 250 mA max. –12V DC (±5%), 100 mA typ., 250 mA max.
Operating temperature	0° C to 55° C (32° to 131° F) entry air with forced-air cooling (refer to *Cooling Requirements*)
Storage temperature	–40° C to +85° C (–40° to 185° F)
Relative humidity	5% to 90% (non-condensing)
Physical dimensions (Board only) Height Depth (Board with front panel and connectors) Height Depth Front panel width	Double-high VMEboard (base board or processor/memory mezzanine) 9.2 in. (233 mm) 6.3 in. (160 mm) 10.3 in. (262 mm) 7.4 in. (188 mm) 0.8 in. (20 mm) each board; 1.6 in. (40 mm) overall

Cooling Requirements

The Motorola MVME3600 and 4600 series family of VME Processor Modules is specified, designed, and tested to operate reliably with an incoming air temperature range from 0° to 55° C (32° to 131° F) with forced air cooling of the entire assembly (base board and modules) at a velocity typically achievable by using a 100 CFM axial fan. Temperature qualification is performed in a standard Motorola VMEsystem chassis. Twenty-five-watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 100 CFM per fan, is placed directly under the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors' specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55° C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

EMC Compliance

The MVME3600 and 4600 series VME Processor Module was tested in an EMC-compliant chassis and meets the requirements for EN55022 Class B equipment. EMC compliance was achieved under the following conditions:

- Shielded cables on all external I/O ports.
- Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

Serial Interconnections B

Introduction

As described in previous chapters of this manual, the serial communications interface on the MVME3600 and 4600 series VMEmodule has four ports. Two of them are combined synchronous/ asynchronous ports; the other two are asynchronous only. Both synchronous and asynchronous ports support various types of DCE/DTE serial interfaces via P2 and the MVME712M or MVME761 transition module.

Asynchronous Serial Ports

The MVME3600 and 4600 series VMEmodule uses a PC87308 ISASIO chip from National Semiconductor to implement the two asynchronous serial ports (in addition to the disk drive controller, parallel I/O, and keyboard/mouse interface).

The asynchronous ports provided by the ISASIO device are routed through P2 and the associated transition module. The TTL-level signals from the ISASIO chip are buffered through TTL drivers and series resistors, then routed through EIA-232-D drivers and receivers to complete the asynchronous serial interface enroute to the MVME712M or MVME761 transition module.

The MVME3600 and 4600 series hardware supports asynchronous serial baud rates of 110B/s to 38.4KB/s. For detailed programming information, refer to the PCI and ISA bus discussions in the *MVME3600/4600 Series Programmer's Reference Guide*, listed in *Appendix D, Related Documentation*, and to the vendor documentation for the ISASIO device.

Synchronous Serial Ports

The MVME3600 and 4600 series VMEmodule uses a Zilog Z85230 ESCC (Enhanced Serial Communications Controller) with a 10 MHz clock to implement the two synchronous/asynchronous serial communications ports, which are routed through P2 to the transition module. The Z85230 handles both synchronous (SDLC/HDLC) and asynchronous protocols. The hardware supports asynchronous serial baud rates of 110B/s to 38.4KB/s and synchronous baud rates of up to 2.5MB/s.

Each port supports the CTS, DCD, RTS, and DTR control signals, as well as the TxD and RxD transmit/receive data signals and TxC/RxC synchronous clock signals. Since not all modem control lines are available in the Z85230, a Z8536 CIO device is used to furnish the missing modem lines.

EIA-232-D Connections

The EIA-232-D standard defines the electrical and mechanical aspects of this serial interface. The interface employs unbalanced (single-ended) signaling and is generally used with DB-25 connectors, although other connector styles (for example, DB-9 and RJ-45) are sometimes used as well.

Table B-1 lists the standard EIA-232-D interconnections. Not all pins listed in the table are necessary in every application.

To interpret the information correctly, remember that the EIA-232-D serial interface was developed to connect a terminal to a modem. Serial data leaves the sending device on a Transmit Data (TxD) line and arrives at the receiving device on a Receive Data (RxD) line. When computing equipment is interconnected without modems, one of the units must be configured as a terminal (data terminal equipment: DTE) and the other as

a modem (data circuit-terminating equipment: DCE). Since computers are normally configured to work with terminals, they are said to be configured as a modem in most cases.

Table B-1. EIA-232-D Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1		Not used.
2	TxD	**Transmit Data**. Data to be transmitted; input to modem from terminal.
3	RxD	**Receive Data**. Data which is demodulated from the receive line; output from modem to terminal.
4	RTS	**Request To Send**. Input to modem from terminal when required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
5	CTS	**Clear To Send**. Output from modem to terminal to indicate that message transmission can begin. When a modem is used, CTS follows the off-to-on transition of RTS after a time delay.
6	DSR	**Data Set Ready**. Output from modem to terminal to indicate that the modem is ready to send or receive data.
7	SG	**Signal Ground**. Common return line for all signals at the modem interface.
8	DCD	**Data Carrier Detect**. Output from modem to terminal to indicate that a valid carrier is being received.
9-14		Not used.
15	TxC	**Transmit Clock** (DCE). Output from modem to terminal; clocks data from the terminal to the modem.
16		Not used.
17	RxC	**Receive Clock**. Output from terminal to modem; clocks input data from the terminal to the modem.
18, 19		Not used.
20	DTR	**Data Terminal Ready**. Input to modem from terminal; indicates that the terminal is ready to send or receive data.
21		Not used.

Table B-1. EIA-232-D Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Name and Description
22	RI	**Ring Indicator**. Output from modem to terminal; indicates that an incoming call is present. The terminal causes the modem to answer the phone by carrying DTR true while RI is active.
23		Not used.
24	TxC	**Transmit Clock** (DTE). Input to modem from terminal; same function as TxC on pin 15.
25	BSY	**Busy**. Input to modem from terminal; a positive EIA signal applied to this pin causes the modem to go off-hook and make the associated phone busy.

Notes

1. A high EIA-232-D signal level is +3 to +15 volts. A low level is –3 to –15 volts. Connecting units in parallel may produce out-of-range voltages and is contrary to specifications.
2. The EIA-232-D interface is intended to connect a terminal to a modem. When computers are connected without modems, one computer must be configured as a modem and the other as a terminal.

Interface Characteristics

The EIA-232-D interface standard specifies all parameters for serial binary data interchange between DTE and DCE devices using unbalanced lines. EIA-232-D transmitter and receiver parameters applicable to MVME4600 series hardware are listed in the following tables.

Table B-2. EIA-232-D Interface Transmitter Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Output voltage (with load resistance of 3000Ω to 7000Ω)	±8.5		V
Open circuit output voltage		±12	V
Short circuit output current (to ground or any other interconnection cable conductor)		±100	mA
Power-off output resistance	300		W
Output transition time (for a transition region of –3V to +3V and with total load capacitance, including connection cable, of less than 2500pF)		2	µs
Open circuit slew rate		30	V/µs

The MVME3600 and 4600 series VMEmodule conforms to EIA-232-D specifications. Note that although the EIA-232-D standard recommends the use of short interconnection cables not more than 50 feet (15m) in length, longer cables are permissible provided the total load capacitance measured at the interface point and including signal terminator does not exceed 2500pF.

B

Table B-3. EIA-232-D Interface Receiver Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Input signal voltage		±25	V
Input high threshold voltage		2.25	V
Input low threshold voltage	0.75		V
Input hysteresis	1.0		V
Input impedance ($-15V < V_{in} < +15V$)	3000	7000	W

EIA-530 Connections

The EIA-530 interface complements the EIA-232-D interface in function. The EIA-530 standard defines the mechanical aspects of this interface, which is used for transmission of serial binary data, both synchronous and asynchronous. It is adaptable to balanced (double-ended) as well as unbalanced (single-ended) signaling and offers the possibility of higher data rates than EIA-232-D with the same DB-25 connector.

Table B-4 lists the EIA-530 interconnections that are available at MVME761 serial ports 3 and 4 (J7 and J8 on the board surface) when those ports are configured via serial interface modules as EIA-530 DCE or DTE ports.

Table B-4. MVME761 EIA-530 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1		Not used.
2	TxD_A	**Transmit Data (A).** Data to be transmitted; output from DTE to DCE.
3	RxD_A	**Receive Data (A).** Data which is demodulated from the receive line; input from DCE to DTE.
4	RTS_A	**Request to Send (A).** Output from DTE to DCE when required to transmit a message.

Table B-4. MVME761 EIA-530 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Name and Description
5	CTS_A	**Clear to Send (A).** Input to DTE from DCE to indicate that message transmission can begin.
6	DSR_A	**Data Set Ready (A).** Input to DTE from DCE to indicate that the DCE is ready to send or receive data. In DCE configuration, always true.
7	SG	**Signal Ground.** Common return line for all signals.
8	DCD_A	**Data Carrier Detect (A)**. Receive line signal detector output from DCE to DTE to indicate that valid data is being transferred to the DTE on the RxD line.
9	RxC_B	**Receive Signal Element Timing—DCE (B).** Control signal that clocks input data.
10	DCD_B	**Data Carrier Detect (B).** Receive line signal detector output from DCE to DTE to indicate that valid data is being transferred to the DTE on the RxD line.
11	TxCO_B	**Transmit Signal Element Timing—DTE (B).** Control signal that clocks output data.
12	TxC_B	**Transmit Signal Element Timing—DCE (B).** Control signal that clocks input data.
13	CTS_B	**Clear to Send (B).** Input to DTE from DCE to indicate that message transmission can begin.
14	TxD_B	**Transmit Data (B).** Data to be transmitted; output from DTE to DCE.
15	TxC_A	**Transmit Signal Element Timing—DCE (A).** Control signal that clocks input data.
16	RxD_B	**Receive Data (B).** Data which is demodulated from the receive line; input from DCE to DTE.
17	RxC_A	**Receive Signal Element Timing—DCE (A).** Control signal that clocks input data.
18	LL_B	**Local Loopback (A).** Reroutes signal within local DCE. In DTE configuration, always tied inactive and driven false. In DCE configuration, ignored
19	RTS_B	**Request to Send (B).** Output from DTE to DCE when required to transmit a message.

Table B-4. MVME761 EIA-530 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Name and Description
20	DTR_A	**Data Terminal Ready (A).** Output from DTE to DCE indicating that the DTE is ready to send or receive data.
21	RL_A	**Remote Loopback (A).** Reroutes signal within remote DCE. In DTE configuration, always tied inactive and driven false. In DCE configuration, ignored.
22	DSR_B	**Data Set Ready (B).** Input to DTE from DCE to indicate that the DCE is ready to send or receive data. In DCE configuration, always true.
23	DTR_B	**Data Terminal Ready (B).** Output from DTE to DCE indicating that the DTE is ready to send or receive data.
24	TxCO_A	**Transmit Signal Element Timing—DTE (A).** Control signal that clocks output data.
25	TM_A	**Test Mode (A).** Indicates whether the local DCE is under test. In DTE configuration, ignored. In DCE configuration, always tied inactive and driven false.

Interface Characteristics

In specifying parameters for serial binary data interchange between DTE and DCE devices, the EIA-530 standard assumes the use of balanced lines, except for the Remote Loopback, Local Loopback, and Test Mode lines, which are single-ended. Balanced-line data interchange is generally employed in preference to unbalanced-line data interchange where any of the following conditions prevail:

- The interconnection cable is too long for effective unbalanced operation.
- The interconnection cable is exposed to extraneous noise sources that may cause an unwanted voltage in excess of ±1V measured differentially between the signal conductor and circuit ground at the load end of the cable, with a 50Ω resistor substituted for the transmitter.
- It is necessary to minimize interference with other signals.

- Inversion of signals may be required (for example, plus polarity MARK to minus polarity MARK may be achieved by inverting the cable pair).

EIA-530 interface transmitter and receiver parameters applicable to MVME3600 and 4600 series hardware are listed in the following tables.

Table B-5. EIA-530 Interface Transmitter Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Differential output voltage (absolute, with 100Ω load)	2.0		V
Open circuit differential voltage output (absolute)		6.0	V
Output offset voltage (with 100Ω load)	2.0		V
Short circuit output current (for any voltage between –7V and +7V)		±180	mA
Power off output current (for any voltage between –7V and +7V)		±100	µA
Output transition time (with 100Ω, 15pF load)		15	ns

Table B-6. EIA-530 Interface Receiver Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Differential input voltage		±12	V
Input offset voltage		±12	V
Differential input high threshold voltage		200	mV
Differential input low threshold voltage		–200	V
Input hysteresis	1.0		V
Input impedance (–15V < V_{in} < +15V)	3000	7000	W

B

Proper Grounding

An important subject to consider is the use of ground pins. There are two pins labeled GND. Pin 7 is the *signal ground* and must be connected to the distant device to complete the circuit. Pin 1 is the *chassis ground*, but it must be used with care. The chassis is connected to the power ground through the green wire in the power cord and must be connected to be in compliance with the electrical code.

The problem is that when units are connected to different electrical outlets, there may be several volts of difference in ground potential. If pin 1 of each device is interconnected with the others via cable, several amperes of current could result. This condition may not only be dangerous for the small wires in a typical cable, but may also produce electrical noise that causes errors in data transmission. That is why Table B-1 and Table B-4 show no connection for pin 1. Normally, pin 7 (*signal ground*) should only be connected to the *chassis ground* at one point; if several terminals are used with one computer, the logical place for that point is at the computer. The terminals should not have a connection between the logic ground return and the chassis.

Troubleshooting CPU Boards

C

Solving Startup Problems

In the event of difficulty with your CPU board, try the simple troubleshooting steps on the following pages before calling for help or sending the board back for repair. Some of the procedures will return the board to the factory debugger environment. (The board was tested under these conditions before it left the factory.) The self-tests may not run in all user-customized environments.

Table C-1. Troubleshooting MVME3600 and 4600 Series Boards

Condition	Possible Problem	Try This:
I. Nothing works, no display on the terminal.	A. If the FUS (or CPU) LED is not lit, the board may not be getting correct power.	1. Make sure the system is plugged in. 2. Check that the board is securely installed in its backplane or chassis. 3. Check that all necessary cables are connected to the board, per this manual. 4. Check for compliance with System Considerations, per this manual. 5. Review the Installation and Startup procedures, per this manual. They include a step-by-step powerup routine. Try it.
	B. If the LEDs are lit, the board may be in the wrong slot.	1. For VMEmodules, the CPU board should be in the first (left-most) slot. 2. Also check that the “system controller” function on the board is enabled, per this manual.
	C. The “system console” terminal may be configured incorrectly.	Configure the system console terminal per this manual.

C

Table C-1. Troubleshooting MVME3600 and 4600 Series Boards (Continued)

Condition	Possible Problem	Try This:
II. There is a display on the terminal, but input from the keyboard and/or mouse has no effect.	A. The keyboard or mouse may be connected incorrectly.	Recheck the keyboard and/or mouse connections and power.
	B. Board jumpers may be configured incorrectly.	Check the board jumpers per this manual.
	C. You may have invoked flow control by pressing a HOLD or PAUSE key, or by typing**:** **CTRL-S**	Press the HOLD or PAUSE key again. If this does not free up the keyboard, type in: **CTRL-Q**
III. Debug prompt `PPC1-Bug>` does not appear at powerup, and the board does not autoboot.	A. Debugger EPROM/Flash may be missing	1. Disconnect *all* power from your system. 2. Check that the proper debugger EPROM or debugger Flash memory is installed per this manual. 3. Reconnect power. 4. Restart the system by "double-button reset": press the RESET and ABORT switches at the same time; release RESET first, wait seven seconds, then release ABORT. 5. If the debug prompt appears, go to step IV or step V, as indicated. If the debug prompt does not appear, go to step VI.
	B. The board may need to be reset.	
IV. Debug prompt `PPC1-Bug>` appears at powerup, but the board does not autoboot.	A. The initial debugger environment parameters may be set incorrectly.	1. Start the onboard calendar clock and timer. Type: **set *mmddyyhhmm* <CR>** where the characters indicate the month, day, year, hour, and minute. The date and time will be displayed. **Caution** — Performing the next step (**env;d**) will change some parameters that may affect your system's operation. (continues>)
	B. There may be some fault in the board hardware.	

Table C-1. Troubleshooting MVME3600 and 4600 Series Boards (Continued)

Condition	Possible Problem	Try This:
IV. *Continued*		2. At the command line prompt, type in: **env;d <CR>** This sets up the default parameters for the debugger environment. 3. When prompted to Update Non-Volatile RAM, type in: **y <CR>** 4. When prompted to Reset Local System, type in: **y <CR>** 5. After clock speed is displayed, immediately (within five seconds) press the Return key: **<CR>** or **<Break>** to exit to the System Menu. Then enter a 3 for "Go to System Debugger" and Return: **3 <CR>** Now the prompt should be: `PPC1-Diag>` 6. You may need to use the **cnfg** command (see your board Debugger Manual) to change clock speed and/or Ethernet Address, and then later return to: **env <CR>** and step 3. 7. Run the selftests by typing in: **st <CR>** The tests take as much as 10 minutes, depending on RAM size. They are complete when the prompt returns. (The onboard selftest is a valuable tool in isolating defects.) 8. The system may indicate that it has passed all the selftests. Or, it may indicate a test that failed. If neither happens, enter: **de <CR>** Any errors should now be displayed. If there are any errors, go to step VI. If there are no errors, go to step V.
V. The debugger is in system mode and the board autoboots, or the board has passed selftests.	A. No apparent problems — troubleshooting is done.	No further troubleshooting steps are required.

Table C-1. Troubleshooting MVME3600 and 4600 Series Boards (Continued)

Condition	Possible Problem	Try This:
VI. The board has failed one or more of the tests listed above, and cannot be corrected using the steps given.	A. There may be some fault in the board hardware or the on-board debugging and diagnostic firmware.	1. Document the problem and return the board for service. 2. Contact local MCG Sales Office.
TROUBLESHOOTING PROCEDURE COMPLETE.		

Related Documentation D

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office,
- Visiting MCG's World Wide Web literature site, http://www.motorola.com/computer/literature

Table D-1. Motorola Computer Group Documents

Document Title	Publication Number
MVME3600/4600 Series VME Processor Modules Installation and Use	V36V46A/IH
MVME3600/4600 Series VME Processor Modules Programmer's Reference Guide	V36V46A/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPC1Bug Diagnostics Manual	PPC1DIAA/UM
MVME712M Transition Module and P2 Adapter Board Installation and Use	VME712MA/IH
MVME761 Transition Module Installation and Use	VME761A/IH
PMCspan PMC Adapter Carrier Board Installation and Use	PMCSPANA/IH

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table D-2. Manufacturers' Documents

Document Title and Source	Publication Number
PowerPC 604™ RISC Microprocessor User's Manual Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 Web Site: http://e-www.motorola.com/webapp/DesignCenter/ E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics PowerPC604e User Manual Web Site: http://www.chips.ibm.com/techlib/products/powerpc/manuals	MPC604EUM/AD G522-0330-00
PowerPC™ Microprocessor Family: The Programming Environment for 32-Bit Microprocessors Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 Web Site: http://e-www.motorola.com/webapp/DesignCenter/ E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Programming Environment Manual Web Site: http://www.chips.ibm.com/techlib/products/powerpc/manuals	MPCFPE/AD G522-0290-01
MPC2604GA Integrated Secondary Cache for PowerPC Microprocessors (Glance) Data Sheets Web Site: http://e-www.motorola.com/webapp/DesignCenter/	MPC2604GA
DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual Web Site: http://developer.intel.com/design/network/mature/21140a.htm	21140-AF Revision 1.0

Table D-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PC87308VUL (Super I/O Enhanced Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Telephone: 1-800-272-9959 Web Site: http://www.national.com/pf/PC/PC87308.html	PC87308.html
M48T59 CMOS 8K x 8 TIMEKEEPER™ SRAM Data Sheet STMicroelectronics; Web Site: http://eu.st.com/stonline/index.shtml	M48T59
SYM 53CXX (was NCR 53C8XX) Family PCI-SCSI I/O Processor Data Manual LSI Logic Corporation Web Site: http://www.lsilogic.com	SYM53C875/875E Data Manual
SCC (Serial Communications Controller) User's Manual (for Z85230 and other Zilog parts) Web Site: http://www.zilog.com/pdfs/serial/scc_escc_iscc_manual/contents.html	SCC/ESCC User's Manual
Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification and User's Manual (in Z8000® Family of Products Data Book) Web Site: http://www.zilog.com/products/zx80dev.html#um	DM10001176
W83C553 Enhanced System I/O Controller with PCI Arbiter (PIB) Winbond Electronics Corporation; Web Site: http://www.winbond.com.tw/product/	W83C553F
Universe II User Manual Tundra Semiconductor Corporation Web Site: http://www.tundra.com/page.cfm?tree_id=100008#Universe II (CA91C142)	8091142_MD300_01.pdf

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

D

Table D-3. Related Specifications

Document Title and Source	Publication Number
ANSI Small Computer System Interface-2 (SCSI-2), Draft Document Global Engineering Documents Web Site: http://global.ihs.com/index.cfm	X3.131.1990
VME64 Specification VITA (VMEbus International Trade Association) Web Site: http://www.vita.com/	ANSI/VITA 1-1994
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Web Site: http://standards.ieee.org/catalog/	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Web Site: http://standards.ieee.org/catalog/	P1386.1 Draft 2.0
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Web Site: http://standards.ieee.org/catalog/	IEEE Standard 1284
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0 PCI Special Interest Group; Web Site: http://www.pcisig.com/	PCI Local Bus Specification

Table D-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 Web Site: http://e-www.motorola.com/webapp/DesignCenter/ E-mail: ldcformotorola@hibbertco.com OR Morgan Kaufmann Publishers, Inc. Telephone: (415) 392-2665 Telephone: 1-800-745-7323 Web Site: http://www.mkp.com/books_catalog/	
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II; International Business Machines Corporation Web Site: http://www.ibm.com	MPR-PPC-RPU-02
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Web Site: http://standards.ieee.org/catalog/	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents; Web Site: http://global.ihs.com/index.cfm (for publications) *(This document can also be obtained through the national standards body of member countries.)* Web Site: http://www.eia.org/	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange; Electronic Industries Alliance; Web Site: http://global.ihs.com/index.cfm (for publications) Web Site: http://www.eia.org/	TIA/EIA-232 Standard

Glossary

10Base-5	An Ethernet implementation in which the physical medium is a doubly shielded, 50-ohm coaxial cable capable of carrying data at 10 Mbps for a length of 500 meters (also referred to as thicknet). Also known as thick Ethernet.
10Base-2	An Ethernet implementation in which the physical medium is a single-shielded, 50-ohm RG58A/U coaxial cable capable of carrying data at 10 Mbps for a length of 185 meters (also referred to as AUI or thinnet). Also known as thin Ethernet.
10BaseT	An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 10 Mbps for a maximum distance of 185 meters. Also known as twisted-pair Ethernet.
100BaseTX	An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 100 Mbps for a maximum distance of 100 meters. Also known as fast Ethernet.
ACIA	**A**synchronous **C**ommunications **I**nterface **A**dapter
AIX	**A**dvanced **I**nteractive e**X**ecutive (IBM version of UNIX)
architecture	The main overall design in which each individual hardware component of the computer system is interrelated. The most common uses of this term are 8-bit, 16-bit, or 32-bit architectural design systems.
ASCII	**A**merican **S**tandard **C**ode for **I**nformation **I**nterchange, a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to 8 bits to encode a total of 256 alphanumeric and control characters.
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
AUI	**A**ttachment **U**nit **I**nterface
BBRAM	Battery Backed-up Random Access Memory
bi-endian	Having big-endian and little-endian byte ordering capability.

big-endian A byte-ordering method in memory where the address *n* of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.

BIOS **B**asic **I**nput/**O**utput **S**ystem. The built-in program that controls the basic functions of communications between the processor and the I/O devices (peripherals). Also referred to as ROM BIOS.

BitBLT **Bit** Boundary **BL**ock **T**ransfer. A type of graphics drawing routine that moves a rectangle of data from one area of display memory to another. The data need not have any particular alignment.

BLT **BL**ock **T**ransfer

board The term more commonly used to refer to a PCB (printed circuit board). Basically, a flat board made of nonconducting material, such as plastic or fiberglass, on which chips and other electronic components are mounted. Also referred to as a circuit board or card.

bpi **b**its **p**er **i**nch

bps **b**its **p**er **s**econd

bus The pathway used to communicate between the CPU, memory, and various input/output devices, including floppy drives and hard disk drives. Available in various widths (8-, 16-, and 32-bit), with accompanying increases in speed.

cache A high-speed memory that resides logically between a central processing unit (CPU) and the main memory. This temporary memory holds the data and/or instructions that the CPU is most likely to use over and over again and avoids frequent accesses to the slower hard drive or floppy disk drive.

CAS **C**olumn **A**ddress **S**trobe. The clock signal used in dynamic RAMs to control the input of column addresses.

CD **C**ompact **D**isc. A hard, round, flat portable storage unit that stores information digitally.

CD-ROM **C**ompact **D**isk **R**ead-**O**nly **M**emory

CFM **C**ubic **F**eet per **M**inute

CHRP See Common Hardware Reference Platform (CHRP).

CHRP-compliant See Common Hardware Reference Platform (CHRP).

CHRP Spec See Common Hardware Reference Platform (CHRP).

CISC **C**omplex-**I**nstruction-**S**et **C**omputer. A computer whose processor is designed to sequentially run variable-length instructions, many of which require several clock cycles, that perform complex tasks and thereby simplify programming.

CODEC **CO**der/**DEC**oder

Color Difference (CD) The signals of (R-Y) and (B-Y) without the luminance (-Y) signal. The Green signals (G-Y) can be extracted by these two signals.

Common Hardware Reference Platform (CHRP)
A specification published by the Apple, IBM, and Motorola which defines the devices, interfaces, and data formats that make up a CHRP-compliant system using a PowerPC processor.

Composite Video Signal (CVS/CVBS)
Signal that carries video picture information for color, brightness and synchronizing signals for both horizontal and vertical scans. Sometimes referred to as “Baseband Video”.

cpi **c**haracters **p**er **i**nch

cpl **c**haracters **p**er **l**ine

CPU **C**entral **P**rocessing **U**nit. The master computer unit in a system.

DCE **D**ata **C**ircuit-terminating **E**quipment.

DLL **D**ynamic **L**ink **L**ibrary. A set of functions that are linked to the referencing program at the time it is loaded into memory.

DMA **D**irect **M**emory **A**ccess. A method by which a device may read or write to memory directly without processor intervention. DMA is typically used by block I/O devices.

DOS **D**isk **O**perating **S**ystem

dpi **d**ots **p**er **i**nch

DRAM **D**ynamic **R**andom **A**ccess **M**emory. A memory technology that is characterized by extremely high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.

DTE **D**ata **T**erminal **E**quipment.

ECC **E**rror **C**orrection **C**ode

ECP **E**xtended **C**apability **P**ort

EEPROM — **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down.

EISA (bus) — **E**xtended **I**ndustry **S**tandard **A**rchitecture (bus) (IBM). An architectural system using a 32-bit bus that allows data to be transferred between peripherals in 32-bit chunks instead of the 16-bit or 8-bit units that most systems use. With the transfer of larger bits of information, the machine is able to perform much faster than the standard ISA bus system.

EPP — **E**nhanced **P**arallel **P**ort

EPROM — **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written once (per erasure cycle) and read many times.

ESCC — **E**nhanced **S**erial **C**ommunication **C**ontroller

ESD — **E**lectro-**S**tatic **D**ischarge/Damage

Ethernet — A local area network standard that uses radio frequency signals carried by coaxial cables.

Falcon — The DRAM controller chip developed by Motorola for the MVME2600 and MVME3600 series of boards. It is intended to be used in sets of two to provide the necessary interface between the Power PC60*x* bus and the 144-bit ECC DRAM (system memory array) and/or ROM/Flash.

fast Ethernet — See 100Base-TX.

FDC — **F**loppy **D**isk **C**ontroller

FDDI — **F**iber **D**istributed **D**ata **I**nterface. A network based on the use of optical-fiber cable to transmit data in non-return-to-zero, invert-on-1s (NRZI) format at speeds up to 100 Mbps.

FIFO — **F**irst-**I**n, **F**irst-**O**ut. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.

firmware — The program or specific software instructions that have been more or less permanently burned into an electronic component, such as a ROM (read-only memory) or an EPROM (erasable programmable read-only memory).

frame	One complete television picture frame consists of 525 horizontal lines with the NTSC system. One frame consists of two Fields.
graphics controller	On EGA and VGA, a section of circuitry that can provide hardware assistance for graphics-drawing algorithms by performing logical functions on data written to display memory.
HAL	**H**ardware **A**bstraction **L**ayer. The lower-level hardware interface module of the Windows NT operating system. It contains platform-specific functionality.
hardware	The term used to describe any of the physical embodiments of a computer system, with emphasis on the electronic circuits (the computer) and electromechanical devices (peripherals) that make up the system. A computing system is normally spoken of as having two major components: hardware and software.
HCT	**H**ardware **C**onformance **T**est. A test used to ensure that both hardware and software conform to the Windows NT interface.
I/O	**I**nput/**O**utput
IBC	PCI/**I**SA **B**ridge **C**ontroller
IDC	**I**nsulation **D**isplacement **C**onnector
IDE	**I**ntelligent **D**evice **E**xpansion
IEEE	**I**nstitute of **E**lectrical and **E**lectronics **E**ngineers
interlaced	A graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. Its advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware and may also make it possible to display a resolution that would otherwise be impossible on given hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a few scanlines high.
IQ Signals	Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.
ISA (bus)	**I**ndustry **S**tandard **A**rchitecture (bus). The de facto standard system bus for IBM-compatible computers until the introduction of VESA and PCI. Used in the reference platform specification. (IBM)

ISASIO — **ISA S**uper **I**nput/**O**utput device

ISDN — **I**ntegrated **S**ervices **D**igital **N**etwork. A standard for digitally transmitting video, audio, and electronic data over public phone networks.

LAN — **L**ocal **A**rea **N**etwork

LED — **L**ight-**E**mitting **D**iode

LFM — **L**inear **F**eet per **M**inute

little-endian — A byte-ordering method in memory where the address *n* of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.

MBLT — **M**ultiplexed **BL**ock **T**ransfer

MCA (bus) — **M**icro **C**hannel **A**rchitecture

MCG — **M**otorola **C**omputer **G**roup

MFM — **M**odified **F**requency **M**odulation

MIDI — **M**usical **I**nstrument **D**igital **I**nterface. The standard format for recording, storing, and playing digital music.

MPC — **M**ultimedia **P**ersonal **C**omputer

MPC601 — Motorola's component designation for the PowerPC 601 microprocessor.

MPC603 — Motorola's component designation for the PowerPC 603 microprocessor.

MPC604 — Motorola's component designation for the PowerPC 604 microprocessor.

MPIC — **M**ulti-**P**rocessor **I**nterrupt **C**ontroller

MPU — **M**icro**P**rocessing **U**nit

MTBF — **M**ean **T**ime **B**etween **F**ailures. A statistical term relating to reliability as expressed in power-on hours (poh). It was originally developed for the military and can be calculated several different ways, yielding substantially different results. The specification is based on a large number of samplings in one place, running continuously, and the rate at which failure occurs. MTBF is not

	representative of how long a device or any individual component is likely to last, nor is it a warranty, but rather an indicator of the relative reliability of a family of products.
multisession	The ability to record additional information, such as digitized photographs, on a CD-ROM after a prior recording session has ended.
non-interlaced	A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, and is usually said to have a more pleasing appearance.
nonvolatile memory	A memory in which the data content is maintained whether the power supply is connected or not.
NTSC	**N**ational **T**elevision **S**tandards **C**ommittee (USA)
NVRAM	**N**on-**V**olatile **R**andom **A**ccess **M**emory
OEM	**O**riginal **E**quipment **M**anufacturer
OMPAC	**O**ver-**M**olded **P**ad **A**rray **C**arrier
OS	**O**perating **S**ystem. The software that manages the computer resources, accesses files, and dispatches programs.
OTP	**O**ne-**T**ime **P**rogrammable
palette	The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 or 256 simultaneous colors out of 262,144.
parallel port	A connector that can exchange data with an I/O device eight bits at a time. This port is more commonly used for the connection of a printer to a system.
PCI (local bus)	**P**eripheral **C**omponent **I**nterconnect (local bus) (Intel). A high-performance, 32-bit internal interconnect bus used for data transfer to peripheral controller components, such as those for audio, video, and graphics.
PCMCIA (bus)	**P**ersonal **C**omputer **M**emory **C**ard **I**nternational **A**ssociation (bus). A standard external interconnect bus which allows peripherals adhering to the standard to be plugged in and used without further system modification.
PCR	**P**CI **C**onfiguration **R**egister

PHB — **P**CI **H**ost **B**ridge

PDS — **P**rocessor **D**irect **S**lot

physical address — A binary address that refers to the actual location of information stored in secondary storage.

PIB — **P**CI-to-**I**SA **B**ridge

pixel — An acronym for picture element, also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.

PLL — **P**hase-**L**ocked **L**oop

PMC — **P**CI **M**ezzanine **C**ard

POWER — **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC architecture (IBM)

PowerPC™ — The trademark used to describe the **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC microprocessor architecture for **P**ersonal **C**omputers developed by the IBM Corporation. PowerPC is superscalar, which means it can handle more than one instruction per clock cycle. Instructions can be sent simultaneously to three types of independent execution units (branch units, fixed-point units, and floating-point units), where they can execute concurrently, but finish out of order. PowerPC is used by Motorola, Inc. under license from IBM.

PowerPC 601™ — The first implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 256-entry buffer and a 32KB unified (instruction and data) cache. It provides a 64-bit data bus and a separate 32-bit address bus. PowerPC 601 is used by Motorola, Inc. under license from IBM.

PowerPC 603™ — The second implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 64-entry buffer and an 8KB (instruction and data) cache. It provides a selectable 32-bit or 64-bit data bus and a separate 32-bit address bus. PowerPC 603 is used by Motorola, Inc. under license from IBM.

PowerPC 604™ — The third implementation of the PowerPC family of microprocessors currently under development. PowerPC 604 is used by Motorola, Inc. under license from IBM.

PowerPC Reference Platform (PRP)
A specification published by the IBM Power Personal Systems Division which defines the devices, interfaces, and data formats that make up a PRP-compliant system using a PowerPC processor.

PowerStack™ RISC PC (System Board)
A PowerPC-based computer board platform developed by the Motorola Computer Group. It supports Microsoft's Windows NT and IBM's AIX operating systems.

PRP See PowerPC Reference Platform (PRP).

PRP-compliant See PowerPC Reference Platform (PRP).

PRP Spec See PowerPC Reference Platform (PRP).

PROM **P**rogrammable **R**ead-**O**nly **M**emory

PS/2 **P**ersonal **S**ystem/**2** (IBM)

QFP **Q**uad **F**lat **P**ackage

RAM **R**andom-**A**ccess **M**emory. The temporary memory that a computer uses to hold the instructions and data currently being worked with. All data in RAM is lost when the computer is turned off.

RAS **R**ow **A**ddress **S**trobe. A clock signal used in dynamic RAMs to control the input of the row addresses.

Raven The PowerPC-to-PCI local bus bridge chip developed by Motorola for the MVME2600 and MVME3600 series of boards. It provides the necessary interface between the PowerPC 60x bus and the PCI bus, and acts as interrupt controller.

Reduced-Instruction-Set Computer (RISC)
A computer in which the processor's instruction set is limited to constant-length instructions that can usually be executed in a single clock cycle.

RFI **R**adio **F**requency **I**nterference

RGB The three separate color signals: **R**ed, **G**reen, and **B**lue. Used with color displays, an interface that uses these three color signals as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

RISC See Reduced-Instruction-Set Computer (RISC).

ROM	**R**ead-**O**nly **M**emory
RTC	**R**eal-**T**ime **C**lock
SBC	**S**ingle **B**oard **C**omputer
SCSI	**S**mall **C**omputer **S**ystems **I**nterface. An industry-standard high-speed interface primarily used for secondary storage. The SCSI-1 implementation provides up to 5 Mbps data transfer.
SCSI-2 (Fast/Wide)	An improvement over plain SCSI; and includes command queuing. Fast SCSI provides 10 Mbps data transfer on an 8-bit bus. Wide SCSI provides up to 40 Mbps data transfer on a 16- or 32-bit bus.
serial port	A connector that can exchange data with an I/O device one bit at a time. It may operate synchronously or asynchronously, and may include start bits, stop bits, and/or parity.
SIM	**S**erial **I**nterface **M**odule
SIMM	**S**ingle **I**nline **M**emory **M**odule. A small circuit board with RAM chips (normally surface mounted) that is designed to fit into a standard slot.
SIO	**S**uper **I/O** controller
SMP	**S**ymmetric **M**ulti**P**rocessing. A computer architecture in which tasks are distributed among two or more local processors.
SMT	**S**urface **M**ount **T**echnology. A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Instead, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.
software	The term used to describe any single program or group of programs, languages, operating procedures, and documentation of a computer system. A computing system is normally spoken of as having two major components: hardware and software. Software is the real interface between the user and the computer.
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SSBLT	**S**ource **S**ynchronous **BL**ock **T**ransfer
standard(s)	A set of detailed technical guidelines used as a means of establishing uniformity in an area of hardware or software development.

SVGA — **S**uper **V**ideo **G**raphics **A**rray (IBM). An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 800 x 600 pixels.

Teletext — One-way broadcast of digital information. The digital information is injected in the broadcast TV signal, VBI, or full field, The transmission medium could be satellite, microwave, cable, etc. The display medium is a regular TV receiver.

thick Ethernet — See 10Base-5.

thin Ethernet — See 10Base-2.

twisted-pair Ethernet — See 10Base-T.

UART — **U**niversal **A**synchronous **R**eceiver/**T**ransmitter

Universe — Bus bridge ASIC that interfaces between the PCI bus and the VMEbus.

UV — **U**ltra**V**iolet

UVGA — **U**ltra **V**ideo **G**raphics **A**rray. An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

Vertical Blanking Interval (VBI) — The time it takes the beam to fly back to the top of the screen in order to retrace the opposite field (odd or even). VBI is on the order of 20 TV lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

VESA (bus) — **V**ideo **E**lectronics **S**tandards **A**ssociation (or VL bus). An internal interconnect standard for transferring video information to a computer display system.

VGA — **V**ideo **G**raphics **A**rray (IBM). The third and most common monitor standard used today. It provides up to 256 simultaneous colors and a screen resolution of 640 x 480 pixels.

virtual address — A binary address issued by a CPU that indirectly refers to the location of information in primary memory, such as main memory. When data is copied from disk to main memory, the physical address is changed to the virtual address.

VL bus — See **V**ESA **L**ocal bus (VL bus).

volatile memory — A memory in which the data content is lost when the power supply is disconnected.

VRAM — **V**ideo (Dynamic) **R**andom **A**ccess **M**emory. Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

Windows NT™ — The trademark representing **Windows N**ew **T**echnology, a computer operating system developed by the Microsoft Corporation.

XGA — E**X**tended **G**raphics **A**rray. An improved IBM VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

Y Signal — Luminance. Parameter that determines the brightness (but not the color) of each spot (pixel) on a CRT screen in color or B/W systems.

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