AXIOMTEK

CEM860

2nd Generation Intel® Core™ Processor COM Express™ Type 6 Basic Module

User's Manual

RoHS

Disclaimers

This manual has been carefully checked and believed to contain accurate information. Axiomtek Co., Ltd. assumes no responsibility for any infringements of patents or any third party's rights, and any liability arising from such use.

Axiomtek does not warrant or assume any legal liability or responsibility for the accuracy, completeness or usefulness of any information in this document. Axiomtek does not make any commitment to update the information in this manual.

Axiomtek reserves the right to change or revise this document and/or product at any time without notice.

No part of this document may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior written permission of Axiomtek Co., Ltd.

CAUTION

If you replace wrong batteries, it causes the danger of explosion. It is recommended by the manufacturer that you follow the manufacturer's instructions to only replace the same or equivalent type of battery, and dispose of used ones.

November 2011, Version A1

Printed in Taiwan

ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. It discharges static electricity from your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

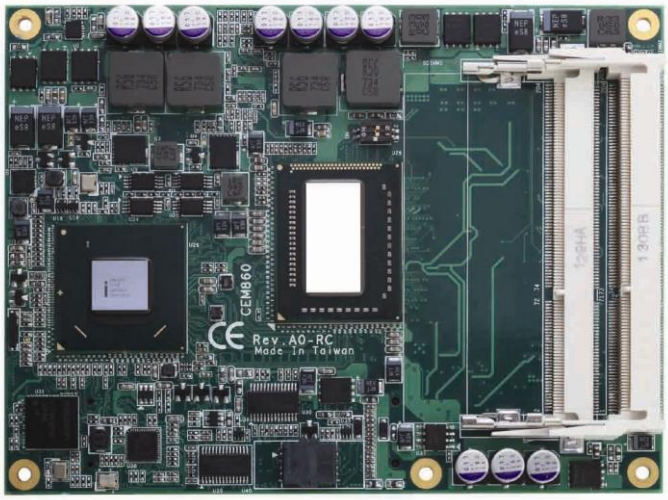
Trademarks Acknowledgments

Table of Contents

Appendix A Watchdog Timer and GPIO

This page is intentionally left blank.

Chapter 1
Introduction



The CEM860 is a new COM Express™ Type 6 Basic Module to support BGA type quad/dual core 2nd generation Intel® Core™ i7/ i5/ i3/ Celeron processors. It integrates Intel® PCH QM67 chipset which supports the most updated high speed I/Os like PCIe gen 2 at 5GT/s, SuperSpeed USB 3.0 at 5Gb/s (optional with NEC controller), and SATA-600 at 6Gb/s. The CEM860 does fully comply with COM Express™ Type 6 specification. It provides 22 lanes of PCIe, gigabit ethernet, HD audio interface, VGA/LVDS LCD and 3 configurable DDI for more flexible digital display options.

1.1 Features

- Intel® 2nd generation Core™ i7/ i5/ i3/ Celeron BGA processor

  Product Configurations:

CEM860DG-i7-2715QE	TPM / USB3.0 / AMT
CEM860DG-i7-2610UE	TPM / USB3.0 / AMT
CEM860DG-i5-2515E	TPM / USB3.0 / AMT
CEM860DG-i3-2340UE	TPM / USB3.0
CEM860DG-B810E	TPM

- Intel® PCH QM67
- 2 DDR3 1066/1333 MHz SO-DIMMs support up to 16 GB memory capacity
- 22 lanes of PCIe gen 2 at 5GT/s
- 2 SATA-600 and 2 SATA-300
- 8 USB 2.0 ports
- 2 USB 3.0 ports (optional)
- TPM

1.2 Specifications

- **CPU**
  - Intel® Core™ i7/ i5/ i3/ Celeron BGA processors.

- **Chipset**
  - Intel® QM67 Express Chipset.

- **BIOS**
  - American Megatrends Inc. BIOS.
  - 64Mbit SPI Flash, DMI, Plug and Play.
  - RPL/PXE Ethernet Boot ROM, customized default saving features, LPC-free supported, uses SPI type Flash memory.

- **System Memory**
  - Two 204-pin DDR3 SO-DIMM slots.
  - Maximum up to 16GB DDR3 1066/1333MHz memory.

- **TPM**
  - Trusted Platform Module compatible with TPM1.2 Main and PC Client specification based on Intel LPC Bus Interface (optional).

- **Expansion Interface**
  - One PCI-Express x16 (gen 2) for discrete graphics or general purpose PCI Express (2 x8 or 1 x8 with 2 x4).
  - Six PCI-Express x1 (lanes 1/2/3/4/7/8 are free); lane 5 is occupied by USB 3.0 controller and lane 6 is occupied by GbE.

- **USB Interface**
  - Eight USB ports comply with USB Spec. Rev. 2.0.
  - Two USB ports comply with USB Spec. Rev. 3.0 (optional).

- **SATA Interface**
  - Two SATA 6Gb/s ports supported through COM Express™ connector.
  - Two SATA 3Gb/s ports supported through COM Express™ connector.

- **Video**
  - Integrated in processor HD graphics 3000 at 650~1300MHz.
  - CRT interface supports up to QXGA (2048 x 1536).
  - 18 / 24-bit dual chanel LVDS interface.
  - Three DDI ports supporting HDMI / DVI / DisplayPort or SDVO.

- **Ethernet**
  - One 10/100/1000 Base-T provided by Intel 82579LM with integrated boot ROM.

- **Audio**
  - Integrated on Intel® PCH QM67.

- **Power Management**
  - ACPI (Advanced Configuration and Power Interface).

- **Form Factor**
  - Basic module 125mm x 95mm.

1.3 Utilities Supported

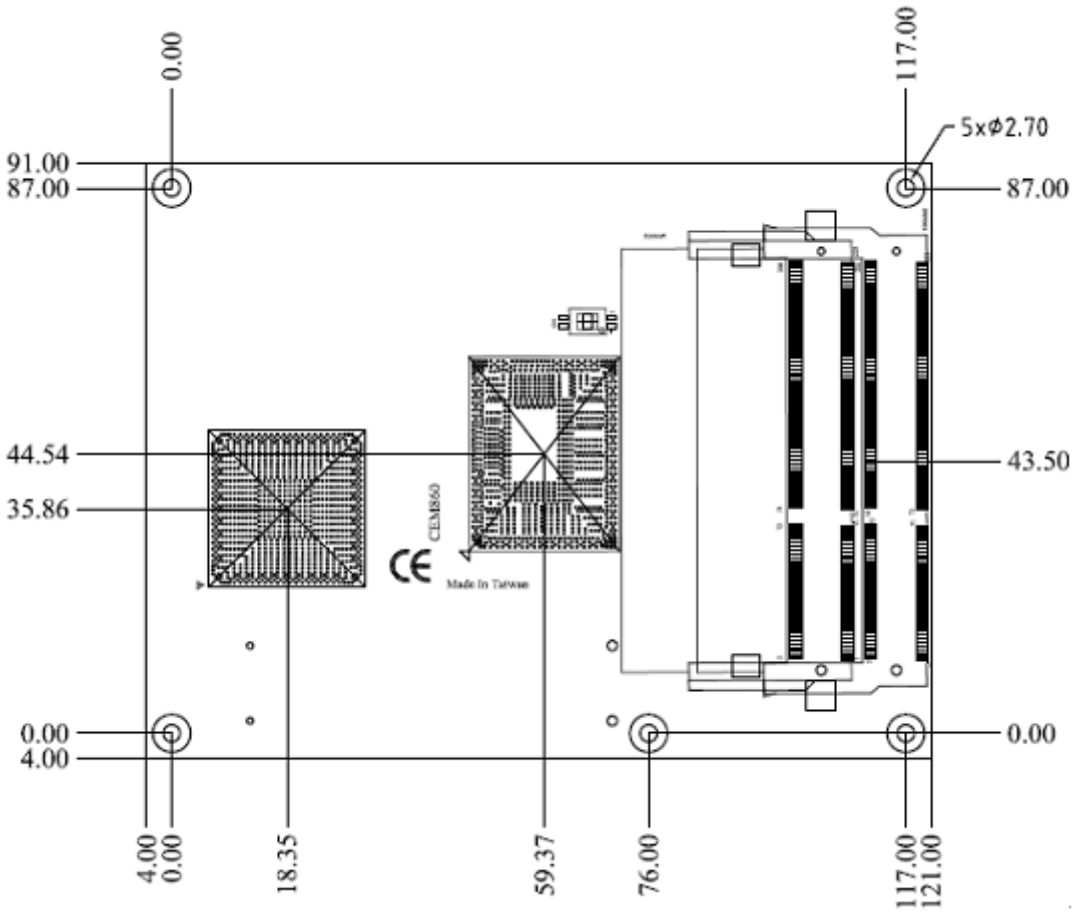
- Intel® QM67 utility and driver
- VGA driver
- Ethernet utility and driver
- ME driver
- TPM utility
- USB 3.0 driver

Note: ***All specifications and images are subject to change without notice.***

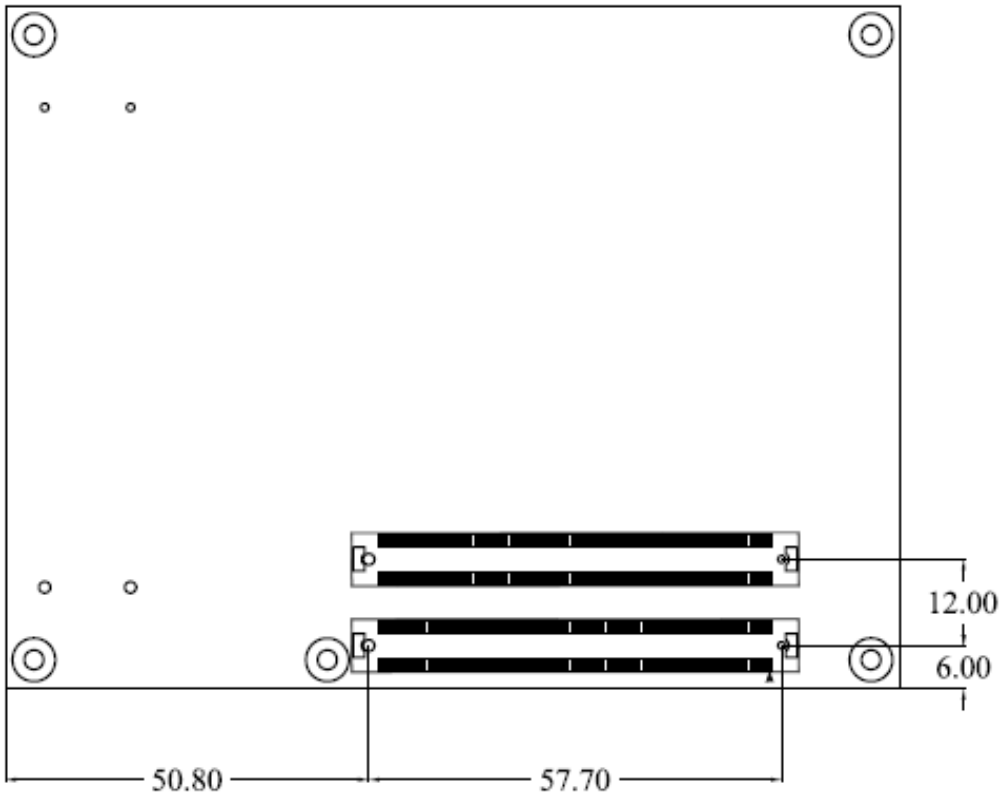
This page is intentionally left blank.

Chapter 2
Module and Pin Assignments

2.1 Module Dimensions and Fixing Holes

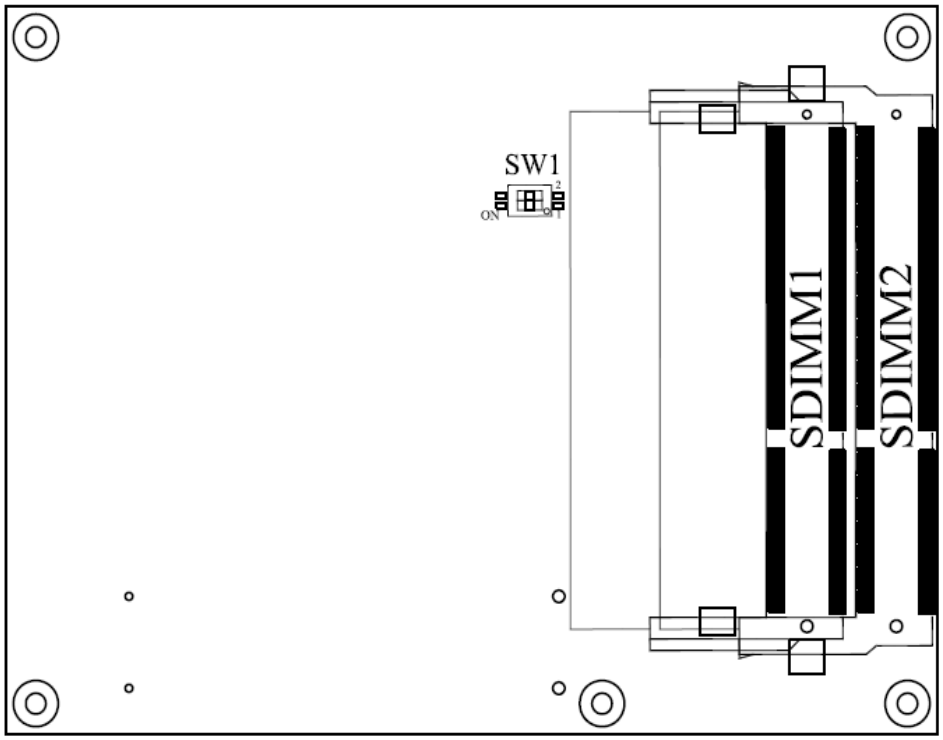


Top Side

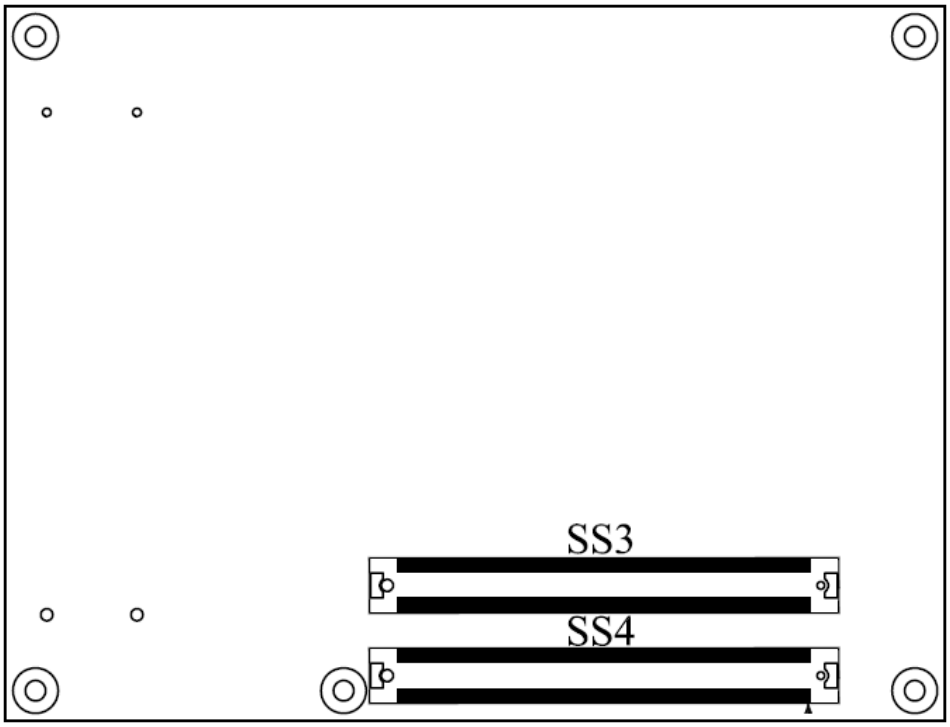


Bottom Side

2.2 Module Layout



Top Side



Bottom Side

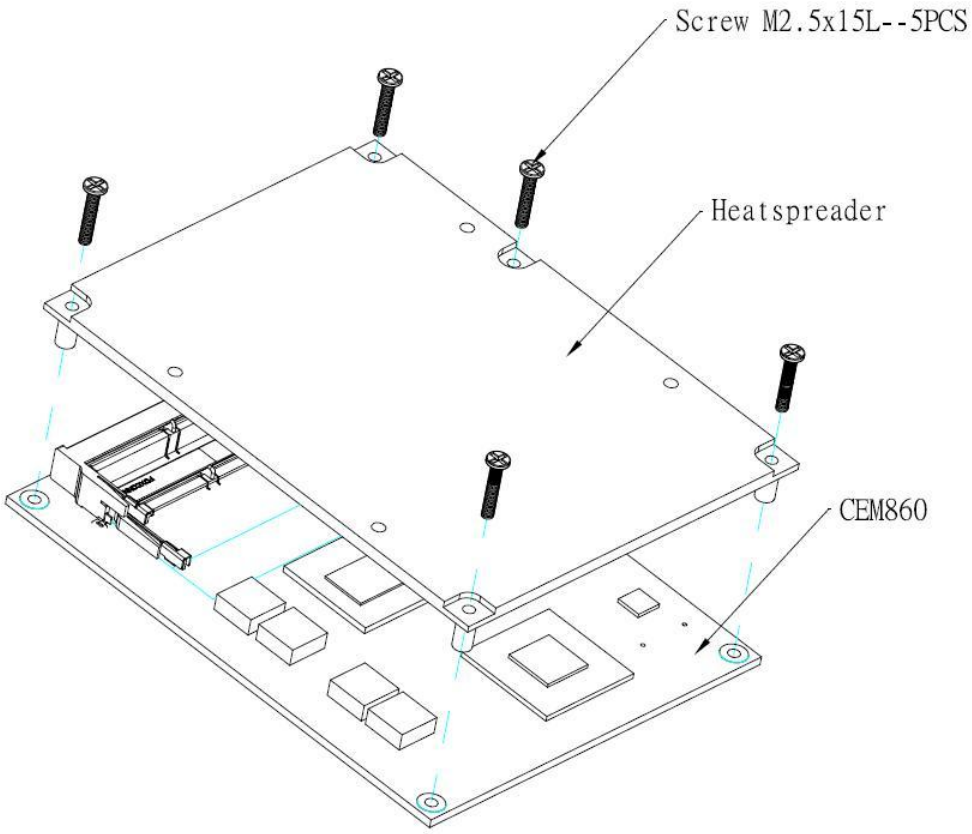
2.3 Installing Heatspreader

For thermal dissipation, a heatspreader enables the CEM860's components to dissipate heat efficiently. All heat generating components are thermally conducted to the heatspreader in order to avoid hot spots. Below images illustrate how to install the heat spreader.

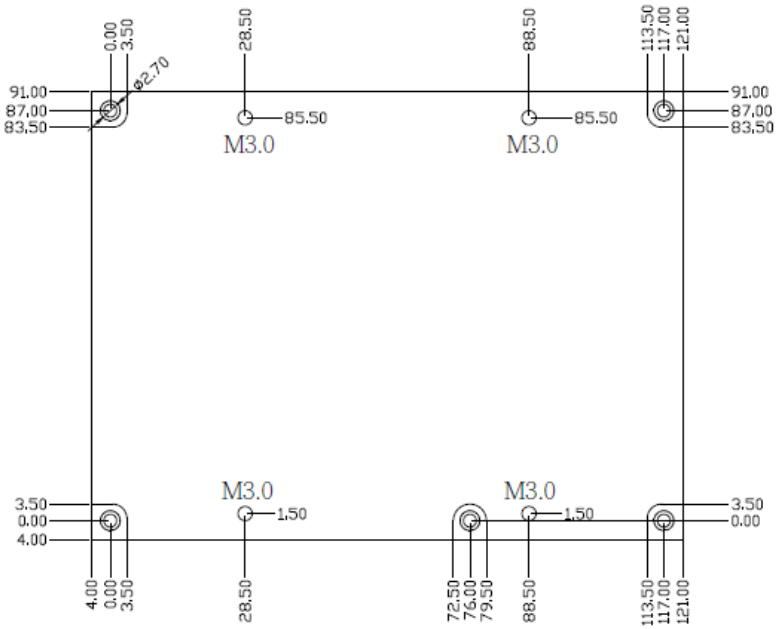
1. There is a protective plastic covering on the thermal pads. This must be removed before the heatspreader can be mounted.

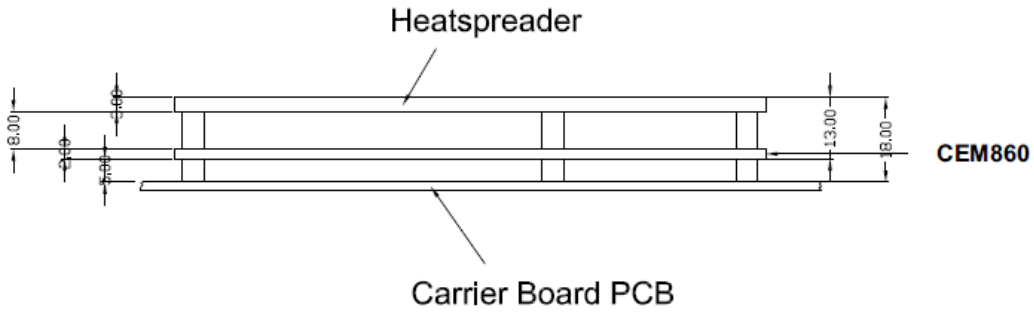
2. Each heatspreader is designed for a specific CEM module. The thermal pads on the heatspreader are designed to make contact with the necessary components on the CEM module. When mounting the heatspreader you must make sure that the thermal pads on the heatspreader make complete contact (no space between thermal pad and component) with the corresponding components on the CEM module. This is especially critical for CEM modules that have higher CPU speeds (for example 1.0GHz or more) to ensure that the heatspreader acts as a proper thermal interface for cooling solutions.

3. This CPU module has five assembly holes for installing heat spreader plate. Use the five screws (M2.5x15L) to secure the heat spreader plate to the CEM860. Be careful not to over-tighten the screws.



4. If you need additional information for thermal solution, please refer to below image to design your system's cooling.





2.4 Switch Setting (SW1)

Properly configure switch settings on the CEM860 to meet your application purpose.

If SW1 is enabled for AC power input, the system will be automatically power on without pressing soft power button. If SW1 is disabled for AC power input, it is necessary to manually press soft power button to turn on the system.

Function	Setting
Disable auto power on (Default)	OFF position
Enable auto power on	ON position

SW1

Note: ***This function is similar to the feature of power on after power failure, which is controlled by hardware circuitry instead of BIOS.***

2.5 Connectors

Signals go to the other parts of the system through connectors. Loose or improper connection might cause problems, please make sure all connectors are properly and firmly connected. Here is a summary table which shows all connectors on the hardware.

Connector	Description
SDIMM1	DDR3 SO-DIMM Connector
SDIMM2	DDR3 SO-DIMM Connector
SS3	COM Express™ Connector
SS4	COM Express™ Connector

2.5.1 COM Express™ Connectors (SS3 and SS4)

Below table shows the pin assignments for the 220-pin COM Express™ connectors.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND (FIXED)	D2	GND (FIXED)
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK100#	B4	LPC_AD0	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	GND (FIXED)	D5	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	C6	USB_SSRX1-	D6	USB_SSTX1-
A7	GBE0_MDI2+	B7	LPC_AD3	C7	USB_SSRX1+	D7	USB_SSTX1+
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	GND (FIXED)	D8	GND (FIXED)
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	USB_SSRX2-	D9	USB_SSTX2-
A10	GBE0_MDI1+	B10	LPC_CLK	C10	USB_SSRX2+	D10	USB_SSTX2+
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	USB_SSRX3-	D12	USB_SSTX3-
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+	D13	USB_SSTX3+
A14	GBE0_CTREF	B14	SMB_DAT	C14	GND (FIXED)	D14	GND (FIXED)
A15	SUS_S3#	B15	SMB_ALERT#	C15	DDI1_PAIR6+	D15	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+	B16	SATA1_TX+	C16	DDI1_PAIR6-	D16	DDI1_CTRLDATA_AUX-
A17	SATA0_TX-	B17	SATA1_TX-	C17	RSVD	D17	RSVD
A18	SUS_S4#	B18	SUS_STAT#	C18	RSVD	D18	RSVD
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCIE_RX6+	D19	PCIE_TX6+
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCIE_RX6-	D20	PCIE_TX6-
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	C22	PCIE_RX7+	D22	PCIE_TX7+
A23	SATA2_TX-	B23	SATA3_TX-	C23	PCIE_RX7-	D23	PCIE_TX7-
A24	SUS_S5#	B24	PWR_OK	C24	DDI1_HPD	D24	RSVD
A25	SATA2_RX+	B25	SATA3_RX+	C25	DDI1_PAIR4+	D25	RSVD
A26	SATA2_RX-	B26	SATA3_RX-	C26	DDI1_PAIR4-	D26	DDI1_PAIR0+
A27	BATLOW#	B27	WDT	C27	RSVD	D27	DDI1_PAIR0-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	C28	RSVD	D28	RSVD
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	C29	DDI1_PAIR5+	D29	DDI1_PAIR1+
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	C30	DDI1_PAIR5-	D30	DDI1_PAIR1-
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC/HDA_BITCLK	B32	SPKR	C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
A33	AC/HDA_SDOUT	B33	I2C_CK	C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
A34	BIOS_DISABLE#	B34	I2C_DAT	C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#	B35	THRM#	C35	RSVD	D35	RSVD
A36	USB6-	B36	USB7-	C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
A37	USB6+	B37	USB7+	C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	DDI3_DDC_AUX_SEL	D38	RSVD
A39	USB4-	B39	USB5-	C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
A40	USB4+	B40	USB5+	C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
A43	USB2+	B43	USB3+	C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	DDI3_HPD	D44	DDI2_HPD
A45	USB0-	B45	USB1-	C45	RSVD	D45	RSVD
A46	USB0+	B46	USB1+	C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
A47	VCC_RTC	B47	EXCD1_PERST#	C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	RSVD	D48	RSVD
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
A50	LPC_SERIRQ	B50	CB_RESET#	C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PEG_RX0+	D52	PEG_TX0+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	PEG_LANE_RV#
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PEG_RX1+	D55	PEG_TX1+

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PEG_RX2+	D58	PEG_TX2+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PEG_RX2-	D59	PEG_TX2-
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PEG_RX3+	D61	PEG_TX3+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PEG_RX3-	D62	PEG_TX3-
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PEG_RX4+	D65	PEG_TX4+
A66	GND	B66	WAKE0#	C66	PEG_RE4-	D66	PEG_TX4-
A67	GPI2	B67	WAKE1#	C67	RSVD	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PEG_RX5+	D68	PEG_TX5+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PEG_RX5-	D69	PEG_TX5-
A70	GND(FIXED)	B70	GND(FIXED)	C70	GND(FIXED)	D70	GND(FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71	PEG_RX6+	D71	PEG_TX6+
A72	LVDS_A0-	B72	LVDS_B0-	C72	PEG_RX6-	D72	PEG_TX6-
A73	LVDS_A1+	B73	LVDS_B1+	C73	GND(FIXED)	D73	SDVO_CLK
A74	LVDS_A1-	B74	LVDS_B1-	C74	PEG_RX7+	D74	PEG_TX7+
A75	LVDS_A2+	B75	LVDS_B2+	C75	PEG_RX7-	D75	PEG_TX7-
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD	D77	RSVD
A78	LVDS_A3+	B78	LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND(FIXED)	B80	GND(FIXED)	C80	GND(FIXED)	D80	GND(FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	RSVD	D83	RSVD
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	RSVD	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	RSVD	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE0_CK_REF+	B88	BIOS_DIS1	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE0_CK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	SPI_MISO	B92	VGA_BLU	C92	PEG_RX12-	D92	PEG_TX12-
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	SPI_CLK	B94	VGA_VSYNC	C94	PEG_RX13+	D94	PEG_TX13+
A95	SPI_MOSI	B95	VGA_I2C_CK	C95	PEG_RX13-	D95	PEG_TX13-
A96	TPM_PP	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	TYPE10#	B97	SPI_CS#	C97	RSVD	D97	RSVD
A98	SER0_TX	B98	RSVD	C98	PEG_RX14+	D98	PEG_TX14+
A99	SER0_RX	B99	RSVD	C99	PEG_RX14-	D99	PEG_TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWMOUT	C101	PEG_RX15+	D101	PEG_TX15+
A102	SER1_RX	B102	FAN_TACHIN	C102	PEG_RX15-	D102	PEG_TX15-
A103	LID#	B103	SLEEP#	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

Chapter 3
Hardware Description

3.1 Microprocessor

The CEM860 supports Intel® Core™ i7/i5/i3 and Celeron processors, which enables your system to operate under Windows® XP, Windows® 7 and Linux environments. The system performance depends on the microprocessor. You must install the heatspreader or cooler carefully and properly to prevent damage.

3.2 BIOS

The CEM860 uses AMI Plug and Play BIOS with a single 64Mbit SPI Flash.

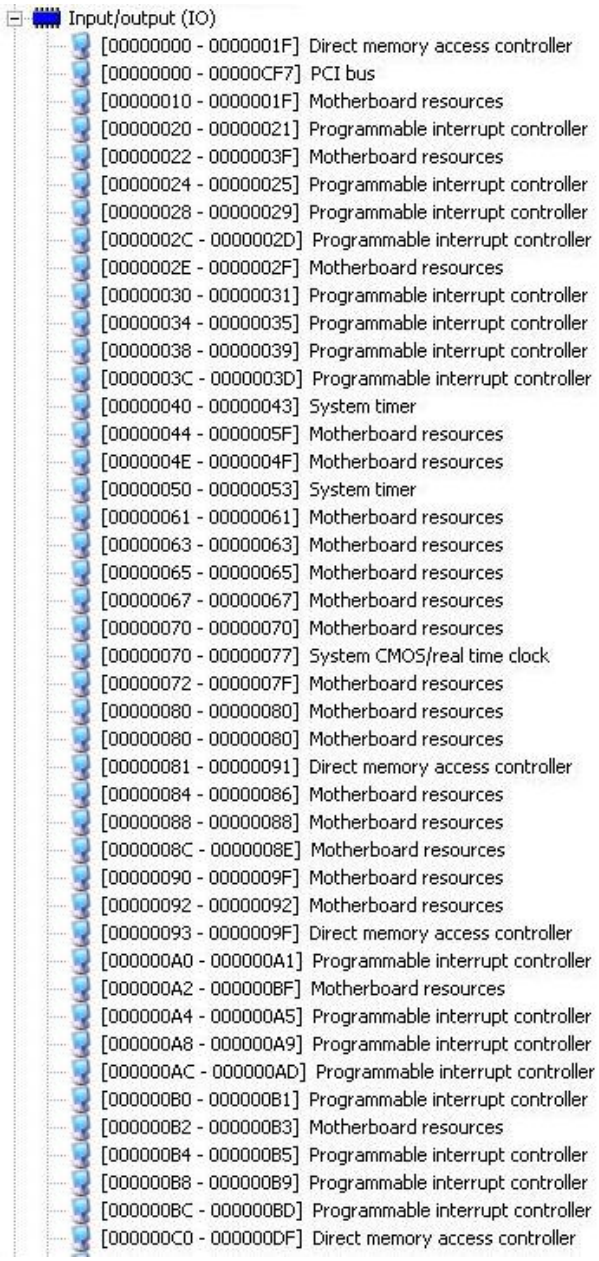
3.3 System Memory

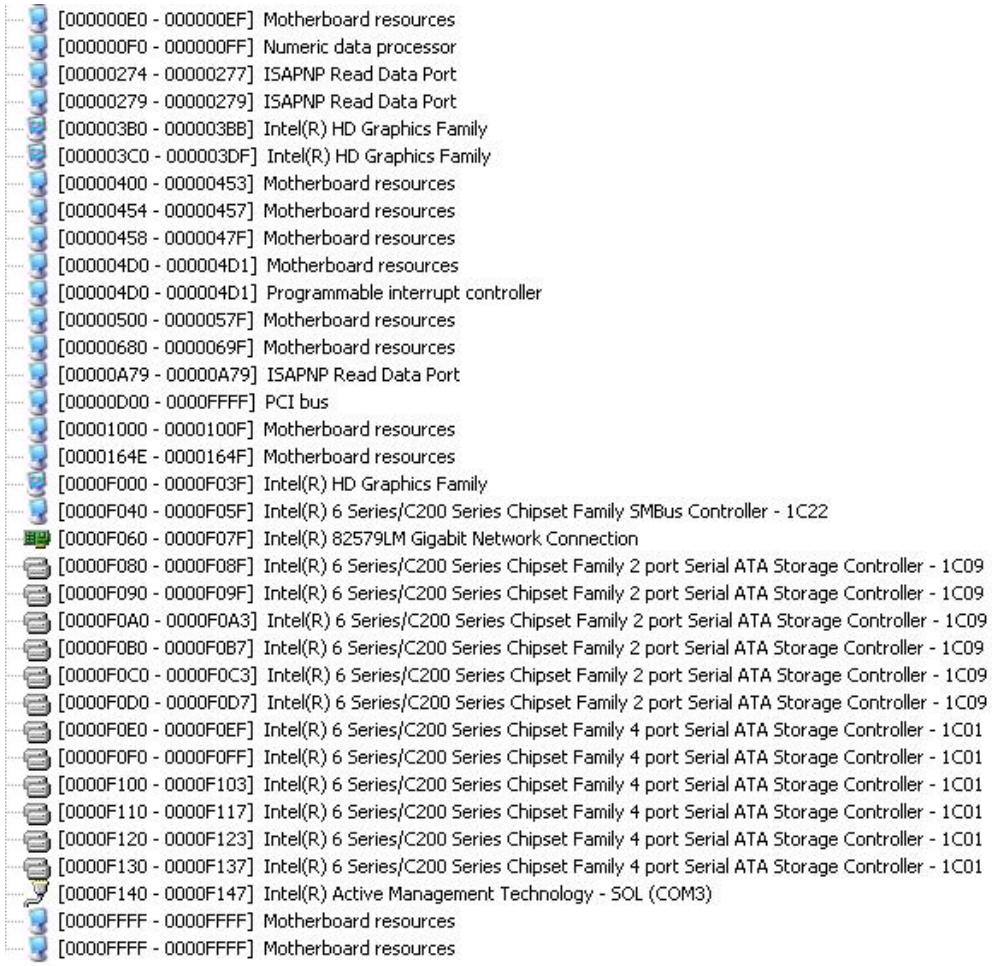
The CEM860 supports two 204-pin DDR3 1066/1333MHz SO-DIMM sockets for a maximum memory of 16GB DDR3 SDRAMs. The memory module can come in sizes of 1GB, 2GB and 4GB.

3.4 I/O Port Address Map

The Intel® Core™ i7/i5/i3 and Celeron processors communicate via I/O ports. Total 1KB port addresses are available for assigning to other devices via I/O expansion cards.

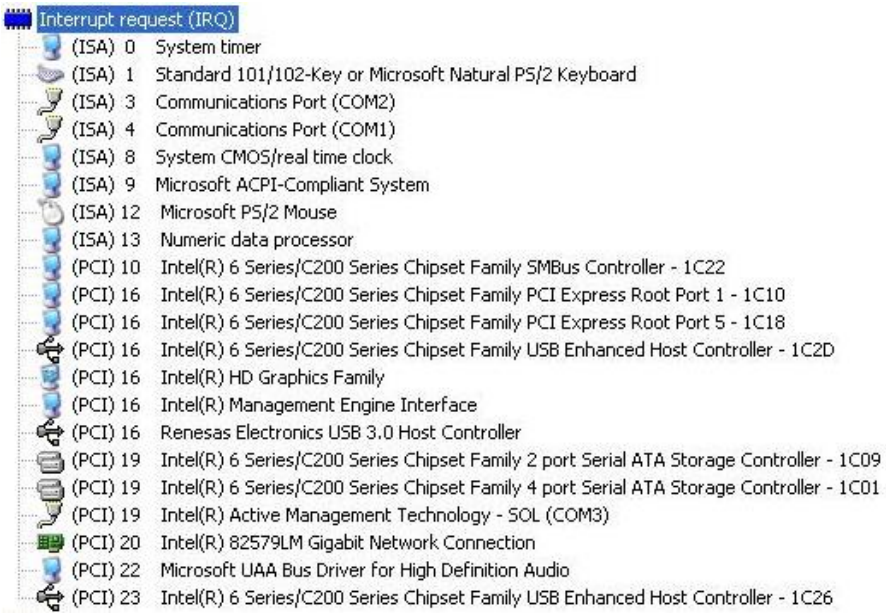
The I/O port addresses (with CEB94006 baseboard under Windows® XP) are as follows:




[000000E0 - 000000EF] Motherboard resources
[000000F0 - 000000FF] Numeric data processor
[00000274 - 00000277] ISAPNP Read Data Port
[00000279 - 00000279] ISAPNP Read Data Port
[000003B0 - 000003BB] Intel(R) HD Graphics Family
[000003C0 - 000003DF] Intel(R) HD Graphics Family
[00000400 - 00000453] Motherboard resources
[00000454 - 00000457] Motherboard resources
[00000458 - 0000047F] Motherboard resources
[000004D0 - 000004D1] Motherboard resources
[000004D0 - 000004D1] Programmable interrupt controller
[00000500 - 0000057F] Motherboard resources
[00000680 - 0000069F] Motherboard resources
[00000A79 - 00000A79] ISAPNP Read Data Port
[00000D00 - 0000FFFF] PCI bus
[00001000 - 0000100F] Motherboard resources
[0000164E - 0000164F] Motherboard resources
[0000F000 - 0000F03F] Intel(R) HD Graphics Family
[0000F040 - 0000F05F] Intel(R) 6 Series/C200 Series Chipset Family SMBus Controller - 1C22
[0000F060 - 0000F07F] Intel(R) 82579LM Gigabit Network Connection
[0000F080 - 0000F08F] Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller - 1C09
[0000F090 - 0000F09F] Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller - 1C09
[0000F0A0 - 0000F0A3] Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller - 1C09
[0000F0B0 - 0000F0B7] Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller - 1C09
[0000F0C0 - 0000F0C3] Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller - 1C09
[0000F0D0 - 0000F0D7] Intel(R) 6 Series/C200 Series Chipset Family 2 port Serial ATA Storage Controller - 1C09
[0000F0E0 - 0000F0EF] Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller - 1C01
[0000F0F0 - 0000F0FF] Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller - 1C01
[0000F100 - 0000F103] Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller - 1C01
[0000F110 - 0000F117] Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller - 1C01
[0000F120 - 0000F123] Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller - 1C01
[0000F130 - 0000F137] Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller - 1C01
[0000F140 - 0000F147] Intel(R) Active Management Technology - SOL (COM3)
[0000FFFF - 0000FFFF] Motherboard resources
[0000FFFF - 0000FFFF] Motherboard resources

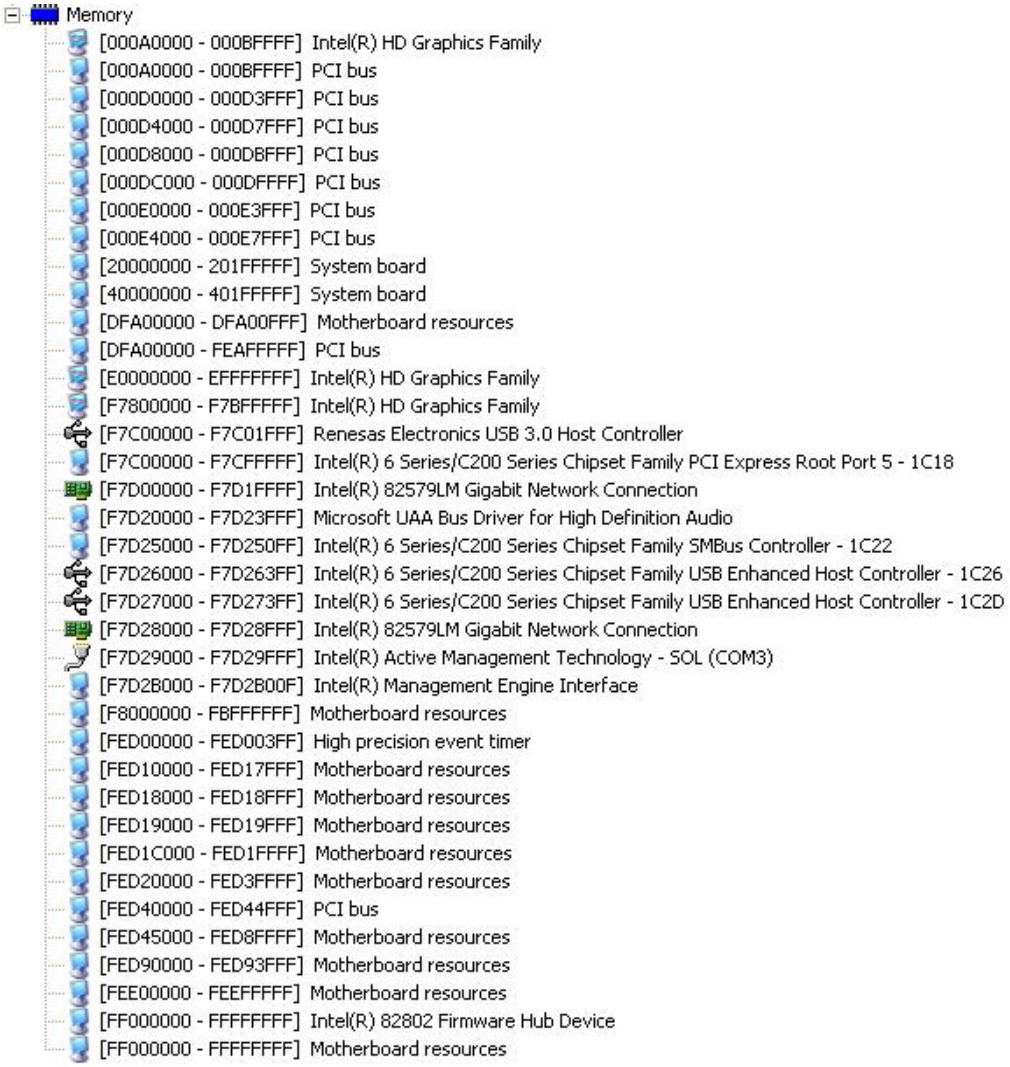
3.5 Interrupt Controller (IRQ) Map

The CEM860 is 100% PC compatible control module which consists of 20 interrupt request lines. Four out of 20 are programmable. The mapping list of the 20 interrupt request lines (with CEB94006 baseboard under Windows® XP) is shown as follows:



3.6 Memory Map

The memory (with CEB94006 baseboard under Windows® XP) mapping list is shown as follows:



This page is intentionally left blank.

Chapter 4
AMI BIOS Setup Utility

The AMI BIOS provides users with a built-in setup program to modify basic system configuration. All configured parameters are stored in a battery-backed CMOS to save the setup information whenever the power is turned off. This chapter provides users with detailed description about how to set up basic system configuration through the AMI BIOS setup utility.

4.1 Starting

To enter the setup screens, follow the steps below:

1. Turn on the computer and press the <Del> key immediately.
2. After you press the <Del> key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Advanced and Chipset menus.

It is strongly recommended that you should avoid changing the chipset's defaults. Both AMI and your system manufacturer have carefully set up these defaults that provide the best performance and reliability.

4.2 Navigation Keys

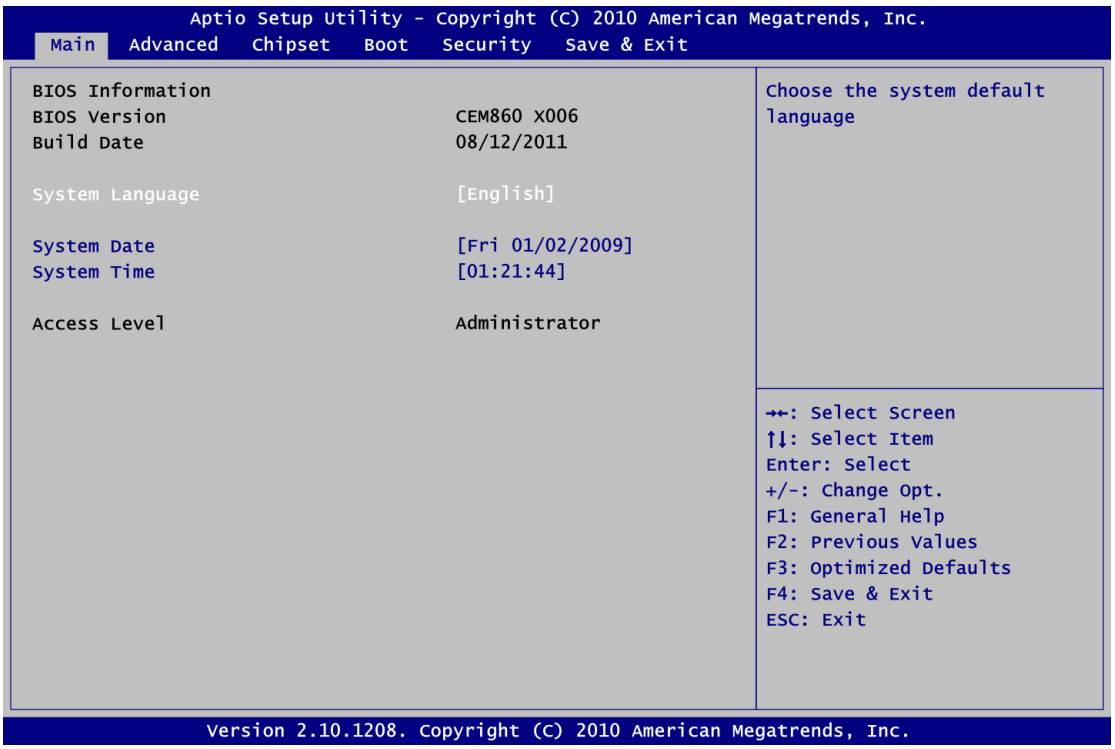
The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F2>, <Enter>, <ESC>, <Arrow> keys, and so on.

Note: ***Some of the navigation keys differ from one screen to another.***

Hot Keys	Description
→← Left/Right	The Left and Right <Arrow> keys allow you to select a setup screen.
↑↓ Up/Down	The Up and Down <Arrow> keys allow you to select a setup screen or sub-screen.
+– Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item.
Tab	The <Tab> key allows you to select setup fields.
F1	The <F1> key allows you to display the General Help screen.
F2	The <F2> key allows you to Load Previous Values.
F3	The <F3> key allows you to Load Optimized Defaults.
F4	The <F4> key allows you to save any changes you have made and exit Setup. Press the <F4> key to save your changes.
Esc	The <Esc> key allows you to discard any changes you have made and exit the Setup. Press the <Esc> key to exit the setup without saving your changes.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub- screens.

4.3 Main Menu

When you first enter the setup utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. System Time/Date can be set up as described below. The Main BIOS setup screen is shown below.



- **System Language**
  Use this item to choose the system default language.

- **System Date/Time**
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

4.4 Advanced Menu

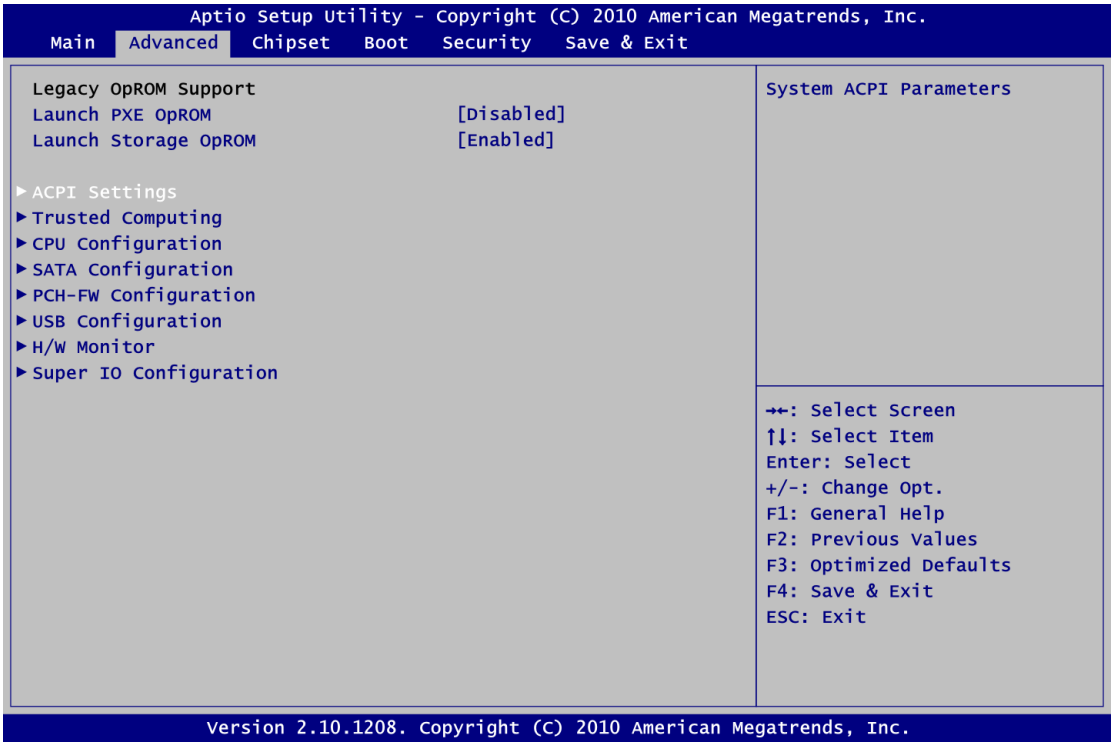
- **Launch PXE OpROM**
  Use this item to enable or disable the boot ROM function of the onboard LAN chip when the system boots up.

- **Launch Storage OpROM**
  This item can enable or disable boot option for legacy mass storage devices with option ROM.

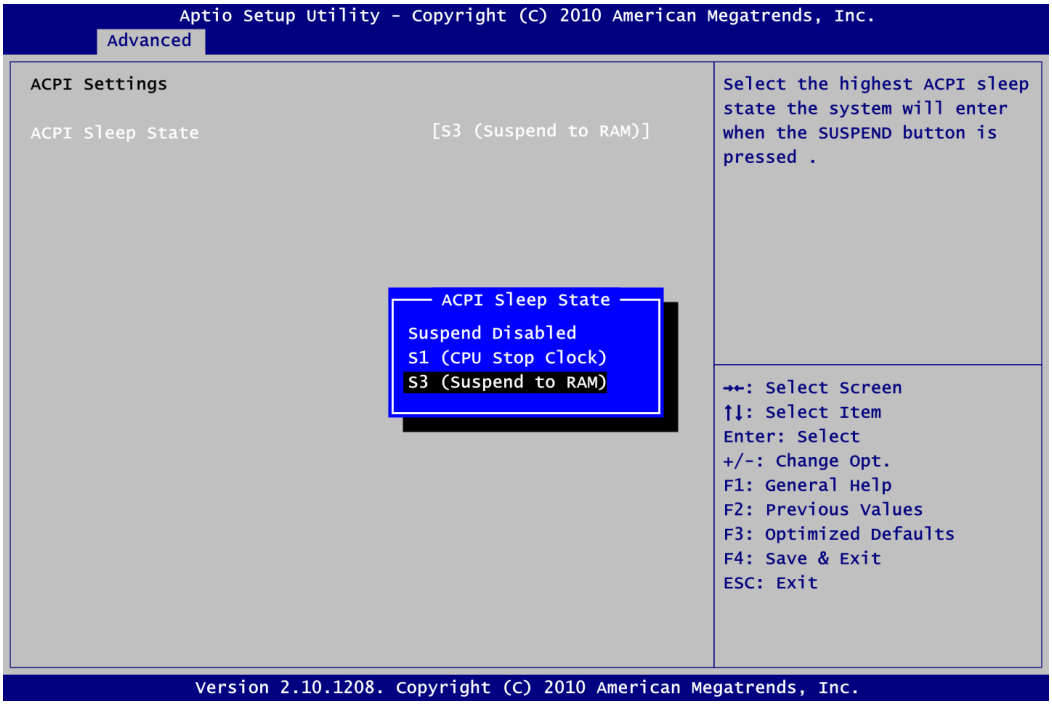
The Advanced menu also allows users to set configuration of the CPU and other system devices. You can select any of the items in the left frame of the screen to go to the sub menus:

- ► ACPI Settings
- ► Trusted Computing
- ► CPU Configuration
- ► SATA Configuration
- ► PCH-FW Configuration
- ► USB Configuration
- ► H/W Monitor
- ► Super IO Configuration

For items marked with "►", please press <Enter> for more options.

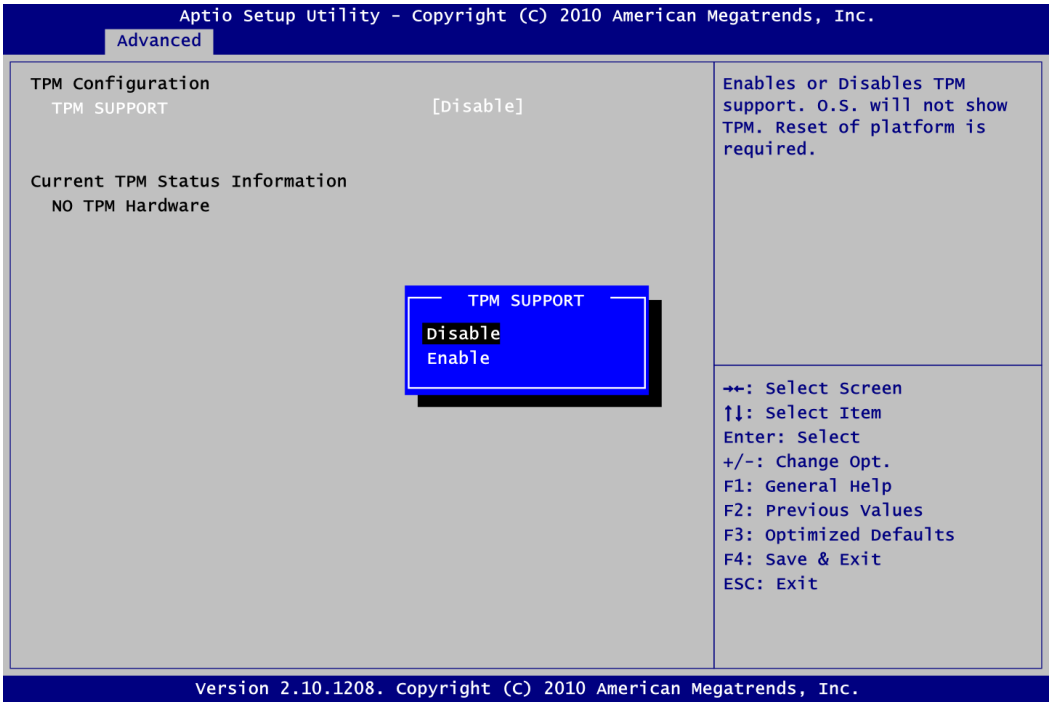


- **ACPI Settings**
  You can use this screen to select options for the ACPI configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen.



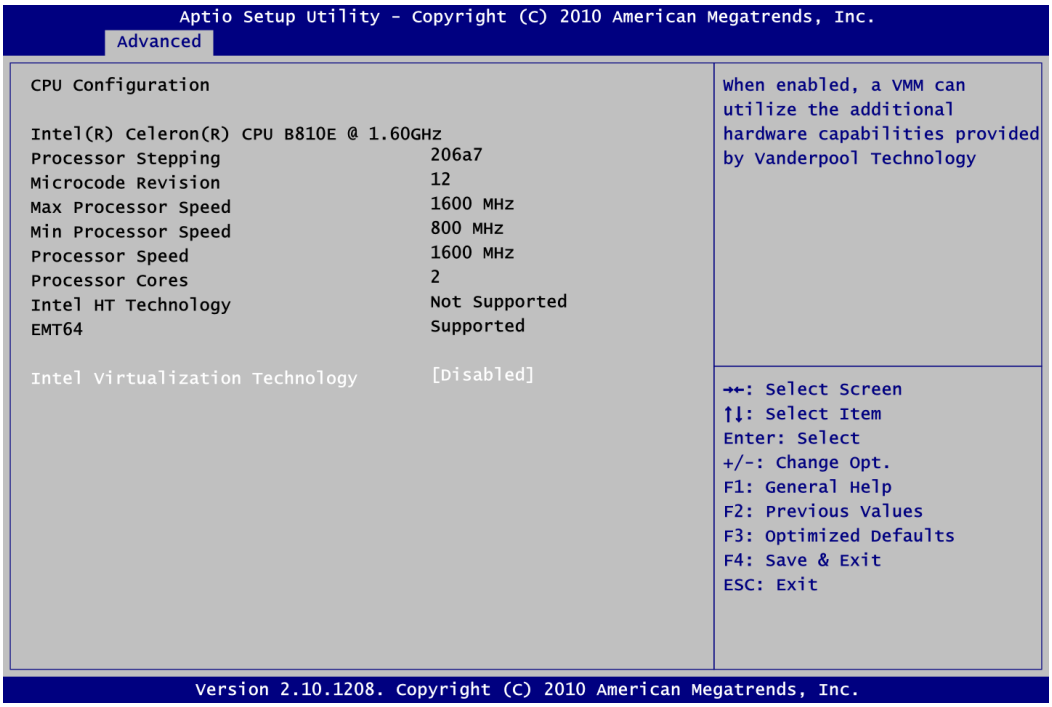
ACPI Sleep State
Allow you to select the Advanced Configuration and Power Interface (ACPI) sleep state. Here are the options for your selection; Suspend Disabled, S1 (CPU Stop Clock) and S3 (Suspend to RAM). The S3 (Suspend to RAM) option selects the highest ACPI sleep state the system will enter when SUSPEND button is pressed.

- **Trusted Computing**
  You can use this screen for TPM configuration. It also shows current TPM status information.



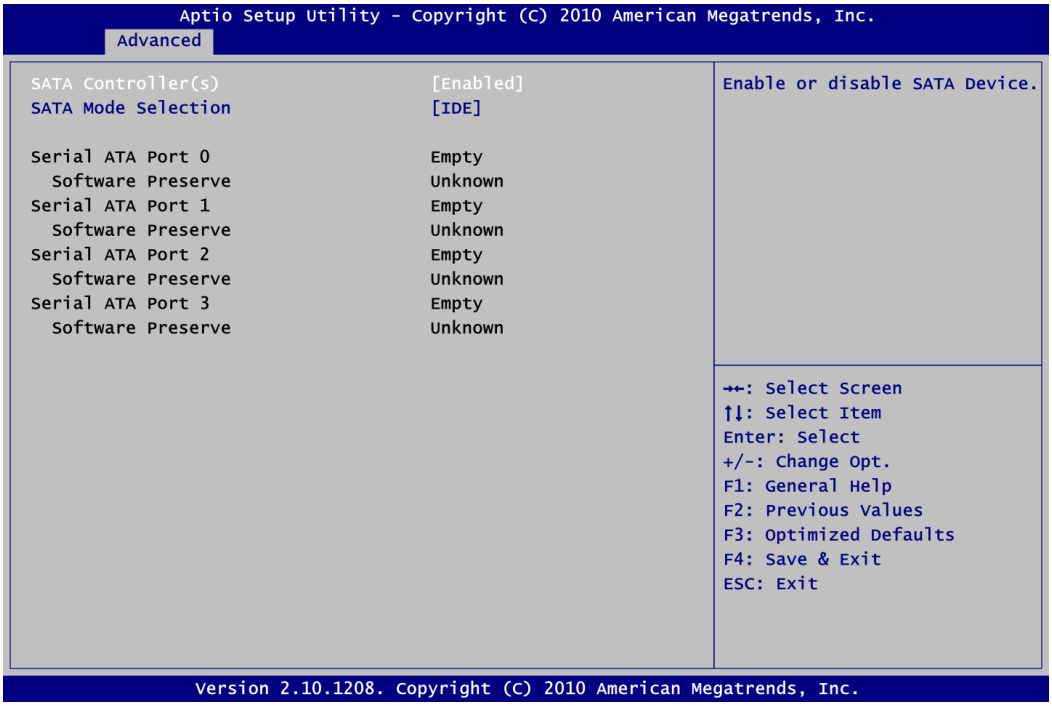
TPM Support
Allow you to enable or disable TPM support. Operating system will not show TPM. Reset of platform is required.

- **CPU Configuration**
  This screen shows the CPU Configuration, and you can change the value of the selected option.



Intel Virtualization Technology
Allow you to enable or disable Intel Virtualization Technology. When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology .

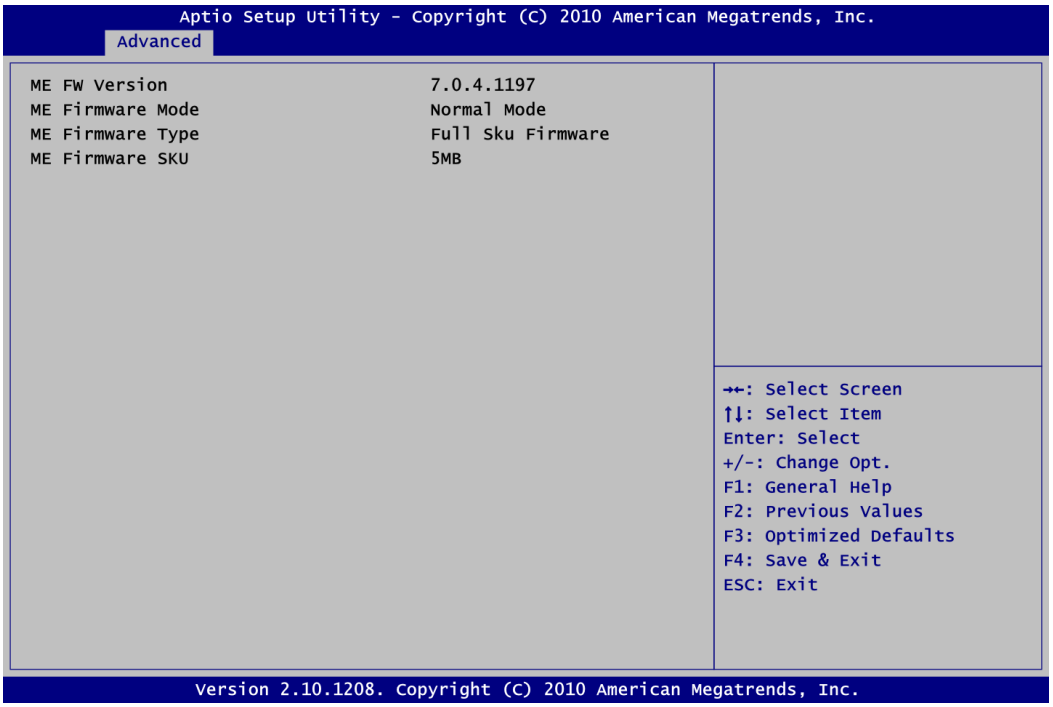
- **SATA Configuration**
  In the SATA Configuration menu, you can see the currently installed hardware in the SATA ports. During system boot up, the BIOS automatically detects the presence of SATA devices.



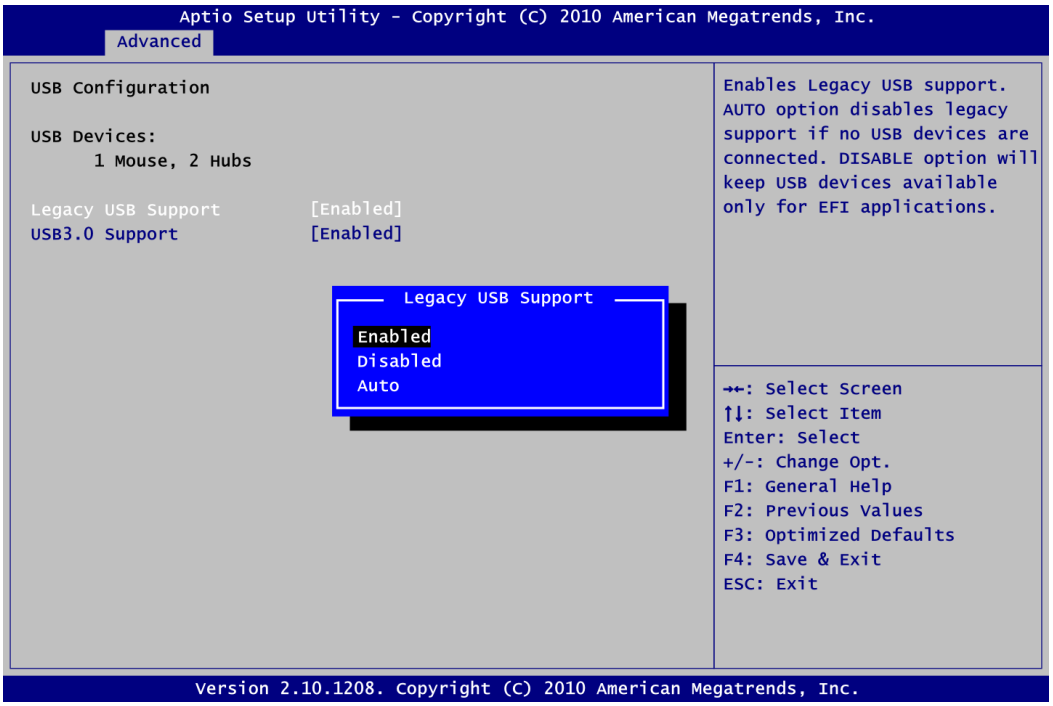
SATA Controller(s)
Use this item to enable or disable SATA device.

SATA Mode Selection
Use this item to choose the SATA operation mode. Here are the options for your selection; IDE Mode, AHCI Mode and RAID Mode.

- **PCH-FW Configuration**
  This screen shows ME firmware information: ME firmware version, mode, type and SKU.



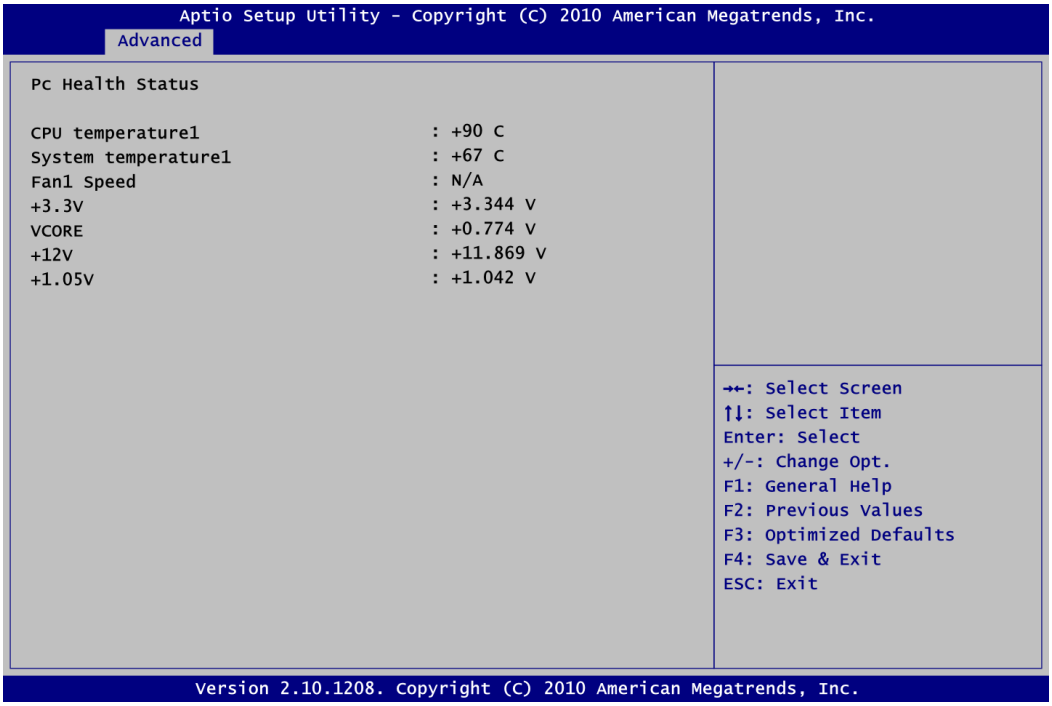
- **USB Configuration**
  You can use this screen to select options for the USB Configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen.



Legacy USB Support
Use this item to enable or disable support for USB device on legacy operating system. The default setting is Enabled. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications.

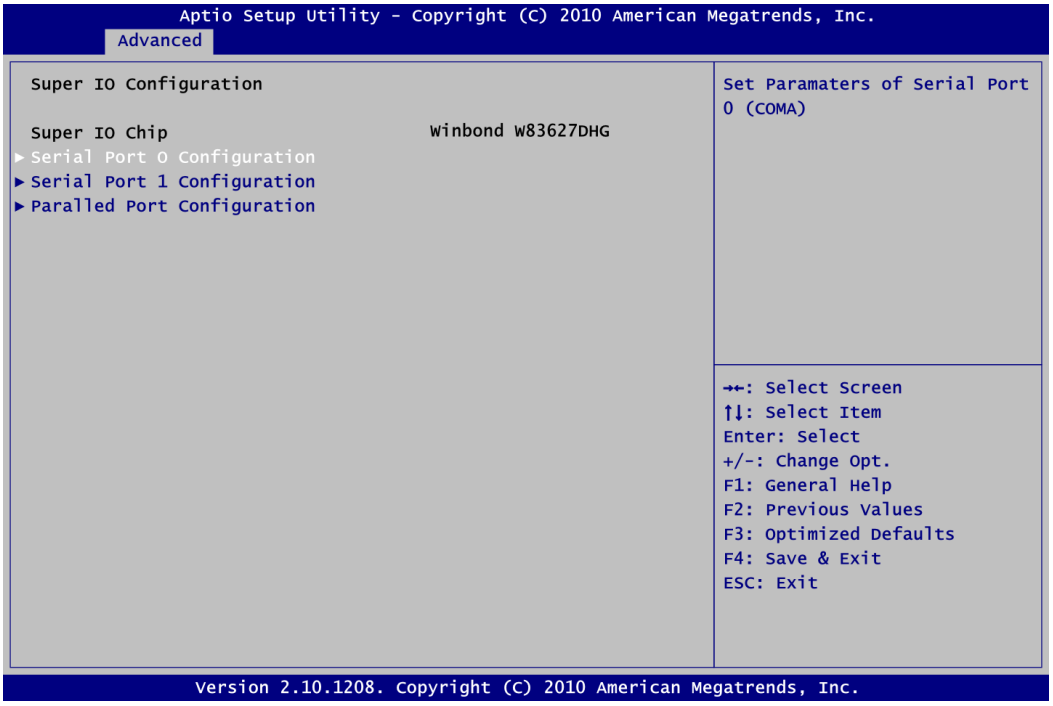
USB 3.0 Support
Use this item to enable or disable support for USB 3.0.

- **H/W Monitor**
  This screen monitors hardware health.

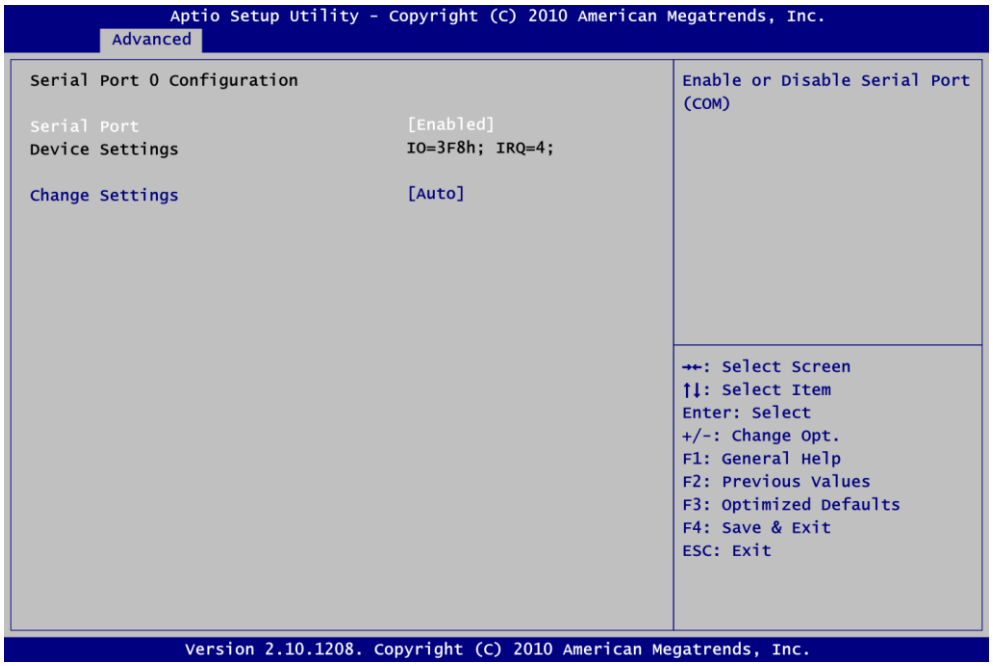


This screen displays the temperature of system and CPU, cooling fan speed in RPM and system voltages (+3.3V, VCORE, +12V and +1.05V).

- **Super IO Configuration**
  You can use this screen to select options for the Super IO Configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen. For items marked with "▶", please press <Enter> for more options.

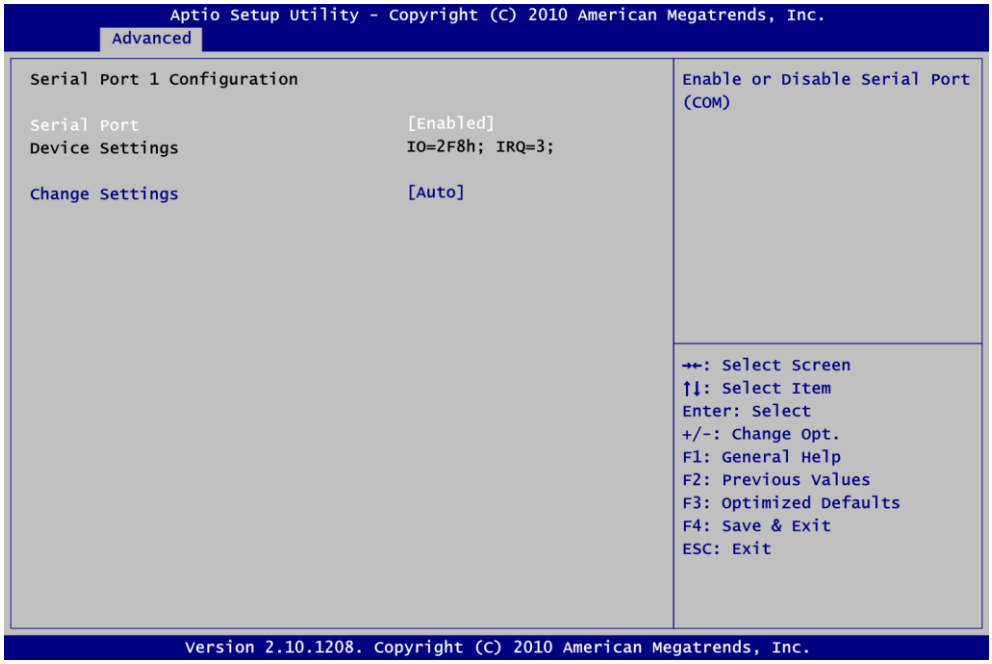


  - **Serial Port 0 Configuration**



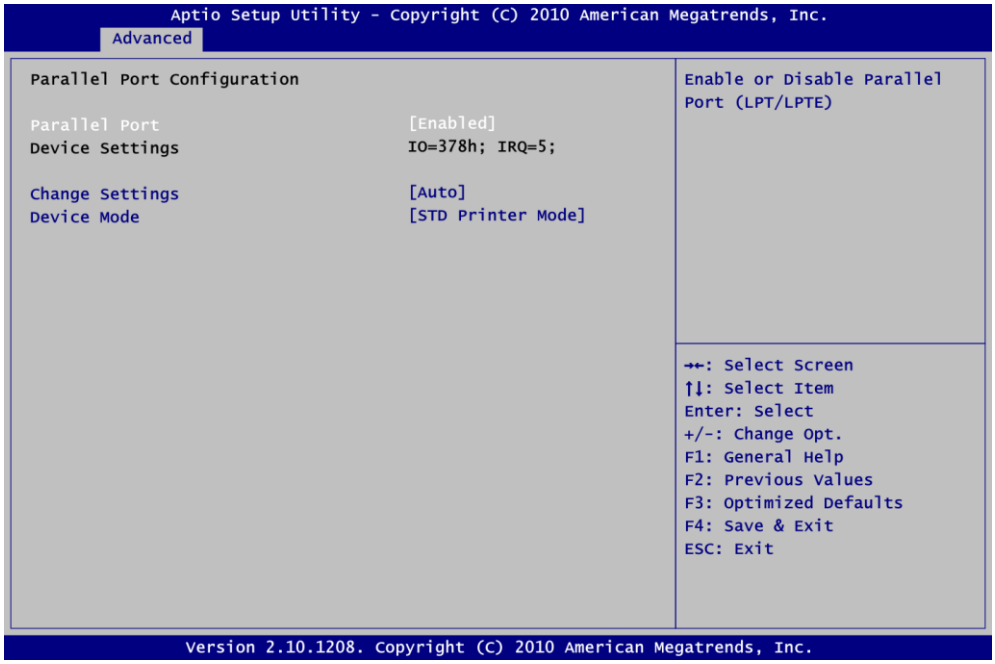
Serial Port
Use this item to enable or disable serial port 0. The optimal setting for base I/O address is 3F8h and for interrupt request line is IRQ4.

- **Serial Port 1 Configuration**



Serial Port
Use this item to enable or disable serial port 1. The optimal setting for base I/O address is 2F8h and for interrupt request line is IRQ3.

- **Parallel Port Configuration**



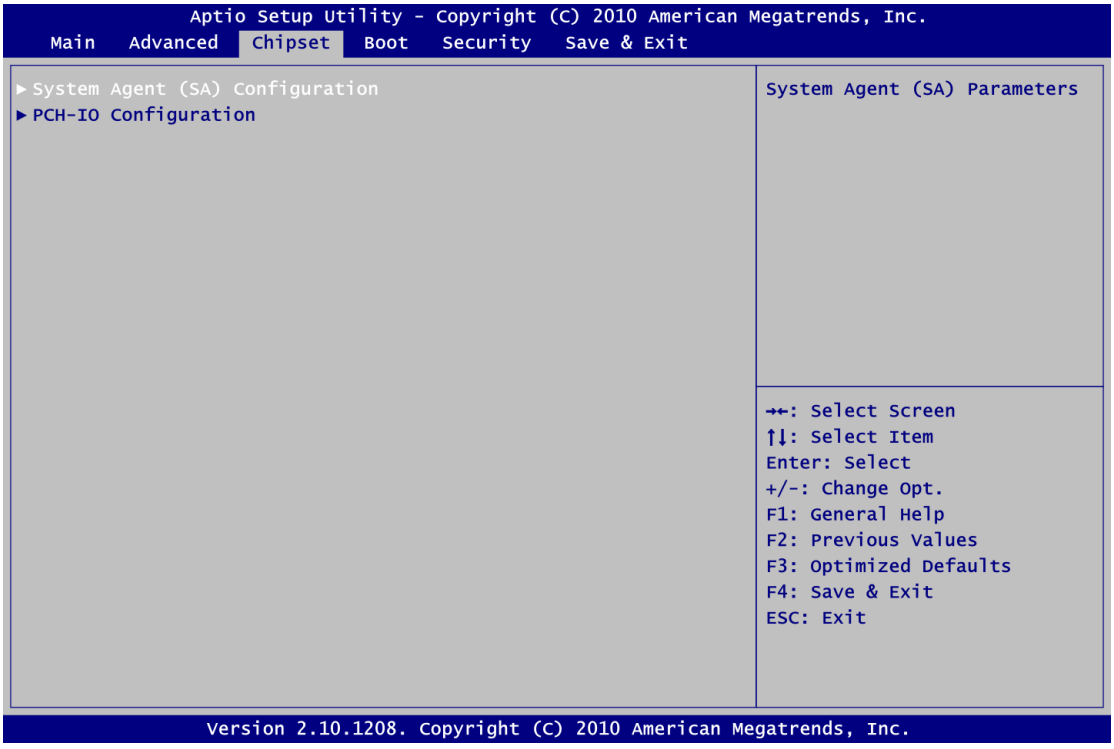
Parallel Port
Use this item to enable or disable parallel port (LPT/LPTE). The optimal setting for base I/O address is 378h and for interrupt request line is IRQ5.

4.5 Chipset Menu

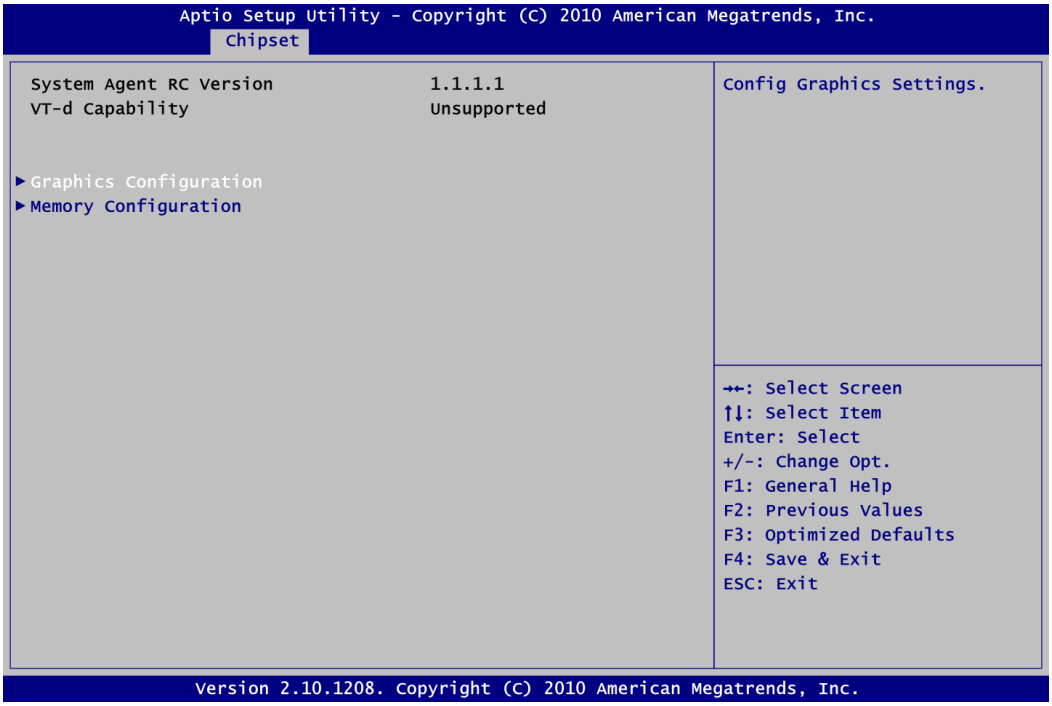
The Chipset menu allows users to change the advanced chipset settings. You can select any of the items in the left frame of the screen to go to the sub menus:

- ► System Agent (SA) Configuration
- ► PCH-IO Configuration

For items marked with "►", please press <Enter> for more options.



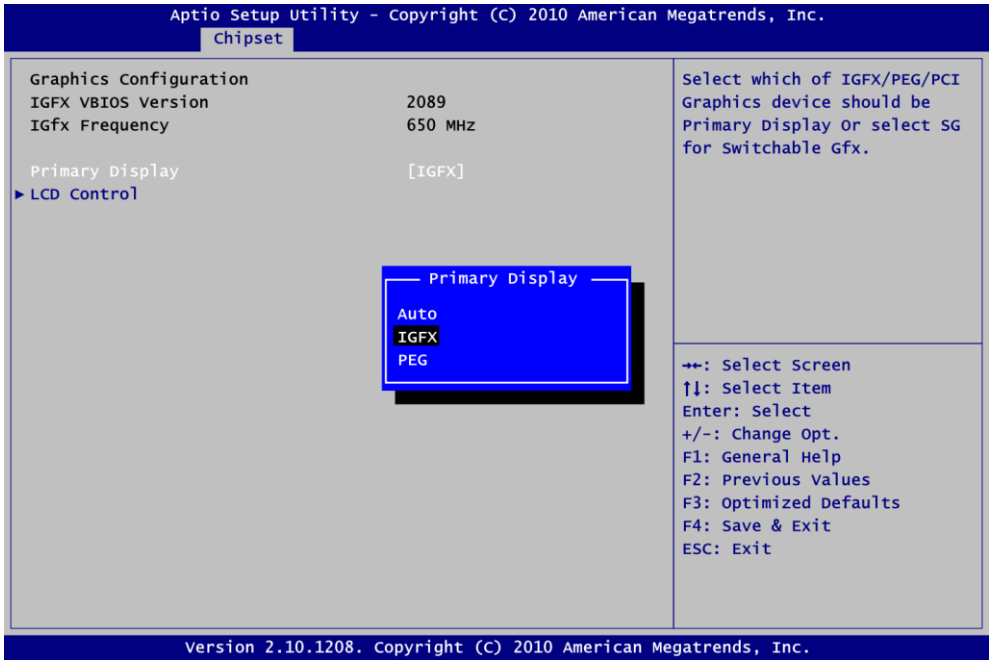
- **System Agent (SA) Configuration**
  This screen allows users to configure System Agent (SA) parameters. For items marked with "►", please press <Enter> for more options.



Graphics Configuration
Use this item for further setting of graphics configuration.

Memory Configuration
This option allows user to set memory configuration.

- **Graphics Configuration**

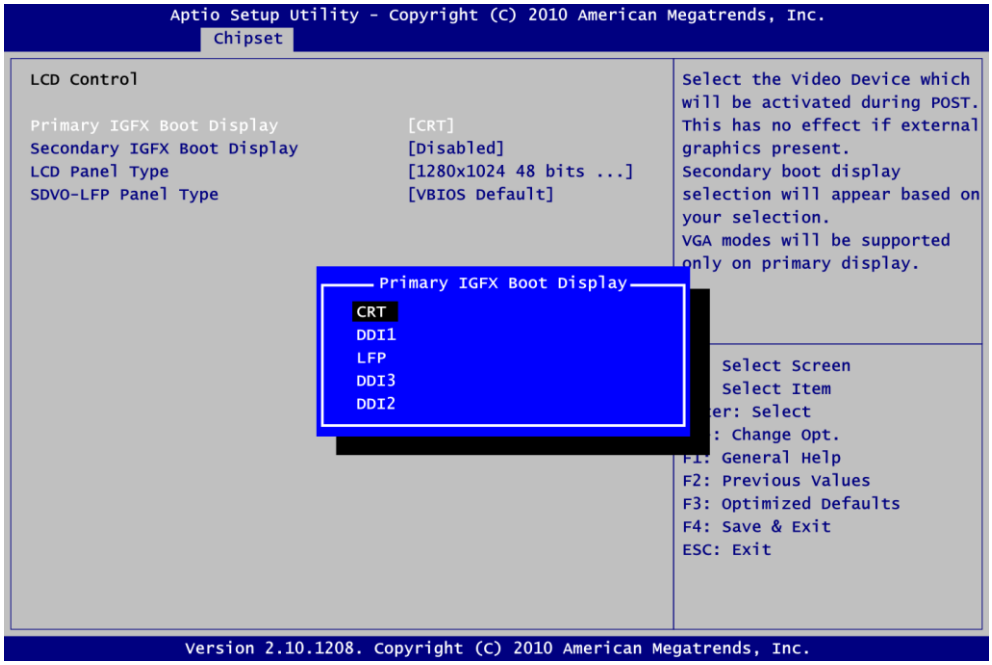


Primary Display
Select which of IGFX/PEG/PCI graphics device should be primary display. Or select SG for switchable Gfx.

LCD Control
This item allows you to select panel control options. Please press <Enter> to go to the sub menus.

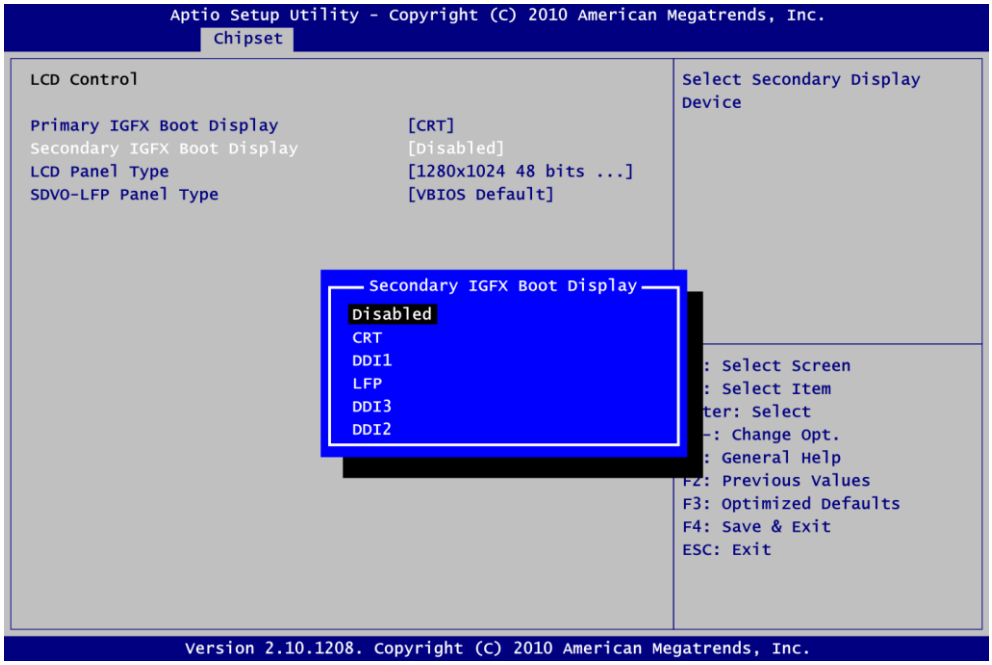
Primary IGFX Boot Display

Allow you to select the video device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display. Here are the options for your selection; CRT, DDI1, LFP, DDI3 and DDI2.



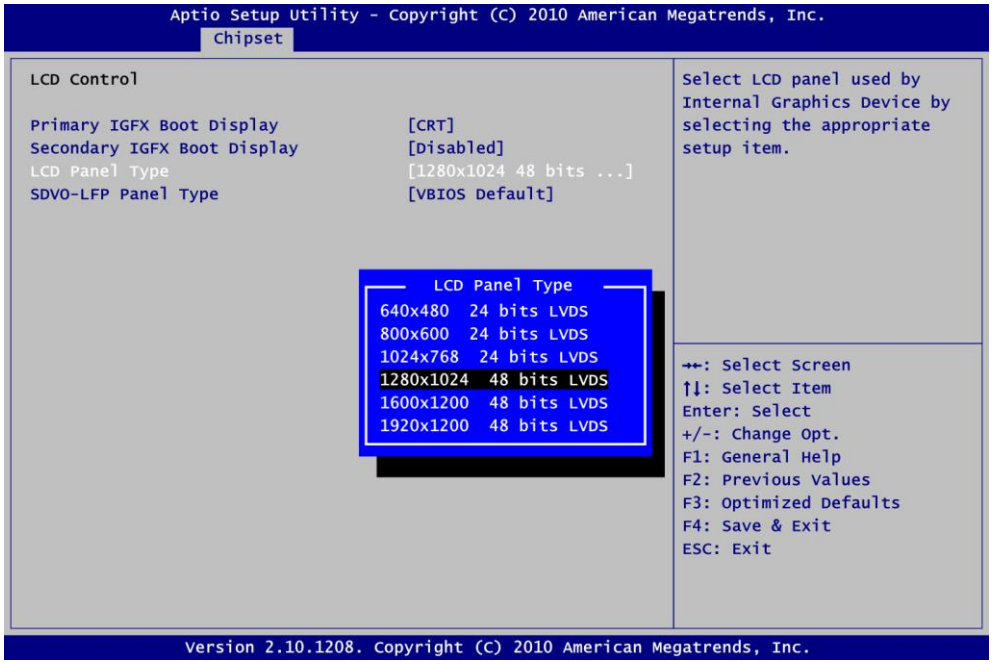
Secondary IGFX Boot Display

Use this option to select secondary display device. Here are the options for your selection; Disabled, CRT, DDI1, LFP, DDI3 and DDI2.



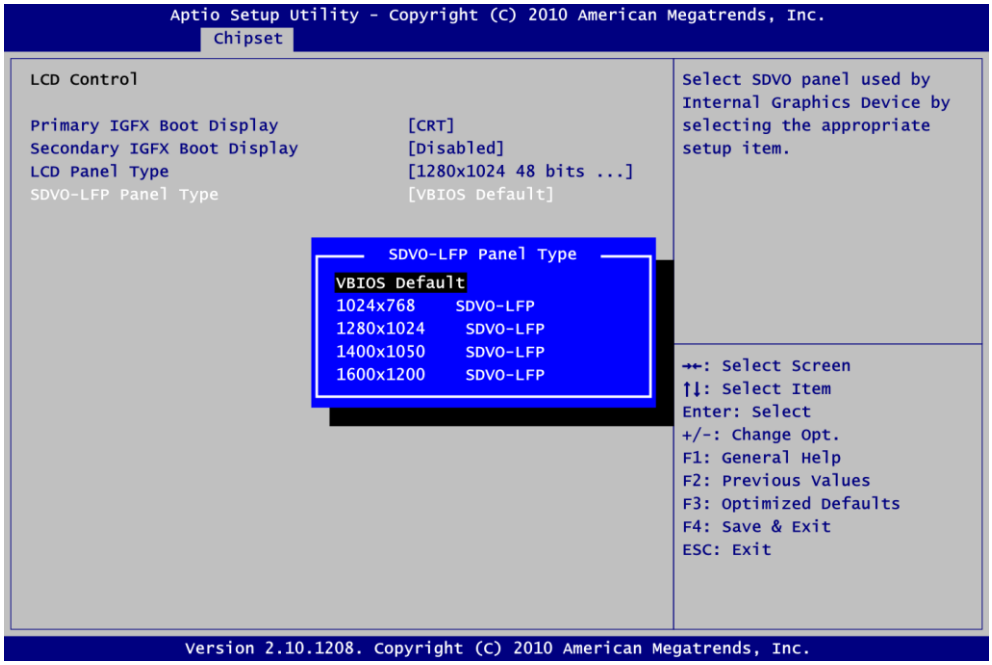
LCD Panel Type

Use this option to select LCD panel used by internal graphics device by selecting the appropriate setup item. Please refer to below image for available LCD panel type options.

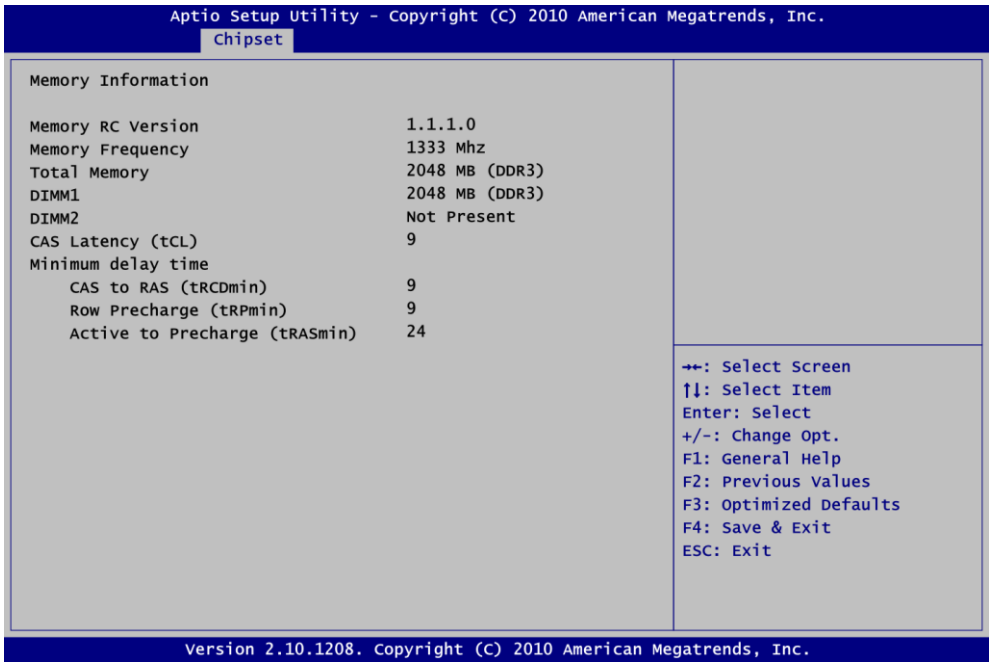


SDVO-LFP Panel Type

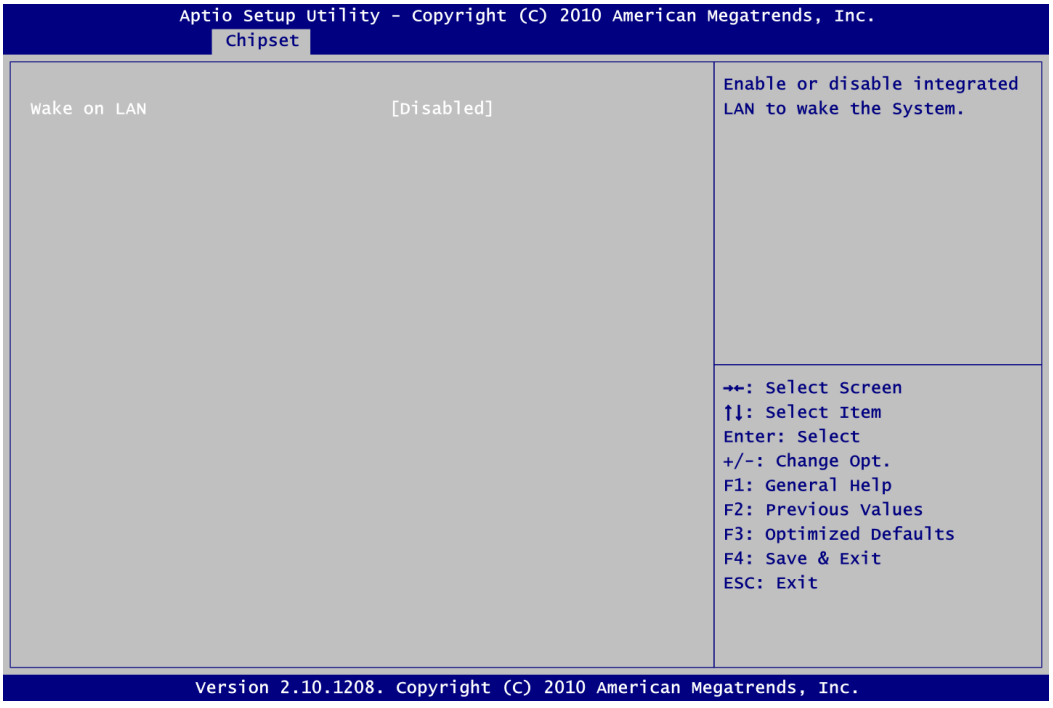
Use this option to select SDVO panel used by internal graphics device by selecting the appropriate setup item. Please refer to below image for available SDVO panel type options.



- **Memory Configuration**
  This screen displays memory information.



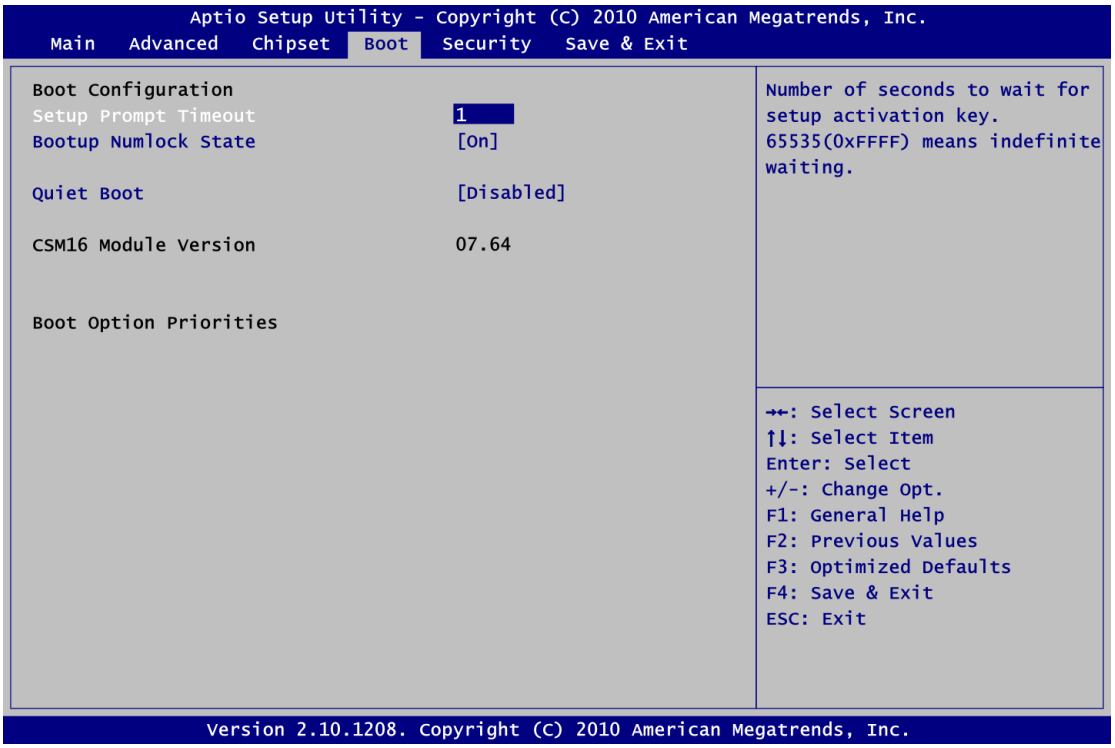
- **PCH-IO Configuration**



Wake on LAN
This option allows user to enable or disable integrated LAN to wake the system.

4.6 Boot Menu

The Boot menu allows users to change boot options of the system.



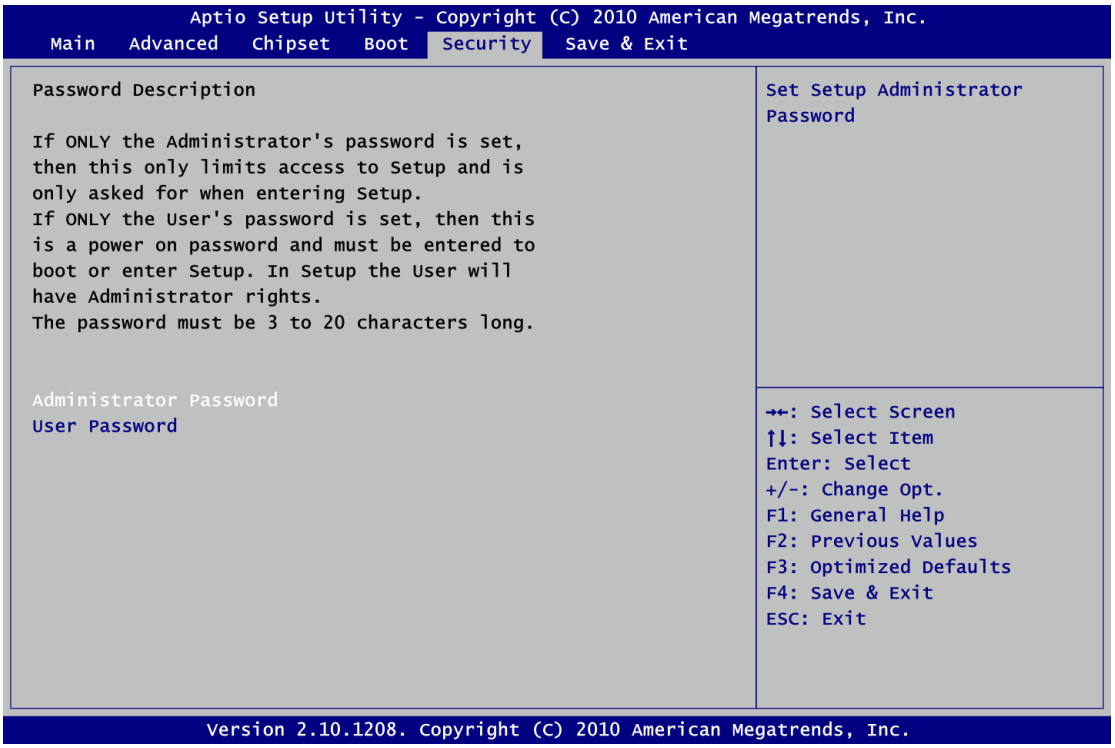
- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

- **Bootup NumLock State**
  Use this item to select the power-on state for the NumLock.

- **Quiet Boot**
  Enable or disable Quiet Boot option.

4.7 Security Menu

The Security menu allows users to change the security settings for the system.

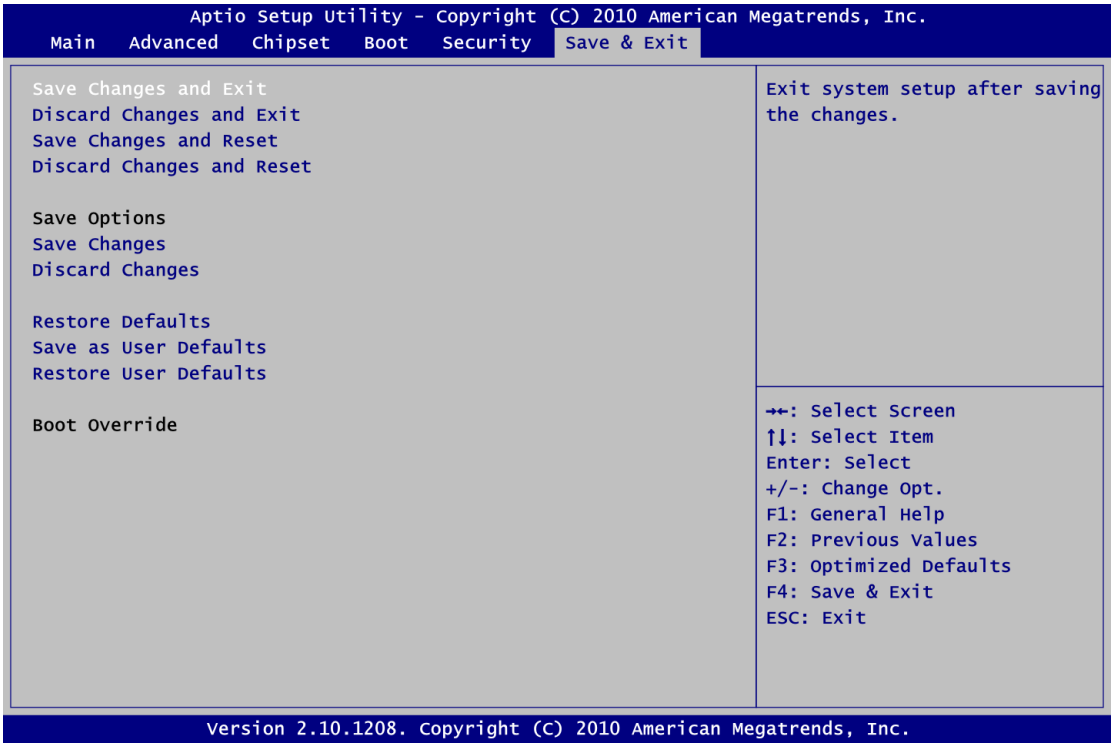


- **Administrator Password**
  This item indicates whether an administrator password has been set (installed or uninstalled).

- **User Password**
  This item indicates whether an user password has been set (installed or uninstalled).

4.8 Save & Exit Menu

The Save & Exit menu allows users to load your system configuration with optimal or fail-safe default values.



- **Save Changes and Exit**
  When you have completed the system configuration changes, select this option to leave Setup and return to Main Menu. Select Save Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to save changes and exit.

- **Discard Changes and Exit**
  Select this option to quit Setup without making any permanent changes to the system configuration and return to Main Menu. Select Discard Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to discard changes and exit.

- **Save Changes and Reset**
  When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Save Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to save changes and reset.

- **Discard Changes and Reset**
  Select this option to quit Setup without making any permanent changes to the system configuration and reboot the computer. Select Discard Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to discard changes and reset.

- **Save Changes**
  When you have completed the system configuration changes, select this option to save changes. Select Save Changes from the Save & Exit menu and press <Enter>. Select Yes to save changes.

- **Discard Changes**
  Select this option to quit Setup without making any permanent changes to the system configuration. Select Discard Changes from the Save & Exit menu and press <Enter>. Select Yes to discard changes.

- **Restore Defaults**
  It automatically sets all Setup options to a complete set of default settings when you select this option. Select Restore Defaults from the Save & Exit menu and press <Enter>.

- **Save as User Defaults**
  Select this option to save system configuration changes done so far as User Defaults. Select Save as User Defaults from the Save & Exit menu and press <Enter>.

- **Restore User Defaults**
  It automatically sets all Setup options to a complete set of User Defaults when you select this option. Select Restore User Defaults from the Save & Exit menu and press <Enter>.

Appendix A
Watchdog Timer and GPIO

About Watchdog Timer

Software stability is major issue in most application. Some embedded systems are not watched by human for 24 hours. It is usually too slow to wait for someone to reboot when computer hangs. The systems need to be able to reset automatically when things go wrong. The watchdog timer gives us solution.

The watchdog timer is a counter that triggers a system reset when it counts down to zero from a preset value. The software starts counter with an initial value and must reset it periodically. If the counter ever reaches zero which means the software has crashed, the system will reboot.

About GPIO

The onboard GPIO (general input and output) has 8 bits (GPI0~3 and GPO0~3). In default, all pins are pulled high with +3.3V level (according to main power). The BIOS default settings are 4 inputs and 4 outputs where all of these pins are set to 1. Use these GPIO signals to control cash drawers and sense warning signals from an Uninterrupted Power System (UPS), or perform store security control.

Sample Program

Programming sample code (from CEM860 FINTEK F75111R):

```
/*---------------- INCLUDE FILE ----------------------*/
#include <stdio.h>
#include <conio.h>
#include <bios.h>

#define UCHAR   unsigned char
#define UINT    unsigned int
#define SMIOBASE      0xF040
/******************
       SMIOBASE can get from PCI device Bus-0,Device-31, Function-3
       Register 20h~23h, the value is the IO base address.
*******************/
#define SM_REG         (SMIOBASE+3)
#define SM_ADDR        (SMIOBASE+4)
#define SM_DATA        (SMIOBASE+5)
#define SM_CMD         (SMIOBASE+2)
#define SM_STATUS      (SMIOBASE+0)
#define SM_byteAccess 0x48
#define Device_Addr    0x6E  // depend on hardware designed Low:0x9C, High:0x6E
UCHAR _read_smbus(UCHAR ,UCHAR);
void _write_smbus(UCHAR,UCHAR, UCHAR);
#define F75111_CHIPID           0x0003
#define F75111_VENDORID         0x3419
#define WDTOUT10_CntlReg1       0x34
#define WDTOUT10_2S_bit         0x04    //bit 2
#define WDTOUT10_OINV_bit       0x02    //bit 1
#define WDTOUT10_Status_bit     0x01    //bit 0 , write 1 for clear status
#define WDTOUT10_CntlReg2       0x35
#define WDTOUT10_Enable_bit     0x80    //bit 7
#define WDTOUT10_PTIME          0x7f    //bit 0~6
```

```
/* ------------------ MAIN PROGRAM -------------------*/
main()
{
UCHAR   xch,xch2;
UINT    chipid=0, vendorid=0;
       //Check the Chip ID information
       xch=_read_smbus(Device_Addr,0x5a);     //Chip ID 1
       xch2=_read_smbus(Device_Addr,0x5b);    //Chip ID 2
       chipid=((UINT)xch2 << 8) + (UINT)xch;
       xch=_read_smbus(Device_Addr,0x5d);     //Vendor ID 1
       xch2=_read_smbus(Device_Addr,0x5E);    //Vendor ID 2
       vendorid=((UINT)xch2 << 8) + (UINT)xch;
       if (F75111_CHIPID != chipid || F75111_VENDORID != vendorid )
         { printf("!!! Not found F75111 chip !!!\n");
           exit(-1);
         }
       printf("=== Found F75111 chip ===\n");
       printf("=== GPIO Output Test ===\n");

       //set GPIO3x  direction
       printf("Set F75111 GPIO3x pin is output direction\n");
       _write_smbus(Device_Addr,0x40,0x0f);   //GPIO3x Output direction

       //set GPIO3x output level or plus
       printf("Set F75111 GPIO3x pin is output Level\n");
       _write_smbus(Device_Addr,0x43,0);      //GPIO3x Level control

       //write GPIO3x data
       printf("Write GPIO3x data is 0x0A\n");
       printf("GPO0=0, GPO1=1, GPO2=0, GPO3=1\n");
       _write_smbus(Device_Addr,0x41,0x0a);
       printf("Please check the GPO level and hit any key to continue\n");
       getch();

       //write GPIO3x data
       printf("Write GPIO3x data is 0x05\n");
       printf("GPO0=1, GPO1=0, GPO2=1, GPO3=0\n");
       _write_smbus(Device_Addr,0x41,0x05);
       printf("Please check the GPO level and hit any key to continue\n");
       getch();


       //set GPIO10,11,12 used
       printf("=== GPIO Input Test ===\n");
       printf("Set F75111 GPIO1x is used GPIO function\n");
       xch=_read_smbus(Device_Addr,0x03);
       xch &= 0xE0 ;
       _write_smbus(Device_Addr,0x03,xch);    //set Pin GPIO10/11/12 used
       _write_smbus(Device_Addr,0x04,0);      //set Pin GPIO1x used

       printf("Set F75111 GPIO10,11,12,13 is input function\n");
       _write_smbus(Device_Addr,0x10,0x00);   //set GPIO1x input direction

       printf("Set F75111 GPIO10,11,12,13 is Level mode\n");
       _write_smbus(Device_Addr,0x13,0x00);   //set GPIO1x Level Control

       xch=_read_smbus(Device_Addr,0x12);     //read GPIO1x Status
       printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
       printf("Please Change the GPIx input and hit any key to continue\n");
       getch();
       xch=_read_smbus(Device_Addr,0x12);     //read GPIO1x Status
       printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
       printf("Please Change the GPIx input and hit any key to continue\n");
       getch();
       xch=_read_smbus(Device_Addr,0x12);     //read GPIO1x Status
       printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
       /*****************************************/
       printf("===== WatchDogTimer Test =====\n");
       printf("Set WDTOUT10 pin used\n");
       _write_smbus(Device_Addr,0x01,0x20);   //Pin1 config

       printf("Set WDTOUT10 output 100ms plus, normal level\n");
       _write_smbus(Device_Addr,WDTOUT10_CntlReg1,0);      //WDT10 control

       printf("Set WDTOUT10 Time 10 seconds and enable WDT\n");
       _write_smbus(Device_Addr,WDTOUT10_CntlReg2,0x8A);   //WDT10 control
```

```
        printf("Please hit any key in period of 10 seconds\n");
        getch();
        _write_smbus(Device_Addr,WDTOUT10_CntlReg2,0x8A);   //WDT10 control
        printf("The sytsem will reset when the 10 seconds times out\n");
}

void _write_smbus(UCHAR xAddr,UCHAR xReg, UCHAR xData)
{
        while (1)
        { if (_check_smbus_busy()==0) break;
        }
        outp(SM_REG, xReg);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_ADDR, xAddr);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_DATA, xData);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_CMD, SM_byteAccess);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_STATUS, 02); //clear interrupt status
}

UCHAR _read_smbus(UCHAR xAddr,UCHAR xReg)
{
UCHAR   xch,xch2;
        while (1)
        { if (_check_smbus_busy()==0) break;
        }
        outp(SM_REG, xReg);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_ADDR, xAddr+1);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_CMD, SM_byteAccess);
        xdelay();             //because the CPU too fast,delay for IO
        while (1)
        { if (_check_smbus_busy()==0) break;
        }
        xch=inp(SM_DATA);
        xdelay();             //because the CPU too fast,delay for IO
        outp(SM_STATUS, 2);  //clear interrupt status
        return xch;
}

_check_smbus_busy(void)
{
UCHAR   xch;
        xch=inp(SM_STATUS);
        if (xch & 0x02 ) outp(SM_STATUS, 2);   //clear interrupt status
        if ( xch & 0x02 ) return 1;
        if ( xch & 0x01 ) return 1;
        return 0;
}

xdelay()
{
int     xxi,xxj,xxk=0;
        for (xxi=0 ; xxi< 0x1000 ; xxi++) {
                for (xxj=0 ; xxj < 0x100 ; xxj++) {
                        xxk++;
                }
        }
}
```