MBus: A 17.5 pJ/bit/chip Portable Interconnect Bus for Millimeter-Scale Sensor Systems with 8 nW Standby Power

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***Abstract* — We propose an ultra-low power interconnect bus for millimeter-scale wireless sensor nodes. Using only 4 IO pads, the bus minimizes the required chip real estate, enabling ultra-small form factors in modular sensor node designs. Low power is achieved using a "clockless" design of member nodes while aggressive power gating allows an ultra-low power standby mode with only 53 gates powered on. An integrated wakeup scheme is compatible with PMUs that have a special low power standby mode. The MBus is fully synthesizable and uses robust timing. Implemented in a 3 module system in 180nm technology, Mbus achieves 8nW of standby power and 17.5 pJ/bit/chip.**

***Index Terms* — Wireless sensor nodes, sensor systems, data buses, interconnections.**

Introduction

Continued advances in ultra-low power circuit techniques have steadily moved the next generation of computer systems towards the vision of "smart dust" – a miniature, integrated sensing, computing, storage, and communication platform [1]. These systems are highly optimized in volume and power draw, targeting a mm^3 form factor and running on single digit µW in active mode and nW in standby mode [2]. Early efforts [1][3] to realize such systems have resulted in monolithic and tightly integrated designs, with little capability for reuse. This design approach is in contrast to the modularity that has characterized embedded systems design and enabled it to address a highly diverse application space. The miniature sensor node application space is similarly diverse, ranging from implantable medical monitors to nearly invisible surveillance, to infrastructure monitoring. Hence, a modular design approach that enables extensive reuse of chip modules is key to fully address its application space.

A critical component in a modular platform is the bus through which the different modules communicate with each other. However, existing bus standards do not address the unique constraints of millimeter-scale sensor systems. We will show that the number of wires required in SPI [4] make it difficult to meet the millimeter size constraint while the power consumption of I^2C [5] is orders of magnitude higher than the allowed power budget. Recently, a low power variant of I^2C [6] was proposed for a modular millimeter sensor node, shown in Fig. 1, right. The system consists of several stacked chip layers, each performing a key function (e.g, processor, memory, sensor interface, radio, etc.). However, the proposed bus requires careful matching of timing between nodes reducing robustness as well as requiring custom design, limiting portability.

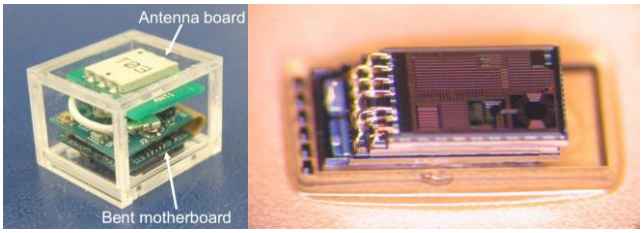

Figure 1. 1cc computer [3] (left) and a 2.2×1.1×0.8 mm stacked miniature wireless sensor node [6] (right).

To address the unique constraints of millimeter-scale sensor nodes, we propose a new chip-to-chip bus interconnect, referred to as *MBus*, that is as conservative with resources as the modules it connects. MBus nodes are arranged in a ring topology, support multi-master communication, and use highly robust, fully synthesizable signaling. MBus uses only 4 IO pads, provides predictable latency, and features a novel, robust reset mechanism. To address the extreme low power constraints, member nodes in MBus are "clockless". Also, all but 53 gates are power gated in standby mode while still enabling any node to wake up the entire system and switch the Power Management Unit (PMU) to active power mode. We present silicon measurements of a 3 layer sensor system implemented in 180 nm technology and achieve >10Mb/s data rate, with 17.55 pJ/bit/chip and 8 nW standby power.

System Interconnect Design Requirements

In this section, we introduce the key design requirements for supporting ultra space-constrained systems and why this poses a unique challenge requiring a new bus interface.

Low, fixed wire count per node. The target systems are highly space-constrained and even state-of-the-art wire bonding techniques require at least 35~65 µm/pad. When accounting for several power supply voltages and a few module-specific IOs, only a handful of pads remain for the bus interface in a 1 mm form factor. This makes the use of serial buses, such as SPI [4], difficult since they require a dedicated chip-select line for each component in the system. Hence, the maximum number of components needs to be anticipated ahead of time, often resulting in over-provisioning and a large total pad area. For instance, in a moderate 10 node system, the SPI controller would require at least 14 bus pads, which is impossible to realize in a millimeter-scale system.

Low active power. A viable interface cannot dominate the µW power budget of millimeter sensors. This eliminates any pad-efficient open drain-based designs that allow bi-

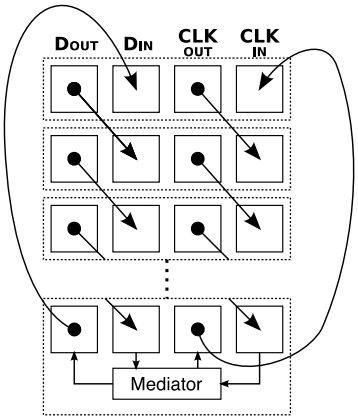

Figure 2. MBus topology. Each node has D_{OUT}, D_{IN}, CLK_{OUT}, and CLK_{IN} and they form a ring.

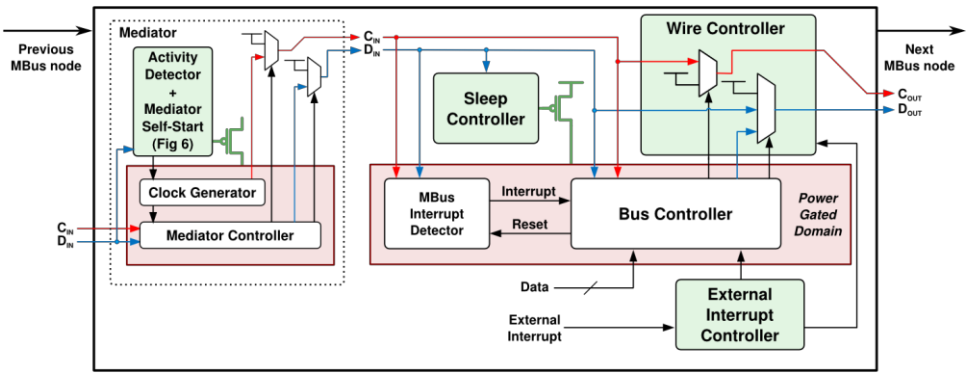

Figure 3. MBus ecosystem. The red shaded areas are power-gated domains, which are the core of MBus. The rest of the components are always powered on and optimized for low-leakage to reduce standby power. Only one node has a mediator block.

directional wires, due to high active power. For instance, I^2C [5] requires only 4 pads per module, but uses a kΩ-range pull-up resistor resulting in 100's of µW of power draw, which is 100× the typical power budget of a millimeter-scale sensor node.

Standby power management. In standby mode, power consumption must be reduced to the nW range to enable long lifetimes with millimeter batteries and perpetual operation with harvesting. This requires aggressive power gating and a PMU that can switch to an ultra-low, nW power mode. To avoid additional wires for communicating wakeup events, the bus interface must support a wakeup request originating from any node. This poses two challenges: 1) The logic that monitors/transmits such an event must be minimized since it remains always active and directly contributes to the standby power; 2) When the wakeup request is transmitted in the bus, the PMU is still in standby mode, meaning that active current draw used for this transmission cannot exceed the nA range.

Fully synthesizable. Use of custom designed components significantly increases time and effort to migrate between technologies and impedes adoption. For example, the I^2C variant in [6] used custom drivers, ratioed logic, and delay chains that require post-silicon tuning. A synthesizable bus interface not only allows fast design by "dropping-in" fully verified Verilog, it also ensures robust timing which is automatically checked by tools. However, disallowing more complex circuit structures increases the challenges to meet the low wire-count and power draw requirements.

Systems Constraints. Finally, to be a viable system bus, MBus must provide multi-master operation, a robust reset mechanism, and data- and device-independent behavior.

Design & Implementation

Each MBus node has four signals: D_{OUT}, D_{IN}, CLK_{OUT}, and CLK_{IN}. MBus nodes are arranged in ring topology, as shown in Fig. 2, connecting D_{OUT}/CLK_{OUT} to the next node's D_{IN}/CLK_{IN} and eventually looping back. Signals "shoot-through", and nodes have no local clock. One node must be a MBus *mediator* module. The mediator is responsible for generating the bus clock and mediating arbitration. While the bus is idle, regular nodes forward both DATA and CLK. The mediator breaks the loop by fixing both CLK_{OUT} and D_{OUT} high in idle/standby mode. To provide a robust, reliable in-band, data-independent reset, MBus nodes feature a separate *Interrupt Detector* block that identifies an *MBus Interrupt*: At least three edges on DATA with no CLK edges. Fig. 3 shows the functional diagram of a single MBus node.

A. Circuit Design

Low active power. Only the MBus mediator node has a clock while all regular MBus node are clock-less. Flip-flops in MBus nodes are purely triggered by CLK_{IN}. Hence, if the MBus is idle, regular nodes draw only static leakage power. This is key since addition of a simple clock generator to each regular node will quickly dominate total power consumption. Second, only a small address detector is permanently clocked by CLK_{IN} and observes the D_{IN} signal to determine if the node is being addressed. Hence, if a node is not receiving a message, it directly forwards D_{IN}/CLK_{IN} to D_{OUT}/CLK_{OUT} and any internal flip-flops used to store/process incoming data do not toggle, reducing power consumption by 23%.

Robust timing. In a modular system, the loading and driving strength of different D_{OUT}/CLK_{OUT} drivers is unpredictable, creating uncertainty in the relative arrival time of D_{IN}/CLK_{IN}. This requires insertion of a large number of hold-time buffers, which would increase power and lower performance. Instead, we separate driving and latching edges to balance setup and hold time margins (Fig. 4). D_{IN} is sampled on positive CLK_{IN} edge and D_{OUT} is driven on negative CLK_{IN} edge. While this also reduces maximum performance it ensures that hold time scales with frequency, ensuring robust operation via sufficient frequency scaling.

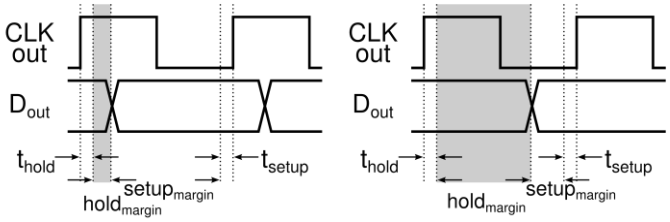

Figure 4. Setup/hold time diagram. Conventional positive edge trigger (left) and MBus clocking (right).

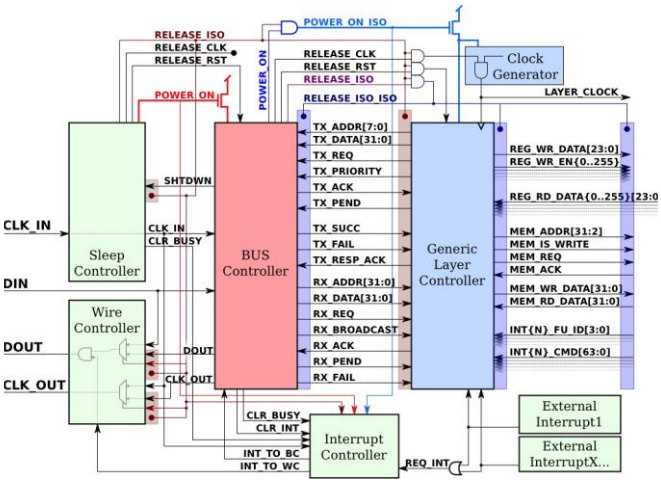

Figure 5. MBus block diagram. Green blocks (Sleep, Wire, Interrupt) are always-on and power-gate the red domain (Bus Controller) which power-gates the blue domain (rest).

B. *MBus Module Design*

In an MBus system, each node has three power domains: a minimalist set of always-on logics power-gate the MBus Controller that in turn power-gates the rest of the node. Fig. 5 shows MBus design integration. The "Layer Controller" can be replaced with any node-specific interface layer.

C. *MBus Protocol Design*

The MBus protocol provides event-driven automatic power management, *in-line* arbitration, and a robust bus interrupt.

MBus Wakeup. In standby mode, all MBus components except the frontend are power-gated. In this state, our system PMU [7] is in its lowest power mode, supplying a maximum of only 10's of nW total, to minimize standby power. The PMU must switch to a high power mode (Fig. 6) before the MBus power gates are released and a full message can be transmitted. To transmit a wakeup request without exceeding the PMU supply current D_{IN}/D_{OUT} are left in a high state in standby mode. Wakeup is then initiated by a node pulling D_{OUT} low, which consumes negligible power. This falling edge is propagated along the daisy chain till it is detected by the mediator which switches the PMU to high-power mode. After the PMU completes the state transition, the mediator starts to propagate clock edges through the daisy chain. The first four edges are used by the regular nodes to sequentially

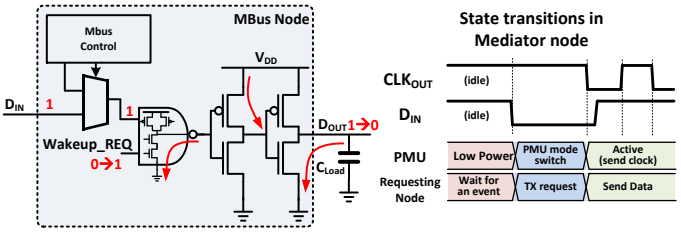

Figure 6. Wake up request with DATA pull down allows PMU mode switch without significant power consumption.

Figure 7. Event-driven wakeup timing. External events generate a "glitch" to initiate a null transaction for wakeup.

release power gates, clock, isolation gates, and reset at which point the member node MBus logic is fully active (Fig. 7).

MBus Arbitration. Arbitration requires only one CLK edge to resolve the bus owner. Fig. 8 shows an example: nodes 1 and 3 request the bus by pulling D_{OUT} low; node 2 simply forwards, while the mediator holds D_{OUT} high; node 1 initially wins. To ensure stable resolution, nodes can only pull D_{OUT} low if CLK_{IN} is high. At the first rising edge of CLK, each node samples its D_{IN}. If a node requested the bus and D_{IN}=*High*, it wins the arbitration. As an in-line protocol, MBus arbitration requires no additional I/O or area cost. Since MBus arbitration priority is topologically dependent we add an additional arbitration cycle for high priority messages.

Interrupt MBus requires a robust, data-independent, in-band means to end a transaction. The interrupt of MBus is based on a key insight that DATA can never meaningfully transition faster than CLK. Hence, the MBus interrupt is defined as three or more rising edges on DATA without corresponding CLK edges. We require three edges so that an erroneous glitch on DATA is insufficient to cause a false interrupt signal. Interrupt detection is performed by three flip-flops connected in series with *D* port tied high. The *reset* ports of first two flops are connected to CLK_{IN} and *clock* port of all flops are connected to D_{IN}. It is essentially a counter incremented by D_{IN} and reset by CLK_{IN}. Fig. 9 shows our interrupt detector and an interrupt waveform.

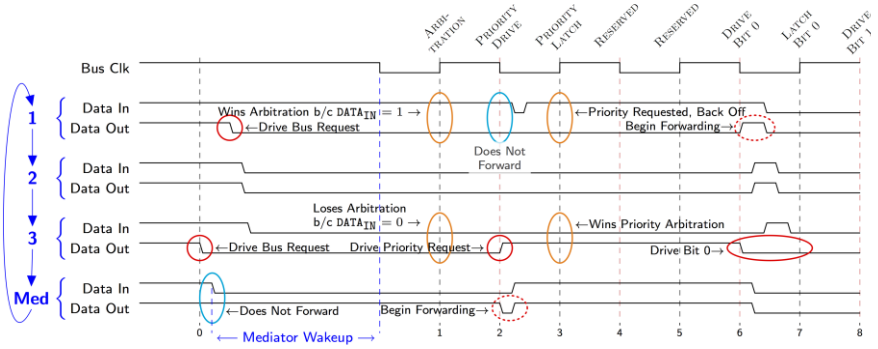

Figure 8. Arbitration and data timing. Shoot-through delay is exaggerated.

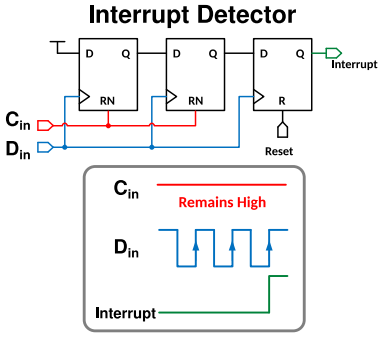

Figure 9. Interrupt timing and detector.

Measurements and Results

We implement MBus in six chips (three shown in Fig. 10) in three different technologies and two FPGA fabrics and find that all interoperate without error and no need for tuning. MBus can achieve higher than 10 Mb/s communication performance (limited by test configuration). We measure energy consumption of MBus when sending, receiving, and forwarding messages at 617 kHz (180 nm). The MBus mediator and local layer controller consume 27.45 pJ/bit when sending messages. MBus consumes 22.71 pJ/bit when a member node is receiving messages and 17.55 pJ/bit when forwarding messages. MBus achieves 22.7% energy saving from minimizing flop switching. We can only measure the total standby power of the entire stack (processor, radio, and temperature sensor). In standby, the system draws 8 nW, a value that is mainly dominated by other components.

Table 1

Energy consumption of MBus

	Energy per bit (pJ/bit)
Mediator, sending	27.45
Member, receiving	22.71
Member, forwarding	17.55

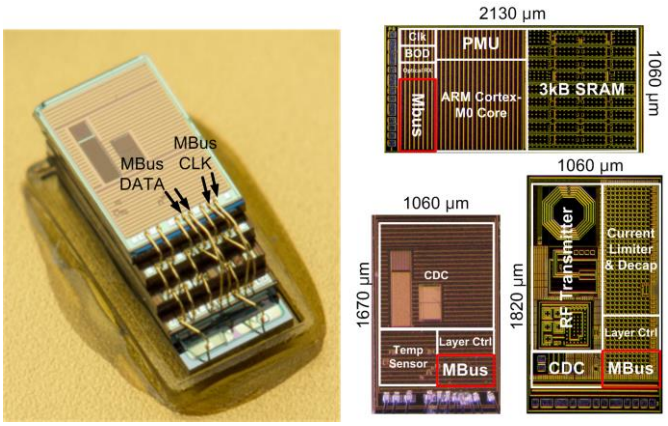

Figure 10. Photo of implemented MBus-based sensor system with control processor, temperature sensor, and wireless radio and individual layer die micrograph.

Table 2

Area ultilization of MBus

Technology	CMOS 180 nm
Sequential (# cells)	227
Combinational (# cells)	2,900
Area (µm²)	37,200

We compare MBus with the two most widely adopted inter-chip communication protocols: I²C [5] and SPI [4].

Consider a traditional I²C configuration running under 1.2 V supply at 400 kHz with 10 kΩ pull-up resistors. The pull-up resistor consumes at minimum 1.8 nJ for every '0' bit sent. Although the resistor could be sized to mitigate energy consumption, it increases the RC time constant and reduces bus speed. The low power I²C variant demonstrated in [6] achieved a two order of magnitude improvement (88 pJ/bit for 3 layers), but required custom ratio logic. MBus, however, provides additional energy savings (67.7 pJ/bit for 3 layers) with no custom logic required.

SPI has little to no protocol overhead and is all single-ended connections, yielding low-power performance. However, SPI is centralized, requiring all slave-to-slave transactions go through a central control, a 2× energy cost. SPI requires a dedicated I/O line to each slave, limiting scalability of the master node. SPI provides no in-band slave interrupt mechanism, requiring additional I/O to support interrupts.

Table 3

Comparison of MBus and other serial protocols

	SPI [4]	I²C [5]	MBus
IO pad count (n node)	3 + 2n[a]	4	4
Scalability	Low	High	High
Active power	Low	High	Low
Multi-Master	No	Yes	Yes
Power-aware	No	No	Yes

[a] *2n is required to support slave interrupts and feature-parity with MBus*

Conclusion

Today's emerging sensing platform needs a bus interconnect that addresses area and energy constraints rather than focusing on increasing performance or bandwidth. We present MBus, a new serial interconnect that addresses inter-chip communication requirements for next generation of ultra-low power, millimeter-scale wireless sensor nodes. We present a complete millimeter-scale modular system composed of sensors, a processor, and a radio connected with MBus. MBus offers a low standby power – 8 nW, low-energy communication – as low as 17.55 pJ/bit/chip, low wire count – four wires per node, is fully synthesizable, and supports multi-master operation, all with robust timing. These features open the door to modular, pervasive computing systems.

Acknowledgements

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References

[1] B. Warneke, B. Atwood, and K. Pister, "Smart dust mote forerunners," in MEMS 2001. pp. 357–360.

[2] G. Chen et al., "Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells," in ISSCC, 2010.

[3] T.Nakagawa, et al., "1-cc computer using UWB-IR for wireless sensor network," in ASPDAC 2008. pp. 392–397.

[4] D.Gonzales,"SPI bus eases multiple MCU hook up, "Design News, pp. 89–95, May 1984.

[5] NXP,"I²C-bus specification and user manual,"Oct.2012.

[6] Y. Lee et al., "A Modular 1mm³ Die-Stacked Sensing Platform with Optical Communication and Multi-Modal Energy Harvesting," in ISSCC, 2012.

[7] G. Kim et al., "A Millimeter-Scale Wireless Imaging System with Continuous Motion Detection and Energy Harvesting," Symp. on VLSI Circuits, 2014.