February 2001
GFK-1440C

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: **PLC CPU Module, Firmware Release 7.85**
IC697CGR935-DB
IC697CGR772-BA

Introduction

Some of the information in this document is not available in any other publication, so we recommend you keep it for future reference. This document describes the features of CPU firmware release 7.85 for the existing IC697CGR935 CPU module and for the new IC697CGR772 CPU module. The purpose of firmware release 7.85 is to:

- Support the release of new CPU model IC697CGR772.
- Provide the capability to use Serial Ports 1 and 2 on these two CPU modules.
- Increase the LD and C program size capacity on the IC697CGR935.

Also, starting with firmware release 7.85, one copy of the IC697 TCP WIN 95 NT upgrade software and one copy of the IC697 DOS programmer upgrade software will be included with these modules.

This document reflects the product catalog number suffix change (from CB to DB and AA to BA) that occurred due to a hardware update of this module. This update does not affect the features, functionality, or compatibility of this product.

Hardware and Firmware Identification Tables

Table 1. Identification of Release 7.85 CPU Hardware

CPU Catalog Number	CPU Board ID	CPU Board Revision
IC697CGR772	CPXA1	44A739520–G01R04 or later (Motherboard)
	HPMB1	44A739564–G01R01 or later (Memory Board)
IC697CGR935	CPXA1	44A739520–G01R04 or later (Motherboard)
	CMVB1	44A735200–G02R02 or later (Memory Board)

Table 2. Identification of Release 7.85 CPU Firmware

CPU Catalog Number	Firmware Diskette Label	Checksum
IC697CGR772	44S750624-G01R01 (3”)	n/a
IC697CGR935	44S750625-G01R02 (3”)	n/a

Table 3. Identification of Release 1.01 Port 1 and Port 2 Firmware

CPU Catalog Number	Firmware Diskette Label	Checksum
IC697CGR772 IC697CGR935	44S750665-G01R02 (3”)	n/a

Updating an IC697CGR935 Module

New versions of the IC697CGR935 modules will be equipped with firmware release 7.85. Users who wish to update their older IC697CGR935 modules to the features of firmware release 7.85 may purchase an update kit. This is an optional update, so no general field update is planned. If you intend to update this module and are also using GBC modules, please read the item "Notice to Update GBC Firmware" in the "Special Operation Notes" section of this document. Note that the IC697CGR772 is a new model and comes equipped with firmware release 7.85.

Table 4. Update Kit for Updating CGR935 Firmware

CPU Catalog Number	Firmware Release 7.85 Update Kit	Update Category
IC697CGR935AA or IC697CGR935BA	44A747170-G01	Optional

Agency Approval

The following versions of these two modules have been granted UL Class I Div 2 and C-UL agency approval:

- IC697CGR772-AA (the initial release version)
- IC697CGR935-BA and later

Documentation Note

The user's manual is not shipped with this product. User manuals are provided as a complete set on CD-ROM or can be ordered individually. The following are available:

- *IC697 Enhanced Hot Standby CPU Redundancy User's Guide (*revision A or later*)*
- CD-ROM documentation set, which contains the above user's guide
- The Data Sheet for the IC697CGR772 is publication number GFK-1437. It is included with the module.
- The Data Sheet for the IC697CGR935 is publication number GFK-1439. It is included with the module.

Special Operation Notes

IC641SWP Programming Software Compatibility

This release of the PLC CPU modules is compatible with the version of the IC641SWP software (the MS-DOS® based programming package) listed in the table below. However, the IC641SWP software does ***NOT*** support the Ethernet Global Data feature contained in the PLC CPU Release 7.85. These versions of the IC641SWP software do support the two additional Serial Ports, Ports 1 and 2.

To work around a compatibility problem with the serial IC641SWP software, the PLC will return 3.70 as its version to all serial IC641SWP software products (WSI and Standard COMM) Release 3.04 and earlier.

Table 5. First Compatible IC641SWP Software Version

CPU Model	IC641SWP Software
IC697CGR772 IC697CGR935	Version 7.02 or later

Windows Programming Software Compatibility

This firmware release is compatible with the Windows® 95 and Windows NT® programming packages listed in the table below:

Table 6. First Compatible Windows Programming Software Version

CPU Model	IC641CTL Software	IC641VPH700 and IC641VPP700
IC697CGR772	Version 2.10, Service Pack 3 or later	Version 2.0 or later
IC697CGR935	Version 2.10 or later	Version 2.0 or later

Microcycle Mode

Microcycle CPU sweep mode was first made available with Firmware Release 6.00 of the IC697 CPU. However, **Microcycle mode is not supported in the IC697CGR772 or IC697CGR935 CPU modules.**

PCM and BTM Compatibility

With the timing improvements and new features first made available in IC697 Release 5.00, it is highly recommended that systems using PCMs use IC697PCM711J or later. It is also highly recommended that systems using BTMs use IC697BEM713B or later. Use of boards of an earlier revision may result in lower system performance.

PCM (to CPU) Communications Timeout

The PCM has a default backplane communications timeout value of 5 seconds. After the PCM has sent a request to the IC697 CPU, the PCM applies this timeout while waiting on a response back from the CPU. In most cases, the CPU will respond well within the 5 second timeout, however, in certain instances the CPU can take longer than 5 seconds to respond. *These cases are limited to LOADs and/or STOREs of program and/or configuration - especially if blocks in the program are larger than 8 KBytes. Folders containing EXE blocks (again with *.EXE files larger than 8 KBytes) are most likely to present problems. Beginning in Release 6.00 Standalone C programs larger than 8 Kbytes also cause this to happen.*

Beginning in Release 5.50 of the IC697 CPUs, the CPU is guaranteed to respond within 8 seconds. To ensure that the PCMs do not observe backplane timeouts, a file must be loaded

(using *termf*) to the PCM. The file must be named *CPU.ENV* and is a binary file. The contents of this file are as follows (all values are specified in hexadecimal):

FILE OFFSET	DATA															
0000	4C	5A	01	01	00	00	00	00-00	00	00	00	01	00	00	00	LZ . . . . .
0010	00	00	00	00	00	00	00	00-00	00	43	50	55	4C	49	4E	. . . . . .CPULIN
0020	4B	2E	43	4F	44	00	2D	62-00	36	34	00	2D	74	00	32	K.COD. –b.64 .–t. 2
0030	30	30	00	00	43	50	55	4C-49	4E	4B	2E	44	43	42	00	00. .CPULINK .DCB.
0040	00	4E	55	4C	4C	3A	00	4E-55	4C	4C	3A	00	4E	55	4C	.NULL:.NULL:.NUL
0050	4C	3A	00	00	00	00	00	00-00	00	00	00	00	00	00	00	L: . . . . .
0060	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00	. . . . .
0070	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00	. . . . .

Once the binary file CPU.ENV (above) is created, use *termf* to load CPU.ENV to the PCM. Then execute a soft reset of the PCM. After executing the soft reset, the PCM's backplane communications timeout should be 10 seconds.

Note

A copy of the above CPU.ENV file can be obtained from the Electronic Bulletin Board Service (BBS). CPU.ENV can be found in the *conference:library* of PLC:PCM and is named *CPU.ENV.*

CAUTION

The CPU.ENV file *will not* be used when a hard reset is performed on the PCM. With the CPU.ENV file resident in the PCM, a soft reset must be performed after every hard reset of the PCM. Be aware that it is possible to issue a *soft reset* COMMREQ from the Ladder Diagram application; therefore, the application can be modified to handle the required soft reset of PCMs after a power cycle of the PLC system

Notice to Upgrade GBC Firmware

Starting with the introduction of the new features in past CPU firmware release 5.00, timings with the IC66* Bus Controllers (GBCs) have changed; this has uncovered a problem in the GBC firmware. GBCs in expanded racks could be lost if the system is fully configured and only the main rack cycles power.

Also, in previous versions of the GBC, there was a problem with input data coherency. In a system with a relatively long CPU sweep time and a relatively short IC66 bus scan time, a problem could be seen if a device was lost. Input data could be defaulted off while the CPU was reading the data from the GBC.

It is recommended to update existing GBC hardware to IC697BEM731M or later when updating PLC CPU firmware to Release 7.85. Operation of the IC697BEM731M, in conjunction with Release 7.85 of the IC697CPU will result in a slight impact to the I/O scan time of the PLC.

Third Party VME Modules

IC641 programming software Release 5.00 (and later) allows Third Party VME modules to be configured for six modes: NONE, INTERRUPT ONLY, BUS INTERFACE, FULL MAIL, I/O

SCAN, and REDUCED MAIL. However, firmware release 7.85 for the IC697CGR935 and IC697CGR772 does not support the INTERRUPT ONLY or REDUCED MAIL modes. When using the BUS INTERFACE configuration mode, the interrupt parameter must be set to DISABLED since 3rd Party VME module interrupts are not allowed in these two "CGR" CPUs.

Maximum PLC Sweep

In systems configured for IC66 Bus Redundancy a complete PLC sweep must be executed every 500 milliseconds or less, even though it is possible to configure the watchdog timer to higher limits. This also means that resetting of the watchdog timer with Service Request #8 cannot be done indefinitely.

Serial Communications

The following operating restrictions exist for the Serial Communications feature:

1. Serial communications can add up to 5 milliseconds of time to any given sweep. This should be taken into account when setting the watchdog timer.
2. The following procedure is recommended when changing baud rates in the PLC and the WSI board. First enter the configuration package and change the baud rate on the PLC, then store the new configuration. Now power off the PLC and then go to the WSI setup screen and change the WSI baud rate. Finally, power the PLC back on.
3. The link idle time setting in the configuration parameter *Config for Serial Communications* should be set to 10 seconds or greater. Otherwise a communications failure will occur when storing the config to the PLC.

Serial Port Mode Configuration

There is a CPU serial port configuration parameter called MODE. This parameter can be one of two values: (1) **SNP,** which is required for the port to communicate with the IC697SWP programming software, or (2) **MSG** to indicate that the serial port will be used to send printf commands from a C program block to the connected device. If you configure the MODE parameter (of the same serial port that your IC641SWP programming software is using) to be **MSG,** you will lose the ability to communicate with that port as soon as you go to RUN mode and the **MSG** value takes effect.

IC641SWP Software/WSI Attach

If you are using a WSI device, do not connect or disconnect the WSI/BTM cable while the programmer host is powered-on. This action may cause a running PLC to Stop.

Expansion Rack ID

The expansion racks for the IC697 PLC are shipped with the rack ID strapped for rack 0 (the main rack). If the rack jumper is not changed, the PLC will not recognize the rack at all and, therefore, may not properly identify the error.

Expansion Rack Cable

If you are using expansion racks, do not connect or disconnect an expansion rack cable while the CPU is running. This will cause the PLC to go to the STOP/HALT mode.

Expansion Rack Power-up Timing Considerations

Expansion racks should be powered up at the same time that the main rack is powered up, or they should be powered up after the main rack has completed its power-up initialization. *Do not power-up an expansion rack while the CPU is running power-up diagnostics.*

Memory Usage

A general rule-of-thumb for memory usage is 48 bytes per I/O point plus register memory in bytes.

Timer Operation

Care should be taken when timers (ONDTR, TMR, and OFDTR) are used in program blocks that are NOT called every sweep. The timers accumulate time across calls to the sub-block unless they are reset. This means that they function like timers operating in a program with a much slower sweep than the timers in the main program block. For program blocks that are inactive for large periods of time, the timers should be programmed in such a manner as to account for this catch up feature.

Similar to this are timers that are skipped because of the use of the JUMP instruction. Timers that are skipped will NOT catch up and will therefore not accumulate time in the same manner as if they were executed every sweep.

I/O Link Interface

When powering up the PLC CPU without a battery, and I/O Link Interface boards are present, an incorrect *Loss of Module* fault will be logged for each I/O Link Interface board; however, the PLC CPU will not consider these boards as lost, and the boards will continue to operate properly.

CommReqs with Retentive Memory

When powering up the PLC CPU with a program being retrieved from Retentive Memory and proceeding to RUN mode, any CommReqs to a PCM should be delayed for 5 seconds.

Constant Sweep

Constant Sweep time, when used, should be set to at least 10 milliseconds greater than the normal sweep time to avoid any oversweep conditions when monitoring or performing on-line changes with the programmer. The smallest valid constant sweep time setting is 10 milliseconds for the models IC697CGR772 and IC697CGR935 CPUs. Window completion faults will occur if the constant sweep setting is not high enough.

Interaction of the IC641SWP Software with Closed Programming Window

The IC641SWP PLC Sweep Control and Monitor screen cannot be used to change the PLC Sweep Modes or timers (Constant Sweep Time, Program Window Times, etc.) while the program window is closed. Use Service Requests #1 through #4 to perform these functions.

Caution

The programming software cannot be used to change the PLC mode (STOP, RUN, etc.) while the programming window is closed. Use the toggle switch on the CPU module instead.

CGR772 and CGR935 Ambient Temperature

Due to the high power dissipation of the CGR772 and CGR935 CPU microprocessors, ambient operating temperature of these modules must be kept at or below 50¿ ¿

limiting of system power may be necessary. For more information, please see the data sheet GFK-1437 for the CGR772 or data sheet GFK-1439A for the CGR935.

With forced air cooling, an ambient operating temperature of 60¿ ¿ Fan assemblies IC697ACC721 (120 VAC) and IC697ACC724 (240 VAC) are available for direct mounting to the IC697 rack.

SFC RESET Function Block

The SFC RESET function block only executes when used in Action Logic or Pre/Post Logic within an SFC block (Main SFC or SFC sub-block). Attempting to execute an SFC RESET function block from a Ladder Diagram Main/sub-block will not reset the SFC network and (as of v6.02) will not pass power flow to any logic right of the SFC RESET.

Ethernet Global Data and Sweep Time

Each Ethernet Global Data Exchange configured for either consumption or production can add up to 1 millisecond to the sweep time. This sweep impact should be taken into consideration when configuring the PLC for constant sweep mode and when setting the CPU watchdog timeout.

Converting GHS Control Strategy to GDB

Dual bus application solutions running the GHS control strategy are not compatible with applications using the GDB control strategy. If the user wishes to convert to using the GDB control strategy, the application must be halted and the logic/configuration changed accordingly.

Problems Resolved by Firmware Release 7.85

When Using an Ethernet Module

The CPU would fail if Loss of Module or System Configuration Mismatch faults were logged against an Ethernet module. The failure only occurred if point faults were enabled in the CPU and the status word for the Ethernet Module was configured for %R memory. This failure has not existed in any CGR PLC releases.

Loss of Option Module Faults

CPU logged two Loss of Option Module faults on the RCM when the Hardware Configuration was cleared.

Masked Compare Function Block Usage

The masked compare function block did not operate correctly when the first input parameter (first bit string) was not aligned on a word boundary (e.g. %M0009 instead of %M0017). Using the masked compare function block in this way would access a byte in memory just before the MASK parameter resulting in an incorrect mask being applied or an invalid memory access.

Run-Mode Store Program Deletion

When Run-Mode Store was used to delete programs and more than 8 programs existed in the PLC, subsequent Run-Mode Store operations that added programs sometimes resulted in one of the programs being deleted.

New Features and Functionality of Firmware Release 7.85

List of New Features of Firmware Release 7.85

The following new features have been added in Release 7.85:

1. Ability to use Serial 1 and 2 for serial communications
2. Increased LD and C Program Size
3. Introduction of the IC697CGR772 CPU module

Support for Serial Ports 1 and 2

Earlier releases of CPU firmware for the IC697CGR935 module supported Serial Port 3 but did not support Serial Ports 1 and 2, even though the port hardware was present. Firmware release 7.85 adds support for these two ports on the IC697CGR935 and also supports them on the new IC697CGR772. Port 1 uses the RS-232 standard, and Port 2 uses the RS-422/485 standard. Both of these serial ports may be used at the following baud rates: 1200, 2400, 9600, 19200, 38400, and 57600. Note that these ports do not yet support 115K baud. Both ports can be operated simultaneously up to 57600 baud without dropping characters.

Serial Port 3, is still the primary connection port for the serial programmer.

The SNP (Series Ninety Protocol) Slave protocol is the only protocol supported by Serial Ports 1 and 2 in firmware release 7.85. All services available through the standard SNP Port 3 are available through the new ports with these exceptions: you cannot do Store/Load of Logic and/or Configuration, and you cannot do Datagrams (Datagrams are the services by which the MS-DOS and Windows programming packages monitor reference table data and program animation). Support for these services will be provided in a subsequent release.

The HMI software does use services other than Datagrams to monitor reference data, and these services are supported through these ports, so you could use the HMI software for monitoring data within the PLC.

Serial Ports 1 and 2 can be configured by both the MS-DOS and Windows programming packages for setting baud rate, parity, stop bits, etc.

Increased LD and C Program Size

With firmware release 7.85, you will be able to store larger LD/SFC programs than previously to the IC697CGR935 CPU module. The following rules will apply in determining LD/SFC program charges:

1. Total memory used for programs, configuration, and reference tables in the CPU must not exceed the daughterboard size. Therefore, the LD/SFC program can never be larger than the daughterboard size.
2. The LD/SFC program can now be up to 544K (557,056 bytes) when the user's selected stack size is 12K or less (the default stack size is 12K and, therefore, the default LD/SFC program limit is 544K). The stack size is not counted against the 544K limit or the daughterboard limit in this case.
3. The LD/SFC program can now be up to 532K (544,768 bytes) when the user's selected stack size is larger than 12K. The first 12K of the user's selected stack size will continue to not count against the program or daughterboard limit; the remainder of the stack size

will be counted against both program and daughterboard limits. For example, if the user selects a 20K stack, then 524K (532K – 20K + 12K) will be available for the LD/SFC program.

4. Memory needed to store the initialization constants for C Program Bloc data will no longer count against the LD/SFC program limit. They will, however, continue to count against the total daughterboard memory used.

The user will also be able to now store Standalone C programs up to 564K (577,536 bytes) including the stack when using daughterboards larger than 512K. For example, if the user has selected a 16K stack for the Standalone C program, then the program can be up to 548K (564K – 16K). The memory needed for initialization constants for the data will continue to be counted against the daughterboard size but not against the program limit.

The IC697CGR772 module is limited to 512K bytes of user memory and will not be able to take advantage of the increased LD and C program sizes.

New IC697CGR772 CPU Module

The new IC697CGR772 has the same functionality as the IC697CGR935 but with the following memory and memory address reference sizes. The IC697CGR772 cannot be used to synchronize with an IC697CPU780 CPU. This information will be added to the Enhanced Hot Standby CPU Redundancy User's Guide.

User Memory	512 K bytes
Maximum %I References	2048
Maximum %Q References	2048
Maximum %M References	4096

The timing for redundancy activities for the CGR772 is shown in the following table:

Synchronized Base Sweep Addition	5.9 ms
Transfer of data from active to backup with point faults disabled	
Discrete References (%I, %M, %Q)	1.5 ms / 1K references (bits)
Registers (%R, %AI, %AQ)	4.6 ms / 1K registers (words)
Transfer of data from active to backup with point faults enabled	
Discrete I/O References (%I, %Q)	1.7 ms / 1K references
Other Discrete References (%M)	1.5 ms / 1K references
I/O Registers (%AI, %AQ)	6.7 ms / 1K registers (words)
Other Registers (%R)	4.6 ms / 1K registers (words)

The following numbers should be used for calculating the number of words to checksum per sweep and the Background Window time setting. Refer to the section ”Background User Checksum and Background Window Timing Instructions” in Chapter 4 of the *Enhanced Hot Standby CPU Redundancy User’s Guide* for further details.

Ms per byte of Program Checksummed (F)	0.0064 ms/byte
Time to perform Background Diagnostics (C)	3479 ms

Restrictions and Open Problems

1. If an expansion rack powers up while the CPU in the main rack is in the RUN mode, the slot fault contacts will prematurely indicate that the modules in the expansion rack are not faulted before they complete their power up.
2. When there is no logic stored in a CPU module the %Q and %M tables will be cleared when the CPU is placed in RUN mode. In this context “no logic stored” means that no program had ever been stored or that the clear function on the IC641SWP software had been used to clear logic and configuration.
3. When the Bit Sequencer sequences from one step to another, the negative transitional contact that corresponds to the original step is not set. The transition contact for the new step is set and remains set until the sequencer sequences to the next step. This operation is identical to the operation of the previous versions of the CPU firmware.
4. If multiple faults exist in an IC697 Remote Drop and one of them is corrected, a FAULT contact that uses the Remote Drop’s module reference will incorrectly indicate that no faults exist at the Remote Drop.
5. An incorrectly formatted COMMREQ (for example, incorrect task id field) directed to a PCM or CMM module does not result in an error being logged in the PLC fault table. Correctly formatted COMREQ’s operate normally.
6. A large number of COMM_REQs (typically greater than 8) sent to a given board in the same sweep; may cause a Module Software fault to be logged in the PLC fault table. The fault group is MOD_OTHR_SOFTWR (16t, 10h) and the error code is COMMREQ_MB_FULL_START (2). When this occurs, the ”FT” (Function Faulted) output of the COMM_REQ function block will also be set. To prevent this situation, COMM_REQs issued to a given board should be spread across multiple sweeps so that only

a limited number (typically 8 or less) of COMM_REQs are sent to a given board in each sweep. In addition, the FT output parameter should be checked for errors. If the FT output is set (meaning an error has been detected), the COMM_REQ could be re-issued by the application logic.

7. If the Primary PLC is the active unit and the Secondary PLC is the backup unit, and a parity error occurs on the RCM in the Primary PLC, then, occasionally, both RCM-BTM links will be lost and each PLC system will operate as a non-synchronized active unit (the Primary PLC will be driving outputs on the Bus).

8. When attempting simultaneous loads of logic through multiple Ethernet connections and a serial connection, the loads through the Ethernet connection may fail with a communication timeout.

9. The size of Standalone C programs reported in the Program Memory screen of the IC697SWR programming software is too larger by about 500 bytes. Therefore, this screen may indicate that a Standalone C program slightly larger than the program limit has been stored to the PLC CPU.

10. On occasion, the PLC may fail to respond to an SNP Attach message issued through the new serial ports (Port 1 or Port 2). Several retries of the SNP attach message may be necessary to successfully attach to the PLC via these two ports. Therefore, if you are developing your own SNP applications to run on these two ports, you should design and code for multiple SNP attach retries.

Additions/Changes to the Reference Manual

Wait Mode COMM_REQs

Wait mode COMM_REQs cannot be directed to the new serial ports (Ports 1 and 2).

MOV_BIT Instruction

The documentation for the MOV_BIT instruction indicates that transition references are modified only for the bits in the range (indicated by the LEN parameter) of the function block. The documentation should say that the transition references of all bytes in the range are affected.

Addition/Changes to User's Guide

Change to IC697CGR935 Transfer Time Table

The IC697CGR935 data transfer time table in Chapter 4 of the *Enhanced Hot Standby CPU Redundancy User's Guide* will be replaced with the following table:

Synchronized Base Sweep Addition	4.7 ms
Transfer of data from active to backup with point faults disabled	
Discrete References (%I, %M, %Q)	1.5 ms / 1K references (bits)
Registers (%R, %AI, %AQ)	4.2 ms / 1K registers (words)
Transfer of data from active to backup with point faults enabled	
Discrete I/O References (%I, %Q)	1.7 ms / 1K references
Other Discrete References (%M)	1.5 ms / 1K references
I/O Registers (%AI, %AQ)	6.2 ms / 1K registers (words)
Other Registers (%R)	4.2 ms / 1K registers (words)

The following numbers should be used for calculating the number of words to checksum per sweep and the Background Window time setting. Refer to the section "Background User Checksum and Background Window Timing Instructions" in Chapter 4 of the *Enhanced Hot Standby CPU Redundancy User's Guide* for further details.

Ms per byte of Program Checksummed (F)	0.0014 ms/byte
Time to perform Background Diagnostics (C)	376 ms

New IC697CGR772 Information

The information in item "New IC697CGR772 CPU Module" of the "New Features and Functionality" section of this document will be added to the User's Guide.