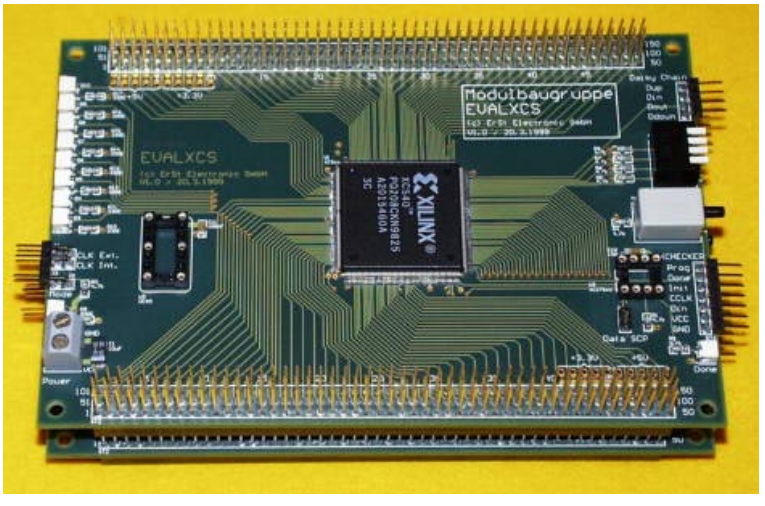
Board Module

for

Xilinx Spartan XCS-20/30/40

FPGA Family



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Manual:	EVALXCS	Version 1.1	August 1999
	EVALXCS	Version 1.2	October 1999

This manual describes the technical properties and the usage of the following products:

5V versions:	EVALXCS-20	Version 1.0	April 1999
	EVALXCS-30	Version 1.0	April 1999
	EVALXCS-40	Version 1.0	April 1999
3.3V versions:	EVALXCS-20XL	Version 1.0	April 1999
	EVALXCS-30XL	Version 1.0	April 1999
	EVALXCS-40XL	Version 1.0	April 1999

Important Note:

The EVALXCS board module has been designed and tested exclusively for the usage as a development tool. In particular, strong electromagnetic radiation may be produced. The ErSt Electronic GmbH does not undertake any liability for damages which may result from an improper use of this product.

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1 Introduction

This manual describes the specific properties of the board module like power supply, FPGA configuration, clocks, reset, LEDs, DIP switches and I/O signals.

Please take information about the FPGA from the Xilinx literature (see chapter *4 Literature*).
Online information can be found on the Xilinx websites:

http://www.xilinx.com

and

http://www.support.xilinx.com

Information about new products and new developments can be found on the ErSt Electronic Website:

http://www.erst.ch

If you have questions you may write to the following E-mail address:

info@erst.ch

2 Overview

2.1 Key Features

- Xilinx FPGA Spartan XCS40/30/20 (5V) or XCS40XL/30XL/20XL (3.3V) in PQ-208 package
- Header connector for Xchecker cable
- Header connector for external daisy chain connections
- SPROM for FPGA Master Serial Mode (DIL-8 package with socket)
- Quarz oscillator up to 80 MHz (DIL-8 or DIL-14 versions possible)
- Four position DIP switch for user configurations
- Push button for reset signal application or arbitrary usage
- Eight LED display for status messages
- 2 pole power connector for +5V/+3.3V power supply
- 4 layer PCB
- Clock signals may be equipped with termination resistors
- Stand alone usage of the board module possible
- The module has a standard size of 15cm x 10cm and a digital interface compatible with future products:
  - 3x50 pole header connectors (2.54mm grid spacing) on each long side of the PCB
  - The header connectors stand off from the top side of the PCB, the socket connectors from the bottom side
  - Modules may be stacked to form a tower

2.2 Applications

- ASIC emulation
- Error monitoring and analysis
- Digital PLLs
- PWM controller
- Adaptive digitale filters
- Signal multiplexer
- Stimuli generators
- High speed encoder/decoder
- Memory controller
- Interface controller

2.3 Function Description

The board module EVALXCS-PQ208 is an ideal tool to test complex digital circuits during the early states of their development. The various configuration options of the Xilinx FPGAs allow the easy implementation of applications. The hardware configuration may be loaded via XChecker or SPROM. Almost all I/O pins of the FPGA are routed to header connectors, a total of 150 signals. These signals may be used as inputs or outputs.

Several board modules may be stacked to form a tower, which enables one to realise circuits whose demand of gates is beyond the scope of a single FPGA. By using an external daisy chain connection, the whole stack can be configured at once with a single download operation.

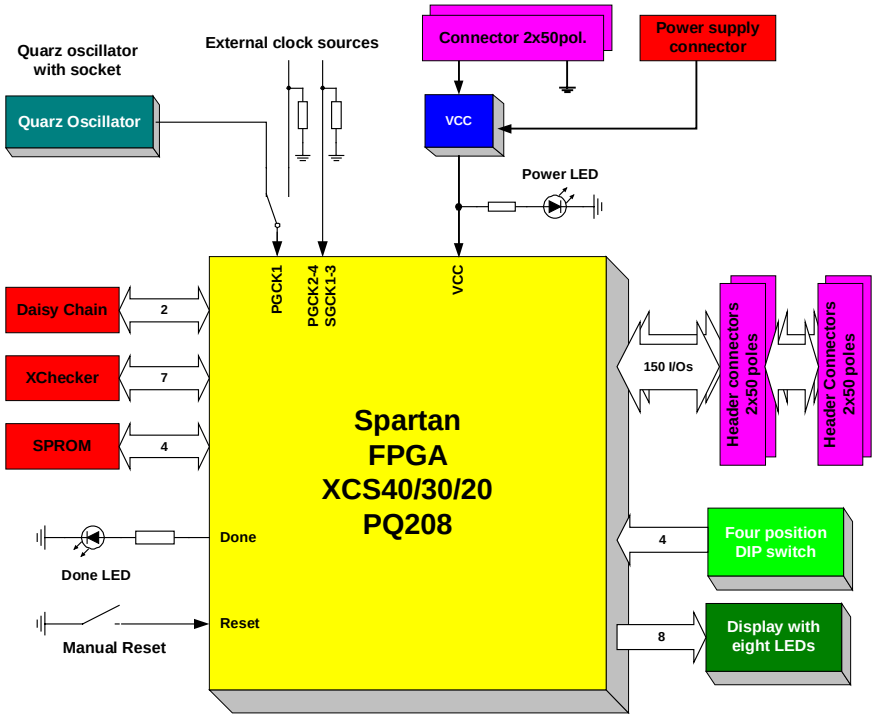

Figure 1: Block diagram of the board module

Seven clock sources can be used whereas one clock source is either the internal quarz oscillator or an external clock source. The quarz oscillator is inserted in a socket and can therefore be exchanged easily. Both DIL-8 and DIL-14 packages can be used. All clock signals may be terminated (parallel termination to ground) with termination resistors. These resistors can be mounted by the user on the bottom side of the PCB.

A four position DIP switch is available for user defined purposes. There is also a push button whose primary intent is to serve as a reset button. Since this button is connected to a general I/O pin it may be used for arbitrary functions.

An LED row with eight SIDELEDs is able to display status messages, error messages etc..

Figure 1 shows the above described function blocks.

3 Technical Information

3.1 Power Supply

The power supply of a single module or a whole stack comes from the power connector ST5. The negative pole is on the side of the power LED, the screw of the positive pole is marked with red color. Within a stack any power connector can be used since all boards are connected together over the header connectors.

Caution: Use only board modules within a stack which are specified for the same supply voltage!

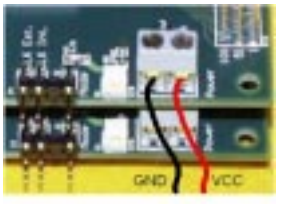

Figure 2: Polarity of the power connector

The power supply voltage is 5V for modules which are equipped with an FPGA of the XCS-20/30/40 family. If the XCS-20XL/30XL/40XL family is used, the power supply voltage is 3.3V.

The supply voltages are also available on certain pins of the header connectors. verfügbar. *Table 1* and *Table 2* list the supply voltages. Only certain voltages are available depending on the used FPGA family (Spartan or SpartanXL) and the usage of the board module (with or without usage of a base board).

Signal Name	Connector Pins on ST1A
+5V	1, 2, 3, 4, 5 36, 37, 38, 39, 40
+3.3V	6, 7, 8, 9, 10 41, 42, 43, 44, 45
GND	11, 12, 13, 14, 15 21, 22, 23, 24, 25 31, 32, 33, 34, 35 46, 47, 48, 49, 50
+12V	16, 17, 18, 19, 20
-12V	26, 27, 28, 29, 30

Table 1: Supply voltages on ST1A

Signal Name	Connector Pins on ST2C
+5V	111, 112, 113, 114, 115 146, 147, 148, 149, 150
+3.3V	106, 107, 108, 109, 110 141,142, 143, 144,145
GND	101, 102, 103, 104, 105 116, 117,118, 119, 120 126, 127, 128, 129, 130 136, 137,138, 139, 140
+12V	131, 132, 133, 134, 135
-12V	121, 122, 123, 124, 125

Table 2: Supply voltages on ST2C

Connector	Pin Numbers
ST1A	11, 12, 13, 14, 15 21, 22, 23, 24, 25 31, 32, 33, 34, 35 46, 47, 48, 49, 50
ST2C	101, 102, 103, 104, 105 116, 117,118, 119, 120 126, 127, 128, 129, 130 136, 137,138, 139, 140
ST1B	51, 53, 55, 57, 59 61, 63, 65, 67 72, 75, 78

Table 3: Ground pins on all connectors

3.2 FPGA Configuration

There are two options to configure the FPGA. The following table shows the possible modes and the jumper settings of J1 and J2:

Mode	Data (J1)	Mode (J2)	CCLK	Daten	Comment
Master Serial	inserted	not inserted	Output	Bit serial	SPROM (DIL-8)
Slave Serial	not inserted	inserted	Input	Bit serial	XChecker (PC)

Table 4: Configuration Modes

3.2.1 Master Serial Mode

The board module contains an 8 pin DIL socket for Serial Configuration PROMs (SCPs). The jumper settings for the master serial mode are as follows:

J1 (Data)	J2 (Mode)
inserted	not inserted

Table 5: Master Serial Mode

Note: The XChecker cable must be disconnected to avoid a contention between CCLK and DIN!

3.2.2 Slave Serial Mode

For this form of FPGA configuration you need an XChecker cable from XILINX, which serves as interface between the board module and the PC, see *Figure 2.*

The jumper settings for the slave serial mode are as follows:

J1 (Data)	J2 (Mode)
not inserted	inserted

Table 6: Slave Serial Mode

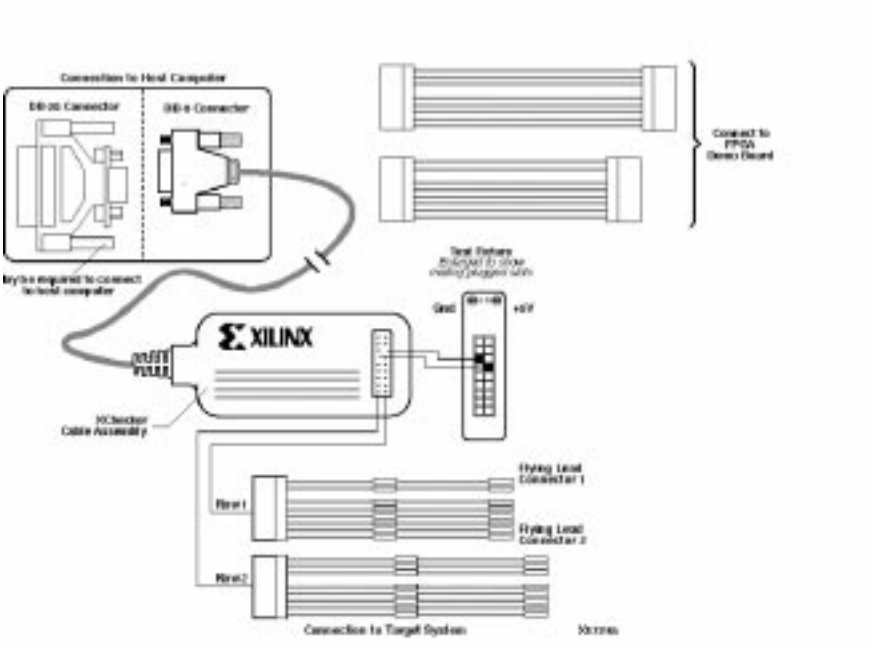

Figure 3: XChecker Cable

The following table shows the pin assignment of the header connector ST3:

ST3 (Header Connector)	XChecker (Connector 1)
1	PROG\
2	DONE
3	INIT\
4	CCLK
5	DIN
6	VCC
7	GND

Table 7: XChecker pin assignment

3.2.2.1 Daisy Chain

A whole stack may be configured with a single download. To accomplish this the individual layers must be connected in form of a daisy chain. External connections of appropriate pins of connector ST4 perform this task (see *Table 8*).

ST4 (Connector)	Pin Name
1	dup
2	din
3	dout
4	ddown

Table 8: Pin assignment of the daisy chain connector ST4

Use the following connection scheme:

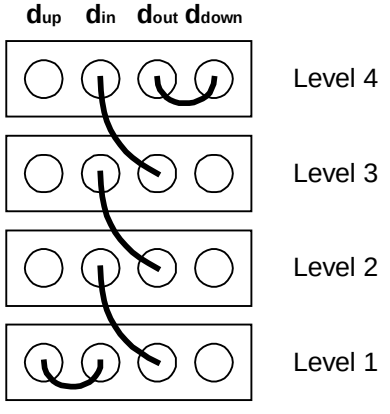

Figure 4: External daisy chain connections

The easiest way to make the connections d_{up}-d_{in} and d_{out}-d_{down} is to insert a jumper. However, these connections are only needed if the stack is connected to a main board and if the configuration data comes from the main board.

If the main board is not used you need only the d_{out}-d_{in} connections. The configuration bit streams are then feeded to the lowest level (SCP or XChecker).

3.3 Clocks

The seven clock signals *pgck1* to *pgck4* and *sgck1* to *sgck3* are routed to the header connectors where *pgck1* may be connected optionally to the internal quarz oscillator, see *Table 9*.

Source	J3 (CLK int.)	J4 (CLK ext.)
Quarz Oscillator	inserted	not inserted
Ext. Clock (pin 52 of ST1B)	not inserted	inserted

Table 9: Clock sources

3.3.1 External Clock

The assignment of the clock signals to the connectors pins is shown in the following table:

Signal Name	Connector ST1B	FPGA Pin	Termination Resistor
pgck1	52	2	R18
pgck2	54	55	R19
pgck3	56	108	R20
pgck4	58	160	R21
sgck1	60	207	R22
sgck2	62	49	R23
sgck3	64	102	R24
sgck4/dout	not connected	154	—

Table 10: External clock signals and termination resistors

3.3.1.1 Termination Resistors

The clock signals *pgck1* to *pgck4* and *sgck1* to *sgck3* may be terminated with resistors (R18 to R24) which are connected immediately from the FPGA pin to ground. These resistors form a parallel termination. The values of the resistors should match the impedance of the circuit board trace which has a nominal value of 100 Ohms. Please consider the maximal output current capability of the clock source!

The resistors (SMD, size 0805) can be soldered to the board directly beneath the FPGA on the bottom side of the PCB. *Figure 5* shows the positions:

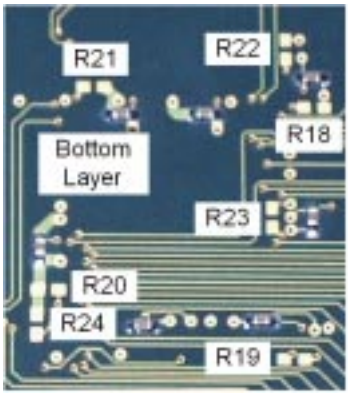

Figure 5: Positions of the termination resistors

3.3.2 Internal Clock (Quarz Oscillator)

Since the clock frequency depends strongly on the application the oscillator must be exchangeable. The oscillator socket can hold DIL-8 or DIL-14 packages. Pin 1 is common for both types of packages.
Oscillators of the VCXO type need a control signal at pin 1 (U_c). To get a closed feedback loop this signal must be connected (via FPGA) to U_{out}.

Osz.	Net Name	FPGA Pin	FPGA I/O
U_c	ch_a_9	27	Output
U_{out}	pgck1	2	Clock Input

Table 11: Quarz oscillator signals

3.4 Reset Button

A functional reset can be issued at any time by pressing the push button T1. The reset signal is active high and needs to be considered in the design appropriately. If no reset function is needed the button may be used for arbitrary purposes.

Button	Net Name	FPGA Pin
T1	reset	56

Table 12: Reset signal

Note 1: A manual reset initialises the internal circuits of the FPGA (registers, counters, finite state machines etc.) and must be implemented in the design appropriately.

Note 2: Do not press the reset button during the download of a bit stream since this may interfere with the HDC function!

Note 3: When used in a stack, all HDC pins of all FPGAs are connected in parallel. Unconfigured FPGAs tie this pin to high level and act therefore like a pressed reset button. Make sure to configure this pin as an input if the reset function is desired!

3.5 LEDs

The eight LEDs D3 to D10 are intended as optical indicators for the display of status information. D2 is connected to the DONE pin of the FPGA and D1 serves as power indicator LED. The DONE LED turns on at the end of a successful bit stream download.

The LEDs D3 to D10 turn on whenever the corresponding FPGA output is low. The following table shows the assignment to the FPGA pins:

LED	Net Name	FPGA Pin
D3	ch_a_1	15
D4	ch_a_2	17
D5	ch_a_3	19
D6	ch_a_4	20
D7	ch_a_5	21
D8	ch_a_6	22
D9	ch_a_7	23
D10	ch_a_8	24

Table 13: LED signals

Note: If the board module is used within a stack the LEDs of all levels are connected in parallel. If one LED is driven by the FPGA the LEDs of the other levels are driven also. The maximal output current of 20mA of an FPGA port is sufficient for up to four levels. If more than four levels are used, the current limiting resistors of the LEDs of the remaining levels must be removed.

3.6 DIP Switch

The four position DIP switch S1 can be used for application specific purposes. In the *On* position the connected FPGA pin is tied to ground. In the *Off* position the connected FPGA pin is pulled to VCC via a resistor.

The assignment of the switches to the FPGA pins is as follows:

Switch	Net Name	FPGA Pin
1	sw1	149
2	sw2	150
3	sw3	151
4	sw4	152

Table 14: DIP switch

3.7 Stimuli and Monitoring Signals

The signals *ch_a_1* to *ch_a_50*, *ch_b_1* to *ch_b_50* and *r_1* to *r_50* are routed to header connectors. All these pins may be used as stimuli and monitoring signals.

The following table shows the assignment of the FPGA pins to the connector pins:

Net Name	Connector			FPGA Pin
	ST1C	ST2B	ST2A	
r_1	101			14
r_2	102			12
r_3	103			11
r_4	104			10
r_5	105			9
r_6	106			8
r_7	107			5
r_8	108			4
r_9	109			3
r_10	110			206
r_11	111			205
r_12	112			204
r_13	113			203
r_14	114			202
r_15	115			201
r_16	116			200
r_17	117			199
r_18	118			198
r_19	119			197
r_20	120			196
r_21	121			194
r_22	122			193
r_23	123			191
r_24	124			190
r_25	125			189
r_26	126			188
r_27	127			187
r_28	128			186
r_29	129			185
r_30	130			184
r_31	131			181
r_32	132			180
r_33	133			179
r_34	134			178
r_35	135			177
r_36	136			176
r_37	137			175
r_38	138			174

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r_39	139			172
r_40	140			171
r_41	141			169
r_42	142			168
r_43	143			167
r_44	144			166
r_45	145			165
r_46	146			164
r_47	147			163
r_48	148			162
r_49	149			161
r_50	150			159
ch_a_1		51		15
ch_a_2		52		17
ch_a_3		53		19
ch_a_4		54		20
ch_a_5		55		21
ch_a_6		56		22
ch_a_7		57		23
ch_a_8		58		24
ch_a_9		59		27
ch_a_10		60		28
ch_a_11		61		29
ch_a_12		62		30
ch_a_13		63		31
ch_a_14		64		32
ch_a_15		65		34
ch_a_16		66		35
ch_a_17		67		36
ch_a_18		68		37
ch_a_19		69		39
ch_a_20		70		40
ch_a_21		71		41
ch_a_22		72		42
ch_a_23		73		43
ch_a_24		74		44
ch_a_25		75		45
ch_a_26		76		46
ch_a_27		77		47
ch_a_28		78		48
ch_a_29		79		57
ch_a_30		80		58

ch_a_31		81		59
ch_a_32		82		61
ch_a_33		83		62
ch_a_34		84		63
ch_a_35		85		64
ch_a_36		86		65
ch_a_37		87		67
ch_a_38		88		68
ch_a_39		89		69
ch_a_40		90		70
ch_a_41		91		72
ch_a_42		92		73
ch_a_43		93		74
ch_a_44		94		75
ch_a_45		95		76
ch_a_46		96		80
ch_a_47		97		81
ch_a_48		98		82
ch_a_49		99		83
ch_a_50		100		84
ch_b_1			1	85
ch_b_2			2	87
ch_b_3			3	88
ch_b_4			4	89
ch_b_5			5	90
ch_b_6			6	92
ch_b_7			7	93
ch_b_8			8	94
ch_b_9			9	95
ch_b_10			10	96
ch_b_11			11	97
ch_b_12			12	98
ch_b_13			13	99
ch_b_14			14	100
ch_b_15			15	101
ch_b_16			16	107
ch_b_17			17	109
ch_b_18			18	110
ch_b_19			19	111
ch_b_20			20	112
ch_b_21			21	113
ch_b_22			22	114

ch_b_23			23	115
ch_b_24			24	116
ch_b_25			25	117
ch_b_26			26	119
ch_b_27			27	120
ch_b_28			28	122
ch_b_29			29	123
ch_b_30			30	124
ch_b_31			31	125
ch_b_32			32	126
ch_b_33			33	127
ch_b_34			34	128
ch_b_35			35	129
ch_b_36			36	132
ch_b_37			37	133
ch_b_38			38	134
ch_b_39			39	135
ch_b_40			40	136
ch_b_41			41	137
ch_b_42			42	138
ch_b_43			43	139
ch_b_44			44	141
ch_b_45			45	142
ch_b_46			46	144
ch_b_47			47	145
ch_b_48			48	146
ch_b_49			49	147
ch_b_50			50	148

Table 15: General I/O signals

3.8 Dedicated Signals

The header connector ST1B contains some dedicated signals which are used as clock and configuration signals.

Signal Name	ST1B Pin	Connected to FPGA pin
pgck_ext	52	2 (over J2)
pgck2	54	55
pgck3	56	108
pgck4	58	160
sgck1	60	207
sgck2	62	49
sgck3	64	102
tdi	68	6
tck	69	7
tms	70	16
tdo	71	157
hdc	73	56
ldc	74	60
dup	76	N/A (goes to pin 1 of ST4)
ddown	77	N/A (goes to pin 4 of ST4)

Table 16: Dedicated signals on connector ST1B

3.9 Stack Extension

When several board modules are stacked the signal direction of I/O pins of different levels must be choosen very carefully. Short circuits between the FPGAs may result in damages or shortens their life. Unconfigured pins of the FPGA are in a high impedance state.

During the assembly of the stack you should pay attention to the fact that the pins of one module are aligned exactly with the holes of the sockets of the other module. A good possibility to accomplish this is the usage of two pieces of a prototyping board. Each of these pieces should have three rows with 50 holes. Before the assembly these pieces are slided up to the ends of the connector pins. Thereby, the pin ends keep their positions.

To disassemble a stack we recommend the usage of pliers which are used to remove locking rings. The claws of the pliers should be covered with plastic or rubber tubes to prevent damages on the boards. The modules are then separated easily by repeated application of gentle pressure with the pliers on all four corners.

4 Literature

The following list is an excerpt from the Xilinx literature concerning the Spartan FPGA family. The correspondent PDF files may be downloaded directly from http://www.xilinx.com/apps/spartapp.htm or be requested from a Xilinx distributor.

Application Notes

- XAPP120: How Spartan Series FPGAs Compete for Gate Array Production
- XAPP125: Conserving Power With Auto Power Down Mode in SpartanXL FPGAs
- XAPP124: Using Manual Power Down Mode With SpartanXL FPGAs
- XAPP123: Using Three-State Enable Registers in XLA, XV, and SpartanXL FPGAs
- XAPP099: How to Design Today for the Upcoming SpartanXL FPGA Family
- XAPP088: I/O Characteristics of the 'XL FPGAs

SelectRAM Memory

- XAPP065: Edge-Triggered and Dual-Port RAM Capability
- XAPP057: Using SelectRAM Memory in FPGAs
- XAPP053: Implementing FIFOs in RAM
- XAPP051: Synchronous and Asynchronous FIFO Designs
- XAPP052: Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators

Carry Logic

- XAPP013: Using the Dedicated Carry Logic
- XAPP023: Accelerating Loadable Counters
- XAPP018: Estimating the Performance of Adders and Counters
- XAPP014: Ultra-Fast Synchronous Counters
- XAPP027: Implementing State Machines in FPGA Devices

Configuration

- XAPP126: Data Generation and Configuration for Spartan Series FPGAs
- XAPP098: The Low-Cost, Efficient Serial Configuration of Spartan FPGAs
- XAPP122: The Express Configuration of SpartanXL FPGAs
- XAPP091: Configuring Mixed FPGA Daisy Chains
- XAPP015: Using the Readback Capability
- XAPP017: Boundary Scan in Xilinx Devices

Application Briefs

- XBRF001: SelectRAM: Flexibility with Speed
- XBRF002: Low Power Benefits: Overview
- XBRF003: SelectRAM: Maximum Configurability
- XBRF007: Xilinx FPGAs: The Best Choice for Delivering Logic Cores
- XBRF014: A Simple Method of Estimating Power in FPGAs

Data Book

- Spartan and SpartanXL Series Datasheet v1.4, 1/99
- Spartan Serial Configuration PROMs Datasheet v1.2, 9/98

Xcell Articles

- The 3.3V SpartanXL FPGA Series Invades New Territory with High Speed and Low Cost Q4 '98
- FPGAs Can Be an Effective Alternative to Mask Gate Arrays Q4 '98
- New Spartan -4 Devices for High Speed Applications Q3 '98
- Esaote Biomedica: A Spartan Success Story Q3 '98
- The Low Cost PCI Solution Q3 '98
- Spartan Series Takes the Lead with Low Power Q2 '98
- Designing with the Spartan Series FPGAs Q2 '98
- Introducing the New Spartan FPGA Family for Low Cost Applications Q1 '98
- Xilinx DSP LogiCORE Advantages Q3 '97
- SelectRAM Memory: Advantages and Uses Q3 '96
- Synchronous RAM Improves System Speed Q4 '95
- Synchronous RAM Timing Q4 '95
- Advanced Carry Logic Techniques Q2 '96

5 Appendix A: Pin Assignment of XCS-20/30/40 FPGA

Active low signals are marked with a \ at the end of the name.

Pin	Description
1	GND
2	I/O, PGCK1
3	I/O
4	I/O
5	I/O
6	I/O, TDI
7	I/O, TCK
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	GND
14	I/O
15	I/O
16	I/O, TMS
17	I/O
18	VCC
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	GND
26	VCC
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	VCC
34	I/O
35	I/O
36	I/O
37	I/O
38	GND
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O, SGCK2
50	Don‘t connect
51	GND
52	**MODE**
53	VCC
54	Don‘t connect
55	I/O, PGCK2
56	I/O(HDC)
57	I/O
58	I/O
59	I/O
60	I/O(LDC\)
61	I/O
62	I/O
63	I/O
64	I/O
65	I/O
66	GND
67	I/O
68	I/O
69	I/O
70	I/O
71	VCC
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O**(INIT\)**
78	VCC
79	GND
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	VCC
87	I/O
88	I/O
89	I/O
90	I/O
91	GND
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O, SGCK3
103	GND
104	**DONE**
105	VCC
106	**PROGRAM**
107	I/O
108	I/O, PGCK3
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O

114	I/O
115	I/O
116	I/O
117	I/O
118	GND
119	I/O
120	I/O
121	VCC
122	I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	VCC
131	GND
132	I/O
133	I/O
134	I/O
135	I/O
134	I/O
137	I/O
138	I/O
139	I/O
140	VCC
141	I/O
142	I/O
143	GND
144	I/O
145	I/O
146	I/O

147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O**(DIN)**
154	I/O, SGCK4**(DOUT)**
155	**CCLK**
156	VCC
157	O, TDO
158	GND
159	I/O
160	I/O, PGCK4
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	I/O
170	GND
171	I/O
172	I/O
173	VCC
174	I/O
175	I/O
176	I/O
177	I/O
178	I/O

179	I/O
180	I/O
181	I/O
182	GND
183	VCC
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	VCC
193	I/O
194	I/O
195	GND
196	I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	I/O
203	I/O
204	I/O
205	I/O
206	I/O
207	I/O, SGCK1
208	VCC

Table 17: Pin assignment of XCS-20/30/40 FPGA in PQ-208 package

6 Appendix B: Schematic Diagram and PCB Layout

The following pages show some technical details of the board:

- Top overlay silk screen
- Layout (signal layers)
- Schematic diagram