RENESAS

RL78/G12

RENESAS MCU

R01DS0193EJ0100
Rev.1.00
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True Low Power Platform (as low as 63 µA/MHz), 1.8V to 5.5V operation,
2 to 16 Kbyte Flash, 31 DMIPS at 24MHz, for General Purpose Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 1.8V to 5.5V operation from a single supply
- Stop (RAM retained): 0.23µA, (LVD enabled): 0.31µA
- Snooze: 0.7mA (UART), 1.20mA (ADC)
- Operating: 63 µA /MHz

16-bit RL78 CPU Core
- Delivers 31 DMIPS at maximum operating frequency of 24MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Main Flash Memory
- Density: 2 KB to 16 KB
- Block size: 1KB
- On-chip single voltage flash memory with protection from block erase/writing

Data Flash Memory
- Data Flash with background operation
- Data flash size: 2 KB size options
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM
- 256 B to 1.5 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed Oscillator Oscillator
- 24MHz with +/- 1% accuracy over voltage (1.8 V to 5.5 V) and temperature (-40°C to 85°C)
- Pre-configured settings: 24MHz, 16MHz, 12MHz, 8MHz, 4MHz & 1MHz

Reset and Supply Management
- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 12 setting options (Interrupt and/or reset function)

Data Memory Access (DMA) Controller
- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces
- Up to 3 x I^2C master
- Up to 1 x I^2C multi-master
- Up to 3 x CSI/SPI (7-, 8-bit)
- Up to 3 x UART (7-, 8-, 9-bit)

Extended-Function Timers
- Multi-function 16-bit timers: Up to 8 channels
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer : 1 channel (window function)

Rich Analog
- ADC: Up to 11 channels, 10-bit resolution, 2.1µs conversion time
- Supports 1.8V
- Internal voltage reference (1.45V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/ frequency detection
- ADC self-test

General Purpose I/O
- 5V tolerant, high-current (up to 20mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature
- Standard: –40°C to +85°C

Package Type and Pin Count
- QFN: 24
- SSOP: 20, 30

*** There is difference in specifications between every product. Please refer to specification for details.**

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	20 pins	24 pins	30 pins
16 KB	2 KB	2 KB	–	–	R5F102AA
	–		–	–	R5F103AA
	2 KB	1.5 KB	R5F1026A[Note]	R5F1027A[Note]	–
	–		R5F1036A[Note]	R5F1037A[Note]	–
12 KB	2KB	1 KB	R5F10269[Note]	R5F10279[Note]	R5F102A9
	–		R5F10369[Note]	R5F10379[Note]	R5F103A9
8 KB	2 KB	768B	R5F10268[Note]	R5F10278[Note]	R5F102A8
	–		R5F10368[Note]	R5F10378[Note]	R5F103A8
4 KB	2KB	512B	R5F10267	R5F10277	R5F102A7
	–		R5F10367	R5F10377	R5F103A7
2 KB	2 KB	256B	R5F10266	–	–
	–		R5F10366	–	–

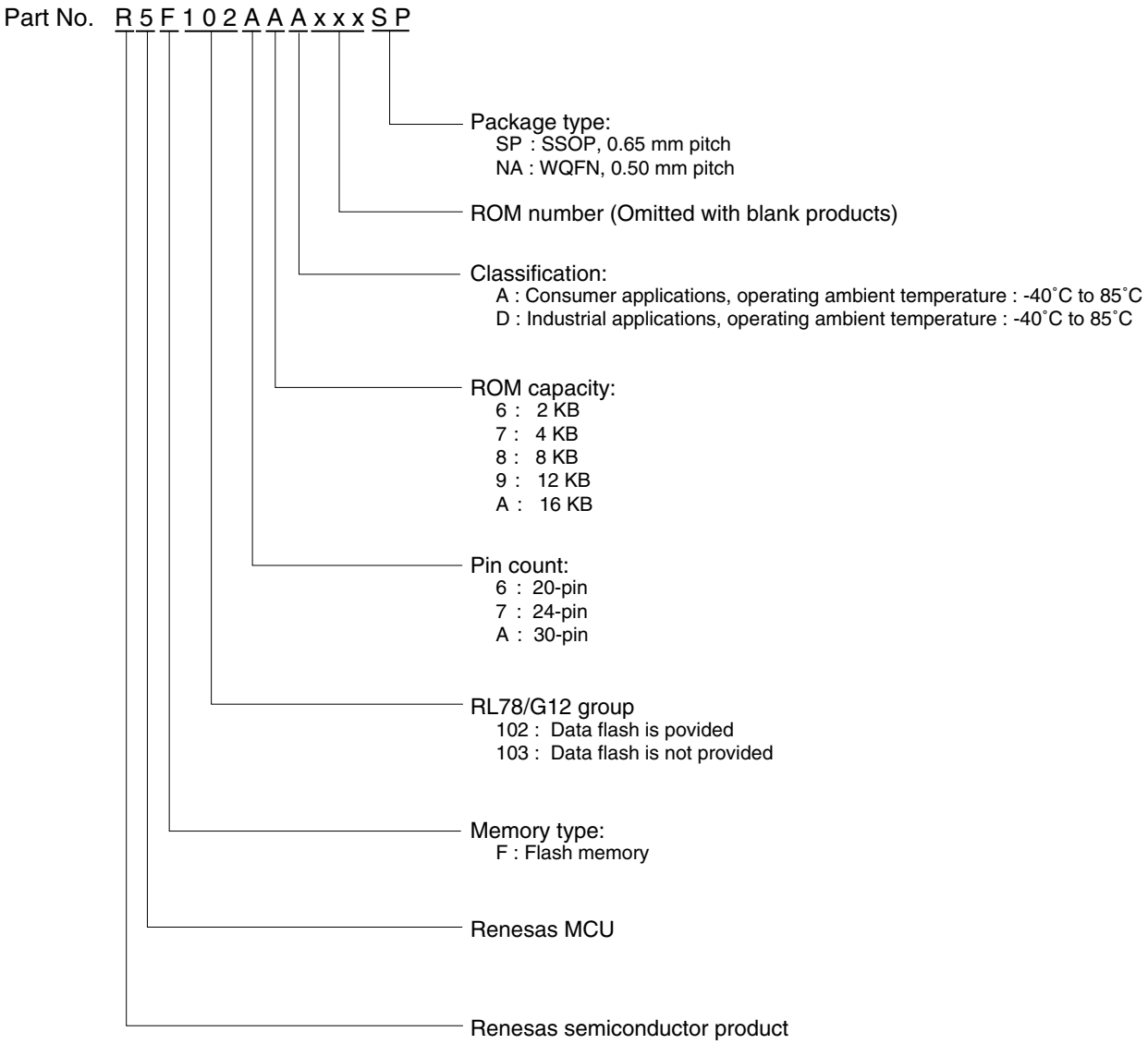
Note This is about 639 byte when the self-programing function and data flash function are used (For detail, see **CHAPTER 3 CPU ARCHITECTURE in the RL78/G12 User's Manual**).

1.2 Ordering Information

Pin count	Package	Data flash	Fields of Application	Part Number
20 pins	20-pin plastic SSOP (4.4 × 6.5)	Mounted	A	R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
		Not mounted	D	R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
24 pins	24-pin plastic WQFN (4 × 4)	Mounted	A	R5F1027AANA, R5F10279ANA, R5F10278ANA, R5F10277ANA R5F1027ADNA, R5F10279DNA, R5F10278DNA, R5F10277DNA
		Not mounted	D	R5F1037AANA, R5F10379ANA, R5F10378ANA, R5F10377ANA R5F1037ADNA, R5F10379DNA, R5F10378DNA, R5F10377DNA
30 pins	30-pin plastic SSOP (7.62 mm (300))	Mounted	A	R5F102AAASP, R5F102A9ASP, R5F102A8ASP, R5F102A7ASP R5F102AADSP, R5F102A9DSP, R5F102A8DSP, R5F102A7DSP
		Not mounted	D	R5F103AAASP, R5F103A9ASP, R5F103A8ASP, R5F103A7ASP R5F103AADSP, R5F103A9DSP, R5F103A8DSP, R5F103A7DSP

Note For fields of application, see **Figure 1-1. Part Number, Memory Size, and Package of RL78/G12**.

Figure 1-1. Part Number, Memory Size, and Package of RL78/G12



1.3 Differences between R5F102 and R5F103

The following are differences between the R5F102 and R5F103.

- Whether the data flash memory is mounted or not
- High-speed on-chip oscillator oscillation frequency accuracy
- Number of channels in serial interface
- Whether the DMA function is mounted or not
- Whether the safety function is mounted or not

1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 but not on the R5F103.

Product	Data Flash
R5F102 R5F1026A, R5F1027A, R5F102AA, R5F10269, R5F10279, R5F102A9, R5F10268, R5F10278, R5F102A8, R5F10267, R5F10277, R5F102A7, R5F10266 Note	2KB
R5F103 R5F1036A, R5F1037A, R5F103AA, R5F10369, R5F10379, R5F103A9, R5F10368, R5F10378 R5F103A8, R5F10367, R5F10377, R5F103A7, R5F10366	Not mounted

Note The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

Caution When the flash memory is rewritten via a user program, the flash ROM area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -20 to +85 °C	-1	+1	%
	T_A = -40 to -20 °C	-1.5	+1.5	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -40 to + 85 °C	-5	+5	%

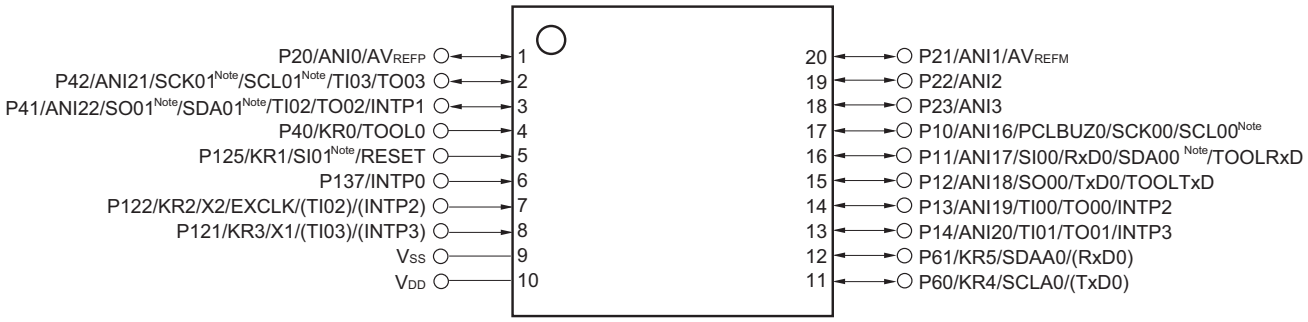
1.3.3 Peripheral Functions

RL78/G12		R5F102		R5F103	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I^2C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

1.4 Pin Configuration (Top View)

1.4.1 20-pin products

- 20-pin plastic SSOP (4.4 × 6.5)



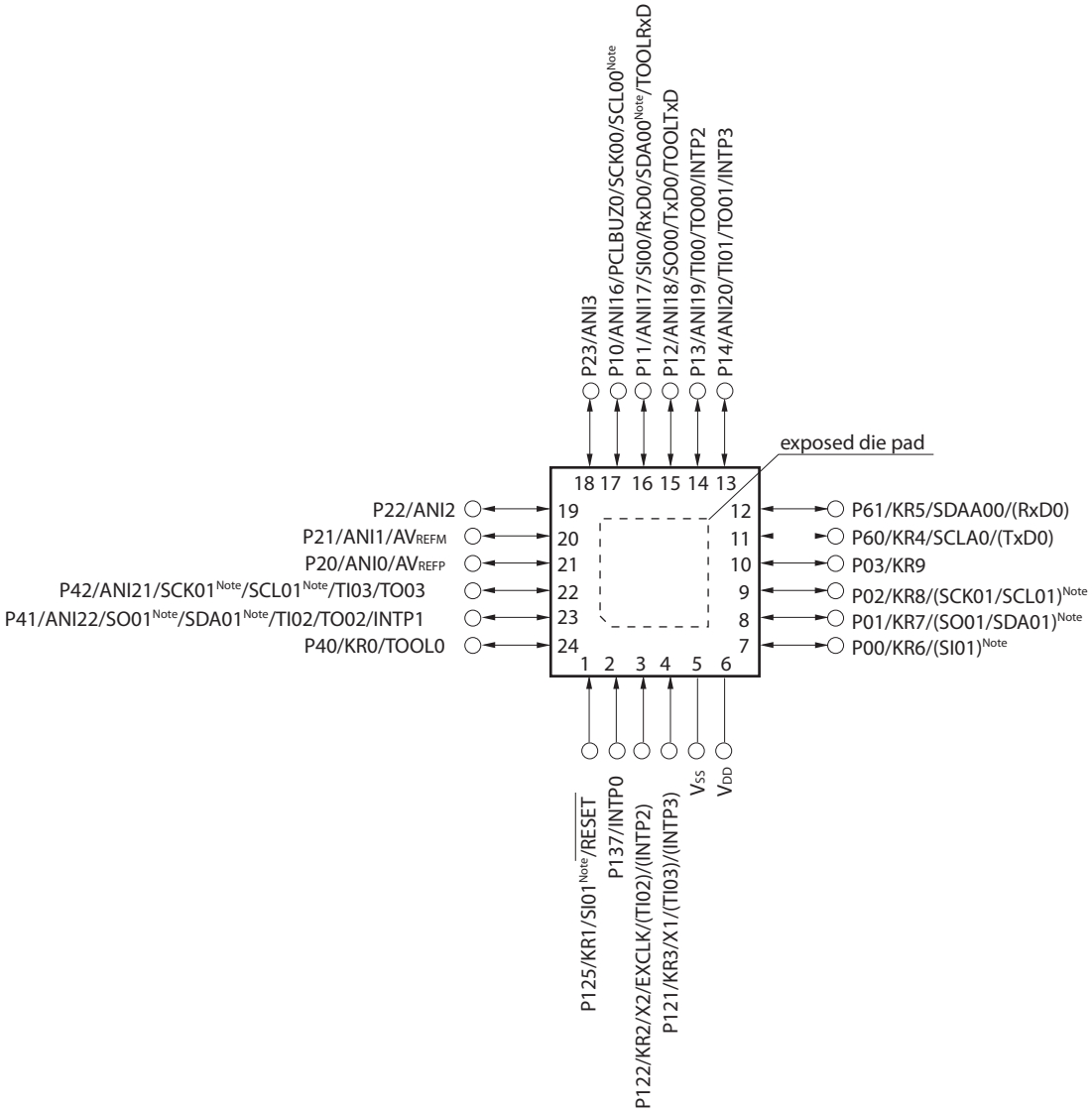
Note Provided in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4.2 24-pin products

- 24-pin plastic WQFN (4 × 4)



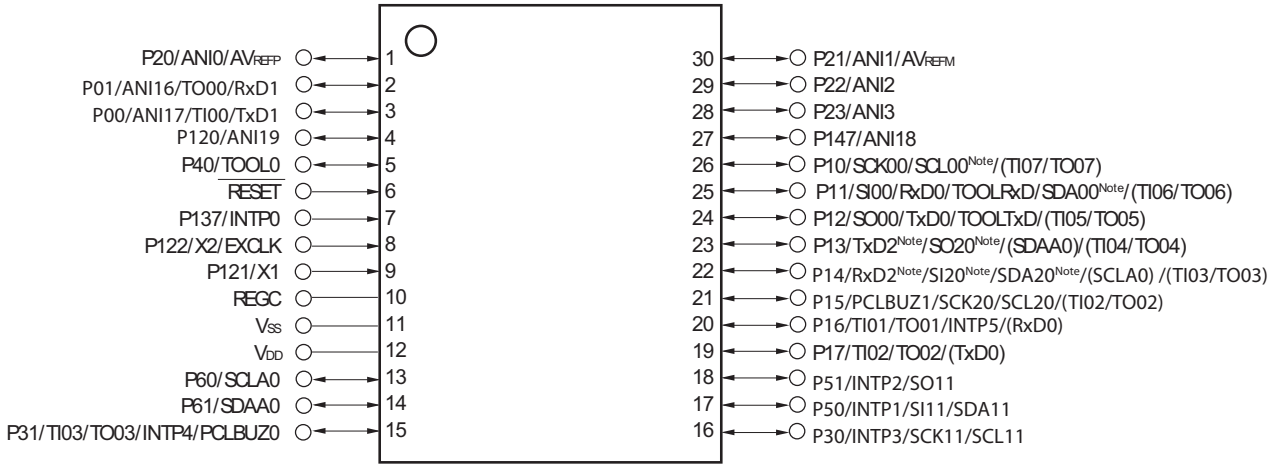
Note Provided in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4.3 30-pin products

- 30-pin plastic SSOP (7.62 mm (300))



Note Provided in the R5F102 products.

Caution Connect the REGC pin to Vss via capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.5 Pin Identification**.

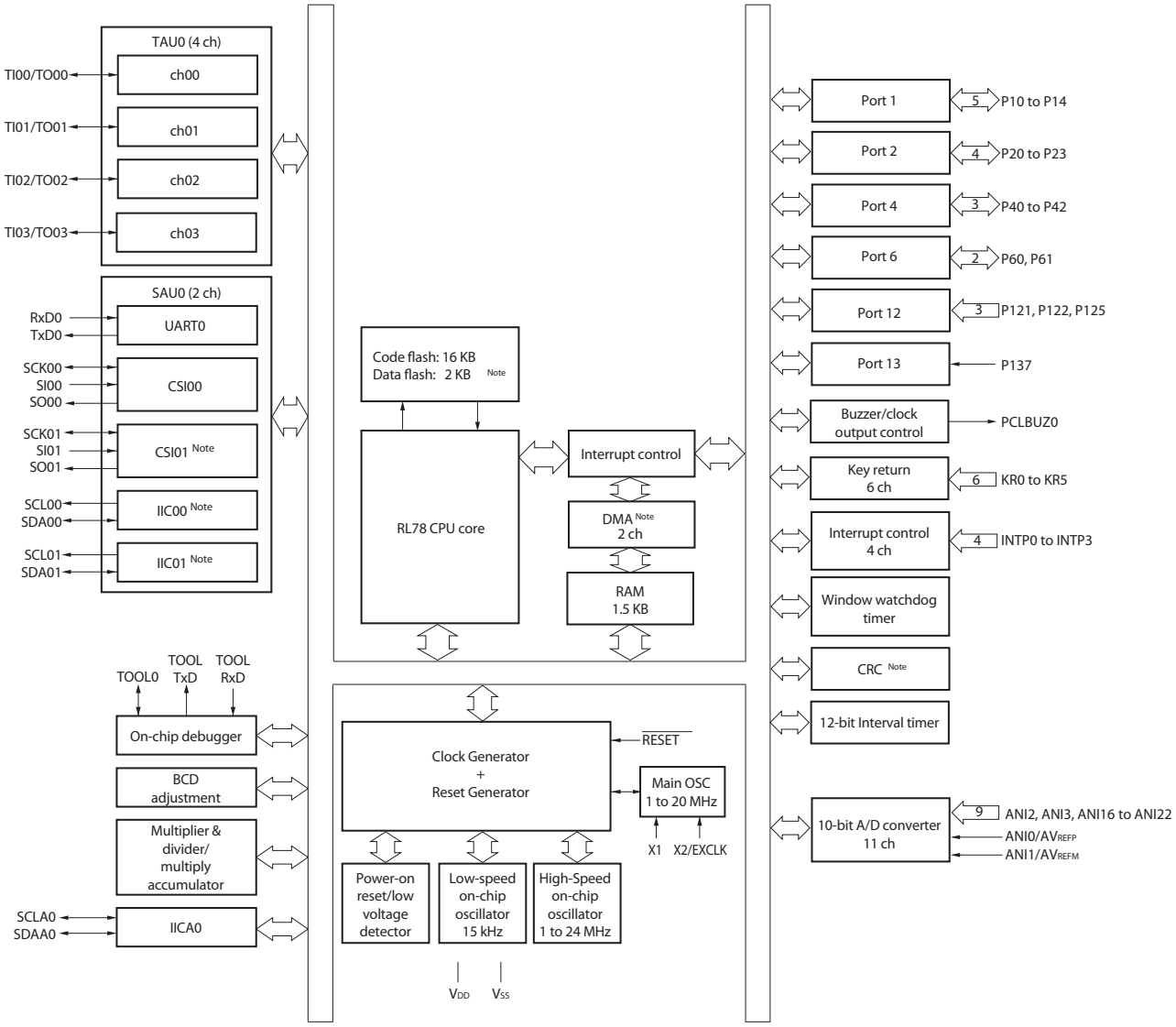
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5 Pin Identification

ANI0 to ANI3, ANI16 to ANI22:	Analog input
AV_{REFM}:	Analog Reference Voltage Minus
AV_{REFP}:	Analog reference voltage plus
EXCLK:	External Clock Input (Main System Clock)
INTP0 to INTP5	Interrupt Request From Peripheral
KR0 to KR9	Key Return
P00 to P03:	Port 0
P10 to P17:	Port 1
P20 to P23:	Port 2
P30 to P31:	Port 3
P40 to P42:	Port 4
P50, P51:	Port 5
P60, P61:	Port 6
P120 to P122, P125:	Port 12
P137:	Port 13
P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/ Buzzer Output
REGC:	Regulator Capacitance
$\overline{\text{RESET}}$:	Reset
RxD0 to RxD2:	Receive Data
SCK00, SCK01, SCK11, SCK20:	Serial Clock Input/Output
SCL00, SCL01, SCL11, SCL20, SCLA0:	Serial Clock Input/Output
SDA00, SDA01, SDA11, SDA20, SDAA0:	Serial Data Input/Output
SI00, SI01, SI11, SI20:	Serial Data Input
SO00, SO01, SO11, SO20:	Serial Data Output
TI00 to TI07:	Timer Input
TO00 to TO07:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOLRxD, TOOLTxD:	Data Input/Output for External Device
TxD0 to TxD2:	Transmit Data
V_{DD}:	Power supply
V_{SS}:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)

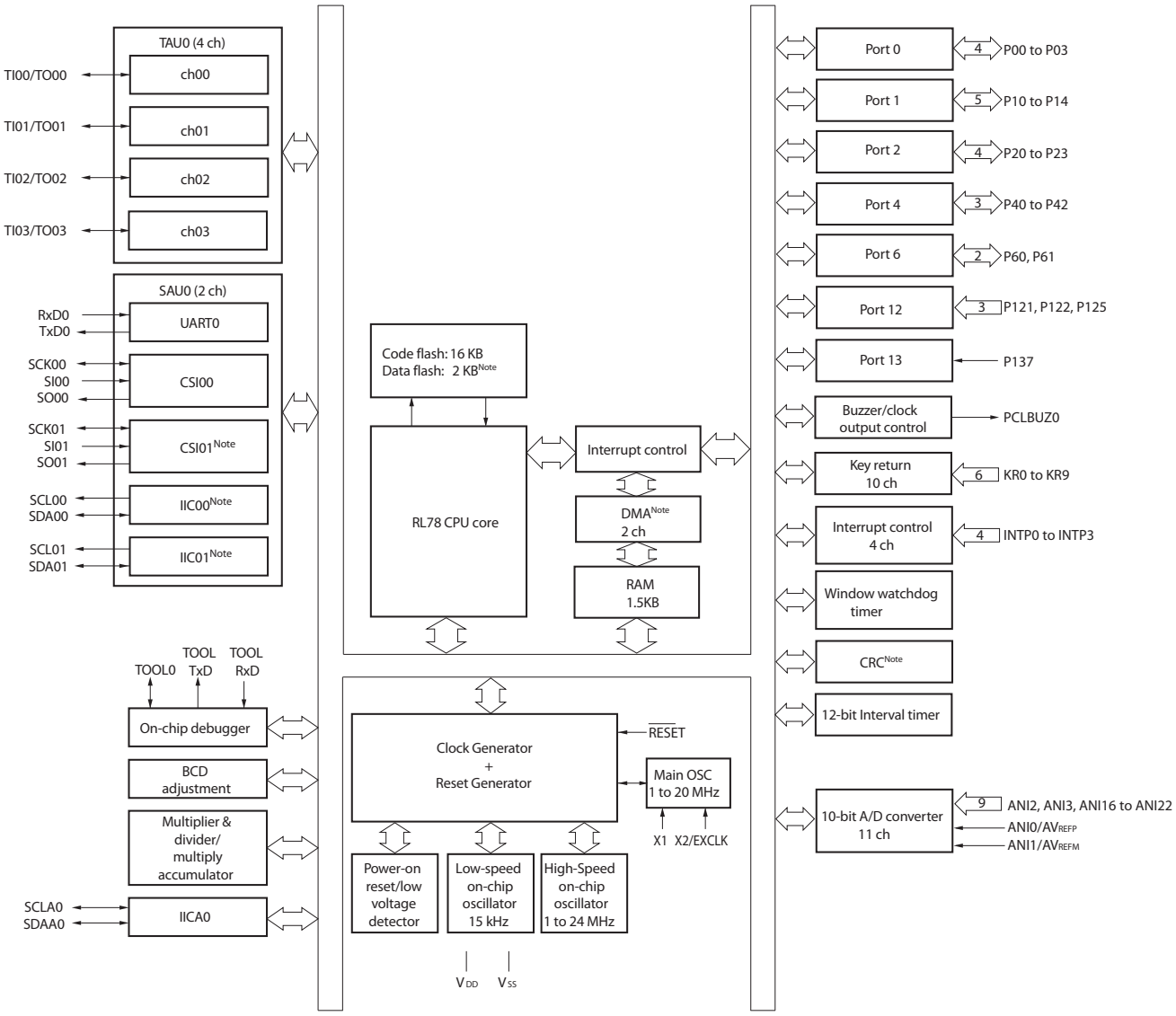
1.6 Block Diagram

1.6.1 20-pin products



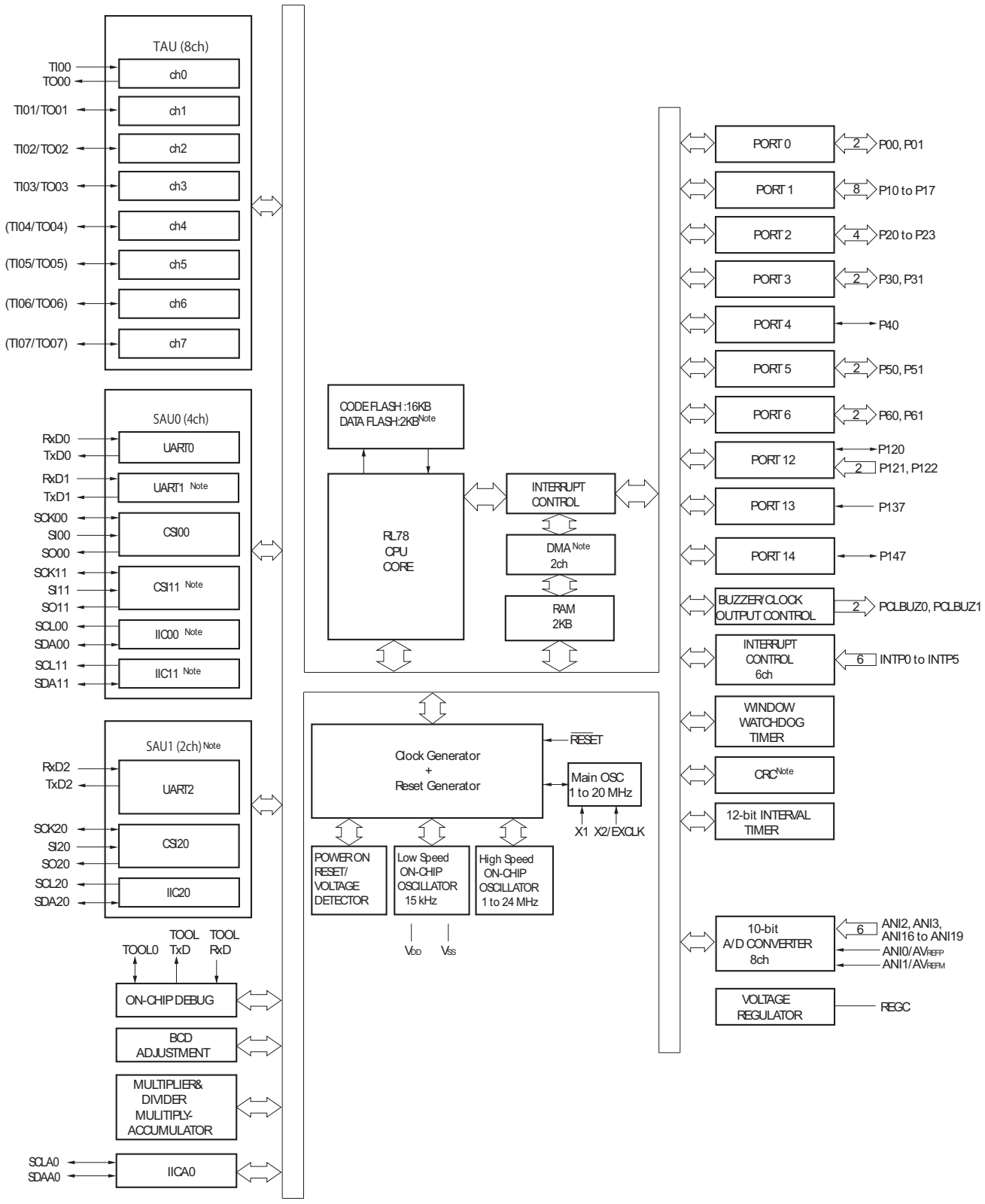
Note Provided for the R5F102 products.

1.6.2 24-pin products



Note Provided for the R5F102 products.

1.6.3 30-pin products



Note Provided for the R5F102 products.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.7 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H (except timer output of R5F102Ax)

(1/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Code flash memory		2 to 16 KB Note 1		4 to 16 KB			
Data flash memory		2 KB	–	2 KB	–	2 KB	–
RAM		256 B to 1.5 KB		512 B to 1.5 KB		512 B to 2KB	
Address space		1 MB					
Main system clock	High-speed system clock	X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 5.5 V					
	High-speed on-chip oscillator clock	HS (High-speed main) mode : 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode : 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V)					
Low-speed on-chip oscillator clock		15 kHz (TYP)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)					
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total	18		22		26	
	CMOS I/O	12		16		21	
	CMOS input	4		4		3	
	N-ch open-drain I/O (6 V tolerance)	2					
Timer	16-bit timer	4 channels				8 channels	
	Watchdog timer	1 channel					
	12-bit Interval timer	1 channel					
	Timer output	4/8 Note 2 (PWM Output Note 3: 3/7 Note 2)					

Notes 1. The self-programming function cannot be used in the R5F10266 and R5F10366.

2. When PIOR0 is set to 1 in R5F102Az.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (see **6.8.3 Operation as multiple PWM output function in the RL78/G12 User's Manual**).

Caution When the flash memory is rewritten via a user program, the flash ROM area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

(2/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Clock output/buzzer output		1					
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)					
8/10-bit resolution A/D converter		11 channels				8 channels	
Serial interface		CSI/UART/Simplified I^2C + CSI/Simplified I^2C [Product with data flash memory (30-pin)] CSI/UART/Simplified I^2C x 3 CSI + UART					
	I^2C bus	1 channel					
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (unsigned or signed)					
DMA controller		2 channels	–	2 channels	–	2 channels	–
Vectored interrupt sources	Internal	18	16	18	16	26	19
	External	5				6	
Key interrupt		6		10		–	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		• Power-on-reset: 1.51 ± 0.03 V • Power-down-reset: 1.50 ± 0.03 V					
Voltage detector		• Rising edge : 1.88 to 4.06 V (12 stages) • Falling edge : 1.84 to 3.98 V (12 stages)					
On-chip debug function		Provided					
Power supply voltage		V_{DD} = 1.8 to 5.5 V					
Operating ambient temperature		T_A = −40 to +85°C					

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

Cautions 1. The RL78/G12 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product in the RL78/G12 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to + 6.5	V
	V_{SS}			−0.5 to + 0.3	V
REGC terminal input voltage[Note 1]	V_{IREGC}	REGC		−0.3 to +2.8 and −0.3 to V_{DD} + 0.3[Note 2]	V
Input Voltage	V_{I1}	Other than P60, P61		−0.3 to V_{DD} + 0.3[Note 3]	V
	V_{I2}	P60, P61 (N-ch open drain)		−0.3 to 6.5	V
Output Voltage	V_O			−0.3 to V_{DD} + 0.3[Note 3]	V
Analog input voltage	V_{AI}	ANI0 to ANI22		−0.3 to V_{DD} + 0.3[Note 3] and −0.3 to AVREF(+)+0.3[Note 3]	V
Output current, high	I_{OH1}	Per pin	Other than P20 to P23	−40	mA
		Total of all pins	All the terminals other than P20 to P23	−170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	−70	mA
			20-, 24-pin products: P00 to P03[Note 4], P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	−100	mA
	I_{OH2}	Per pin	P20 to P23	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	Other than P20 to P23	40	mA
		Total of all pins	All the terminals other than P20 to P23	170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	70	mA
			20-, 24-pin products: P00 to P03, P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	100	mA
	I_{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Notes 1. 30-pin product only.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

3. Must be 6.5 V or lower.

4. 24-pin product only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

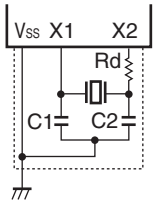
Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

2.2 Oscillator Characteristics

2.2.1 X1 clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Recommended Circuit	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator / crystal oscillator		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation frequency Note 1	f_{IH}			1		24	MHz
High-speed on-chip oscillator oscillation frequency accuracy Note 2		R5F102	T_A = -20 to +85°C	-1		+1	%
			T_A = -40 to -20°C	-1.5		+1.5	%
		R5F103		-5		+5	%
Low-speed on-chip oscillator oscillation frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator oscillation frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin	20-, 24-pin products: P00 to P03 [Note 3], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				–10.0	mA
		Total of all pins[Note 2]	20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V			–30.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			–6.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–4.5	mA
			20-, 24-pin products: P00 to P03 [Note 3], P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	4.0 V ≤ V_{DD} ≤ 5.5 V			–80.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			–18.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
			All the terminals				–100	mA
	I_{OH2}	Per pin	P20 to P23				–0.1	mA
		Total of all pins[Note 2]					–0.4	mA

Notes 1. value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(50 × 0.01) = –14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. 24-pin products only.

Caution P10 to P12, P41 for 20-pin products, P01, P10 to P12, P41 for 24-pin products, and P00, P10 to P15, P17, P50 for 30-pin products, do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/4)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin	20-, 24-pin products: P00 to P03 [Note 3], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				20.0	mA
			P60, P61				15.0	mA
		Total of all pins[Note 2]	20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	4.0 V ≤ V_{DD} ≤ 5.5 V			60.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			9.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			1.8	mA
			20-, 24-pin products: P00 to P03 [Note 3], P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			27.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			5.4	mA
			All the terminals				140	mA
	I_{OL2}	Per pin	P20 to P23				0.4	mA
		Total of all pins[Note 2]					1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(50 × 0.01) = 14.0 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Normal input buffer 20-, 24-pin products: P00 to P03 Note 2, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147		0.8V_{DD}		V_{DD}	V
	V_{IH2}	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			1.8 V ≤ V_{DD} < 3.3 V	1.50		V_{DD}	V
	V_{IH3}	P20 to P23		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60, P61		0.7V_{DD}		6.0	V
	V_{IH5}	P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	Normal input buffer 20-, 24-pin products: P00 to P03 Note 2, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147		0		0.2V_{DD}	V
	V_{IL2}	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			1.8 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P23		0		0.3V_{DD}	V
	V_{IL4}	P60, P61		0		0.3V_{DD}	V
	V_{IL5}	P121, P122, P125 Note 1, P137, EXCLK, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
Output voltage, high	V_{OH1}	20-, 24-pin products: P00 to P03 Note 2, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –10.0 mA	V_{DD}–1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD}–0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –2.0 mA	V_{DD}–0.6			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	V_{DD}–0.5			V
	V_{OH2}	P20 to P23	I_{OH2} = –100 μA	V_{DD}–0.5			V

Notes 1. 20, 24-pin products only.

2. 24-pin products only.

Caution The maximum value of V_{IH} of pins P01, P10 to P12, P41, for 20-, 24-pin products and P00, P10 to P15, P17, P50 for 30-pin products is V_{DD} even in N-ch open-drain mode.
High level is not output in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, IOL1 = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P23	I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
Input leakage current, high	I_{LIH1}	Other than P121, P122	V_I = V_{DD}			1	μA
	I_{LIH2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{DD} Input port or external clock input			1	μA
			V_I = V_{DD} When resonator connected			10	μA
Input leakage current, low	I_{LIL1}	Other than P121, P122	V_I = V_{SS}			–1	μA
	I_{LIL2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{SS} Input port or external clock input			–1	μA
			V_I = V_{SS} When resonator connected			–10	μA
On-chip pull-up resistance	R_U	20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$ 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147, $\overline{\text{RESET}}$	V_I = V_{SS}, input port	10	20	100	kΩ

Note 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) 20-, 24-pin products

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS(High-speed main) mode[Note 2]	f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Noramal operation	V_{DD} = 5.0 V		3.3	5.0	mA
						V_{DD} = 3.0 V		3.3	5.0	
				f_{IH} = 16 MHz[Note 3]		V_{DD} = 5.0 V		2.5	3.7	mA
						V_{DD} = 3.0 V		2.5	3.7	
			LS(Low-speed main) mode[Note 2]	f_{IH} = 8 MHz[Note 3]		V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			HS(High-speed main) mode[Note 2]	f_{MX} = 20 MHz[Note 4], V_{DD} = 5.0 V		Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
				f_{MX} = 20 MHz[Note 4], V_{DD} = 3.0 V		Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
				f_{MX} = 10 MHz[Note 4], V_{DD} = 5.0 V		Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	
				f_{MX} = 10 MHz[Note 4], V_{DD} = 3.0 V		Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	
			LS(Low-speed main) mode[Note 2]	f_{MX} = 8 MHz[Note 4], V_{DD} = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz[Note 4], V_{DD} = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

3. When high-speed system clock is stopped

4. When high-speed on-chip osicllator clock is stopped.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}	HALT mode[Note 2]	HS(High-speed main) mode[Note 3]	f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		440	1210	μA
					V_{DD} = 3.0 V		440	1210	
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 5.0 V		400	950	μA
					V_{DD} = 3.0 V		400	950	
			LS(Low-speed main) mode[Note 3]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		270	542	μA
					V_{DD} = 2.0 V		270	542	
			HS(High-speed main) mode[Note 3]	f_{MX} = 20 MHz[Note 5], V_{DD} = 5.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 20 MHz[Note 5], V_{DD} = 3.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 10 MHz[Note 5], V_{DD} = 5.0 V	Square wave input		190	590	μA
					Resonator connection		260	660	
				f_{MX} = 10 MHz[Note 5], V_{DD} = 3.0 V	Square wave input		190	590	μA
					Resonator connection		260	660	
			LS(Low-speed main) mode[Note 3]	f_{MX} = 8 MHz[Note 5], V_{DD} = 3.0 V	Square wave input		110	360	μA
					Resonator connection		150	416	
				f_{MX} = 8 MHz[Note 5], V_{DD} = 2.0 V	Square wave input		110	360	μA
					Resonator connection		150	416	
	I_{DD3}	STOP mode[Note 6]	T_A = –40°C				0.19		μA
			T_A = +25°C				0.24	0.50	
			T_A = +50°C				0.25	0.80	
			T_A = +70°C				0.28	1.20	
			T_A = +85°C				0.88	2.20	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

4. When high-speed system clock is stopped.

5. When high-speed on-chip oscillator clock is stopped.

6. When high-speed on-chip oscillator clock, high-speed system clock, and watchdog timer are stopped.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Except temperature condition of the TYP. value is T_A = 25°C, other than STOP mode

(2) 30-pin products

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS(High-speed main) mode[Note 2]	f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Noramal operation	V_{DD} = 5.0 V		3.7	5.5	mA
						V_{DD} = 3.0 V		3.7	5.5	
				f_{IH} = 16 MHz[Note 3]		V_{DD} = 5.0 V		2.7	4.0	mA
						V_{DD} = 3.0 V		2.7	4.0	
			LS(Low-speed main) mode[Note 2]	f_{IH} = 8 MHz[Note 3]		V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			HS(High-speed main) mode[Note 2]	f_{MX} = 20 MHz[Note 4], V_{DD} = 5.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 20 MHz[Note 4], V_{DD} = 3.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz[Note 4], V_{DD} = 5.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
				f_{MX} = 10 MHz[Note 4], V_{DD} = 3.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS(Low-speed main) mode[Note 2]	f_{MX} = 8 MHz[Note 4], V_{DD} = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz[Note 4], V_{DD} = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

3. When high-speed system clock is stopped

4. When high-speed on-chip osicllator clock is stopped.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}	HALT mode[Note 2]	HS(High-speed main) mode[Note 3]	f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		440	1280	μA
					V_{DD} = 3.0 V		440	1280	
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 5.0 V		400	1000	μA
					V_{DD} = 3.0 V		400	1000	
			LS(Low-speed main) mode[Note 3]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	
			HS(High-speed main) mode[Note 3]	f_{MX} = 20 MHz[Note 5], V_{DD} = 5.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 20 MHz[Note 5], V_{DD} = 3.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 10 MHz[Note 5], V_{DD} = 5.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
				f_{MX} = 10 MHz[Note 5], V_{DD} = 3.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
			LS(Low-speed main) mode[Note 3]	f_{MX} = 8 MHz[Note 5], V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
				f_{MX} = 8 MHz[Note 5], V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
	I_{DD3}	STOP mode[Note 6]	T_A = –40°C				0.18		μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.26	1.10	
			T_A = +70°C				0.29	1.90	
			T_A = +85°C				0.90	3.30	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

4. When high-speed system clock is stopped.

5. When high-speed on-chip oscillator clock is stopped.

6. When high-speed on-chip oscillator clock, high-speed system clock, and watchdog timer are stopped. The values below the MAX. column include the leakage current.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T_A = 25°C.

(3) Common to RL78/G12 all products

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
12-bit interval timer operating current	I_{TMKA} Notes 1, 2	f_{IL} = 15 kHz			0.22		μA
Watchdog timer operating current	I_{WDT} Notes 1, 3	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Note 4	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage current	I_{ADREF} Note 5				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 5				75.0		μA
LVD operating current	I_{LVD} Note 6				0.08		μA
BGO operating current	I_{BGO} Note 7				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 5	ADC operation	The mode is performed Note 8		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. When high speed on-chip oscillator and high-speed system clock are stopped.

2. Current flowing only to the 12-bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78/G12 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode.

3. Current flowing only to the watchdog timer (including the operating current of the 15 KHz low-speed on-chip oscillator). The current value of the RL78/G12 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode.

4. Current flowing only to the A/D converter. The current value of the RL78/G12 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing to the V_{DD}.

6. Current flowing only to the LVD circuit. The current value of the RL78/G12 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{VLD} when the LVD circuit operates in the Operating, HALT or STOP mode.

7. Current flowing only to the BGO. The current value of the RL78/G12 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode.

8. Refer to shift time to the SNOOZE mode, see **17.2.3 SNOOZE mode in the RL78/G12 User's Manual**.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{CLK}: CPU/peripheral hardware clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C

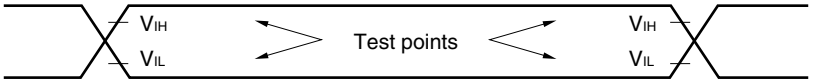
2.4 AC Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

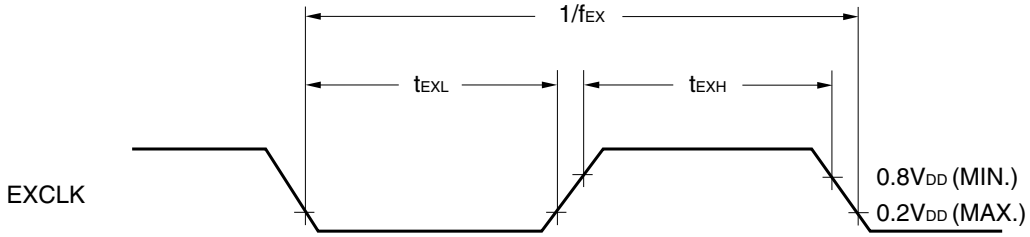
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	HS(High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
			2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		LS(Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.0		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V		1.0		8.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V		24			ns
		1.8 V ≤ V_{DD} < 2.7 V		60			ns
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V				12	MHz
		2.7 V ≤ V_{DD} < 4.0 V				8	MHz
		1.8 V ≤ V_{DD} < 2.7 V				4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V				16	MHz
		2.7 V ≤ V_{DD} < 4.0 V				8	MHz
		1.8 V ≤ V_{DD} < 2.7 V				4	MHz
INTP0 to INTP5 input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
KR0 to KR9 input available width	t_{KR}			250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

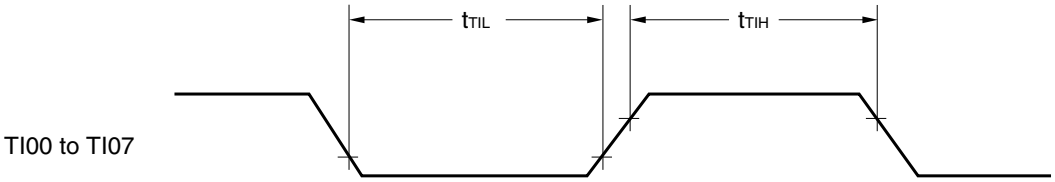
AC Timing Test Point



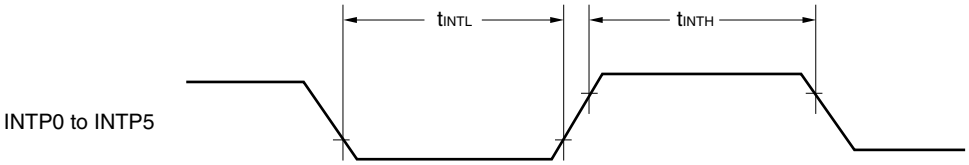
External main system clock timing



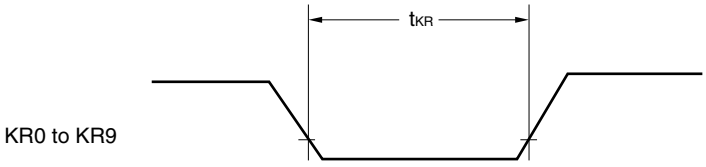
TI timing



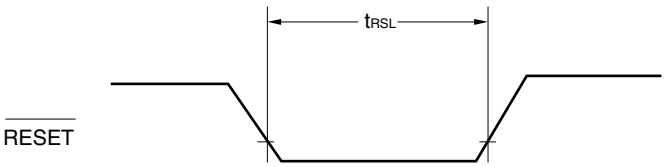
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ input timing



2.5 Serial Communication Characteristics

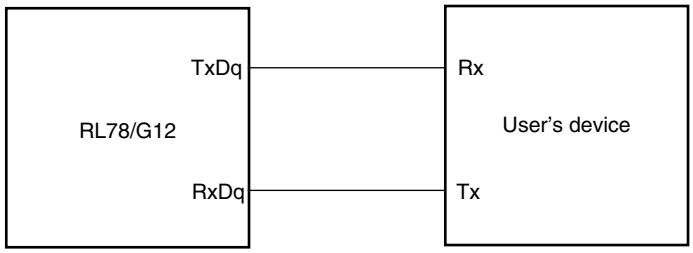
2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

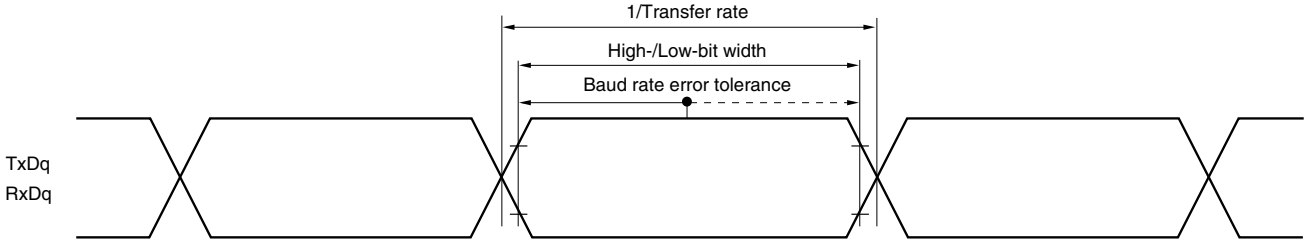
(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		Normal operation			f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 24 MHz			4.0	Mbps
		SNOOZE mode	4800		9600	bps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg)

Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI00 master mode (f_{MCK}/2), SCK00... internal clock output)
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK00 cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V	83.3 Note 1			ns
SCK00 high - /low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 7			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 10			ns
SI00 setup time (to SCK00↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	23			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	33			ns
SI00 hold time (to SCK00↑) Note2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
Delay time from SCK00↓ to SO00 output Note 4	t_{KSO1}	C = 20 pF Note 5			10	ns

Notes 1. The value must also be 2/f_{CLK} or more.

2. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 setup time becomes “to SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

3. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 hold time becomes “from SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

4. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The delay time to SO00 output becomes “from SCK00↑” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

5. C is the load capacitance of the SCK00 and SO0 output lines.

Caution Select the normal input buffer for the SI00 pin and the normal output mode for the SO00 and SCK00 pins by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).

Remarks 1. This specification is valid only when CSI00’s peripheral I/O redirect function is not used.

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS00 bit of serial mode register (SMR00).

(3) During communication at same potential (CSI mode) (master mode (f_{MCK}/4), SCKp... internal clock output)
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V	167 Note 1			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	250 Note 1			ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	500 Note 1			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 12			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 18			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 38			ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 50			ns
SIp setup time (to SCKp↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	44			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	44			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	75			ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	110			ns
SIp hold time (from SCKp↑) Note 3	t_{KSI1}		19			ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	C = 30 pF Note 5			25	ns

Notes 1. The value must also be 4/f_{CLK} or more.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode registers 0, 1 (PIM0, PIM1) and port output mode registers 0, 1 (POM0, POM1).

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unito number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is for the R5F102 products.)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (n = 0, 1, 3; "1, 3" is for the R5F102 products.)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	Normal operation					
		4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		1.8 V ≤ V_{DD} < 2.7 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		SNOOZE mode				1	Mbps
SCKp high-/low-level width	t_{KH2}, t_{KL2}	1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK}+20			ns
		1.8 V ≤ V_{DD} < 2.7 V		1/f_{MCK}+30			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK}+31			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+44	ns
			2.4 V ≤ V_{DD} < 2.7 V			2/f_{MCK}+75	ns
			1.8 V ≤ V_{DD} < 2.4 V			2/f_{MCK}+110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

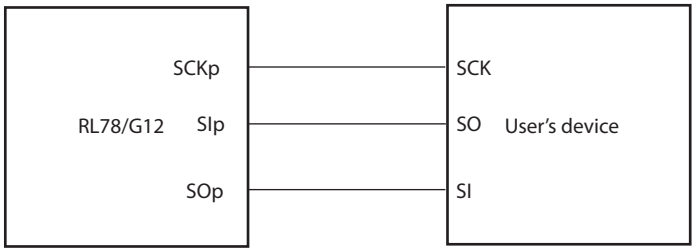
4. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode registers 0, 1 (PIM0, PIM1) and port output mode registers 0, 1 (POM0, POM1).

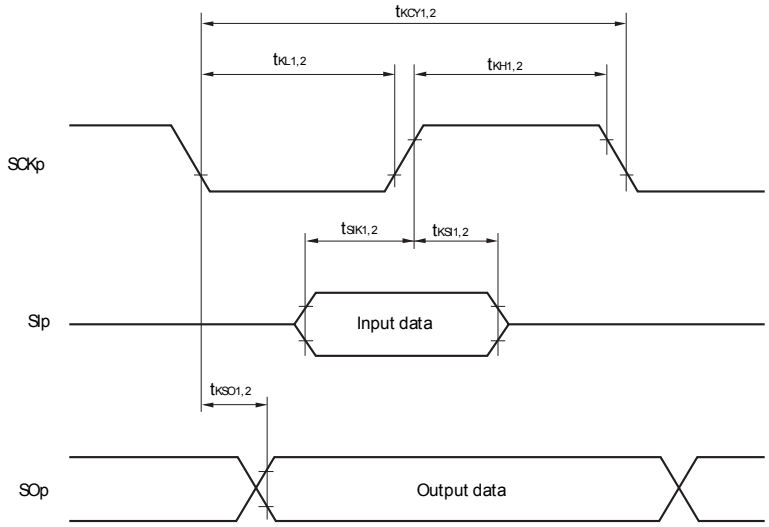
Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3; "1, 3" is for the R5F102 products.)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (n = 0, 1, 3; "1, 3" is for the R5F102 products.)

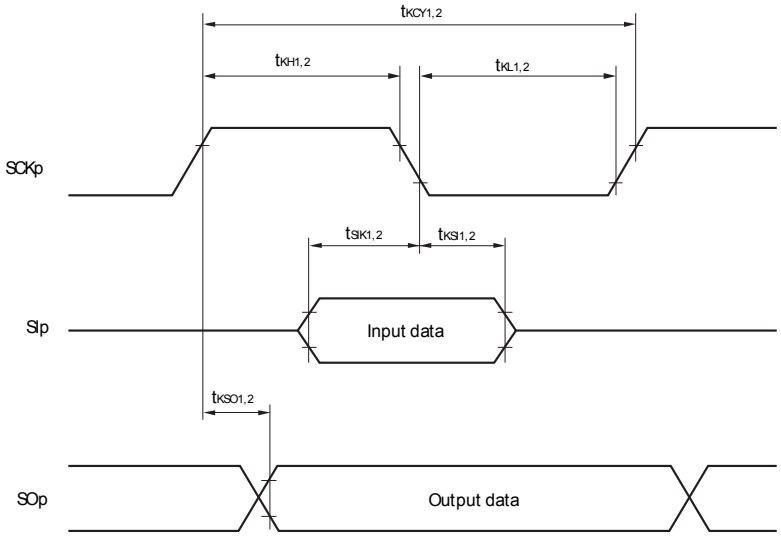
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 11, 20)

2. n: Channel number (0, 1, 3)

(5) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	Typ.	MAX.	Unit
SCLr clock frequency	f_{SCL}	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ			400	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ			300	kHz
Hold time when SCLr = “L”	t_{LOW}	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150			ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550			ns
Hold time when SCLr = “H”	t_{HIGH}	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150			ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550			ns
Data setup time (reception)	$t_{SU:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 Note			ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 230 Note			ns
Data hold time (transmission)	$t_{HD:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0		355	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0		405	ns

Note Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for SDAr by using port output mode register h (POMh).

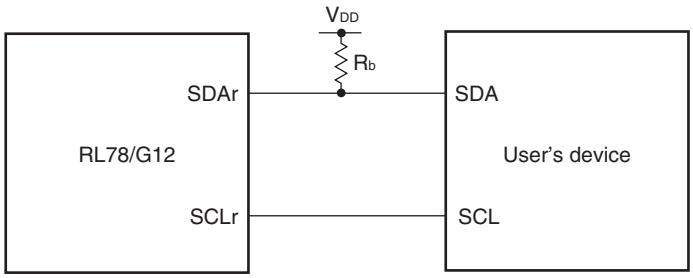
Remarks 1. R_b [Ω]:Communication line (SDAr) pull-up resistance
C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1)

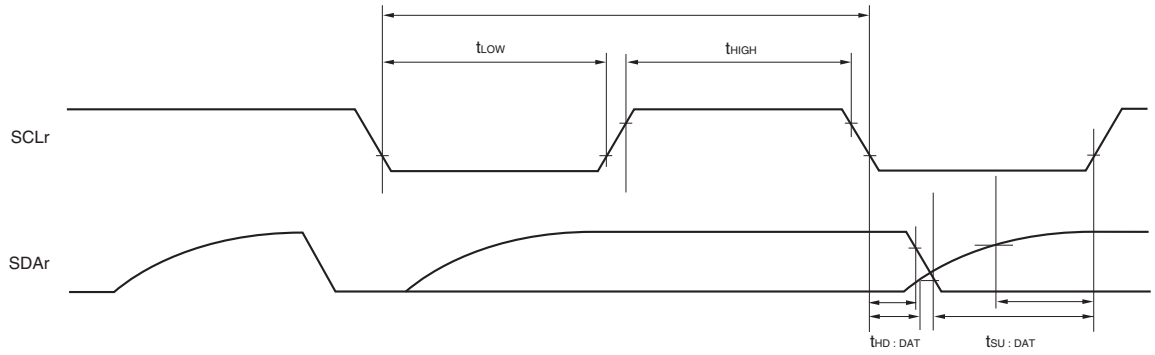
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0, 1), n: Channel number (0, 1, 3)

4. Simplified I^2C mode is supported by the R5F102 products.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (dedicated baud rate generator output)
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate Note 1		Normal operation						
		Reception					f_{MCK}/6	bps
			4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	Theoretical maximum transfer rate f_{CLK} = f_{MCK} = 24 MHz			4.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	Theoretical maximum transfer rate f_{CLK} = f_{MCK} = 24 MHz			4.0	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	Theoretical maximum transfer rate f_{CLK} = f_{MCK} = 8 MHz			1.3	Mbps
		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				**Note 1**	bps
				Theoretical maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V			2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				**Note 3**	bps
				Theoretical maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V			1.2 Note 4	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				**Note 5**	bps
				Theoretical maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V			0.43 Note 6	Mbps
		SNOOZE mode			4800		9600	bps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $2.7\ V \le V_{DD} < 4.0\ V$ and $2.3\ V \le V_b \le 2.7\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

5. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $1.8\ V \le V_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

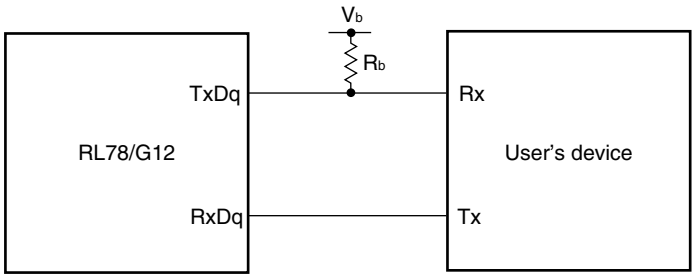
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). (In 20- or 24-pin products, redirect to P6 is not supported.)

Remarks 1. R_b [Ω]:Communication line (TxDq) pull-up resistance,
C_b [F]: Communication line (TxDq) load capacitance,
V_b [V]: Communication line voltage

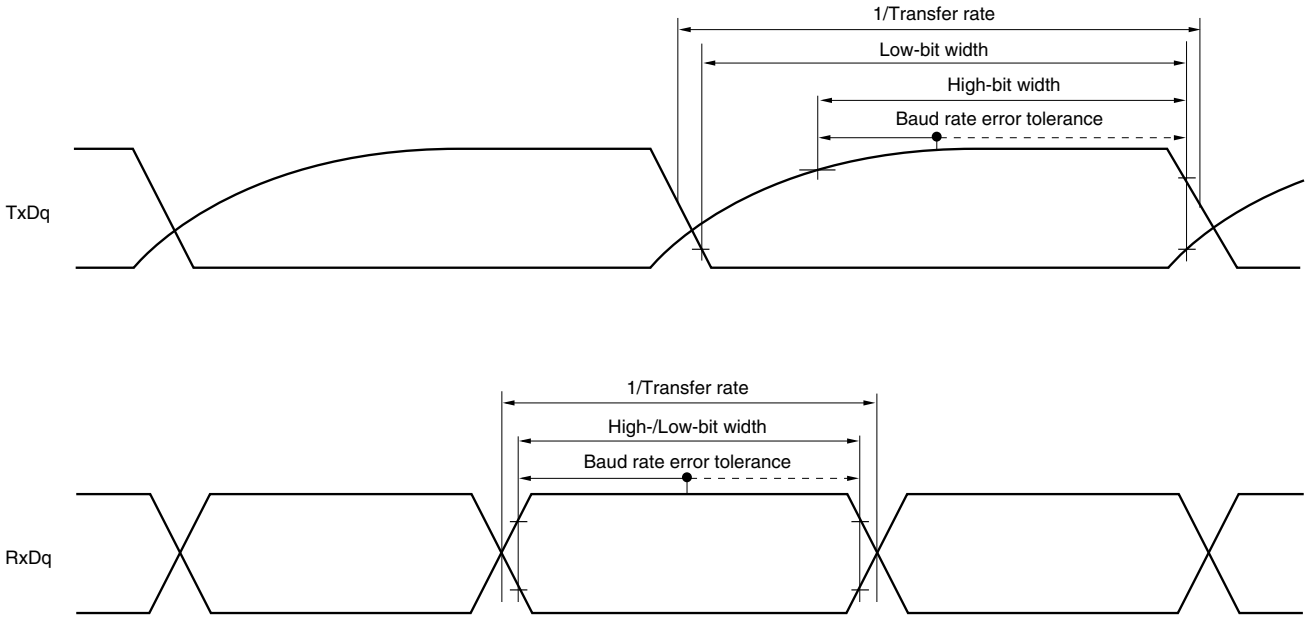
2. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b [Ω]: Communication line (TxD0) pull-up resistance, V_b [V]: Communication line voltage

2. q = UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

(7) Communication at different potential (2.5 V, 3 V) (CSI00 mode) (CSI00 master mode (f_{MCK}/2), SCK00... internal clock output)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK00 cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200 Note 1			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300 Note 1			ns
SCK00 high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 50			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 120			ns
SCK00 low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 7			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 10			ns
SI00 setup time (to SCK00↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	58			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	121			ns
SI00 hold time (from SCK00↑) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10			ns
Delay time from SCK00↓ to SO00 output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130	ns
SI00 setup time (to SCK00↓) Note 3	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	23			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	33			ns
SI00 hold time (from SCK00↓) Note 3	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10			ns
Delay time from SCK00↑ to SO00 output Note 3	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	ns

Notes 1. The value must also be 2/f_{CLK} or more.

2. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1

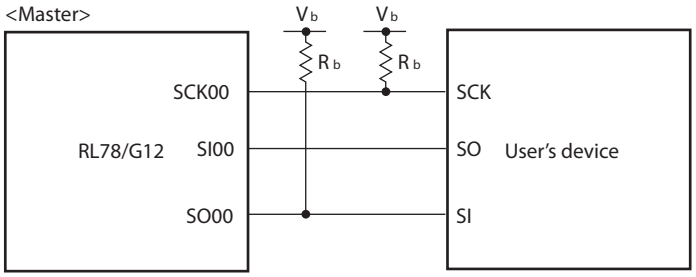
3. When DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

Caution Select the TTL input buffer for the SI00 pin and the N-ch open drain output (V_{DD} tolerance) mode for the SO00 pin and SCK00 pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1) (Redirect to P0 is not supported in 24-pin products).

Remarks 1. R_b [Ω]:Communication line (SCK00, SOp) pull-up resistance, C_b [F]: Communication line (SCK00, SO00) load capacitance, V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS00 bit of serial mode register (SMR00).

CSI mode connection diagram (during communication at different potential)



(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (f_{MCK}/4) (CSI00 mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300 Note			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500 Note			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150 Note			ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 –75			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 –170			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 –458			ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 –12			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 –18			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 –50			ns

Note The value must also be 4/f_{CLK} or more.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 0, 1 (PIM0, PIM1) and port output mode register 0, 1 (POM0, POM1) (Redirect to P0 is not supported in 24-pin products.). Communication at different potential is not allowed in CSI01, CSI11.

Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (f_{MCK}/4) (CSI mode) (master mode, SCKp... internal clock output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19			ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	110			ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19			ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			25	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

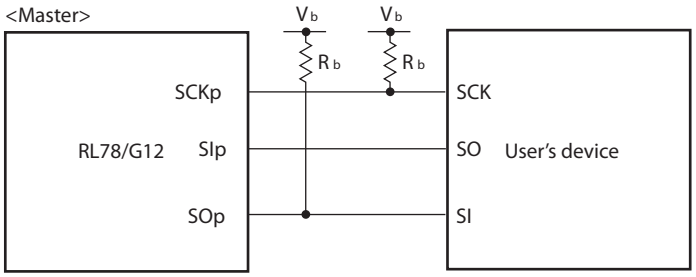
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 0, 1 (PIM0, PIM1) and port output mode register 0, 1 (POM0, POM1) (Redirect to P0 is not supported in 24-pin products.). Communication at different potential is not allowed in CSI01, CSI11.

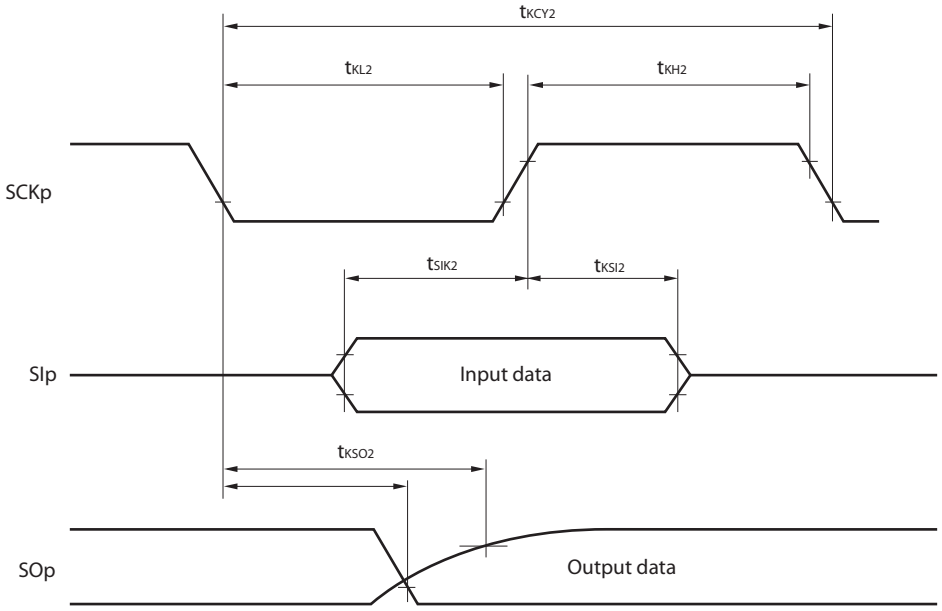
Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

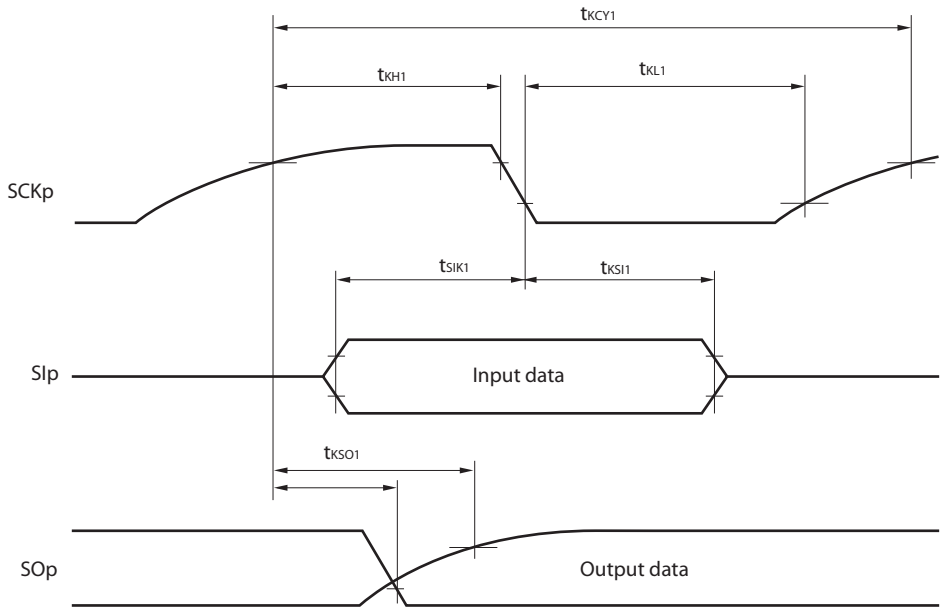
CSI mode connection diagram (during communication at different potential)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	Noromal operation					
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}			ns
		SNOOZE mode				1	Mbps
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 12			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 – 50			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} < 5.5 V		1/f_{MCK} + 20			ns
		1.8 V ≤ V_{DD} < 3.3 V		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 214	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ				2/f_{MCK} + 573	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

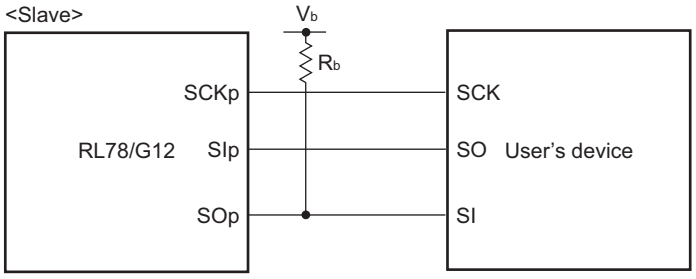
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp and SCKp pins by using port input mode register 0, 1 (PIM0, PIM1) and port output mode register 0, 1 (POM0, POM1) (Redirect to P0 is not supported in 24-pin products.). Communication at different potential is not allowed in CSI01, CSI11.

Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

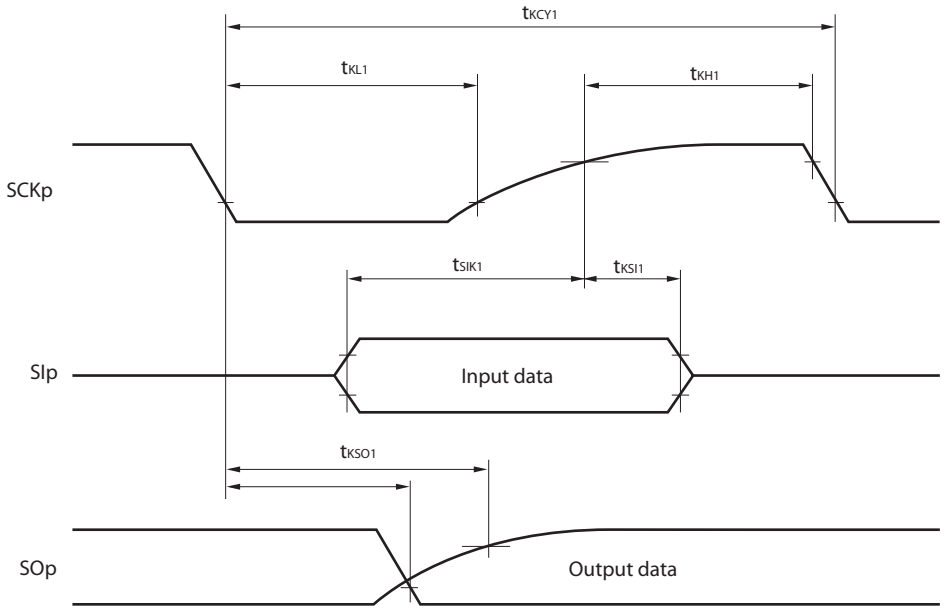
2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)

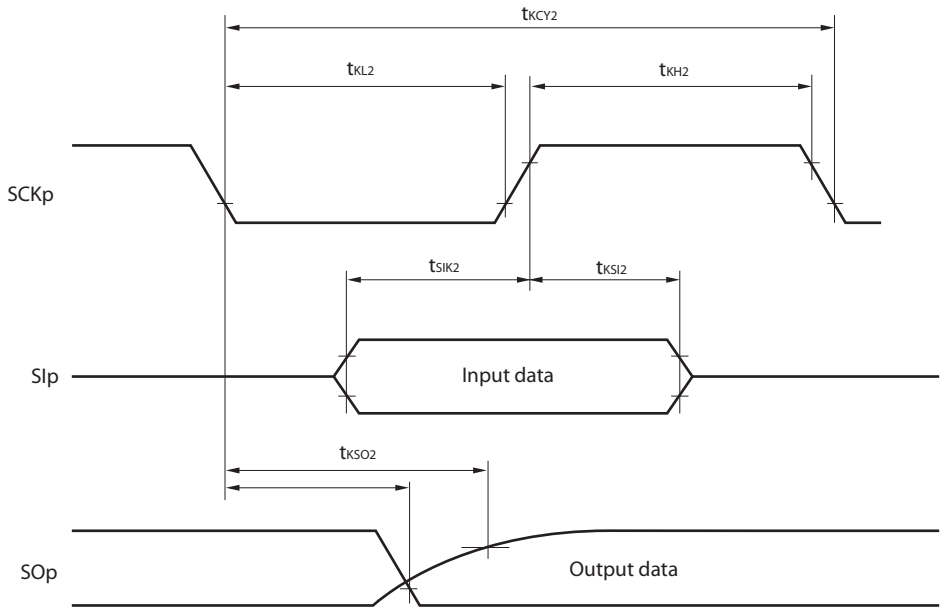
CSI mode connection diagram (during communication at different potential)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.		MAX.	Unit
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ			400	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ			400	kHz
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ			300	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1550			ns
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	610			ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	$1/f_{MCK}$ Note +190			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ Note +190			ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ Note +190			ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0		355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0		355	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0		405	ns

Note Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register 0, 1 (PIM0, PIM1) and port output mode register 0, 1 (POM0, POM1). Communication at different potential is not allowed in IIC01, IIC11.

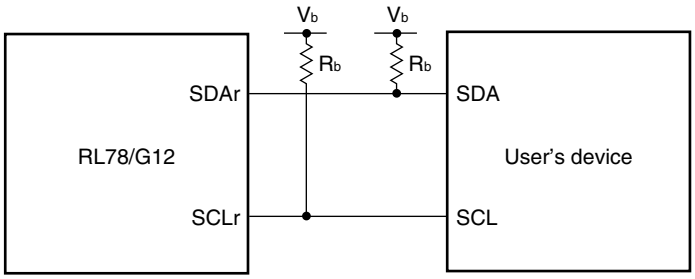
Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

2. r: IIC Number (r = 00, 20)

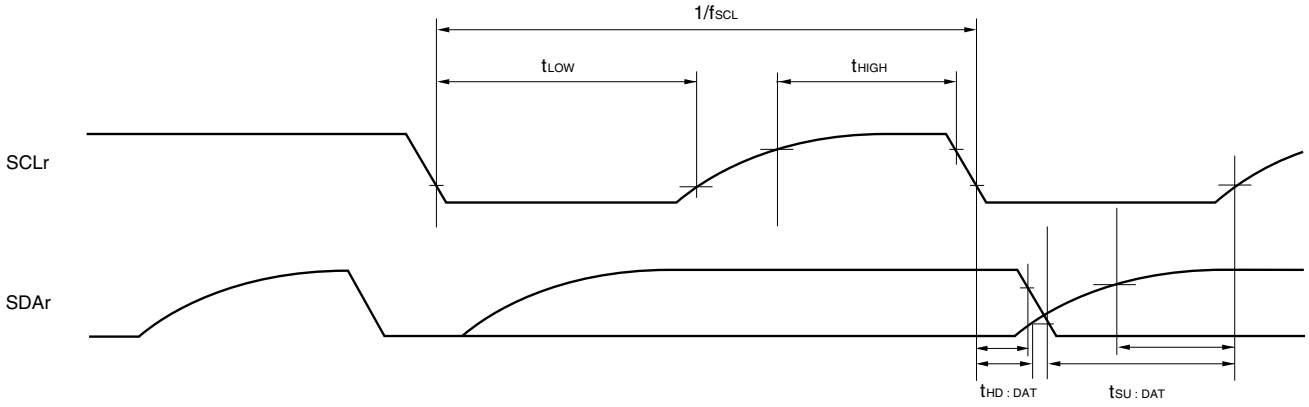
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

4. Simplified I^2C mode is supported by the R5F102 products.

Simplified I^2C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



2.5.2 Serial interface IICA

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz			0	400	kHz
		Normal mode: f_{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition[Note 1]	$t_{SU:STA}$		4.7		0.6		μs
Hold time	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

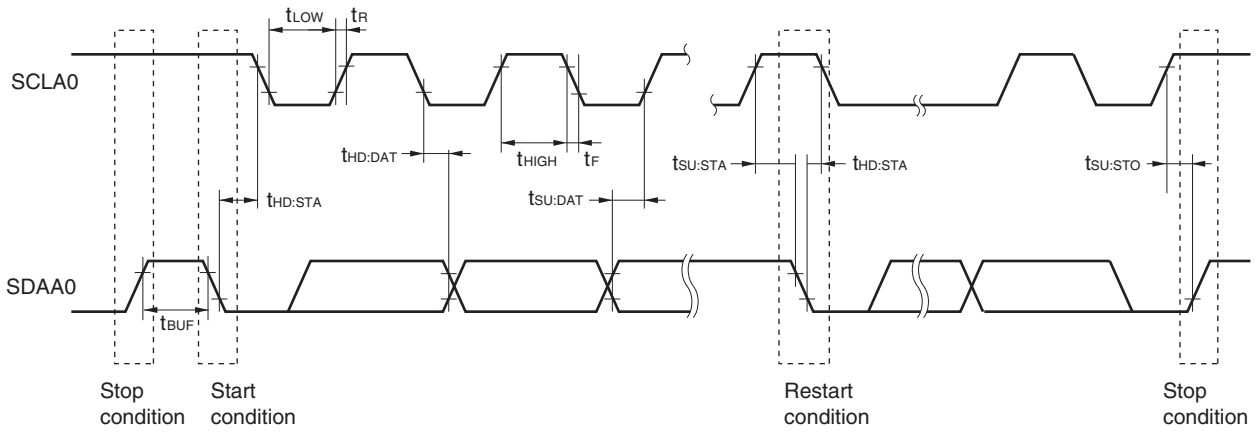
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: C_b = 400 pF, Rb = 2.7 kΩ
Fast mode: C_b = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing



2.5.3 On-chip debug (UART)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(1) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (–) = AV_{REFM}/ANI1 (ADREFM = 1), (target ANI pin : ANI2, ANI3)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}			1.2	±3.5	LSB
Conversion time	t_{CONV}		3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}					±0.25	%FSR
Full-scale error[Notes 1, 2]	E_{FS}					±0.25	%FSR
Integral linearity error[Note 1]	ILE					±2.5	LSB
Differential linearity error[Note 1]	DLE					±1.5	LSB
Reference voltage (+)	AV_{REFP}			1.8		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	Internal reference voltage is selected 2.4 V ≤ V_{DD} ≤ 5.5 V HS (high-speed main) mode		1.38	1.45	1.50	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(2) When AV_{REF} (+)= AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (–) = AV_{REFM}/ANI1 (ADREFM = 1), (target ANI pin : ANI16 to ANI22)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} =0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}			1.2	±5.0	LSB
Conversion time	t_{CONV}		3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}					±0.35	%FSR
Full-scale error[Notes 1, 2]	E_{FS}					±0.35	%FSR
Integral linearity error[Note 1]	ILE					±3.5	LSB
Differential linearity error[Note 1]	DLE					±2.0	LSB
Reference voltage (+)	AV_{REFP}			1.8		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and V_{DD}	V
	V_{BGR}	Internal reference voltage is selected 2.4 V ≤ V_{DD} ≤ 5.5 V HS (high-speed main) mode		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(3) When AV_{REF} (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), AV_{REF} (–) = V_{SS} (ADREFM = 0), (target ANI pin : ANI0 to ANI3, ANI16 to ANI22)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution			1.2	±7.0	LSB
Conversion time	t_{CONV}		3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}					±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}					±0.60	%FSR
Integral linearity error[Note 1]	ILE					±4.0	LSB
Differential linearity error[Note 1]	DLE					±2.0	LSB
Analog input voltage	V_{AIN}			0		V_{DD}	V
	V_{BGR}	Internal reference voltage is selected 2.4 V ≤ V_{DD} ≤ 5.5 V HS (high-speed main) mode		1.38	1.45	1.50	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(4) When AV_{REF} (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), AV_{REF} (–) = AV_{REFM} (ADREFM = 1), (target ANI pin : ANI0, ANI2, ANI3, ANI16 to ANI22)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (–) = AV_{REFM} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		bit
Conversion time	t_{CONV}	8-bit resolution	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	AV_{REFM} = 0 V, 2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE				±2.0	LSB
Differential linearity error[Note 1]	DLE				±1.0	LSB
Reference voltage (+)	V_{BGR}		1.38	1.45	1.5	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}				5	μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.48	1.51	1.54	V
	V_{PDR}	Power supply fall time	1.47	1.50	1.53	V
Minimum pulse width	T_{PW}		300			μs
Detection delay time					350	μs

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs

LVD detection voltage of interrupt & reset mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

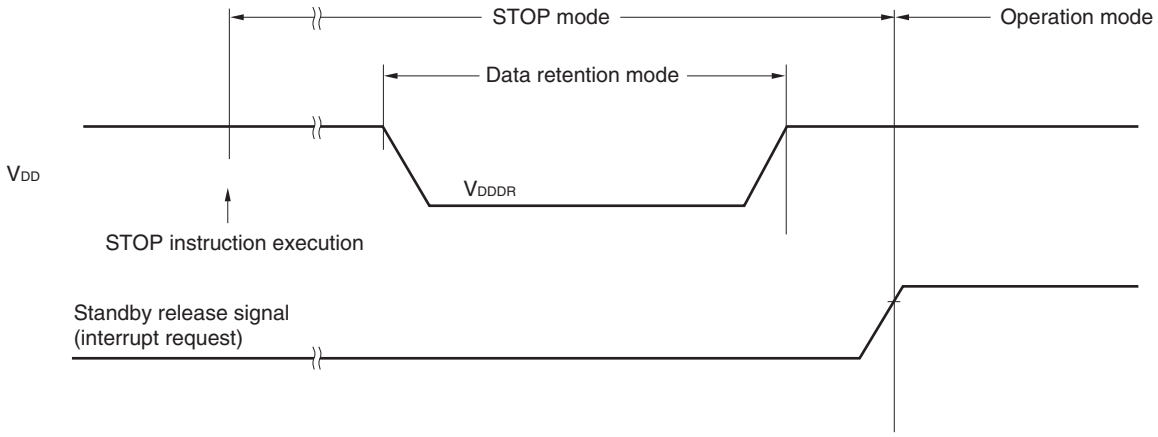
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
LVD detection voltage	V_{LVD11}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage: 1.8 V			1.80	1.84	1.87	V
	V_{LVD10}	LVIS1, LVIS0 = 1, 0 (+0.1 V)		Rising reset release voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVD9}	LVIS1, LVIS0 = 0, 1 (+0.2 V)		Rising reset release voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVD2}	LVIS1, LVIS0 = 0, 0 (+1.2 V)		Rising reset release voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVD8}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage: 2.4 V			2.40	2.45	2.50	V
	V_{LVD7}	LVIS1, LVIS0 = 1, 0 (+0.1 V)		Rising reset release voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVD6}	LVIS1, LVIS0 = 0, 1 (+0.2 V)		Rising reset release voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVD1}	LVIS1, LVIS0 = 0, 0 (+1.2 V)		Rising reset release voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVD5}	V_{POC2}, V_{POC1}, V_{POC1} = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.81	V
	V_{LVD4}	LVIS1, LVIS0 = 1, 0 (+0.1 V)		Rising reset release voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD3}	LVIS1, LVIS0 = 0, 1 (+0.2 V)		Rising reset release voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVD0}	LVIS1, LVIS0 = 0, 0 (+1.2 V)		Rising reset release voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is affected, but data is not retained when a POR reset is affected.



2.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Code flash memory rewritable times Notes 1.2.3	C_{erwr}	Retained for 20 years	T_A = 85°C Note 3	1,000			Times
Data flash memory rewritable times Notes 1.2.3		Retained for 1 year	T_A = 25°C Note 3		1,000,000		
		Retained for 5 years	T_A = 85°C Note 3	100,000			
		Retained for 20 years	T_A = 85°C Note 3	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self program library.

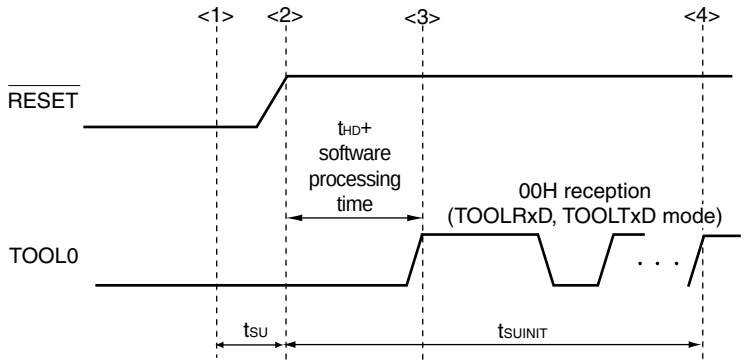
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Caution This specifications show target values, which may change after device evaluation.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.9 Timing Specs for Flash Memory Programming Switching Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset are released before external reset release			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{su}		10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}		1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the pin reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends.

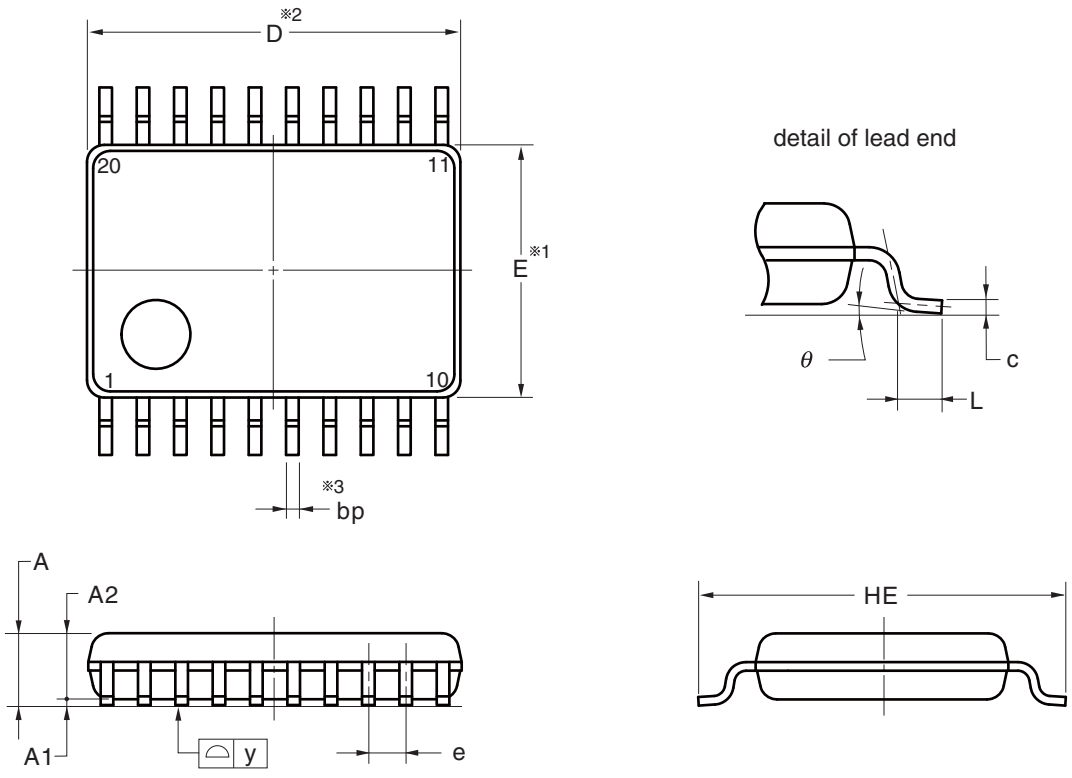
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end. (except soft processing time)

3. PACKAGE DRAWINGS

3.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22^{+0.10}_{-0.05}$
c	$0.15^{+0.05}_{-0.02}$
L	0.50±0.20
y	0.10
θ	0° to 10°

NOTE

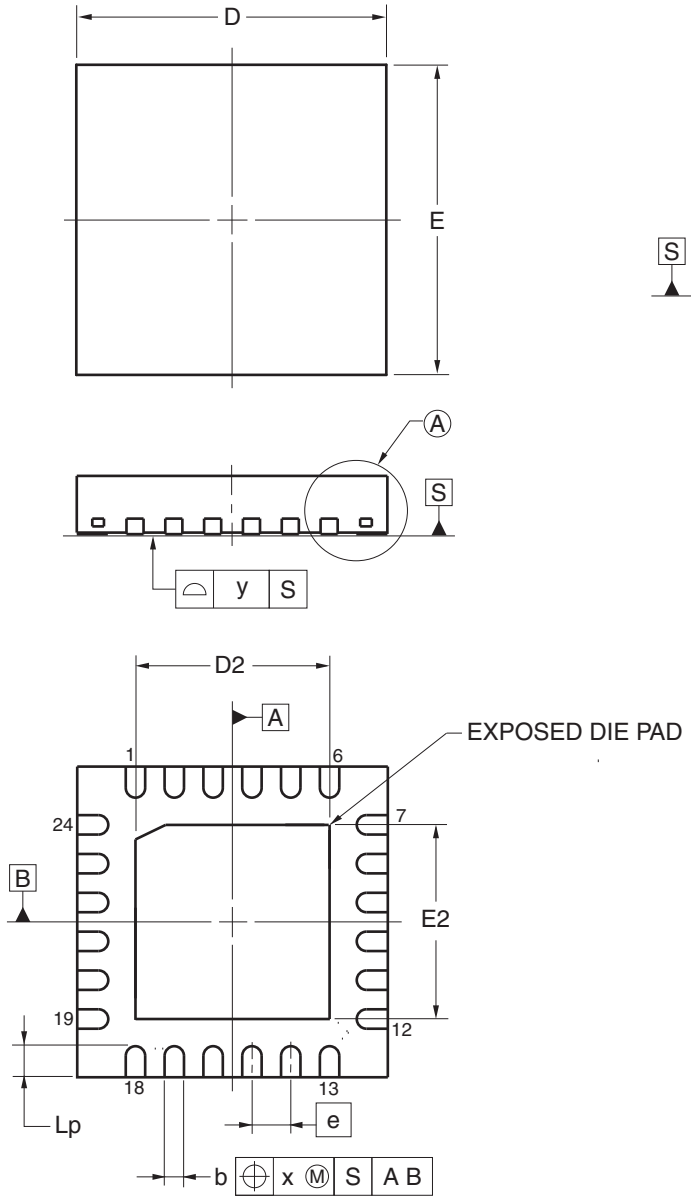
1.Dimensions "※1" and "※2" do not include mold flash.

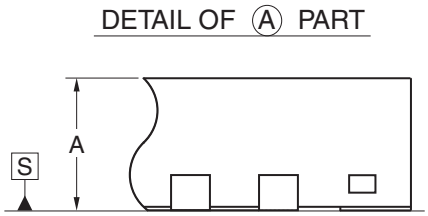
2.Dimension "※3" does not include trim offset.

3.2 24-pin products

R5F1027AANA, R5F10279ANA, R5F10278ANA, R5F10277ANA
R5F1037AANA, R5F10379ANA, R5F10378ANA, R5F10377ANA
R5F1027ADNA, R5F10279DNA, R5F10278DNA, R5F10277DNA
R5F1037ADNA, R5F10379DNA, R5F10378DNA, R5F10377DNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-1	0.04





(UNIT:mm)

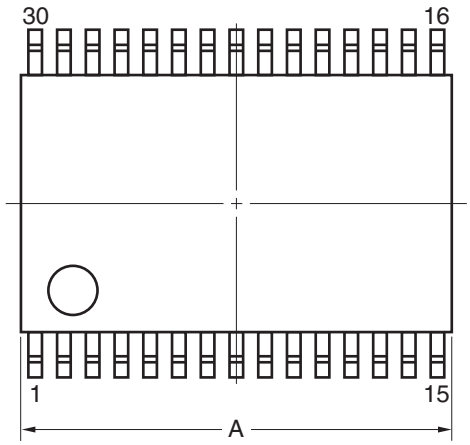
ITEM	DIMENSIONS
D	4.00±0.05
E	4.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	2.45	2.50	2.55	2.45	2.50	2.55

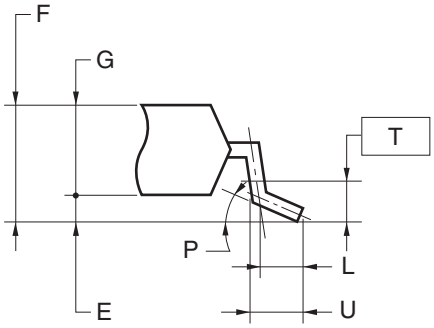
3.3 30-pin products

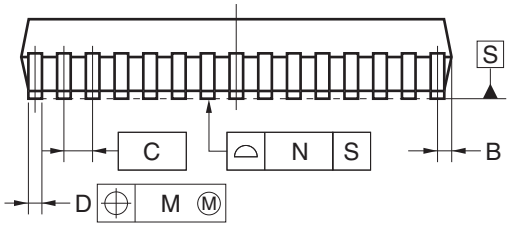
R5F102AAASP, R5F102A9ASP, R5F102A8ASP, R5F102A7ASP
R5F103AAASP, R5F103A9ASP, R5F103A8ASP, R5F103A7ASP
R5F102AADSP, R5F102A9DSP, R5F102A8DSP, R5F102A7DSP
R5F103AADSP, R5F103A9DSP, R5F103A8DSP, R5F103A7DSP

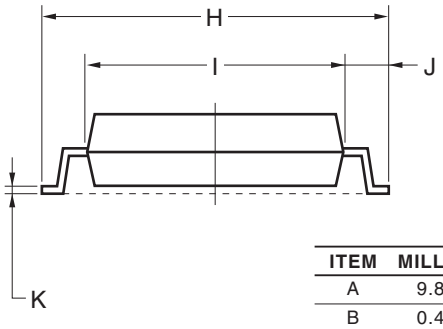
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



detail of lead end







NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

Revision History	RL78/G12 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Dec 10, 2012	-	First Edition issued

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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