

# **ST-105 Demodulator Operation**

Version 2.3

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## **1. ST-105 DESCRIPTION**

### **1.1 Introduction**

This manual describes the installation and operation of the SIGTEK ST-105 Demodulator. The ST-105 Demodulator is a versatile, single card, demodulator and bit sync board designed to demodulate a variety of PSK modulated signals that transmit in either a continuous or burst mode. The ST-105 is designed to be used with the companion ST-106 Programmable Encoder / Decoder or the ST-107 Signal Multiplexer to create a turn-key receiving system.

The ST-105 accepts a wideband input signal from one of two input connectors. The wideband signal is amplified and digitized on the A/D daughter board. The digitized signal is then tuned to the specified frequency where it is lowpass filtered and decimated to a final sample rate of four samples per baud. Additional filtering is performed for equalization or Nyquist pulse shaping. A TDMA Processor feature allows for rapid acquisition of burst signals. The bit sync function provides carrier and bit synchronization error information to a floating point DSP processor, which in turn adjusts the sample clock frequency and the digital tuner tuning frequency. Soft and hard decision bits along with reconstructed clock are available as output on four connectors.

The SIGTEK control software is an easy to use Windows application. Functions of the ST-105 are configured by selecting from a series of pull-down and pop-up menus. Operation of the ST-105 software is described in Section 4.

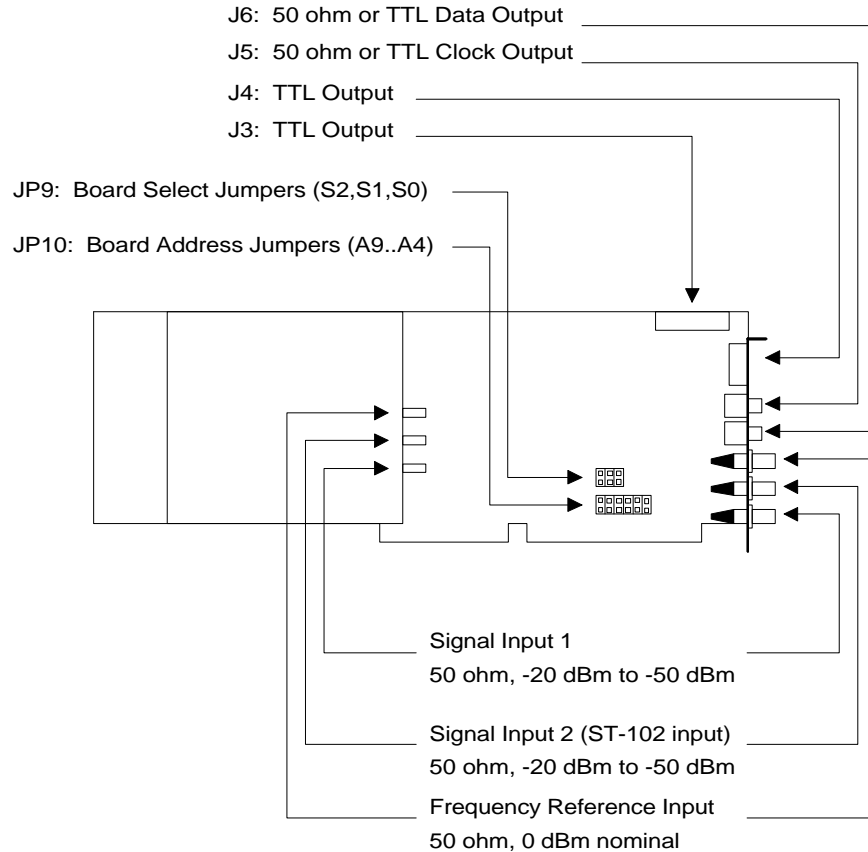
### **1.2 System Requirements**

The following minimum system requirements are necessary for installation and operation of the ST-105 software and hardware:

Computer System:	IBM PC-AT or compatible (486DX-33 MHz processor or faster recommended)
Operating System:	DOS 5.0 or later with Windows 3.1 required.
Display:	VGA or SVGA monitor required.
Disk Space:	5 Mbytes minimum free.
Memory:	8 Mbytes minimum recommended.
Floppy Drive:	3.5" 1.44 Mbyte floppy drive required for software installation.

### 1.3 Connector Locations and Pinouts

Figure 1-1 identifies the ST-105's connectors and jumpers. The primary signal input is the SMA jack located at the bottom of the endplate. The secondary signal input is the SMA jack located just above the primary input. The frequency reference input is the third SMA jack from the bottom. The other two SMA jacks are TTL level, 50  $\Omega$  outputs. Their output is software programmable. J4 is a ten pin IDC style connector located at the top of the endplate. This connector is a programmable I/O port. Currently, it is configured only as an output for soft decision data with clock. It will be configurable as an input for gating TDMA burst in a future software release. J3 is the 20-pin IDC style connector located on the top edge of the card. It is a parallel or serial output for soft decision data with clock. This connector is designed for use with the ST-106 decoder card or the ST-107 multiplexer card. See Section 4 for more information on input and output signal levels.



**Figure 1-1 ST-105 Connector and Jumper Locations**

The drivers for connectors J3 and J4 are designed to drive TTL loads over relatively short ribbon cables. J3 is configured to interface with the ST-107 RS-422 card. The format of the soft decision bits is sign magnitude. There are three soft decision bits. The most

significant bit is a sign bit or hard decision bit. The two least significant bits indicate the quality of confidence in the hard decision value. A value of '00' or zero shows weakest confidence while a value of '11' or three indicates strong confidence in the bit decision. The J3 connector may be configured to operate in a parallel or serial manner depending on the [ST105] setup in the *sigtek.ini* file. Table 1-1 gives pin assignments for connector J3. J4 is provided as an interface to other devices.

**Table 1-1 ST-105 J3 Connector Pin Assignments**

Pin Number	Type	Parallel Mode Pin Assignment	Serial Mode Pin Assignment
1	In	*	*
2	Out	I(0) Soft Decision Bit	I/Q(0) Muxed Soft Decision Bit
3	In	*	*
4	Out	I(1) Soft Decision Bit	I/Q(1) Muxed Soft Decision Bit
5	In	*	*
6	Out	I(2) Sign Bit	I/Q Muxed Sign Bit
7	In	*	*
8	Out	Q(0) Soft Decision Bit	*
9	In	*	*
10	Out	Q(1) Soft Decision Bit	*
11	In	*	*
12	Out	Symbol Clock (data valid rising edge)	Bit Clock (data valid rising edge)
13	In	*	*
14	Out	Q(2) Sign Bit	Symbol Sync (I=1; Q=0)
15	In	*	*
16	Out	Signal Activity (1=Active)	Signal Activity (1=Active)
17 to 20		GND	GND

\* Not Used

JP4 is provided as an interface to other devices. Its output is a serial stream of soft decision bits. One soft decision bit is output for each output clock cycle. A logic zero on the symbol sync output indicates the beginning of a new symbol. For BPSK, the bits are ordered I(k), I(k+1), I(k+2), etc. For QPSK, the bits are ordered I(k), Q(k), I(k+1), Q(k+1), etc. JP4 will be configurable as an input for gating TDMA burst in a future software release. Table 1-2 gives pin assignments for connector.

**Table 1-2 ST-105 JP4 Connector Pin Assignments**

Pin Number	Description
1	I/Q (0) Muxed Soft Decision Bit
4	No connection
5	I/Q (1) Muxed Soft Decision Bit
8	I/Q (2) Muxed Sign Bit
9	Bit Clock (data valid on rising edge)
10	Symbol Sync ( I = 1; Q = 0 )
2, 3, 6, and 7	GND

## 2. OPERATION

### 2.1 System Pull-Down Menu

The ST-105 Board control software is a subset of the ST-203 system control software. The top level control window is shown in Figure 2-1. The System pull down menu is located in the menu pull down bar along the top of the main control window. The items included in this pull down menu are *Configuration*, *Hardware*, *About...*, and *EXIT*.

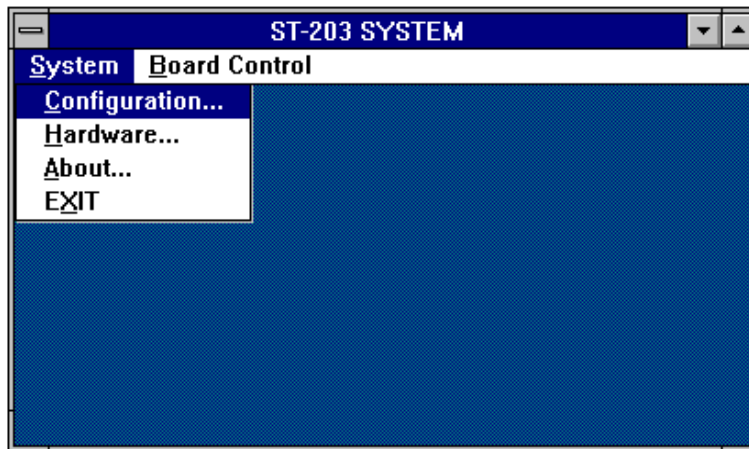


Figure 2-1 System Pull-Down Menu

The *Configuration* control window is shown in Figure 2-2. It is used to create and recall the \*.sys system configuration files that may accessed to save and recall settings for the entire system. Network control and system reference frequency controls are also provided in this window. . Refer to the *sigtek.ini* file description for more information on these system settings.

The system's frequency reference is selected through a drop down menu. The options for frequency reference are *Internal* (10 MHz), *External 5 MHz*, or *External 10 MHz*. **Please note that the ST-105 does not have its own internal reference signal. In order for the *Internal* setting to be valid for the ST-105, a ST-701 Reference Distribution Card must also be installed and connected to the ST-105.**



Remote control of the ST-105 over a local area network is enabled or disabled by clicking on the toggle button in the *Network Control* area. The status of the connection is also displayed

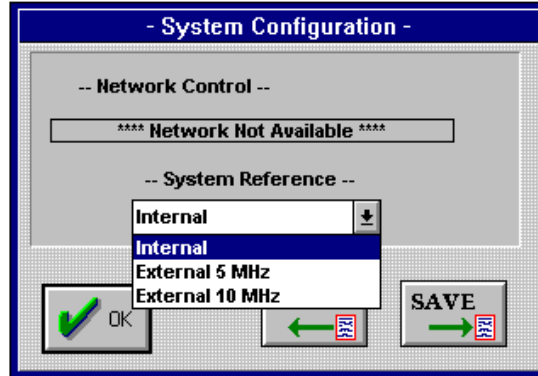


Figure 2-2 System Configuration Window

The *System Hardware* window shown in Figure 2-3 indicates the installed address and status of all installed SIGTEK boards.

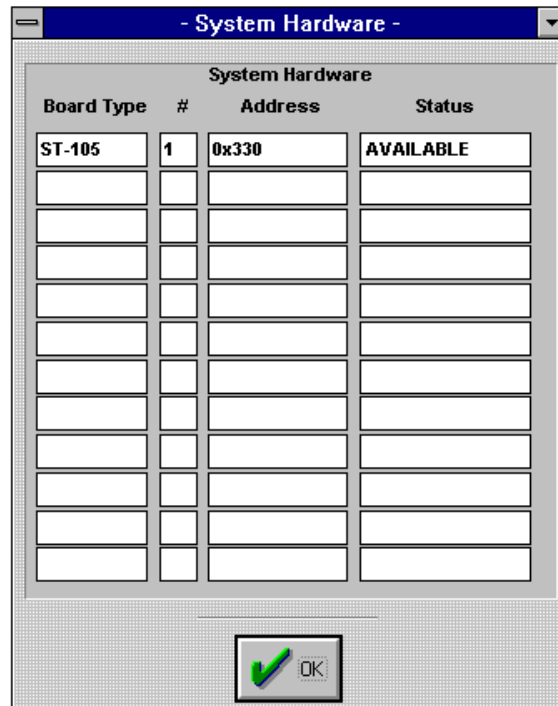


Figure 2-3 System Hardware Window

The *About...* window provides version information about Sigtek hardware control application.

## 2.2 Board Control Pull-Down Menu

Control of individual ST-105 cards is accessed through the *Board Control* pull-down menu shown in Figure 2-4. Specific details for controlling the ST-105 is presented in the following sections.

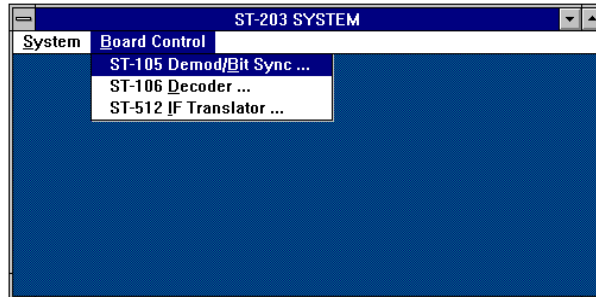


Figure 2-4 Board Control Pull-Down Menu

### 2.2.1 ST-105 DEMOD / BIT SYNC CONTROL

The ST-105 main control window shown in Figure 2-5 is organized as follows. The largest area of the main control window is the *Board Setup* area. It is used to modify *Modulation*, *IF Freq*, *Baud Rate*, *ST-105 Board #*, *Input Source*, *J5/J6 Output Settings*, and *Miscellaneous Setup Info*. Any change to these settings is not affected until the user clicks on the *SEND* button in the bottom left corner of the main control window. The area to the right is the *Board Status* area. This area provides feedback to the user regarding the current status of a specified ST-105 board. The *Board Control* area in the lower right of the main window is used to change system gain, baud or carrier frequencies, or symbol mapping assignments on the fly without issuing a *SEND* command. The File Options area is used to save and to recall setup files for individual boards.

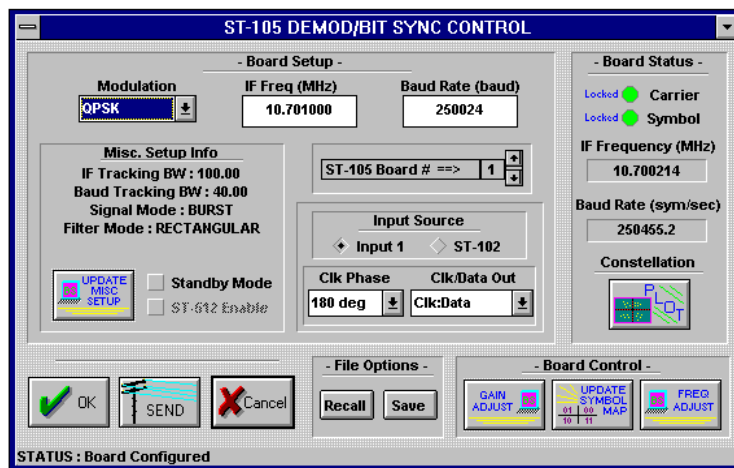


Figure 2-5 ST-105 Main Control Window

### 2.2.1.1 ST-105 Board Number (Selecting a Specific ST-105)

Multiple ST-105 boards are controlled from a single interface. The user may toggle control between boards by clicking on the scroll box below the *Baud Rate* entry box. The board select scroll box shows which ST-105 is currently attached to the control software.

### 2.2.1.2 Specifying Signal Modulation

Once a specific ST-105 is selected, the user may specify other demodulator and bit sync parameters. The first of these is modulation. This parameter is selected by using the Modulation drop down list box. The modulation types that are supported by the ST-105 are:

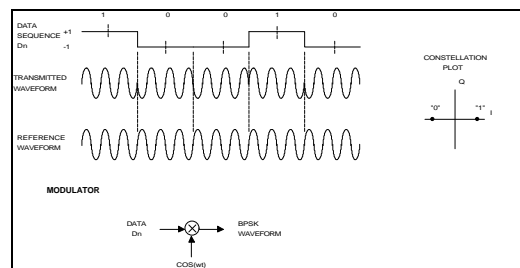
- BPSK (standard and Alternative demodulation)
- DBPSK Waveform Level and Bit Level
- QPSK (standard and Alternative demodulation)
- DQPSK Waveform Level and Bit Level
- OQPSK
- $\pi/4$  DQPSK

The *Waveform* and *Bit* options for the DBPSK and DQPSK modulations specify at which stage of processing the differential operation is performed. When the *Waveform* variation is selected, a phase difference is performed on the signal prior to the symbol decision. This mode is useful when the signal has poor stability carrier stability characteristics. When the *Bit* variation is selected, the differential operation is performed on the hard decision data. For  $\pi/4$  DQPSK, the differential operation is always performed at the waveform level.

A change in modulation is not affected until the user clicks on the *SEND* button in the lower left corner of the main control window. Note that switching from one modulation type to another may cause a *WAIT* message to appear. This is because static RAM look-up tables on the ST-105 board may have to be reloaded.

#### 2.2.1.2.1 BPSK Demodulation (Standard and Alternative Methods)

In standard coherent BPSK (bi-phase shift keying) modulation, the data stream to be transmitted directly modulates a continuous carrier as shown in Figure 2-6. This results in 180° phase shifts in the transmitted sine wave. The demodulator generates a local carrier reference which is phase locked to the transmitted waveform and is used to recover the data.



**Figure 2-6 BPSK Modulation Example**

The Alternative BPSK demodulation also attempts to phase lock to the carrier, but it also implements the same differential phase operation at the waveform level as DBPSK Wave and DQPSK Wave demodulation. The non-differential data is then recovered by integrating the bit decisions following the bit sync process. This mode is useful when the signal has poor stability carrier stability characteristics, or it has been translated from RF to IF using non-digital quality block downconverters.

#### 2.2.1.2.2 DBPSK (Differential BPSK) Demodulation

DBPSK (Differential BPSK) Modulation is similar to coherent BPSK except that the difference between current data bit and previously transmitted bit is used to modulate the carrier as shown in Figure 2-7. The main advantage of DBPSK is that since the phase difference between the current symbol and previous symbol of the received waveform can be used to make a bit decision, no local carrier reference is needed to recover the data. This form of modulation can be useful for systems with inherently high doppler shifts in carrier frequency (such as land mobile systems or low earth orbit satellites) since no carrier tracking circuitry is required to recover the data.

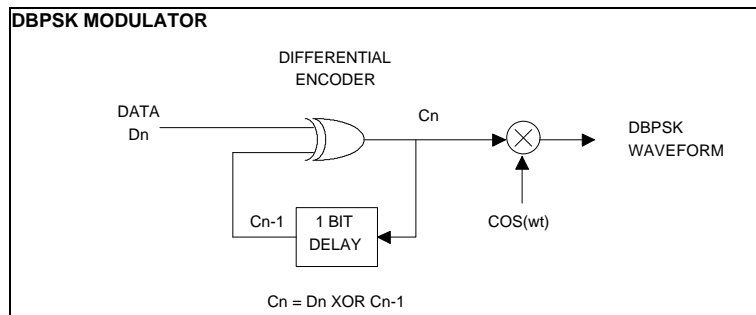
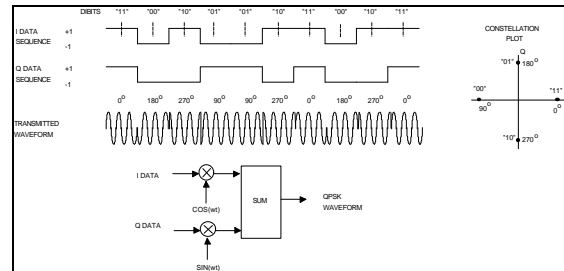


Figure 2-7 DBPSK Modulation Example

The ST-105 implements two flavors of DBPSK demodulation. DBPSK Wave uses the difference between the current symbol and previous symbol of the received waveform to make a bit decision as described above. This method does not require carrier tracking circuitry and is thus useful for signals with carrier instabilities such as high doppler rates or excessive phase noise. DBPSK Bit performs a coherent BPSK demodulation of the signal then uses the current and previous demodulated data to make a bit decision. This method is equivalent to BPSK demodulating the signal then applying a digital differential demodulator circuit on the demodulated output. DBPSK Bit demodulation does not perform as well as DBPSK Wave on signals with carrier instabilities since it requires a carrier tracking circuit. DBPSK Bit can however perform better on low SNR than the DBPSK Wave technique.

### 2.2.1.2.3 QPSK Demodulation (standard and Alternative methods)

In standard coherent QPSK (quadri-phase shift keying) modulation, two data streams to be transmitted directly modulate a two continuous carriers with a  $90^\circ$  phase shift as shown in Figure 2-8.



**Figure 2-8 QPSK Modulation Example**

The resulting waveform has  $90^\circ$  phase shifts in the transmitted carrier. The main advantage of QPSK is that twice the data can be transmitted in the same bandwidth when compared to BPSK modulation. For this reason, QPSK is said to have twice the spectral efficiency of BPSK modulation.

The Alternative QPSK demodulation also attempts to phase lock to the carrier, but it also implements the same differential phase operation at the waveform level as DBPSK Wave and DQPSK Wave demodulation. The non-differential data is then recovered by integrating the symbol decisions following the bit sync process. This mode is useful when the signal has poor stability carrier stability characteristics, or it has been translated from RF to IF using non-digital quality block downconverters.

### 2.2.1.2.4 DQPSK (Differential QPSK) Demodulation

DQPSK (Differential QPSK) Modulation is similar to coherent QPSK except that the difference between current data symbol and previously transmitted symbol is used to modulate the carrier. DQPSK has similar advantages to DBPSK in that since the phase difference between the current symbol and previous symbol of the received waveform can be used to make bit decisions, no local carrier reference is needed to recover the data.

Similar to DBPSK, the ST-105 implements DQPSK Wave and DQPSK Bit techniques for recovering the differentially encoded data from the received waveform. The tradeoffs between the two methods are the same as those discussed for DBPSK demodulation in the previous section.

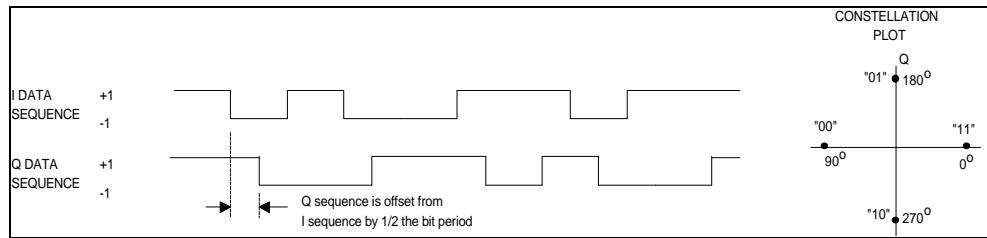
### 2.2.1.2.5 $\pi/4$ DQPSK Demodulation

$\pi/4$  (pronounced “pi over four”) DQPSK Modulation is similar to DQPSK except that carrier phase transitions are limited to  $\pm\pi/4$  ( $\pm 45^\circ$ ) and  $\pm 3\pi/4$  ( $\pm 135^\circ$ ). This eliminates  $\pm\pi/2$  ( $\pm 180^\circ$ ) phase transitions of QPSK. Elimination of these sharp  $180^\circ$  phase transitions is desirable over satellite channels since they can cause nulls in the transmitted waveform which generate unwanted spectral sidelobes when the signal is passed through a hard limiting TWT amplifier typically found on communications satellites. Note that on a conventional demodulator, the  $\pi/4$  DQPSK constellation will appear like 8-PSK; however,

the ST-105 constellation display for  $\pi/4$  DQPSK will appear like a standard 4 point QPSK constellation.

#### 2.2.1.2.6 OQPSK (Offset-QPSK) Demodulation

OQPSK eliminates the  $180^\circ$  transitions in transmitted waveform by shifting one of the modulating data sequences by  $1/2$  a bit period relative to the other as shown in This eliminates sharp nulls in the QPSK signal envelope and reduces the unwanted sidelobe regeneration in hard limiting systems. OQPSK has the same spectral efficiency as QPSK.



**Figure 2-9 OQPSK Modulation Example**

#### 2.2.1.3 Setting Signal Center Frequency and Baud Rate

The center frequency of the signal of interest is selected by using the *IF Freq* text entry box. The frequency value units are megahertz. Valid frequencies range from 200 kHz to 25 MHz. The baud rate text entry box is located to the right of the center frequency input box. The valid range of values for baud rate are 2400 baud to 2.1 Mbaud. Note that software version V2.3 supports demodulation at baud rates up to 3.8 Mbaud; however, not all ST-105s will support this higher baud rate and only operation to the 2.1 Mbaud rate is guaranteed. A change in frequency is not affected until the user clicks on the *SEND* button in the lower left corner of the main control window.

### !!! NOTICE !!!

The user should be careful when processing signals at or near 21.4 MHz. The A/D daughter board samples the wideband signal at rates between 43 MSPS and 60 MSPS. This places the Nyquist frequency of the input signals at between 21.5 MHz and 30 MHz. Since the ST-105's front end lowpass filter does not have a sharp roll-off, signals present in the environment at frequencies higher than 21.4 MHz could be aliased on top of the signal of interest during the sampling process resulting in signal distortion. The user may do one of two things to avoid this problem. First, additional filtering prior to input may be applied to eliminate unwanted signals. Second, the user may use an IF-to-IF converter to translate the signal of interest to a lower frequency, thus eliminating the potential for aliasing.

#### 2.2.1.4 Setting Signal Center Frequency and Baud Rate

The center frequency of the signal of interest is selected by using the *IF Freq* text entry box. The frequency value units are megahertz. Valid frequencies range from 200 kHz to 22 MHz. The baud rate text entry box is located to the right of the center frequency input box. The valid range of values for baud rate are 2400 baud to 2.1 Mbaud. A change in frequency is not affected until the user clicks on the *SEND* button in the lower left corner of the main control window.

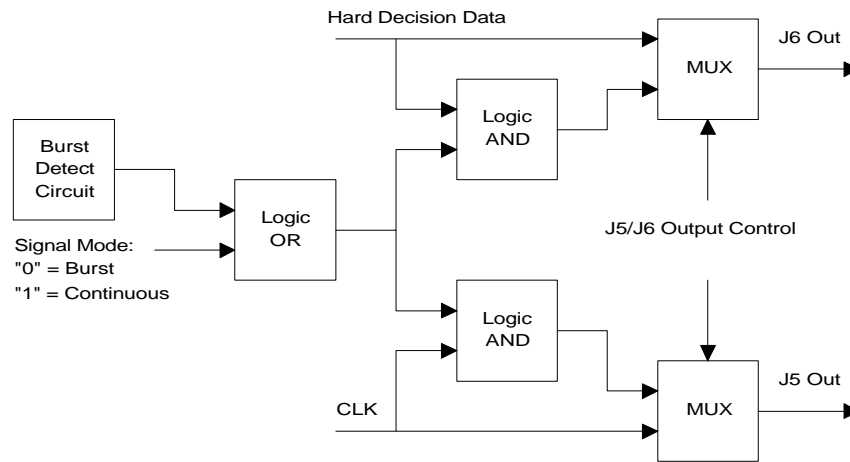
The user should be careful about processing signals at or near 21.4 MHz. The A/D daughter board samples the wideband signal. The Nyquist frequency may be near 21.4 MHz. Also, the ST-105's front end lowpass filter does not have a sharp roll-off. Therefore, if there are other signals present in the environment at frequencies higher than 21.4 MHz, they could be aliased on top of the signal of interest during the sampling process. The user may do one of two things to avoid this problem. Additional filtering prior to input may be applied to eliminate unwanted signals, or the user may use an IF-to-IF converter to translate the signal of interest to a lower frequency.

#### 2.2.1.5 J5/J6 Output Settings

The ST-105 provides two programmable output signal connections. These connections are J5 and J6. They are routed from their SMA connectors located on the ST-105's endplate (See Figure 1-1) to the ST-105 chassis back panel BNCs. These outputs will drive either TTL loads with TTL level signals, or 50 W loads with logic '0' at 0 V and logic '1'  $\geq 2.0$  V. Table 2-1 lists the output combinations that may be selected. The "B\*" entries indicate that the data and/or clock will be gated by the burst detection circuit and held low when no signal is active. When operating the ST-105 in its continuous mode, the output of the burst detection circuit will always be held high to indicate that a signal is active. Figure 2-10 shows the relationship between these signals.

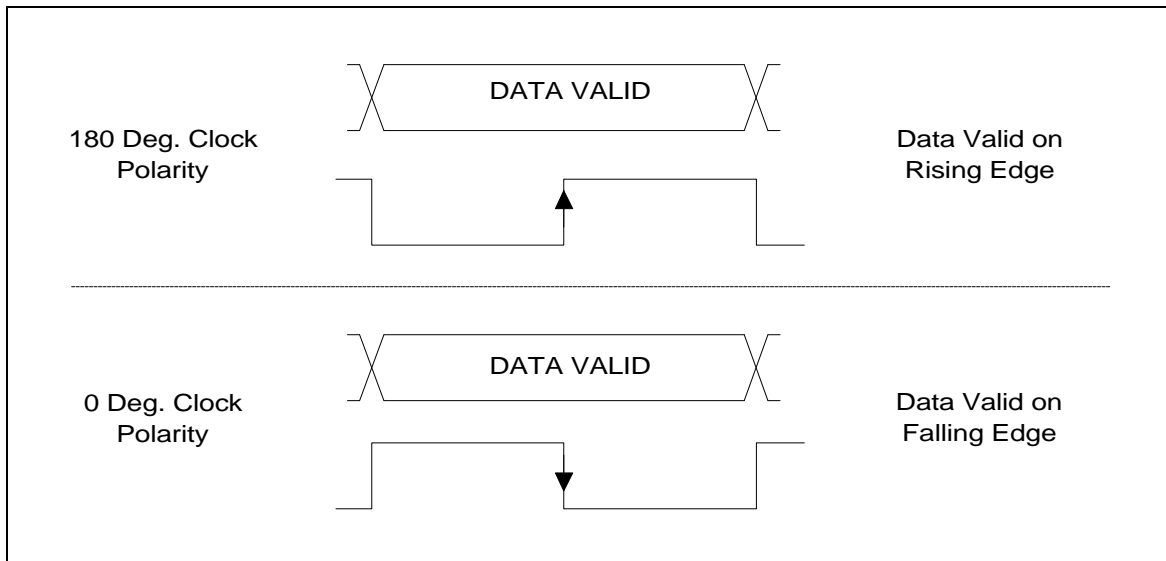
**Table 2-1 J5/J6 Output Combinations**

J5	J6
CLK	DATA
CLK	DATA * BURST_GATE
CLK * BURST_GATE	DATA
CLK * BURST_GATE	DATA * BURST_GATE



**Figure 2-10 Burst Detection and Signal Mode Relationship**

The output clock will be equal to the baud rate when BPSK signals are processed. The clock rate will be twice the baud rate when QPSK signals are processed, and the output data will be in I-Q order. The phase of the clock on J5 relative to the data may be set to either 0 degrees or 180 degrees. When 0 degrees is selected, the rising edge of the clock will occur during data transitions. When 180 degrees is selected, the rising edge of the clock will occur in the center of the data bit. Figure 2-11 illustrates the relationship between the clock and data. Changes to the output setting will not be implemented until the user clicks on the *SEND* button in the bottom left corner of the main control window.



**Figure 2-11 Clock Phase Settings**



### Miscellaneous Bit Sync Parameters

Other control parameters that are less frequently accessed are located in a *Miscellaneous Bit Sync Parameters* window. This window is invoked by clicking on the *UPDATE MISC SETUP* button in the *Misc. Setup Info* area of main control window. The current state of all the parameters contained in this lower level window is listed in the top level window. Figure 2-12 and Figure 2-13 show two variations of the *Misc. Bit Sync Parameters* control window. The parameters that are controlled are *IF Tracking Bandwidth*, *Baud Tracking Bandwidth*, *Filter Mode*, and *Signal Mode* (Burst or Continuous). The details of these parameters are described in the remainder of Section 0.

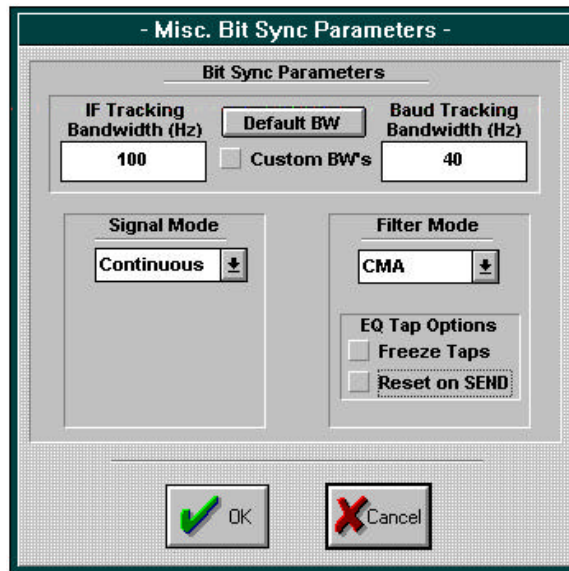


Figure 2-12 Miscellaneous Parameter Settings Window

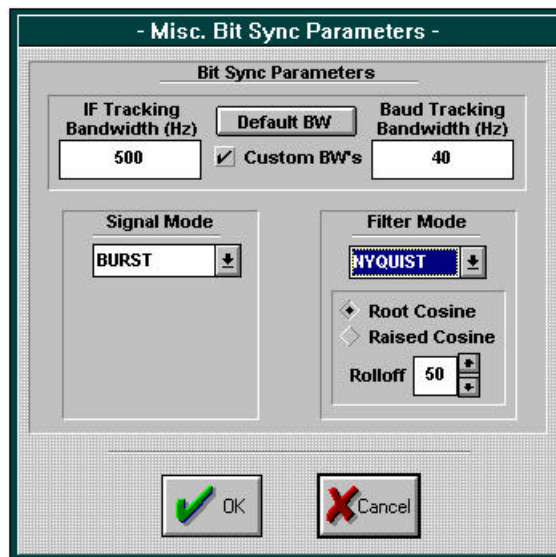


Figure 2-13 Miscellaneous Parameter Settings Window (Variation)

#### 2.2.1.5.1 Carrier and Baud Tracking Bandwidths

The ST-105 uses a baud synchronous sampling approach to implement the demodulation and bit synchronization functions. Regardless of baud rate, the signal is decimated to four samples per baud. The tracking control loops operate at the decimated sampling rates; therefore, the tracking control loops bandwidth are limited by the signal's baud rate. Because of this, the ST-105 control software will automatically compute tracking bandwidths that will work well for the given baud rate. The user has the ability to vary these values and to restore the defaults by clicking on the *Default BW* button. If the user wishes to use bandwidths other than the defaults, the *Custom BW's* box must be checked.

#### 2.2.1.5.2 Filter Mode

The ST-105 implements a configurable filter between the decimation filters and the TDMA Processor. This filter may be implemented a rectangular pulse shaped filter (RECTANGLE), as a fixed tap Nyquist pulse shaping filter for processing bandlimited signals (NYQUIST), or as an adaptive equalizer (CMA). The Nyquist pulse shaping filter can be used to match the transmitted signal pulse shaping. The Nyquist mode offers selection of two families of pulse shaping filters. They are raised cosine and root cosine. The percent rolloff of the filter can be varied from zero percent to one-hundred percent in ten percent increments. The default Nyquist filter is a root cosine filter with a fifty percent rolloff. The CMA equalizer may be used as an alternative to reduce the effects of channel distortions and improve signal quality.

A change in the filter mode is not affected until the user clicks the *OK* button in the *Misc. Bit Sync Parameter* window and then clicks the *SEND* button in the lower left corner of the main control window. Note that changing filter modes may result in a *WAIT* message box because the ST-105 has to reload static RAM look-up tables for different filters.

#### 2.2.1.5.3 RECTANGULAR Filter Mode

The RECTANGULAR Filter Mode configures the ST-105 digital filters to match a rectangular pulse-shaped waveform. An example of a rectangular waveform was given in Section 4 where the TTL output of the ST-106 decoder was used in a selftest mode to modulate a carrier. The resulting signal spectrum was the familiar  $\sin x/x$  spectrum shown in Figure 4-9.

#### 2.2.1.5.4 Nyquist Filter Mode

Most satellite transmission systems employ some type of filtering prior to transmission in order to use the limited transponder bandwidth more effectively. The most common form of filtering found in satellite channels is called Nyquist pulse-shaped filtering. Nyquist pulse-shaped filtering has the unique characteristic no intersymbol interference is introduced by the filtering if the demodulated signal is sampled correctly. The spectrum of Nyquist pulse-shaped signals has an easily recognized "flat-top" look.

The Nyquist pulse shaping filter should be used when the transmitted signal uses pulse shaping, or whenever there are other signals in the environment that are very close in frequency to the signal of interest. As shown in Figure 2-13, the Nyquist mode offers

selection of two families of pulse shaping filters. They are raised cosine and root cosine with root cosine being the most commonly used filter.

The percent rolloff of the Nyquist sets the amount of pulse-shaping but doesn't effect the filter bandwidth which is typically 1 to 1.2 times the transmitted symbol rate. The percent rolloff of the filter can be varied from zero percent to one-hundred percent in ten percent increments with typical setting being between forty and sixty percent. The default Nyquist filter is a root cosine filter with a fifty percent rolloff.

#### **2.2.1.5.5 CMA Filter Mode**

In addition to the RECTANGULAR and NYQUIST filter modes, the ST-105 digital filter can be configured as an adaptive equalizer implementing a constant-modulus algorithm (*CMA*). The constant-modulus algorithm attempts to adjust the coefficients of a 15 tap digital filter in order to maintain a constant signal amplitude (called the modulus). This technique works for all the modulation types listed for the ST-105 which are a class of signals called "constant-envelope" signals. The CMA equalizer is useful for removing distortion or interference from sources such as multipath propagation.

As shown in Figure 2-12, the CMA equalizer has two settings which control the updating of the equalizer tap coefficients. The *Freeze Taps* setting freezes the filter coefficient values once the equalizer has adapted to the signal. The *Reset on SEND* setting resets the equalizer taps to their initial values when the SEND button is pressed on the main Bit Sync menu. The equalizer is then allowed to continuously adapt to the signal. *Reset on SEND* setting takes effect only on the first time the SEND button is pressed and must be selected again if the equalizer is to be reset.

#### **2.2.1.5.6 Signal Transmission Modes (Burst or Continuous)**

The ST-105 supports both burst and continuous signal transmission modes. A change in the signal mode is not affected until the user clicks the *OK* button in the *Misc. Bit Sync Parameter* window and then clicks the *SEND* button in the lower left corner of the main control window.

#### **2.2.1.6 Stand-by Mode**

The ST-105 control software provides a stand-by mode that will disable the selected ST-105 and put it into a low power mode. This reduces power consumption and heat dissipation when the board is not in use. The user must click on the *SEND* button to affect the change in status.

### **2.2.1.7 ST-512 IF Translator Check Box**

The ST-512 IF Translator Enable check box allows for mapping the entered and displayed carrier frequency when using the ST-512 is used to translate the signal IF down to a 10 MHz center. The following two examples illustrate the use of this control.

#### **Example 1: System Input IF at 140 MHz; ST-512 Box NOT Checked**

The signal environment is centered around a 140 MHz IF and the signal of interest is centered at 145 MHz, the ST-512 would be used to translate the IF to a 10 MHz center frequency for input to the ST-105 demodulators. One of the ST-105s would then be tuned to 15 MHz to demodulate the signal. The displayed center frequency of the carrier tracker would be centered around 15 MHz.

#### **Example 2: System Input IF at 160 MHz; ST-512 Box IS Checked**

The signal environment is centered around a 160 MHz IF and the signal of interest is centered at 155 MHz, the ST-512 would be used to translate the IF to a 10 MHz center frequency for input to the ST-105 demodulators. One of the ST-105s would then be tuned to 155 MHz to demodulate the signal. The displayed center frequency of the carrier tracker would be centered around 155 MHz.

## 2.2.2 ST-105 Status

The *ST-105 STATUS* area of the main control window can be seen in Figure 2-5. The items included in this status area are *Carrier Lock* and *Symbol Lock*, the current values of center frequency and baud rate from the tracking loops, and a constellation display control button. The details of the individual items is described in the remainder of Section 2.2.1.7.

### 2.2.2.1 Carrier and Baud Tracking Status

The ST-105 control software provides indicators to show when carrier and or baud lock has been achieved. When lock is achieved, the indicator will have a solid fill pattern. Note that it is possible to have carrier lock without symbol lock and vice versa. Also note that the accuracy of these indicators will begin to degrade as the signal's SNR drops to low values (approximately 10 dB or lower). The carrier or baud lock indicators will be grayed out if their function has been disabled from the *Frequency Adjust* window. The ST-105 displays the current values of the signal's center frequency and baud rate as reported by the tracking loops. The variance of these values will vary with the selected tracking bandwidths, and the accuracy will depend on whether or not a precision, external frequency reference is being used.

### 2.2.2.2 Constellation Display

The constellation display can be used to determine how well the ST-105 is performing. Figure 2-14 shows the *Plot Control Options* window along with three examples of constellation displays. This display is accessed by clicking on the *PLOT* button in the *ST-105 STATUS* area of the main control window. The *Persistence* scroll control determines the number of constellation points that are held in the display buffer. The *Start Plot* button opens a new plot window for the selected ST-105 card. The *Refresh Plot* button will flush out the display buffer, erase the constellation display, and start drawing new points. The *Close Plot* button will close the constellation display window of the selected ST-105 card. The *EXIT* button closes the *Plot Control Options* window but leaves all current constellation displays open.

The first constellation display is an example of a signal that is correctly locked up. The next shows the constellation when the ST-105 is carrier locked but has not achieved baud synchronization. The last display shows the constellation when neither carrier lock nor baud lock has been achieved.

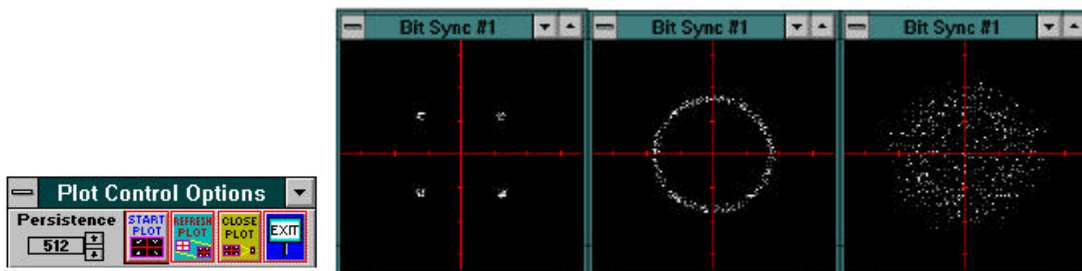


Figure 2-14: Constellation Display with Signal in Various States

## 2.2.3 Other Controls and Status

The remaining controls of the main control window can be seen in Figure 2-5. These items include the *SEND* and *Cancel* buttons, the *File Options*, *GAIN ADJUST*, *FREQUENCY ADJUST* control, and *SYMBOL MAP* control. The details of the individual items is described in the remainder of Section 2.2.3.

### 2.2.3.1 SEND Button

The *SEND* button is used to affect any changes made to system setup parameters.

### 2.2.3.2 Cancel Button

The *Cancel* button is used to discard any changes made to system setup parameters. Using the *Cancel* button cannot undo changes that came before the *SEND* button was clicked.

### 2.2.3.3 File Options

Figure 2-15 shows the *Save Bit Sync Setup* control window. Complete bit sync configurations can be saved to disk by pressing the "Save" button under the File Options in the main menu. Similarly, complete bit sync configurations can be restored by clicking on the Recall button. When the *Save* or *Recall* button is clicked on, a control window will appear that allows the name of the configuration file to be entered. Bit sync files are saved with a \*.bs file extension; all other file extensions are invalid.

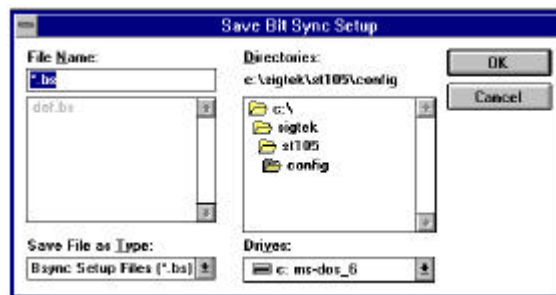


Figure 2-15 Bit Sync Configuration Save Control Window

### 2.2.3.4 ST-105 Control

Three additional control features are provided to allow the user to modify the system gain, change baud or carrier frequencies, and symbol mapping settings on the fly.

#### 2.2.3.4.1 Gain Adjust

The ST-105 control software provides the ability for the user to control the three gain stages of the ST-105's Automatic Gain Control (AGC) system. This function is initiated

by clicking on the *GAIN ADJUST* button in the *Bit Sync Control* area of the main control window. Figure 2-16 shows the *Gain Adjust* window when the system has been configured to process continuous signals. Figure 2-17 shows the *Gain Adjust* window when the system has been configured to process burst signals. Both windows provide a graphical representation of the processes that are controlled by this window. The burst variation provides an additional *BURST GRAPH* button which opens the *Bit Sync Burst Threshold* Graph display window (see Figure 2-18). An *AGC Timeout* parameter is provided to prevent the system gain from rapidly increasing if a signal is not active. The AGC will hold off on increasing the gain for the specified period of time if no signal energy is detected. The timeout value ranges from 1 second to 1024 seconds in power of two steps. This is most useful for low duty cycle or intermittent burst signals.

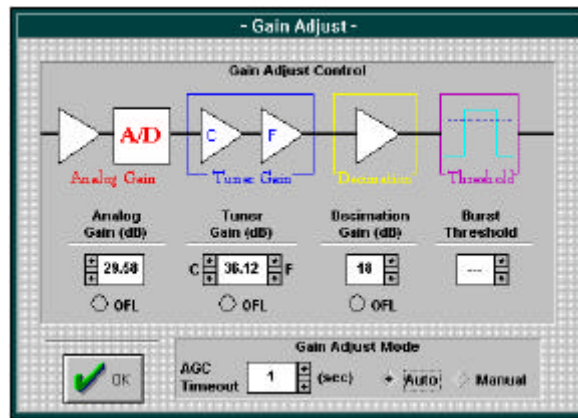


Figure 2-16 Gain Adjust Window (Continuous Mode)

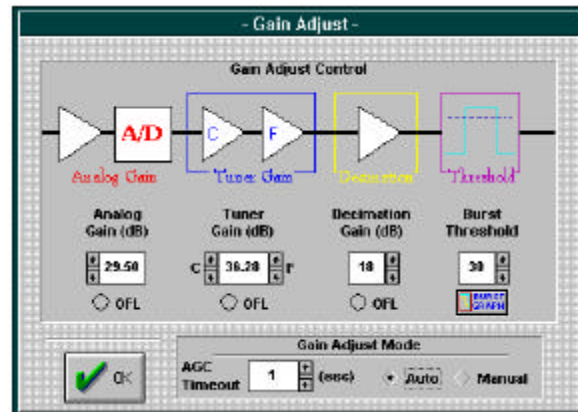


Figure 2-17 Gain Adjust Window (Burst Mode)

Figure 2-18 shows the Bit Sync Burst Threshold Graph with the gain values correctly set. The graph shows the detected amplitude of a burst signal in noise. The signal plus noise is the irregular trace. The straight, horizontal line across the entire plot is the detection threshold, and the box car function outlining the bursts is an indicator from the burst detection circuitry. The procedure for manually setting the gain is as follows. Click on the *Manual* radio button to switch the mode to manual. If the *Analog Gain OFL* (overflow) indicator is active, then decrease the analog gain until the *OFL* indicator is not

active. If the *Analog Gain OFL* indicator is not active, increase the analog gain until overflow is indicated, then back off a few dB. Repeat this procedure for the *Tuner Gain* and the *Decimation Gain*. Now click on the *BURST GRAPH* button to open the *Bit Sync Burst Threshold Graph*. Increase or decrease the *Tuner Gain* to frame the bursts by the white burst detection trace. Figure 2-18 is an example of correct gain settings. Figure 2-19 is an example of the gain set too high, and Figure 2-20 is an example of the gain set too low.

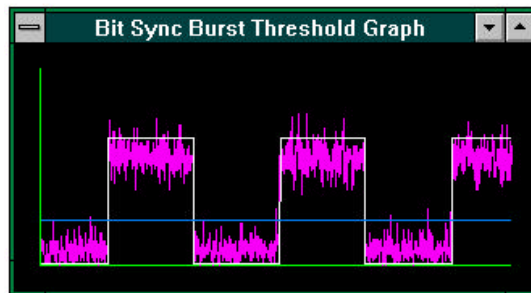


Figure 2-18 Burst Graph

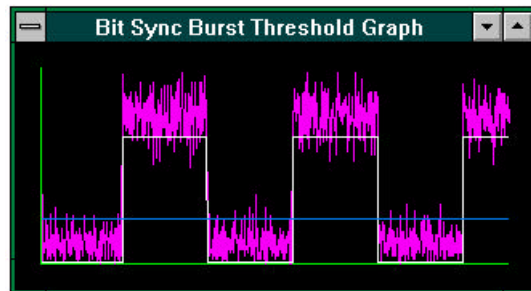


Figure 2-19 Burst Graph (Gain Too High)

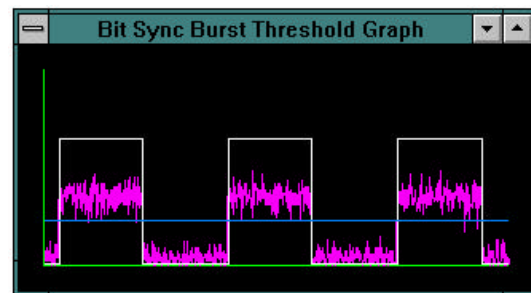


Figure 2-20 Burst Graph (Gain Too Low)



The default setting for the detection threshold will work very well in most cases. The only time it may need adjustment is when processing signals with very low signal-to-noise ratios. Figure 2-21 shows an example of the threshold set too high. Notice that the white burst detection indicator trace is dropping out in the middle of signal bursts. Figure 2-22 shows an example of the threshold set too low. Notice that the burst detection indicator trace is false trigger on noise in-between signal bursts.

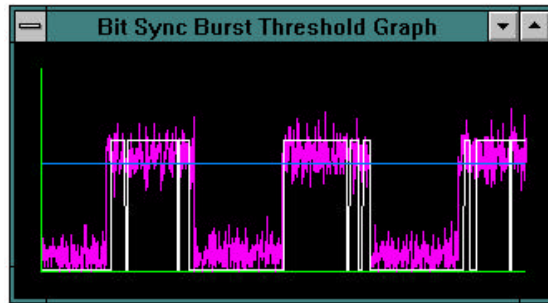


Figure 2-21 Burst Graph (Threshold Too High)

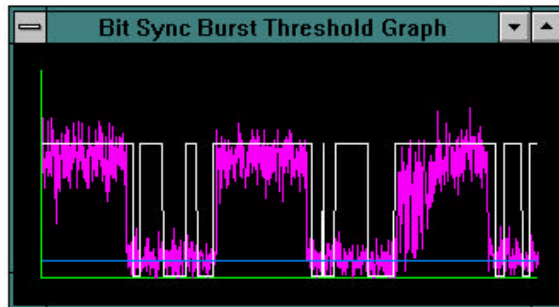


Figure 2-22 Burst Graph (Threshold Too Low)

### 2.2.3.4.2 Update Symbol Map

If the ST-105 System's follow on processor is not able to resolve symbol mapping ambiguities, the *Update Symbol Map* function may be used to re-map the dibits associated with the constellation points. This function is initiated by clicking on the *UPDATE SYMBOL MAP* button in the *Bit Sync Control* area of the main control window. When this button is clicked, the window shown in Figure 2-23 will pop up.

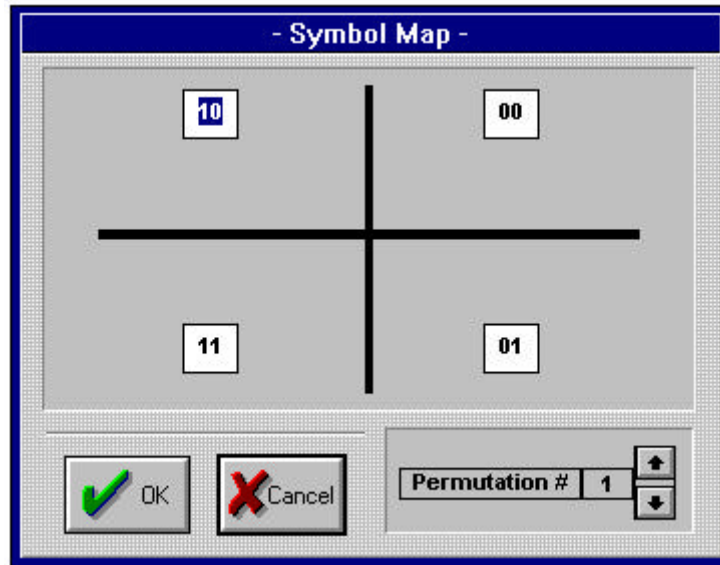


Figure 2-23 Symbol Map Assignment Window

The user may manually edit constellation/bit mapping values, or may alternatively click through the different permutations. The dibit pairs in the display are ordered as I then Q. For example, the value 01 is shown in the fourth quadrant (bottom right). If the demodulated symbol fell into the fourth quadrant, the output I bit would be 0 and the output Q bit would be 1. This parameter can be saved with the other system setup parameters. When operating on differential PSK signals the quadrants are interpreted differently. For DBPSK, the left side of the plane represents phase changes of 180 degrees, and the right side of the plane represents phase changes of 0 degrees. For DQPSK, the first quadrant (top right) represents phase changes of 0 degrees, the second quadrant (top left) represents phase changes of 90 degrees, the third quadrant (bottom left) represents phase changes of 270 degrees, and the fourth quadrant (bottom right) represents phase changes of 270 degrees. Note that if the user sets the symbol map and then changes the modulation to another type, the symbol map will change to a new default value that is modulation dependent.

### 2.2.3.4.3 Frequency Adjust

The ST-105 control software provides the capability to update the baud rate or carrier frequency on the fly without performing all the functions associated with changing the frequencies from the text entry box in the main control window. If it appears that carrier or baud acquisition is failing (see Figure 2-14), the user may manually tune these inside the *Frequency Adjust* window shown in Figure 2-24. This is accessed by selecting the *FREQ ADJUST* button in the lower right corner of the main control window. Both the baud rate and carrier frequencies may be manually tuned. The user also has the option to disable tracking of these frequencies. The *FFT Carrier Tuning* function is useful for determining the carrier frequency when it is not well known. Once the user clicks the *Start FFT* button, all processing will halt while the ST-105 takes a data snapshot and processes it to determine the center frequency of the signal. A *Stop FFT* button becomes available to allow aborting the FFT. After finding the center frequency, the ST-105 will automatically re-tune itself and resume processing. The number of FFTs averaged may be increased when working with low SNR signals. The *OK* button returns the operator to the main menu and updates the main window's carrier and symbol rate values. The *Cancel* button allows return to the main window without updating the carrier and symbol rate values.

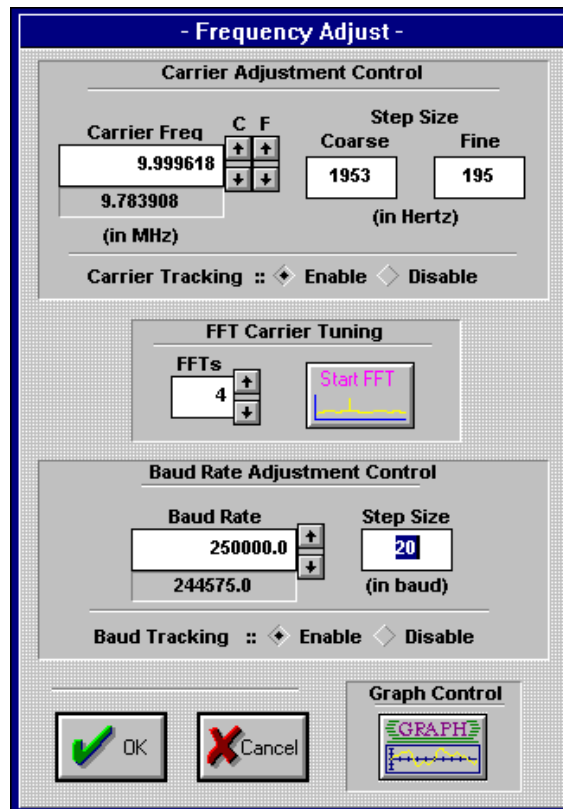
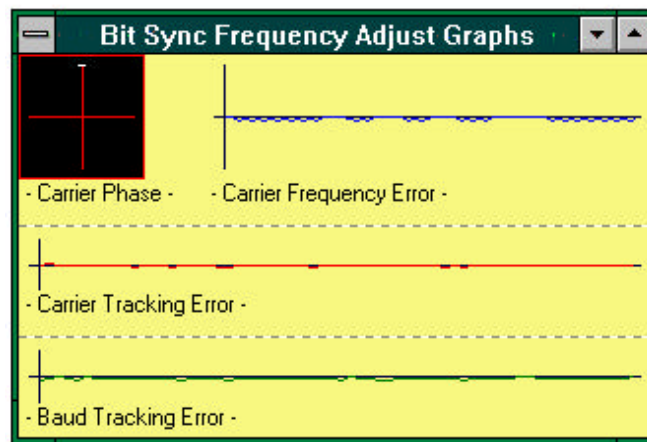


Figure 2-24 Frequency Adjust Modal Window

Tuning feedback is provided by the *Bit Sync Frequency Adjust Graphs* display shown in Figure 2-25. This is initiated by clicking on the *GRAPH* button in the bottom right hand

corner of the *Frequency Adjust* window. This display is composed of four graphs. The *Carrier Phase* graph is a polar plot showing the current value of the carrier phase. When the ST-105 is locked to a continuous signal, this display will show a cluster of dots on one of the display axes. When a burst signal is being processed or the carrier of a continuous signal is not locked, the display will show points distributed in a circular pattern. The *Carrier Frequency Error* display provides a relative indicator as to whether the specified carrier frequency is too high or too low. The *Carrier Tracking Error* and *Baud Tracking Error* graphs display the error signal from the frequency tracking functions. Figure 2-25 is an example of the ST-105 correctly locking up to a continuous signal.



**Figure 2-25** Frequency Adjust Graphs

Figure 2-26 through Figure 2-29 show various examples of the frequency error displays with different types and magnitudes of frequency error. Notice that when the errors are small, the error signals are more continuous than the large error displays which are more noise like. The slope and frequency of the carrier and baud tracking errors is a function of the sign and magnitude of the error. The frequency of the error signal increases with larger frequency error and the slope of the error curves changes when the error goes from positive to negative or vice versa.

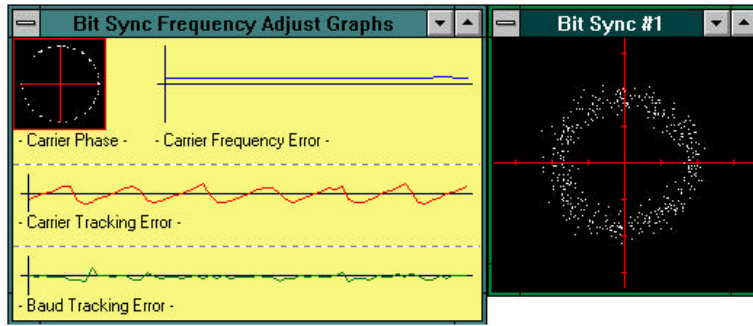


Figure 2-26 Frequency Adjust Graphs (Small Carrier Error)

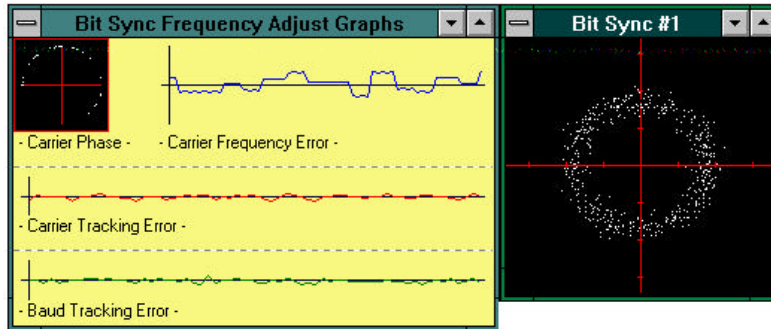


Figure 2-27 Frequency Adjust Graphs (Large Carrier Error)

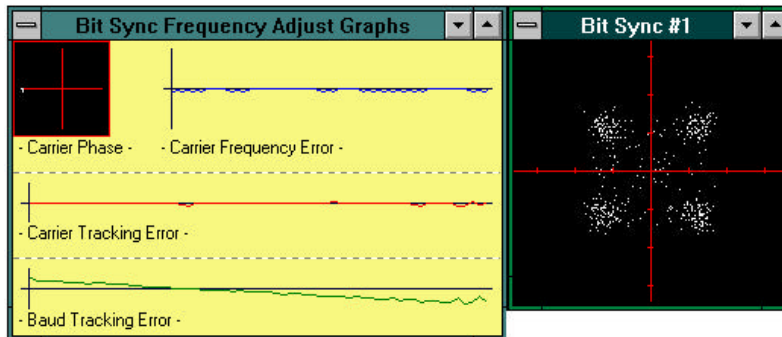


Figure 2-28 Frequency Adjust Graphs (Small Baud Error)

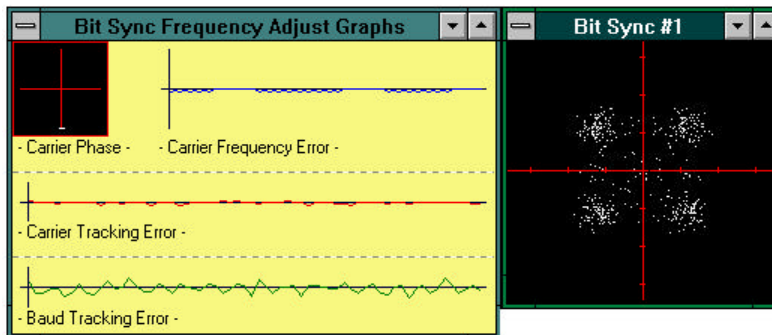


Figure 2-29 Frequency Adjust Graphs (Large Baud Error)

### **2.2.3.5 STATUS Message Bar**

The *STATUS* message bar is located on the bottom of the main control window. It informs the user of the current status of the current ST-105 board. If any parameters have been changed, the message bar will show the last change that was made. After the user clicks on the *SEND* button, the message will read "STATUS: Board Configured".

### **2.2.4 Burst and TDMA Processing**

The ST-105 is designed to be a flexible and easy to use device. Emphasis has been placed on minimizing the amount of tweaking required by the operator. However, some manual control may be required to process burst or TDMA signals depending on the signal's parameters and environment. For high SNR cases with high duty cycles, the ST-105 will perform well with bursting signals without any manual intervention. As the duty cycle and SNR decrease, the ST-105 may have difficulty in reliably locking up to a burst signal. In these cases there are several things the operator can do to help with signal acquisition and tracking.

The first thing to do if the ST-105 is having difficulty with burst signals is to switch from automatic gain control to manual gain control. See Section 2.2.3.4.1 for details on setting the gain.

If carrier acquisition is a problem, then the user should bring up the *Frequency Adjust* window. The user may then either manually tune the carrier and attempt to locate the correct frequency, or preferably use the *FFT Carrier Acquisition* function. If it appears that baud acquisition is failing, then the user may manually tune this inside the *Frequency Adjust* window. This is accessed by selecting the *FREQ ADJUST* button in the lower right corner of the main control window. See Section 2.2.3.4.3 for details on these tuning functions.

When processing burst signals, the Carrier Tracking mode in the *Frequency Adjust* window can be disabled in order to bypass the slower response Costas Tracking Loop and only use the fast response Block Phase for demodulation. This can often improve burst acquisition performance.

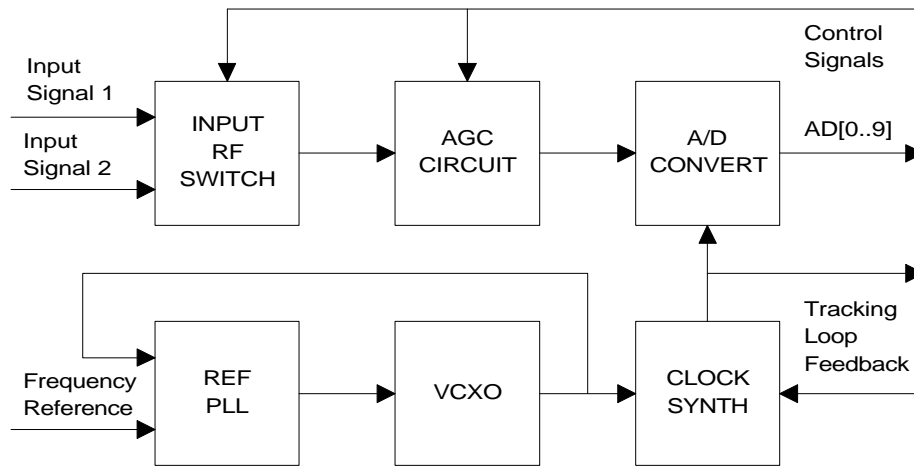
### **3. ST-105 THEORY OF OPERATION**

The SIGTEK ST-105 Demodulator/Bit sync is designed to demodulate and bit sync BPSK or QPSK signals at rates of 2400 baud to 2.1 Mbaud, and with center frequencies from 200 kHz to 21.4 MHz. The ST-105 implements a digital baud synchronous sampling approach. In this approach the entire input frequency range is digitized and a digital tuner is used to tune to the signal of interest. Digital lowpass decimation filters are then used to decimate the quadrature baseband signal down to an integer number of samples per baud. The ST-105 uses four samples per baud. After baseband tuning and decimation, additional filtering may be applied to the complex signal to perform adaptive equalization or fixed tap Nyquist pulse shaping filtering for band limited signals. A TDMA processor is implemented to increase the rate of signal acquisition for processing burst TDMA signals. The bit sync function uses an in-phase/mid-phase approach to synchronize to the data stream and to reconstruct a baud clock. Carrier acquisition is accomplished through use of an automatic frequency control loop. Once this loop converges, control is handed off to a quadrature Costas tracking loop. A floating point DSP processor is used to process baud and carrier tracking error signals in order to update the sample clock rate and the digital tuners center frequency. The DSP processor also performs digital gain control and equalizer tap update functions.

The ST-105 is composed of two boards. The main board is a full size PC/AT form factor board. This board contains all processing elements from the digital tuner to the end of the processing chain. A daughter or mezzanine board is attached to the main board. This board performs the front end analog signal processing, generates a sample clock, and digitizes the wideband input signal. The ST-105 makes use of several Field Programmable Gate Array (FPGA) devices. These devices are programmed to perform specific functions of the demodulator/bit sync. The ST-105 also makes use of static RAM devices for converting complex data from rectangular to polar coordinates, for scaling integrate and dump outputs, for looking up soft decision output values, and for looking up phase error values for carrier tracking lock detection.

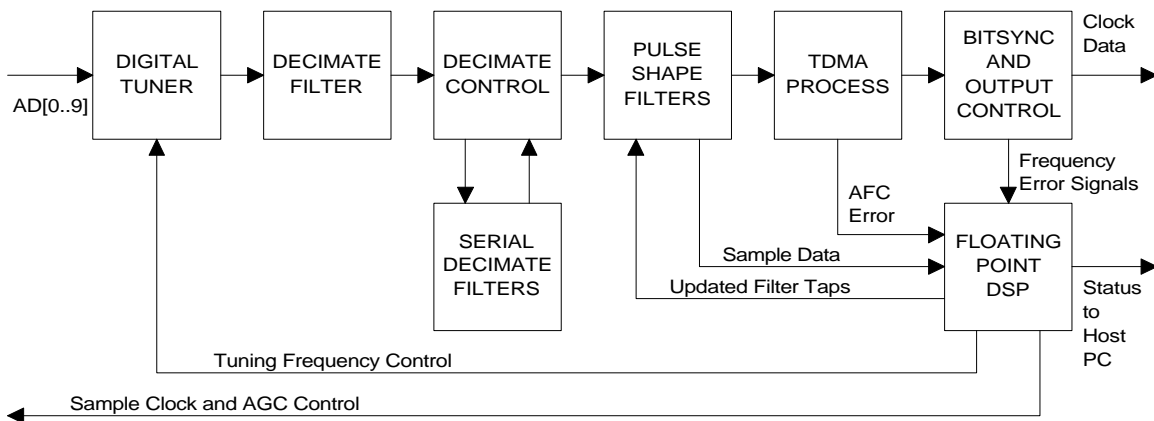
Figure 3-1 shows the block diagram of the daughter board. The two input signal sources go into an RF switch. The control software sets the control signal to choose on of the two input sources. The chosen signal then goes to an AGC circuit. The AGC circuit acts to maintain proper loading on the input of the 10-bit A/D converter. Output of the A/D converter goes to the main board for processing. One of the functions performed on the main board is to monitor the A/D output loading, and to provide feedback to the AGC circuit. The third external input to the daughter board is an external frequency reference. The ST-105 will phase lock its VCXO to this reference signal. The output of the VCXO is a 50 MHz clock which sources a clock synthesizer circuit. The clock synthesizer circuit is composed of a numerically controlled oscillator (NCO) device with a built in D/A converter. This device receives clock rate input from the main board, and generates a divided clock output which is then output to a clock multiplier device. The clock multiplier device has an internal VCO with two internal clock divider circuits. One divider circuit is used to divide the VCO output down to match the input clock signal. The other divider circuit is used to divide the VCO output down to the desired clock frequency. The

output of the clock multiplier is a TTL level signal that operates in the low 40 MHz to upper 50 MHz range.



**Figure 3-1 ST-105 Daughter Card Block Diagram**

Figure 3-2 shows the block diagram of the ST-105's main board. The A/D data from the daughter board is input to a wideband digital tuner ASIC. The digital tuner ASIC has an internal NCO which generates a digital, quadrature local oscillator (LO). The input digital data is multiplied by the quadrature LO to tune the signal to baseband. Internal digital lowpass filters inside the tuner device remove the other signal images and decimates the signal to a lower sample rate. The digital tuner decimates the signal by powers of two from two to sixty-four. The tuner outputs in-phase (I) and quadrature (Q) data. This data then proceeds to a pair of digital FIR filters. These filters have a cutoff frequency that matches the bandwidth of the signal of interest. In addition to filtering, the digital FIR filters provide a second level of decimation.



**Figure 3-2 ST-105 Main Board Block Diagram**



The next device in the processing chain is a Decimation and AGC control. This function is implemented using a FPGA device. If the signal of interest has a baud rate that is lower than approximately 10 kHz, a third level of decimation filtering is performed by a pair of serial input decimation filters. In these cases, the FPGA will route the output of the preceding filters to the serial filters. Otherwise, the output of the preceding filters will be passed on to the next processing step. The second key function performed by the Decimation and AGC FPGA is to monitor the output of the A/D converter and its overflow signal in order to complete the AGC loop. The FPGA compares the A/D loading to a preset threshold. The gain of the AGC on the daughter board is adjusted to match the A/D loading to the desired level.

Following the Decimation and AGC function is a reconfigurable pair of filters. The digital filters are the same type as used in the second level decimation stage following the digital tuner. In one mode, the filters act as pulse shaping digital filters. In this case the filters are configured as two fixed tap, real filters. One operates on the I-arm and the other operates on the Q-arm. The length of the filters spans three symbols. In the other two modes of operation, DISABLED and CMA, the filters are configured to implement a complex filter. The complex filter can be a fixed tap impulse response filter which passes the signal through without modifying it (DISABLED), or it can be an adaptive filter. In the case of the adaptive filter, input data values are stored into the pipeline delay buffer and the output values are captured by the FPGA device. The FPGA reads the input values from the pipeline buffer and sends them to the DSP processor along with the corresponding filter output. The DSP processor then uses this information to update the filter taps according to the Constant Modulus Algorithm. Other equalizer algorithms may be implemented in the future.

TDMA processing is implemented using an FPGA, a pipeline delay buffer, and coordinate conversion look-up tables in static RAM. The burst TDMA processor converts the complex I and Q data to phase and amplitude data. It then performs a modulo operation on the phase data to calculate the carrier phase offset. This information is also used to compute a frequency error for the AFC carrier acquisition function. When the signal transmission mode is burst, the TDMA processor will use the carrier phase offset to correct the data as it comes out of the pipeline delay buffer so that the signal constellation will have the proper orientation. During continuous signal transmission, this correction is not applied.

The bit sync function uses an in-phase/mid-phase approach to synchronize to the data stream and to reconstruct a baud clock. Carrier acquisition is accomplished through use of an automatic frequency control loop. Once this loop converges, control is handed off to a quadrature Costas tracking loop. The bit sync FPGA uses static RAM tables to look up normalized values for the constellation display and compressed soft decision values for output. The lookup tables also include phase error and amplitude data which are used to detect baud and carrier lock. A floating point DSP processor is used to process baud and carrier tracking error signals in order to update the sample clock rate and the digital tuners center frequency. The DSP processor also performs digital gain control and equalizer tap update functions.

## **4. ST-105 INSTALLATION**

<p>This section discusses the hardware and software installation procedures for the ST-105. If the ST-105 is installed as part of an integrated SIGTEK system such as the ST-205, refer to the system level user's manual for specific cabling and configuration instructions.</p>
--

### **4.1 Hardware Installation**

Please note the following precautions before handling or installing the ST-105.

- Electro-static discharge (ESD) CAN damage this board. Before unpacking the board, ground yourself by approved procedures and handle the board only by the endplate and edge of the circuit board. Be careful not to touch the gold-plated edge connections nor the device pins. A charge too small to be felt or seen can weaken or damage an IC.
- The ST-105 is a thick board. When installing the ST-105 in your computer, make sure none of the daughter board pins can make contact with a board in an adjacent slot, or with a metal wall of the chassis. Take into consideration any movement of the board due to vibration or jarring. If necessary, leave the slot next to the ST-105 empty.
- Make sure your computer chassis has good air flow characteristics. The ST-105 implements several devices that operate at clock frequencies approaching 60 MHz. These devices get very hot, and performance may be affected if the computer chassis does not provide adequate air flow.
- When connecting input signal sources, verify that the power level is between -20 dBm and -50 dBm. The front end does have protection circuitry built in for moderate overloads, but excessive input power can damage the ST-105.
- Do not separate the daughter board and the main board. The main board contains many integrated circuits with fine pitch, surface mount, quad flat pack packages. The force require to separate the two boards can flex the main board and stress the pin to pad connections
- The drivers for connectors JP3 and JP4 are designed to drive TTL loads over relatively short ribbon cables. Signals may be degraded if the ribbon cables become excessively long or if the impedance differs from that of the input of a TTL device. The drivers for JP5 and JP6 are designed to send TTL level signals over a 50 W coaxial cable.
- Before installing the board in your computer, make sure the board address will not conflict with other devices installed in your computer. The board is typically shipped with a hex address of 0x330.

The ST-105 board I/O address must be correctly set for proper operation. The ST-105 occupies sixteen consecutive I/O addresses starting with the configured board address. The board I/O address is selected using the jumpers of JP10. The jumpers for JP10 from left to right are A9 (pins 1-2), A8 (pins 3-4), A7 (pins 5-6), A6 (pins 7-8), A5 (pins 9-10),

and A4 (pins 11-12). The address of the ST-105 must also be set in software to an even 16 byte boundary. Table 4-2 lists the jumper installation for hex addresses ranging from 0x200 to 0x3f0. Installing a jumper sets the corresponding address line to logic '0'. Removing a jumper sets the corresponding address line to logic '1'. A dark square in the table indicates where a jumper should be installed. **JP9 is used to specify a secondary board address. This feature has not been implemented so all three jumpers must be installed on JP9 for correct operation of the ST-105.**

Table 4-2 ST-105 JP10 Address Jumper Settings

Hex Address	A 9	A 8	A 7	A 6	A 5	A 4	Hex Address	A 9	A 8	A 7	A 6	A 5	A 4
200		■	■	■	■	■	300			■	■	■	■
210		■	■	■	■	■	310			■	■	■	■
220		■	■	■	■	■	320			■	■	■	■
230		■	■	■	■	■	330			■	■	■	■
240		■	■	■	■	■	340			■	■	■	■
250		■	■	■	■	■	350			■	■	■	■
260		■	■	■	■	■	360			■	■	■	■
270		■	■	■	■	■	370			■	■	■	■
280		■	■	■	■	■	380			■	■	■	■
290		■	■	■	■	■	390			■	■	■	■
2A0		■	■	■	■	■	3A0			■	■	■	■
2B0		■	■	■	■	■	3B0			■	■	■	■
2C0		■	■	■	■	■	3C0			■	■	■	■
2D0		■	■	■	■	■	3D0			■	■	■	■
2E0		■	■	■	■	■	3E0			■	■	■	■
2F0		■	■	■	■	■	3F0			■	■	■	■

Table 4-3 PC XT/AT I/O Map

Hex Range	Usage	Hex Range	Usage
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 Timer	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	Serial Port
060-064	8742 Controller (AT)	2F8-2FF	Serial Port
070-071	CMOS RAM & NMI Mask Register (AT)	300-30F	Prototype Card
080-08F	DMA Page Registers	310-31F	Prototype Card
0A0-0A1	8259 - PIC #2 (AT)	320-32F	Hard Disk (XT)
0A0-0AF	NMI Mask Register (XT)	378-37F	Parallel Printer
0C0-0DF	8237 DMA #2 (AT - word mapped)	380-38F	SDLC
0F0-0FF	80287 Numeric Processor (AT)	3A0-3AF	SDLC
1F0-1FF	Hard Disk (AT)	3B0-3BB	MDA
200-20F	Game/Control	3BC-3BF	Parallel Printer
210-21F	Expansion Unit (XT)	3C0-3CF	EGA
238-23B	Bus Mouse	3D0-3DF	CGA
23C-23F	Alternate Bus Mouse	3E8-3EF	Serial Port
278-27F	Parallel Printer	3F0-3F7	Floppy Disk
2B0-2BF	EGA	3F8-3FF	Serial Port

## **4.2 Software Installation (Stand Alone ST-105 Operation)**

Control of the ST-105 decoder is performed using SIGTEK's ST-203 board control software. The ST-203 control software allows control on any combination of the following SIGTEK board level products:

ST-102 Spread Spectrum Demodulator

ST-105 Burst Demodulator

ST-106 Decoder - Derandomizer

ST-107 RS-422 Multiplexer Board

ST-512 IF Translator

ST-701 Frequency Reference and Distribution Board.

These boards can either be shipped stand alone or as part of a preconfigured system (such as an ST-203 PCM Receiver or ST-205 Multichannel Receiver).

A separate section of the User's Manual contains installation instructions for the ST-203 board control software. When installing an ST-105 for stand alone use, follow the installation procedures in that section which pertain to the ST-105.

## 5. ST-105 DEMODULATOR SPECIFICATIONS

### General

Size	Single Full Size PC-AT ISA Board
Power Requirements	+5V @ 1.9A, +12V @ 0.7A

### Signal Input

Impedance	50 $\Omega$
Power Level	-20 dBm to -50 dBm
Center Frequency	200 kHz to 21.4 MHz

### Reference Input

Impedance	50 $\Omega$
Power Level	0 dBm to 6 dBm
Center Frequency	5 MHz or 10 MHz

### Modulation

BPSK, QPSK, DBPSK, DQPSK,  
OQPSK, and  $\pi/4$  DQPSK

### Transmission Modes

Burst or Continuous

### Data Rate

2400 Symbol/sec to 2.1 Msymbol/sec  
(Operation to 3.8 Msymbol/sec is supported in  
software version V2.3; however, older ST-105  
boards may not support the higher baud rate  
operation)

### Filter Modes

Rectangular pulse  $\sin(x)/x$   
Nyquist pulse shaping, or  
adaptive CMA equalizer

### Clock and Data Out

Level	TTL levels with TTL load output = 0 V out for logic '0' and output $\geq 2.0$ V for logic '1' with 50 $\Omega$ load
Data	Programmable for various combinations of clock and hard decision data