To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

RENESAS

User's Manual

Multimedia Processor for Mobile Applications

PDMA

EMMA Mobile1

Document No. S19373EJ2V0UM00 (2nd edition)
Date Published April 2009

© NEC Electronics Corporation 2009
Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

The names of other companies and products are the registered trademarks or trademarks of the respective company.

These commodities, technology or software, must be exported in accordance with the export administration regulations of the exporting country. Diversion contrary to the law of that country is prohibited.

- **The information in this document is current as of August, 2008. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".
  The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)
(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).

M8E 02. 11-1

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the PDMA functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of PDMA of EM1, and be useful as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Registers
- Chapter 3 Description of functions
- Chapter 4 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of PDMA of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μPD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	This manual
	One Chip (MC-10118A)	S19598E
	One Chip (μPD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

CONTENTS

LIST OF FIGURES

CHAPTER 1 OVERVIEW

1.1 General

This manual describes the PCM DMA (PDMA) for EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

The PDMA macro transfers Internal SRAM data to PM0 by using DMA transfer.

1.2 Features

PDMA is a DMA macro designed especially for PCM to reduce power consumption during music playback. This macro can continuously transfer data from Internal SRAM to PM0 with the EM1 power saving mode enabled.

- Input: Internal SRAM (128 KB) only
- Output: PM0 via SWL0

- Transfer direction: TX direction only (memory-to-peripheral transfer)
- Transfer address: 4 Byte aligned
- Transfer length: 4 to 128 KB (minimum transfer unit: 1 word = 4 Byte)

- Transfer reservation (When a transfer is completed, the next transfer starts automatically.)
- Compatible with the existing DMA (PDMA is used exclusively with DMA implemented in the L1 power domain.)

1.3 Restriction

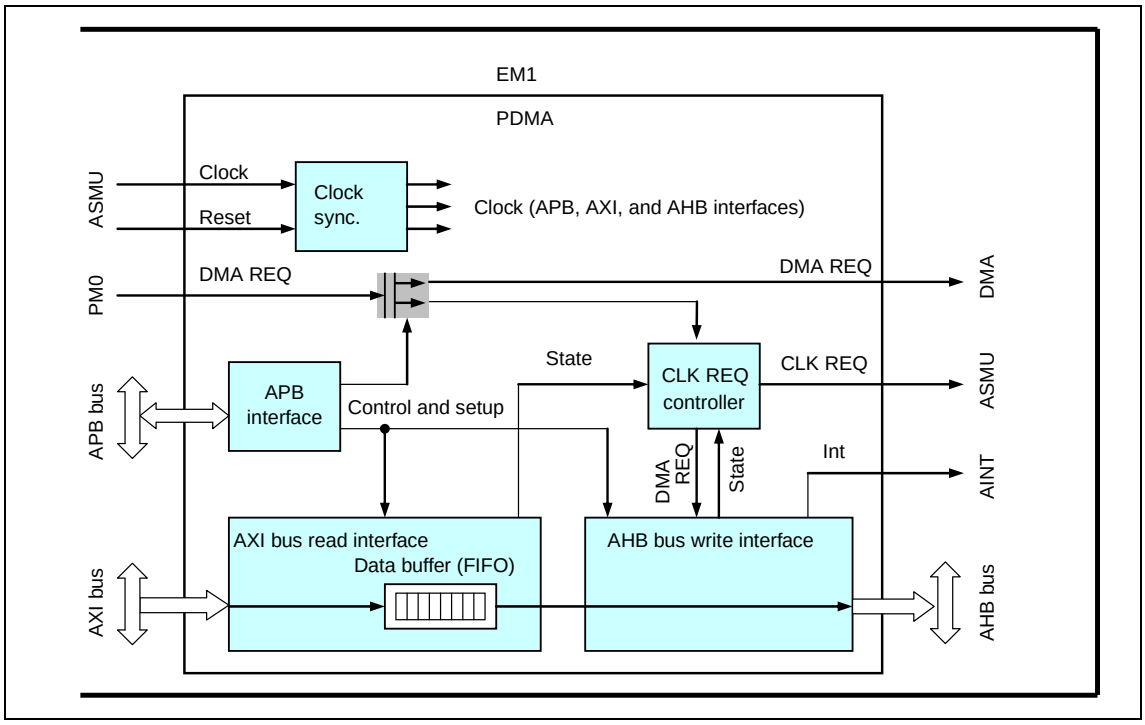
It's necessary to invalidate clock automatic control of a Internal SRAM at the time of the transmission starting time of PDMA Macro and reservation.

Please make transmission starting of PDMA / a reservation (PDMA_CONT=1) in the state which invalidated clock automatic control of a Internal SRAM. In case of the state that the clock automatic control was made effective, you can't sometimes normally begin to forward.

After beginning to forward, it's recommended to make the clock automatic control of SRC effective. Further when status of PDMA completes transmission during reservation, and PDMA begins to forward automatically, I don't come under a restriction matter.

1.4 Function Blocks

Figure 1-1. PDMA Block Diagram



Clock synchronizer

This circuit synchronizes the clocks and supplies the clock to each processing block. PDMA handles the following three clocks:

PCLK: APB clock for accessing registers that belongs to the LBUS clock domain
ACLK: AXI clock that belongs to the HBUS clock domain
HCLK: AHB clock that belongs to the LBUS domain

Clock request controller

This circuit monitors the status of each interface and asserts CLKREQ when a clock is required. The ASMU supplies clocks while CLKREQ is asserted.

CHAPTER 2 REGISTERS

The PDMA registers are accessed via the APB. The base address is C008_0000H.
The PDMA registers can be accessed only in word units. Accesses in halfword or byte units are not supported.

2.1 Registers

Base address: C008_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	PDMA/DMA selection register (exclusively switched)	PDMA_DMA_SEL	R/W	0000_0000H
0004H	Transfer start/reserve register (used for both starting and reserving transfer)	PDMA_CONT	W	0000_0000H
0008H	Status register (stopped/transferring/reserved)	PDMA_STATUS	R	0000_0000H
000CH	Reservation cancel register	PDMA_RSV_CANCEL	W	0000_0000H
0010H	Forced stop register	PDMA_END	W	0000_0000H
0014H-001CH	Reserved	–	–	–
0020H	Transfer start address register (for reservation, 4-byte alignment)	PDMA_RSV_ADD	R/W	0000_0000H
0024H	Transfer length register (for reservation, in word (4-byte) units)	PDMA_RSV_LENG	R/W	0000_0000H
0028H	Transfer start address register (during transfer, 4-byte alignment)	PDMA_RUN_ADD	R	0000_0000H
002CH	Transfer length register (during transfer, in word (4-byte) units)	PDMA_RUN_LENG	R	0000_0000H
0030H	Interrupt status register	PDMA_INT_STATUS	R	0000_0000H
0034H	Interrupt raw status register	PDMA_INT_RAW_STATUS	R	0000_0000H
0038H	Interrupt enable set register	PDMA_INT_ENABLE	R/W	0000_0000H
003CH	Interrupt enable clear register	PDMA_INT_ENABLE_CL	W	0000_0000H
0040H	Interrupt source clear register	PDMA_INT_REQ_CL	W	0000_0000H
0050H	Address pointer register (during transfer, 4-byte aligned)	PDMA_RUN_ADP	R	0000_0000H
0054H	Error register (operational violation)	PDMA_ERR	R/W	0000_0000H
0058H	Temporary register (can be used for reservation management)	PDMA_TMP	R/W	0000_0000H
005CH	AXI address pointer (for debugging)	PDMA_AXI_ADP	R	0000_0000H

2.2 Register Descriptions

2.2.1 PDMA/DMA selection register

This register (PDMA_DMA_SEL: C008_0000H) specifies whether to transfer PCM data by using PDMA or DMA (exclusive). The selected status can be checked by reading this register. DMA (0) is selected after a reset. To use PDMA, this register must be set to 1.

Only the following DMA logical channels are excluded from PDMA:

LCH9 of PCH2 (memory-to-peripheral transfer)

LCH9 of PCH3 (peripheral-to-memory transfer)

Other channels can be used even if PDMA is selected.

The setting of this register cannot be changed dynamically during music playback.

Hardware operation:

PDMA switches the output destination of the DMAREQ signal input from PCM between PDMA and DMA. PDMA detects the DMAREQ signal based on levels, not edges.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							DMA_MODE

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
DMA_MODE	R/W	0	0	Selects which type of transfer is used, DMA or PDMA. 0: DMA 1: PDMA

2.2.2 Transfer start/reserve register

This write-only register (PDMA_CONT: C008_0004H) directs the PDMA macro to start a transfer. Three statuses are provided for PDMA: stopped, transferring, and reserved. Before making a reservation by using this register, make sure that PDMA has not been reserved by using the status register (PDMA_STATUS).

If this register is set up while PDMA is stopped, transferring starts.

If this register is set up while PDMA is transferring data, the next transfer is reserved.

If this register is set up while PDMA is reserved, the setting is regarded to be invalid and the OP_ERR bit of the error register (PDMA_ERR) is set to 1.

31	30	29	28	27	26	25	24
Reserved							

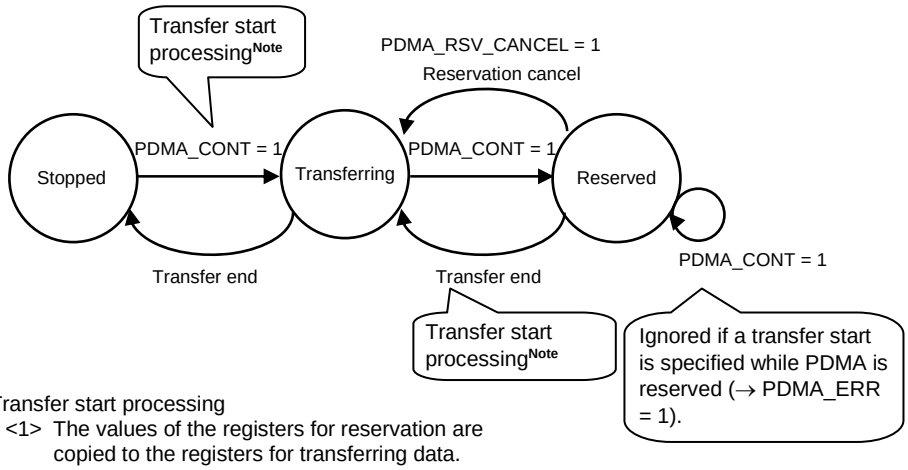
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							START

Name	R/W	Bit	After Reset	Function
Reserved	—	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
START	W	0	0	Starts or reserves a transfer. 1: Transfer start or reservation

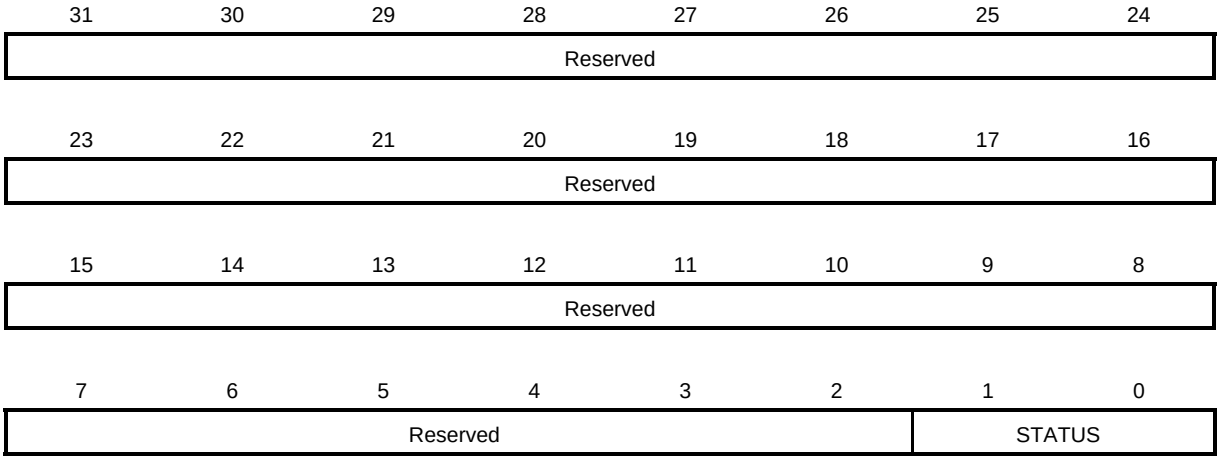
Figure 2-1. PDMA Status Transition



Note Transfer start processing
<1> The values of the registers for reservation are copied to the registers for transferring data.
PDMA_RSV_ADD → PDMA_RUN_ADD
PDMA_RSV_LENG → PDMA_RUN_LENG
<2> DMA transfer starts.

2.2.3 Status register

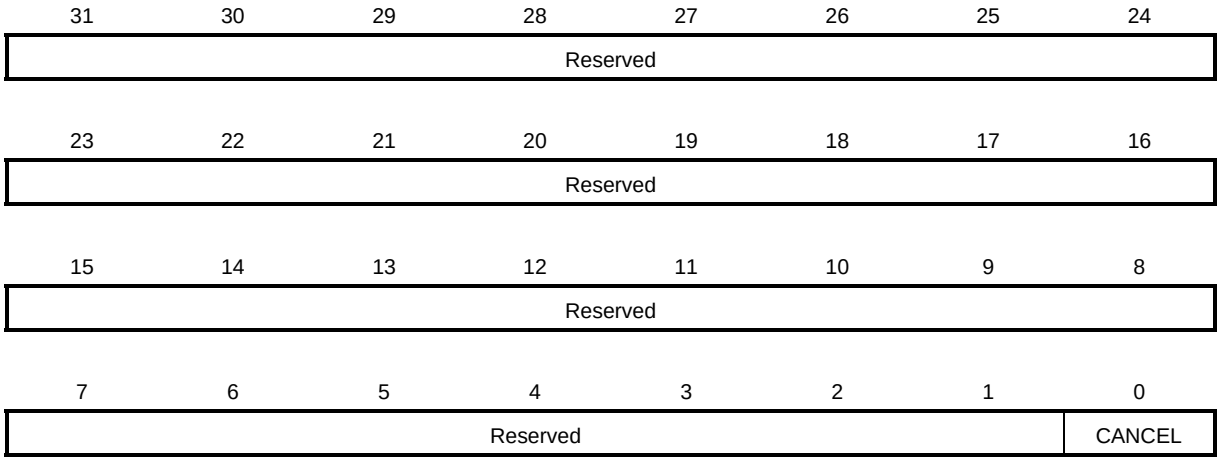
This read-only register (PDMA_STATUS: C008_0008H) indicates the PDMA macro operating status. Three statuses are provided for PDMA: stopped, transferring, and reserved. Before making a reservation, make sure that PDMA has not been reserved by reading this register.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
STATUS	R	1:0	0	Indicates the PDMA operating status. 00: Stopped 01: Transferring 10: Reserved

2.2.4 Reservation cancel register

This write-only register (PDMA_RSV_CANCEL: C008_000CH) directs PDMA to cancel reservation. If this register is set up, the reserved transfers are cancelled and PDMA transitions to the transferring status. Even if this register is set up, it is invalid if PDMA is not transferring data.



Name	R/W	Bit	After Reset	Function
Reserved	—	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
CANCEL	W	0	0	Cancels reservation. 1: Cancels reservation.

2.2.5 Forced stop register

This write-only register (PDMA_END: C008_0010H) directs PDMA to forcibly stop transferring. After transferring is stopped, all PDMA registers are reset. Before resuming transferring, set up transfer registers, the PDMA/DMA selection register (PDMA_DMA_SEL), and interrupt registers.

Hardware operation:

When an instruction to forcibly stop transferring is received, the PDMA module is reset.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							END

Name	R/W	Bit	After Reset	Function
Reserved	—	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
END	W	0	0	Forcibly stops transferring. 1: Forcibly stops transferring.

2.2.6 Transfer start address register (for reservation)

This register (PDMA_RSV_ADD: C008_0020H) specifies the transfer start address as a 4-byte aligned address. Only the internal SRAM can be used as the transfer source memory. Set up this register before setting up the transfer start/reserve register (PDMA_CONT).

31	30	29	28	27	26	25	24
RSV_ADD							

23	22	21	20	19	18	17	16
RSV_ADD							

15	14	13	12	11	10	9	8
RSV_ADD							

7	6	5	4	3	2	1	0
RSV_ADD						0	0

Name	R/W	Bit	After Reset	Function
RSV_ADD	R/W	31:0	0	Specifies the transfer start address of the transfer source memory as a 4-byte aligned address. Therefore, the lower 2 bits are fixed to 0.

2.2.7 Transfer length register (for reservation)

This register (PDMA_RSV_LENG: C008_0024H) specifies the transfer length in word units (1 word = 4 bytes) in the range from 1 to 8000H. Specifying 0 is prohibited. Set up this register before setting up the transfer start/reserve register (PDMA_CONT). The value of this register does not change during a transfer.

Hardware operation:

Because this register is set to 0 after a reset, specify a value in the settable range before starting a transfer. Specifying 0 is not supported. (If it is set, no bus transaction occurs and the status register value does not change.)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
RSV_LENG							

7	6	5	4	3	2	1	0
RSV_LENG							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0	Reserved. When these bits are read, 0 is returned for each bit.
RSV_LENG	R/W	15:0	0	Specifies the transfer length in word units. Specifying 0 is prohibited. A value in the range from 1 to 8000H must be specified.

2.2.8 Transfer start address register (during transfer)

This read-only register (PDMA_RUN_ADD: C008_0028H) indicates the transfer start address of the DMA transfer being processed. The address is shown as a 4-byte aligned address. The value of the transfer start address register (PDMA_RSV_ADD) is copied to this register when the PDMA status changes from stopped or reserved to transferring.

31	30	29	28	27	26	25	24
RUN _ADD							

23	22	21	20	19	18	17	16
RUN _ADD							

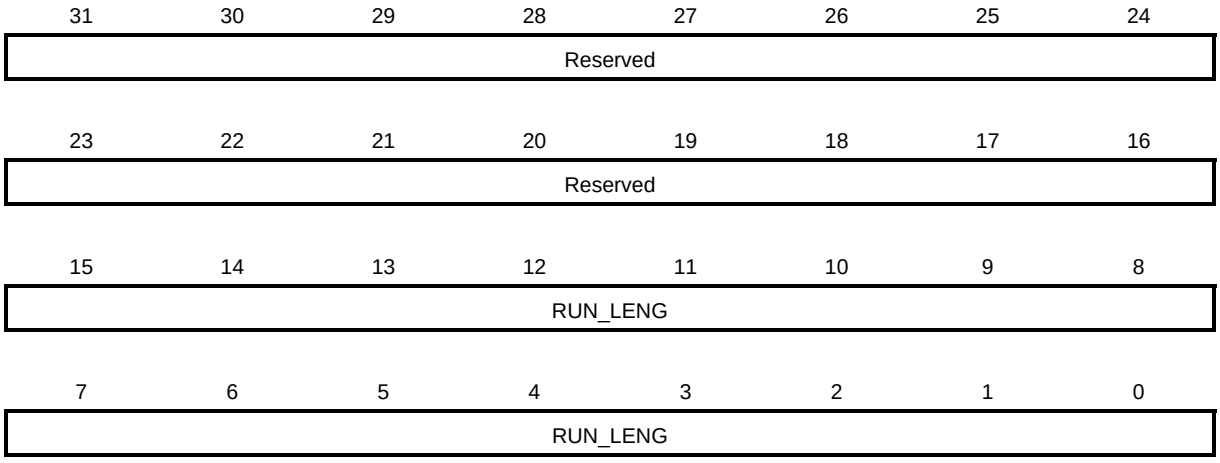
15	14	13	12	11	10	9	8
RUN _ADD							

7	6	5	4	3	2	1	0
RUN _ADD						0	0

Name	R/W	Bit	After Reset	Function
RUN _ADD	R	31:0	0	Indicates the transfer start address of the DMA transfer being processed as a 4-byte aligned address. Therefore, the lower 2 bits are fixed to 0.

2.2.9 Transfer length register (during transfer)

This read-only register (PDMA_RUN_LENG: C008_002CH) indicates the transfer length of the DMA transfer being processed. The length is shown in word units (1 word = 4 bytes). The value of the transfer length register (PDMA_RSV_LENG) is copied to this register when the PDMA status changes from stopped or reserved to transferring. The value of this register does not change during a transfer.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0	Reserved. When these bits are read, 0 is returned for each bit.
RUN_LENG	R	15:0	0	Indicates the transfer length in word units. Value range: 1 to 8000H

2.2.10 Interrupt status register

This read-only register (PDMA_INT_STATUS: C008_0030H) indicates the status of interrupt sources. The status of the interrupt sources enabled with the interrupt enable set register (PDMA_INT_ENABLE) can be read.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

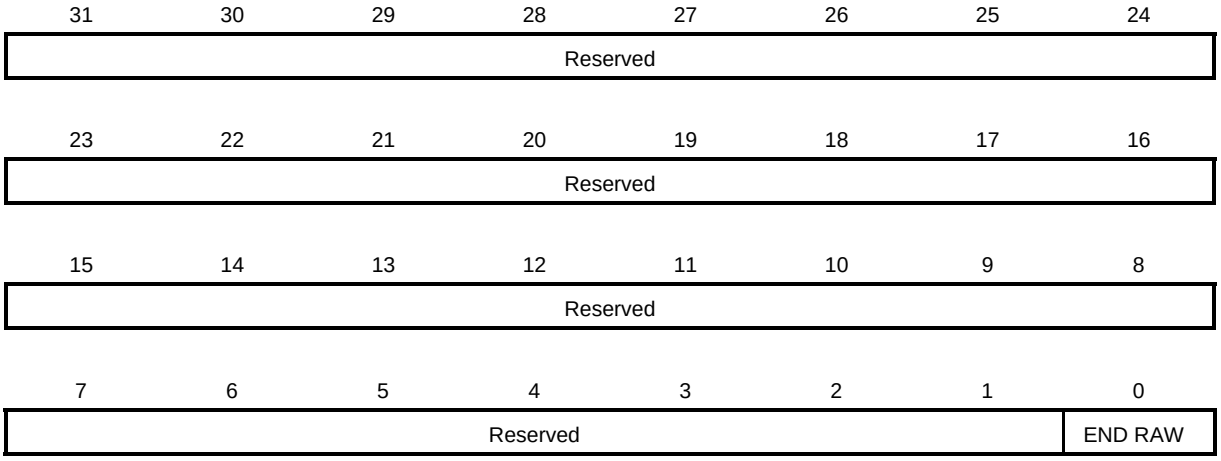
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							END

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
END	R	0	0	Indicates the status of the transfer end interrupt. 0: No interrupt source 1: Interrupt source occurred

2.2.11 Interrupt raw status register

This read-only register (PDMA_INT_RAW_STATUS: C008_0034H) indicates the status of interrupt sources. The bits corresponding to the interrupt sources are set to 1 regardless of the settings of the interrupt enable set register and the interrupt enable clear register (PDMA_INT_ENABLE_CL).



Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
END RAW	R	0	0	Indicates the raw status of the transfer end interrupt. 0: No interrupt source 1: Interrupt source occurred

2.2.12 Interrupt enable set register

This register (PDMA_INT_ENABLE: C008_0038H), when written, enables the issuance of interrupt requests. When read, the status whether the issuance of interrupt requests is enabled is acquired.

Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source is set to 1 in this register, the interrupt source is set, the relevant interrupt request is issued, and the corresponding bit of the interrupt status register is set to 1. If no bits are set in this register, no interrupt requests are issued even if the interrupt source is set, but the corresponding bit of the interrupt raw status register is set to 1.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

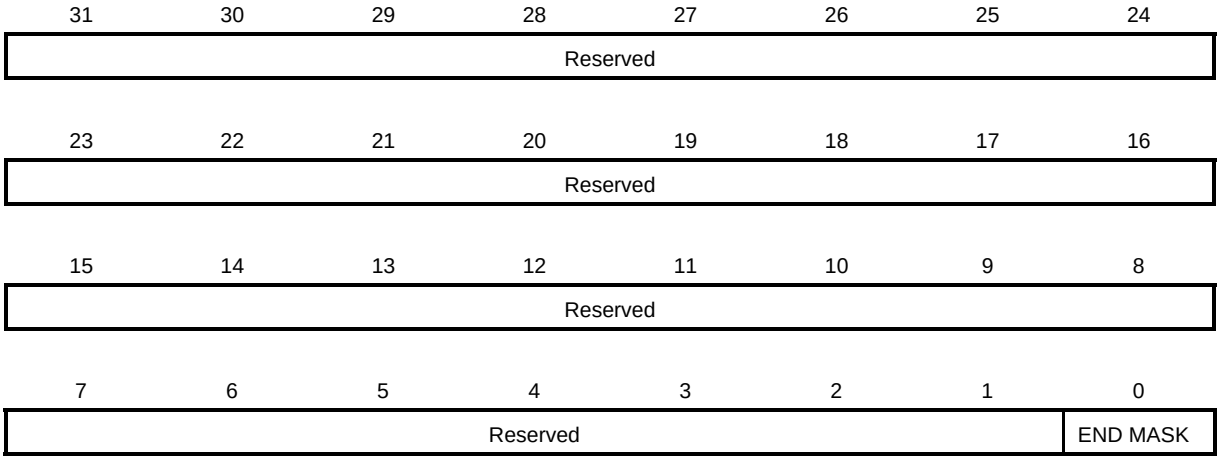
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							END EN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
END EN	R	0	0	Indicates whether the issuance of the transfer end interrupt request is enabled. 0: Not enabled 1: Enabled
	W	0	–	1: Cancels interrupt masking.

2.2.13 Interrupt enable clear register

This write-only register (PDMA_INT_ENABLE_CL: C008_003CH) disables issuance of interrupt sources. Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source in this register is set to 1, no interrupt requests are issued even if the interrupt source is generated. The status of the corresponding bit in the interrupt status register also remains unchanged. If no bits are set to 1 in this register, an interrupt request is issued and the corresponding bit of the interrupt status register is set to 1 when the interrupt source is set to 1.



Name	R/W	Bit	After Reset	Function
Reserved	–	31:1	0	Reserved.
END MASK	W	0	0	Disables issuance of the transfer end interrupt request. 1: Masks the interrupt.

2.2.14 Interrupt source clear register

This register (PDMA_INT_REQ_CL: C008_0040H) requests clearing of interrupt sources. Only data of bits to which 1 is written is updated. Setting the bit corresponding to an interrupt source to 1 clears the interrupt source.

If setting an interrupt source due to the internal operation and clearing an interrupt source by writing to this register are performed at the same time, setting takes precedence.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							END CLR

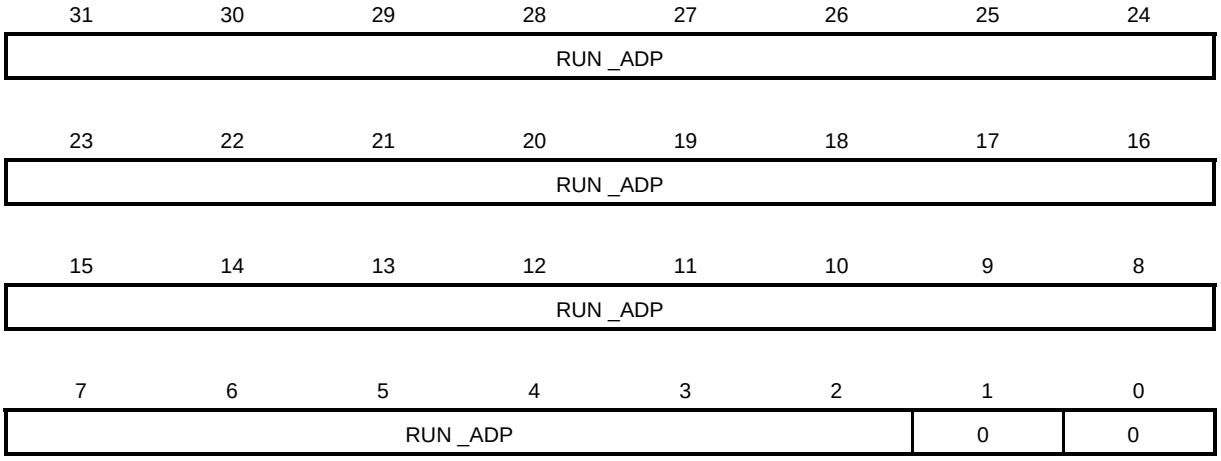
Name	R/W	Bit	After Reset	Function
Reserved	–	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
END CLR	W	0	0	Requests clearing of a transfer end interrupt source. 1: Clears the interrupt source.

2.2.15 Address pointer register (during transfer)

This read-only register (PDMA_RUN_ADP: C008_0050H) indicates the address used during DMA transfer. The address is shown as a 4-byte aligned address. The address is incremented in word units during DMA transfer.

Hardware operation:

This register shows the value of the address counter for the AHB bus interface of PDMA.



Name	R/W	Bit	After Reset	Function
RUN _ADP	R	31:0	0	Indicates the address used during DMA transfer, as a 4-byte aligned address. Therefore, the lower 2 bits are fixed to 0.

2.2.16 Error register

If the transfer start/reserve register (PDMA_CONT) is set to 1 when PDMA is in the reserved status, no transfer is executed and the OP_ERR bit of this register (PDMA_ERR: C008_0054H) is set to 1. Before making a reservation, confirm that PDMA is not in the reserved status by using the status register (PDMA_STATUS). Because this register is used for debugging, no interrupt is issued due to this error.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

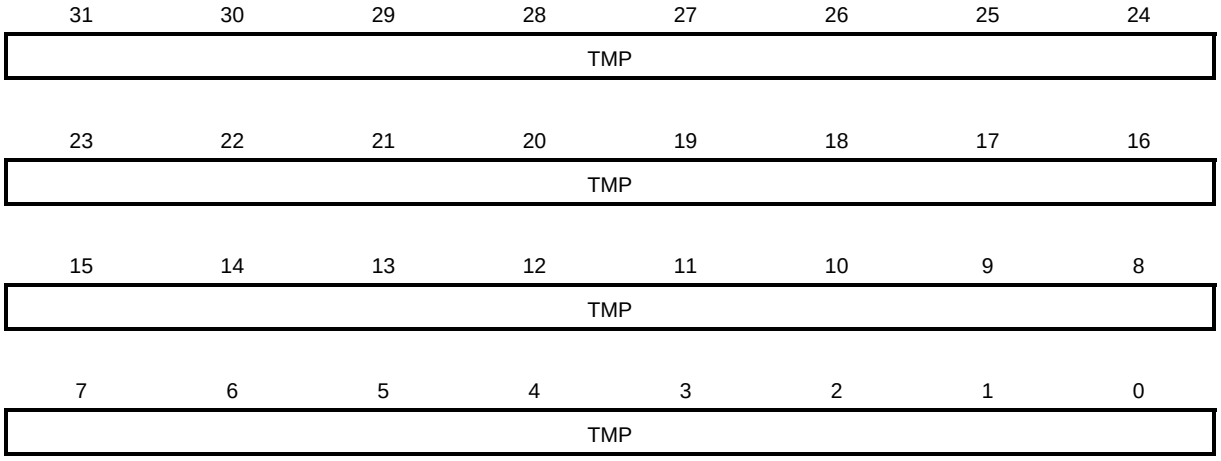
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							OP_ERR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
OP_ERR	R/W	0	0	This bit is set to 1 if the PDMA_CONT register is set to 1 when PDMA is in the reserved status. 0: No error 1: Error occurred
	W	0	–	1: Clears the error.

2.2.17 Temporary register

This temporary register (PDMA_TMP: C008_0058H) can be read or written freely by using software. It can be used for purposes such as reservation management.



Name	R/W	Bit	After Reset	Function
TMP	R/W	31:0	0	Any value can be written to and stored in these bits.

2.2.18 AXI address pointer register

This is a read-only register (PDMA_AXI_ADP: C008_005CH) for debugging that indicates the addresses of transactions in the AXI bus read interface. The address is shown as a 4-byte aligned address.

The address is incremented in doubleword units during DMA transfer.

Hardware operation:

This register shows the value of the address counter of the AXI bus read interface of PDMA.

31	30	29	28	27	26	25	24
AXI_ADP							

23	22	21	20	19	18	17	16
AXI_ADP							

15	14	13	12	11	10	9	8
AXI_ADP							

7	6	5	4	3	2	1	0
AXI_ADP					0	0	0

Name	R/W	Bit	After Reset	Function
AXI_ADP	R	31:0	0	Indicates the address used during transfer as a 4-byte aligned address. Therefore, the lower 3 bits are fixed to 0.

CHAPTER 3 DESCRIPTION OF FUNCTIONS

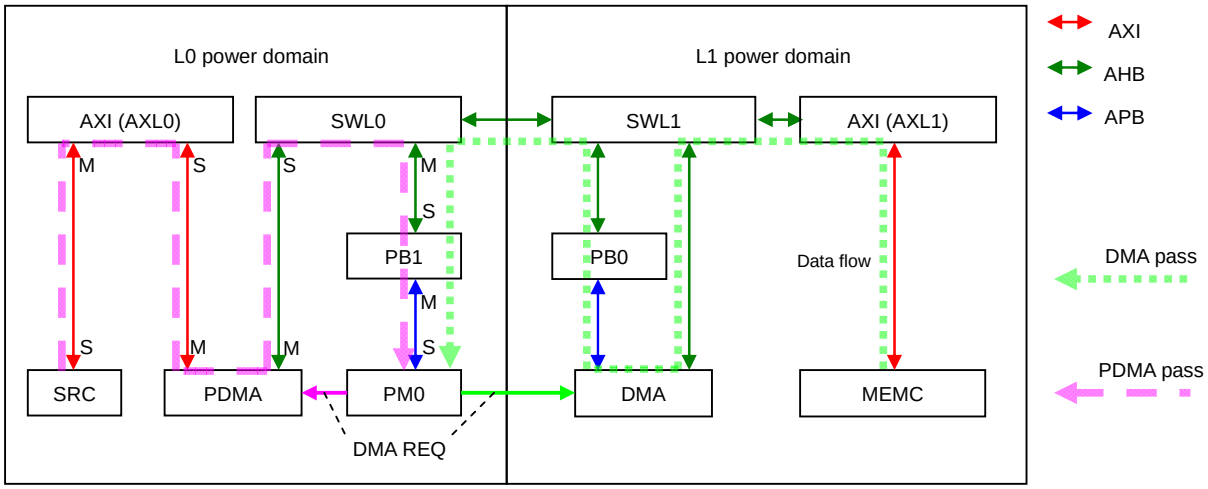
3.1 Power Domain and Data Flow

EM1 has an L0 power domain that is always on and an L1 power domain that can be turned on and off. Transfer to PM0 is performed by using PDMA or DMA. If PDMA is used with the L1 power domain off during a transfer, the leakage current can be reduced. If DMA is used, the L1 power domain must always be on.

To reduce the leakage current, the system must be designed so that the L1 power domain can be off as long as possible. In the following cases, the leakage current is reduced less.

The DMA transfer length is too short.
The system is designed so that processing is executed by processors in a short cycle.

Figure 3-1. Format Conversion Operation



3.2 Transfer Reservation

PDMA can reserve transfers. If transfers are reserved in advance, the next transfer starts automatically when a DMA transfer transaction ends. This eliminates the time lag that occurs during power supply control or interrupts and enables continuous data transfer to PM0. PDMA can also cancel reservations.

Specifying a transfer length that is too short ends the transfer before completion of the reservation and PDMA does not transition to the reserved status.

3.3 Power Supply Control and Interrupts

The L1 power domain is controlled by using the processors and the PMU module. If the L1 power domain is off, the PMU manages the system. When the PMU detects an interrupt, the L1 power domain is turned on.

The power of EM1 is designed to be restored only by interrupts issued by the ACPU. Controlling PDMA by using the ADSP must be performed using the sequence below. For details about power supply control, see the **Multimedia Processor for Mobile Application - One Chip User's Manual (S19268E)** and **System Control/ General-Purpose I/O Interface User's Manual (S19265E)**.

PDMA control sequence:

- Set up AINT to enable ACPU interrupts and disable ADSP interrupts.
- Turn off the L1 power domain.
- When PDMA issues a transfer end interrupt, the PMU turns on the L1 power supply, and the ADSP and ACPU start. (Here, the ADSP has already started and the bus is available.)
- The ACPU control jumps to the interrupt handler, searches for the interrupt source, and enables issuance of the ADSP interrupt.
- The relevant ADSP interrupt is issued.

PDMA detects interrupts based on the level. Therefore, design the system so that an interrupt occurs after the source of the previous interrupt is cleared. If clearing the source of an interrupt that has occurred takes a while, the next interrupt might not be detected correctly.

- When the ACPU searches for an interrupt source, the source of PDMA interrupts must be given a higher priority.
- Determine the transfer length, taking the overhead for power control and interrupts into consideration.

CHAPTER 4 USAGE

4.1 How to Control PDMA

The PDMA register setup procedure is described below.

- Example sequence from transfer start to end

<Start>
===== PDMA initialization =====
PDMA_DMA_SEL=0x1 select PDMA
PDMA_INT_ENABLE=0x1 interrupt enable
===== DMA setting =====
PDMA_RSV_ADD=Start address word address
PDMA_RSV_LENG=Length word
===== Start transfer =====
PDMA_CONT=0x1 start transfer
(Wait interrupt)
:
===== Interrupt occurred =====
PDMA_INT_REQ_CL=0x1 interrupt clear
<End>

- Example sequence from transfer start to reservation to transfer end to reservation to transfer end to transfer end

<Start>
===== PDMA initialization =====
PDMA_DMA_SEL=0x1 select PDMA
PDMA_INT_ENABLE=0x1 interrupt enable

===== DMA setting (transfer1) =====
PDMA_RSV_ADD=Start address word address
PDMA_RSV_LENG=Length word
===== Start transfer (transfer1) =====
PDMA_CONT=0x1 start

===== DMA setting (transfer2) =====
PDMA_RSV_ADD=Start address word address
PDMA_RSV_LENG=Length word

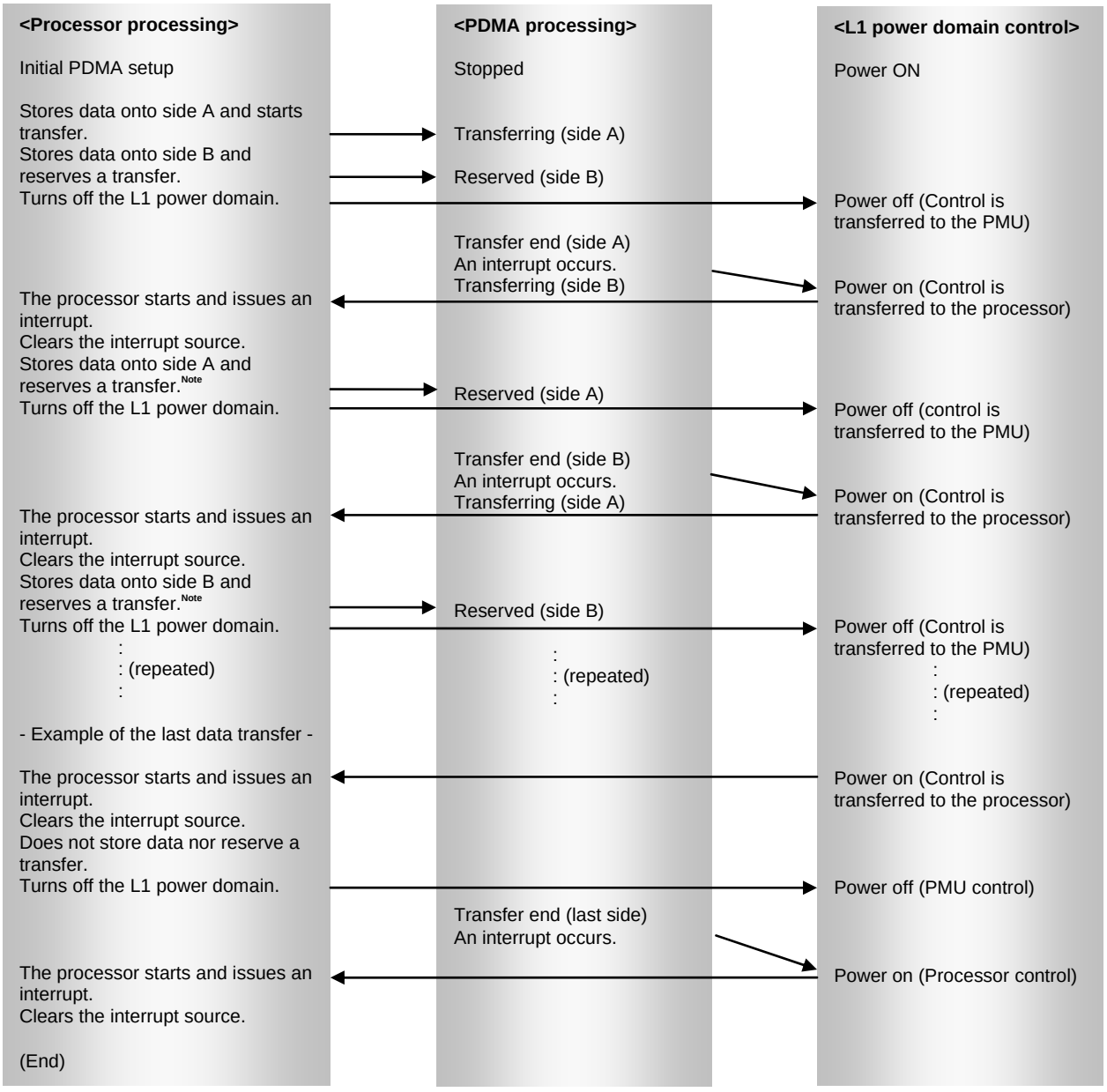
```
===== Reserve (transfer2) =====
If (PDMA_STATUS!=0x2)                    status check
PDMA_CONT=0x1                            reserve
(Wait interrupt)
        :
===== Interrupt occurred (transfer1) =====
PDMA_INT_REQ_CL=0x1                      interrupt clear

===== DMA setting (transfer3) =====
PDMA_RSV_ADD=Start address       word address
PDMA_RSV_LENG=Length                     word
===== Reserve (transfer3) =====
If (PDMA_STATUS!=0x2)                    status check
PDMA_CONT=0x1                            reserve
(Wait interrupt)
:
===== Interrupt occurred (transfer2) =====
PDMA_INT_REQ_CL=0x1                      interrupt clear
(Wait interrupt)
:
===== Interrupt occurred (transfer3) =====
PDMA_INT_REQ_CL=0x1                      interrupt clear
<End>
```

The control sequence that uses the PDMA transfer reservation function is shown below.

The sequence that stores data on two sides (sides A and B) of Internal SRAM and transfers it by making a reservation in advance is shown as a typical example.

Figure 4-1. Example Control Sequence



Note Make the reservation after confirming that PDMA has not been reserved.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0..

For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
http://www.cn.necel.com/

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

G0706