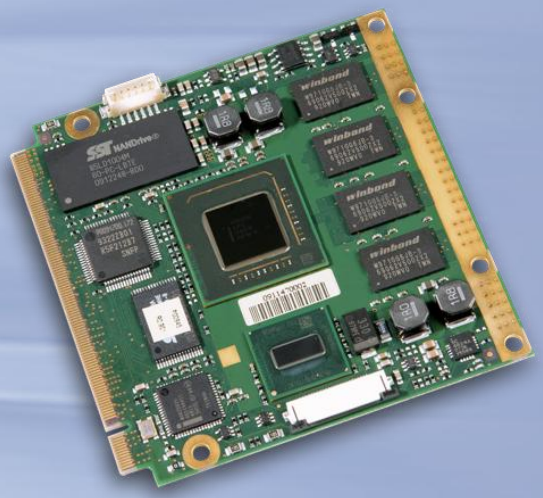
User's Manual



Q7-TCTC-FD

MSC Qseven™ Module

Rev. 1.7
October 11th, 2013

Preface

Copyright Notice

Important Information

This documentation is intended for qualified audiences only. The product described herein is not an end user product. It was developed and manufactured for further processing by trained personnel.

Disclaimer

Although this document has been generated with the utmost care no warranty or liability for correctness or suitability for any particular purpose is implied. The information in this document is provided "as is" and is subject to change without notice.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her owns expense.

Trademarks

All used product names, logos or trademarks are property of their respective owners.

Certification

MSC Vertriebs GmbH is certified according to DIN EN ISO 9001:2000 standards.

Life-Cycle-Management

MSC products are developed and manufactured according to high quality standards. Our life-cycle-management assures long term availability through permanent product maintenance. Technically necessary changes and improvements are introduced if applicable. A product-change-notification and end-of-life management process assures early information of our customers.

Product Support

MSC engineers and technicians are committed to provide support to our customers whenever needed.

Before contacting Technical Support of MSC Vertriebs GmbH, please consult the respective pages on our web site at www.mscembedded.com for the latest documentation, drivers and software downloads.

If the information provided there does not solve your problem, please contact our Technical Support:

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Content

1. General Information

1.1 Revision History

Rev.	Date	Description
1.0	April 27th, 2012	First released version
1.1	May 24th, 2012	Bios chapter updated
1.2	July 25th, 2012	EAPI support added
1.3	January 17th, 2013	SMBus address added
1.4	April 2nd, 2013	Updated Bios chapter
1.5	April 3rd, 2013	Pin description of THRM# corrected
1.6	June 19th, 2013	Added SDIO Card specification
1,7	October 11th, 2013	Corrected blind reset to default description

1.2 Reference Documents

[1] Qseven Specification
Revision 1.20
Last update: Aug. 12th 2010

[2] PCI Local Bus Specification Rev. 2.1
PCI21.PDF
Last update: June 1st, 1995
http://www.pcisig.com

[3] Serial ATA Specification
Serial ATA 1.0 gold.pdf
Last update: August 29th, 2002 Rev.1.0
http://www.sata-io.org/

[4] IEEE Std. 802.3-2002
802.3-2002.pdf
http://www.ieee.org

[5] Universal Bus Specification
usb_20.pdf
Last update: April 27th, 2000
http://www.usb.org

1.3 Introduction

Qseven modules are compact, highly integrated Single Board Computers.

Typically a Qseven module consists of a CPU, chipset, memory, Ethernet controller,

BIOS flash, SATA- and USB controller. Interface controllers or connectors (e.g. RJ45) are implemented on a base board on to which the Qseven module can be mounted.

In addition to the power supply PCIe, SATA, USB, LPC etc. interfaces are present on the connector.

Due to the standardized mechanics and interfaces the system can be scaled arbitrarily. Despite the modular concept the system design is very flat and compact.

Qseven modules require a carrier board to build a working system. For evaluation purposes MSC recommends the official Qseven Reference Platform MSC Q7-MB-RP2.

2 Technical Description

2.1 Key features

Core:

Processors:

Commercial Version:
Intel Atom E620 (600MHz)
Intel Atom E640 (1000GHz)
Intel Atom E660 (1300GHz)
Intel Atom E680 (1600GHz)

Industrial Temperature Version:
Intel Atom E620T (600MHz)
Intel Atom E640T (1000GHz)
Intel Atom E660T (1300GHz)
Intel Atom E680T (1600GHz)

Intel Platform Controller Hub EG20T:

Intel CS82TPCF

Memory:

DDR2-667/800, soldered on module
512MB,1GB or optionally up to 2GB

PCI Express Interface:

Three PCIe x1 V1.0 channels

Video:

The Intel ATOM processor E6xx/E6xxT series offers a single channel 80MHz LVDS interface (via Display Pipe A). This supports an 18 or 24 bpp single channel LCD panel.

Additionally the processor supports an SDVO-Interface (via Display Pipe B) with a maximum frequency of 160MHz. Multiple video interfaces can be supported over SDVO for example DisplayPort, HDMI, DVI as well as an additional higher resolution LVDS Interface.

With the single channel LVDS interface, display panels up to 1366x768 (60Hz) 18 or 24bpp can be supported.

Using the SDVO interface display resolutions up to 1920x1200 (60Hz) can be supported.

Ethernet:

The Intel Platform Controller Hub EG20T provides a Gigabit Ethernet MAC interface that conforms to IEEE802.3 and is connected to a Marvell 88E1118 PHY. The resulting Ethernet signals can be connected on the carrier board to a standard RJ45 10/100/1000 Base-T connector via isolation magnetics.

Audio:

The MSC Q7-TCTC-FD module supports the connection of High-Definition Audio Codecs.

USB:

The module provides six USB1.1/2.0 compliant Host Ports. These signals are connected to Port 0 and Ports 2-6.

The platform controller hub also supports one USB 2.0 Client controller. USB Port 1 is always configured as a USB Client port.

I2C Bus

The I2C-Interface integrated in the Intel platform controller hub is directly connected to the Qseven connector as described in the Qseven specification. Thus all EG20T I2C features are available on the carrier board.

- Philips I2C Bus Specification V2.1 conformed controller
- Standard mode 100kHz
- Fast mode 400kHz
- 7-bit/10-bit address

SMBus

The Intel Atom processor E6xx Series provide an SMBus 1.0-compliant host controller. The host controller provides a mechanism for the CPU to communicate with SMB peripherals (slaves).

LPC Bus

The processor implements a LPC-interface as described by the LPC1.1 Specification. Devices such as Super IO's are available for connection to this Bus.

TPM Support

For additional security functions a module variant assembled with a Trusted Platform Module can be ordered. The TPM device on the LPC-Bus is the Infineon SLB9635 TT 1.2 chip.

SATA / SATA SSD

The EG20T supports 2x SATA ports (SATA GEN1 and GEN2). If the optional SSD is assembled then only one SATA port is available on the carrier board.

Controller Area Network - CAN

The CAN interface from the EG20T is directly routed to the Qseven connector.

SPI - Interface of EG20T

A low cost high speed interface is available via the EG20T SPI-Interface. This interface can be used to connect microcontrollers or other SPI devices on the carrier board. The carrier board interface uses SPI_CS1. (The SPI-BIOS flash uses SPI_CS0).

SDIO/MMC:

The Intel Platform Controller Hub EG20T supports two SDIO/MMC interfaces. One interface is directly routed to the carrier board via the Qseven connector. The other interface is available on-module via a µSD-Card connector.

Supports SDIO Card Specification V1.1 and MMC System Specification 4.1.

BIOS:

AMI Aptio with TPM support.

Supports SPI-Flash on carrier board or on module.

EEPROM:

An SMBus EEPROM is implemented for backup of the CMOS data including user BIOS setup configuration.

Realtime Clock:

The MSC Q7-TCTC-FD provides two separate RTC's. The first one is integrated in the Tunnel Creek CPU and is referred to in this manual as the "internal RTC".

A second "external RTC" with lower power dissipation is also on the MSC Q7-TCTC-FD and connected via SMBus.

In the power off state only the external RTC is connected to VCC_RTC and buffered by the battery on the carrier board. The registers in the internal RTC will be cleared in the case of power loss.

The external RTC can be enabled in the BIOS Setup (see section 4.2.3.13). Setting time and date in the BIOS Setup affects the registers in the external RTC. The BIOS copies time and date values during reboot from the external RTC to the internal RTC.

Changing the time and date in the operating system affects only the internal RTC. The internal RTC will be synchronised with the external RTC if a clean OS shutdown is performed. In the event of a power fail whilst the OS is running, the internal RTC values will be lost and not synchronised.

The internal RTC is therefore only synchronised with the external RTC on start-up and clean shutdown of the module.

IEEE1588

The EG20T contains a clock synchronization block. This block supports the IEEE1588-2008 standard with IEEE1588 over Ethernet and IEEE1588 over CAN. In order to support/trigger a Snapshot event from the carrier board the signal FAN_TACHOIN/GP_TIMER_IN should be used.

Watchdog

The Intel Atom Processor E6xx Series supports a user configurable watchdog timer. It contains a selectable timer with timeouts of approximately 1us to 10min. When the Watchdog triggers, WDOUT signal is asserted. The Watchdog can be triggered from the carrier board using the WDTRIG# signal.

System Monitoring:

The Hardware Monitoring Chip is the EMC2104 on the SMBus.

Monitored values:

- Temperatures (CPU and Board)
- System fan speed

Power Management:

The module is capable of supporting suspend to RAM (S3) and suspend to disk (S4) power states, when used with an ACPI compliant operating system.

Thermal management:

The CPU used on the module has various thermal management schemes

Passive thermal management – this scheme uses clock throttling to modulate the CPU clock and so reduce the effective load on the CPU and therefore the power dissipated, as well as speed stepping to reduce the actual CPU frequency if needed.

For CPUs with commercial temperature range the throttling starts at a CPU temperature of approximately 90°C.

For CPUs with extended temperature range the throttling starts at a CPU temperature of approximately 110°C.

The hardware monitoring chip also provides a FAN_PWM output und FAN_TACHOIN input circuit for active cooling. These signals on the Qseven connector can be used to implement a FAN Control solution on the carrier board.

The CPU also includes a thermal trip circuit which forces a shutdown if the maximum CPU temperature is exceded.

SuperIO support:

The Bios supports the following Super IO chips:

Winbond 82627 HF

SMSC SCH3114-NU

EAPI support:

The MSC Q7-TCTC supports the Embedded Application Programming Interface.

For more information please contact MSC Technical Support

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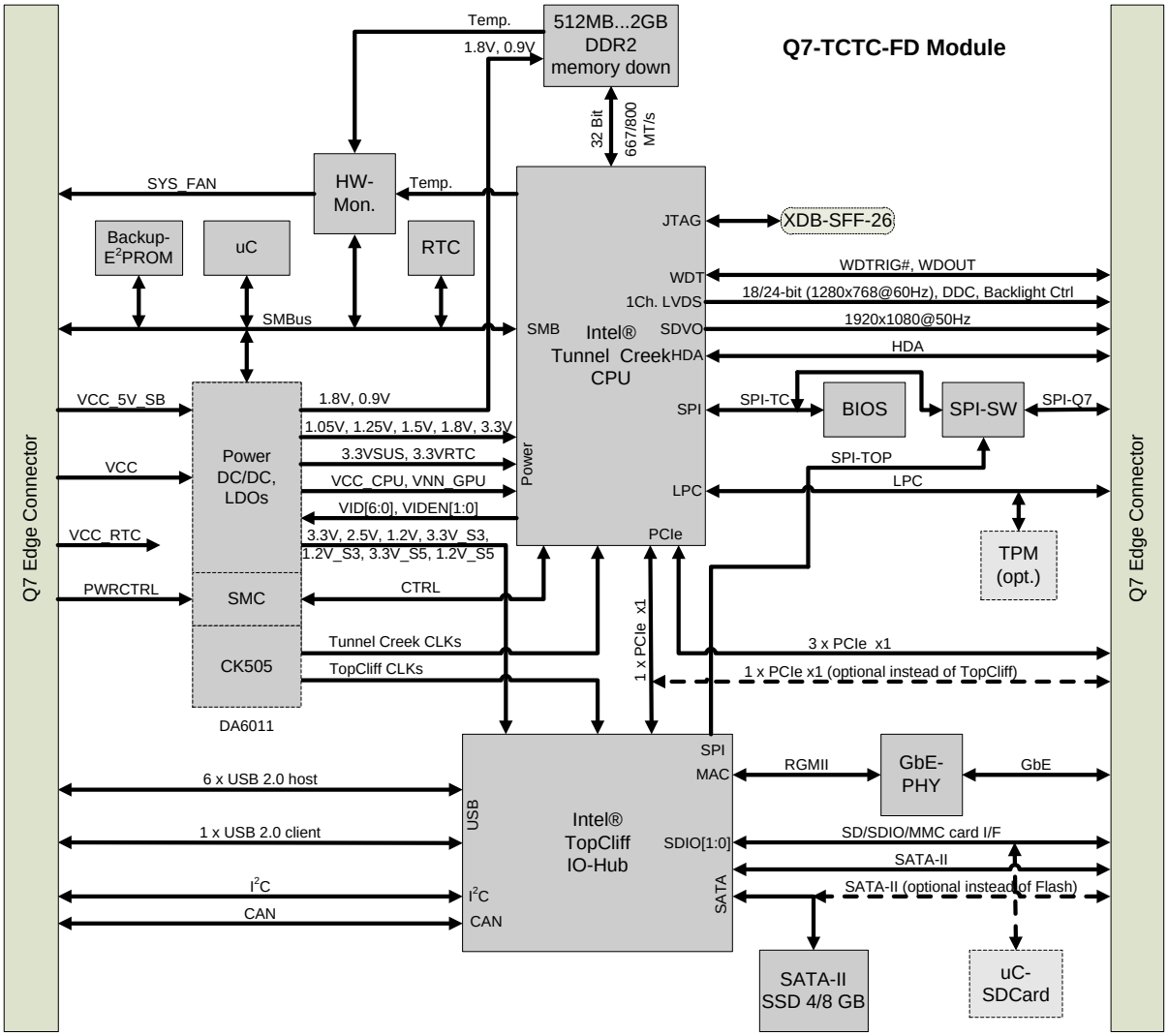
Fax: +49 - 8165 906 - 201
Email: support@mscembedded.com

2.2 Block diagram



MSC-Q7-TCTC-FD-xxx

SSD Flash is not populated on all module versions.

2.3 Power Supply

- **+5V primary power supply input**
- **+5V standby**
- **3.3V RTC power supply**
  BIOS SETUP data is stored in a non volatile backup memory device (EEPROM), therefore all configuration data (except for time and date) will be retained during RTC-Power loss. For the functional description of the external RTC see section 532.1.

Power Rail		
+5V	Voltage Range	+4.75V ... +5.25V
	Rate of Voltage Rising	< 250V/s
+5V Standby	Voltage Range	+4.75V ... +5.25 V
	Rate of Voltage Rising	< 250V/s
+3V RTC power supply in G3 (Mechanical Off)	Voltage Range	+2.0V ... +3.3V
	Current	typ. 275nA; max. 700nA

2.4 Power dissipation

Intel ATOM E620/E620T 600MHz, MSC Q7-TCTC-FD-102
RAM: 1GByte
SSD: no
Hardware Rev. 2.x / BIOS Rev. X2.00a

Testsoftware: Performance Test (from PassMark), SlotMachine (MSC DirectX Application)

		Idle	Calculation	Memory	Graphic	Graphic	Graphic
		Idle	Find prime Number	Block read	2D Graphic complex test	3D Graphic complex test	Slot Machine
DOS		4,5W					
Windows XP	S0	4,8W	5,1W	5,3W	5,6W	5,8W	5,9W
Windows XP	S3	0,4W					

Intel ATOM E640/E640T 1.0GHz, MSC Q7-TCTC-FD-105
RAM: 1GByte
SSD: no
Hardware Rev. 2.x / BIOS Rev. X2.00a

Testsoftware: Performance Test (from PassMark), SlotMachine (MSC DirectX Application)

		Idle	Calculation	Memory	Graphic	Graphic	Graphic
		Idle	Find prime Number	Block read	2D Graphic complex test	3D Graphic complex test	Slot Machine
DOS		4,8W					
Windows XP	S0	4,8W	5,5W	6,0W	5,9W	6,4W	6,4W
Windows XP	S3	0,4W					

Intel ATOM E660/E660T 1.3GHz, MSC Q7-TCTC-FD-106
RAM: 1GByte
SSD: no
Hardware Rev. 2.x / BIOS Rev. X2.00a

Testsoftware: Performance Test (from PassMark), SlotMachine (MSC DirectX Application)

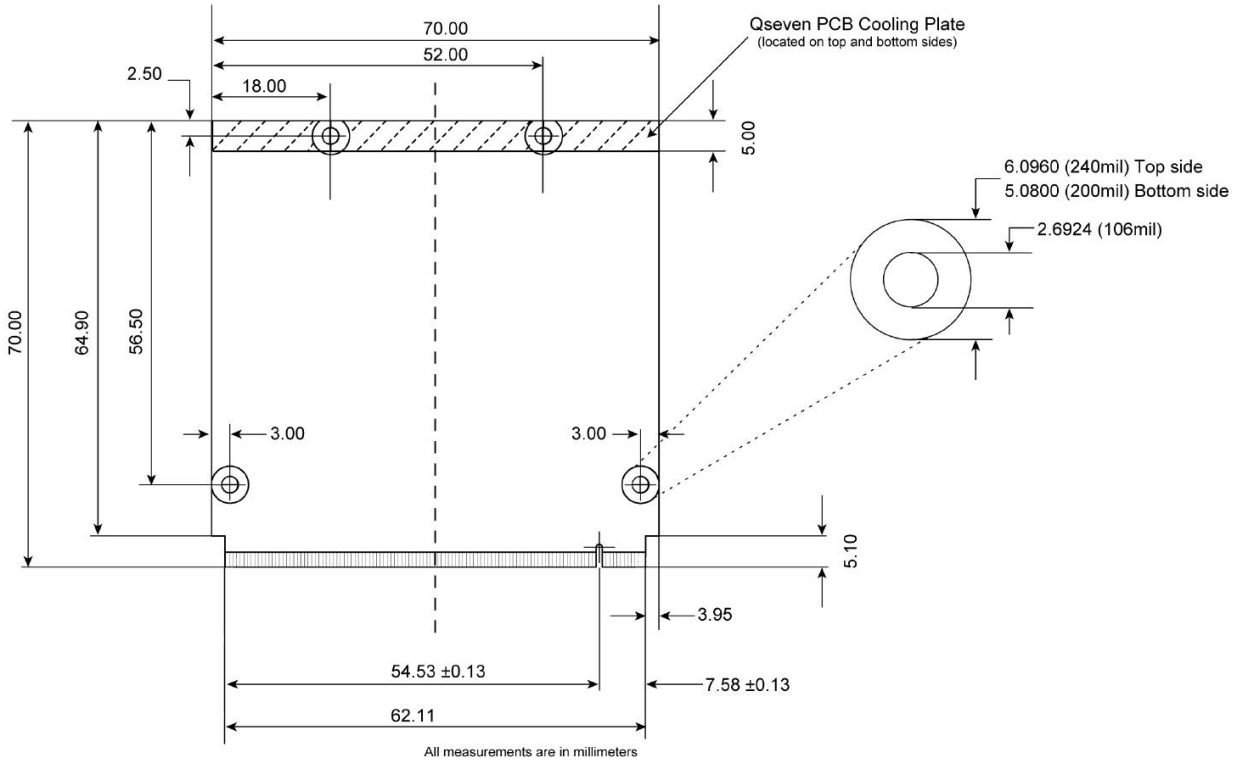
		Idle	Calculation	Memory	Graphic	Graphic	Graphic
		Idle	Find prime Number	Block read	2D Graphic complex test	3D Graphic complex test	Slot Machine
DOS		5,4W					
Windows XP	S0	5,1W	6,3W	6,9W	6,5W	7,0W	6,9W
Windows XP	S3	0,4W					

Intel ATOM E680/E680T 1.6GHz, MSC Q7-TCTC-FD-104
RAM: 1GByte
SSD: 4GB
Hardware Rev. 2.x / BIOS Rev. X2.00a

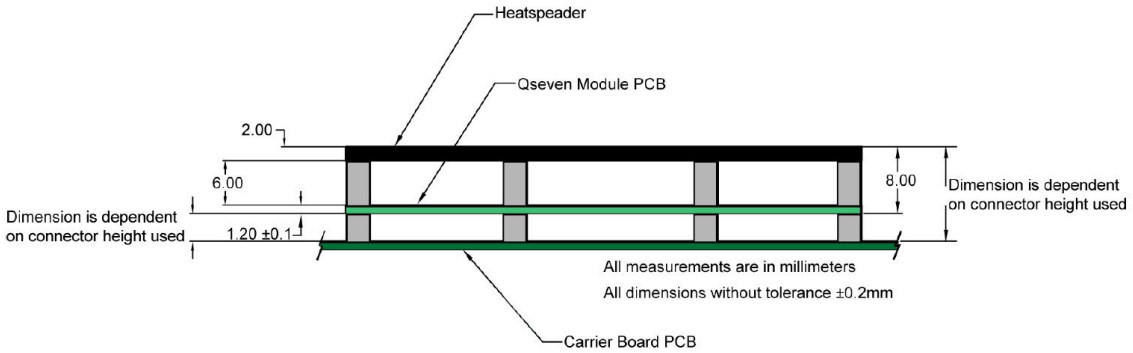
Testsoftware: Performance Test von PassMark + SlotMachine (MSC DirectX Application)

		Idle	Calculation	Memory	Graphic	Graphic	Graphic
		Idle	Find prime Number	Block read	2D Graphic complex test	3D Graphic complex test	Slot Machine
DOS		5,8W					
Windows XP	S0	5,1W	6,9W	7,5W	7,1W	7,7W	7,5W
Windows XP	S3	0,4W					

2.5 Mechanical Dimensions



Qseven Module Top Side



The overall height is dependent on the MXM-II connector used on the baseboard.

2.6 Thermal specifications

The cooling solution for a QSeven module is based on a heatspreader concept.

A heatspreader is a metal plate (typically aluminium) mounted on top of the module. The connection between this plate and the module components is typically made using thermal interface materials such as phase change foils, gap pads and copper or aluminium blocks. A very good thermal conductivity is required in order to transfer the heat from the CPU and the chipset to the heatspreader plate.

The heatspreader used by the MSC module is thermally attached using phase change materials and small aluminium blocks filling the gap between CPU and chipset dies and heatspreader plate.

The heatspreader is not a heatsink! It is a defined thermal interface for the system designer with fixed mechanical dimensions, so it should be possible to use different module types without problem. There must be a cooling solution for the system, the surface temperature of the heatspreader should not exceed 60°C

The main goal for the thermal design of a system is that each device on the module is operated within its specified thermal limits. There may be system implementations where the heatspreader temperature could be higher. In such a case the cooling solution design should be validated such that the thermal specifications of all the components on the module are not violated across the system operating temperature range even under worst case conditions.

2.7 Signal description

In the following tables signals are marked with the power rail associated with the pin, and for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different.

An additional label, "Suspend", indicates that the pin is active during suspend states (S3, S4, S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

2.7.1 High Definition Audio

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
HDA_RST#	Output	CMOS	Core	3.3V		Reset output to CODEC, active low.	E6xx
HDA_SYNC	Output	CMOS	Core	3.3V		48kHz fixed-rate, sample-synchronization signal to the CODEC(s).	E6xx
HDA_CLK	Output	CMOS	Core	3.3V		24.00 MHz serial data clock	E6xx
HDA_SDO	Output	CMOS	Core	3.3V		Serial TDM data output to the CODEC.	E6xx
HDA_SDI	Input	CMOS	Core	3.3V		Serial TDM data inputs from up to 3 CODECs.	E6xx

2.7.2 Ethernet

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	Input/ Output	Analog	3.3V Sus			Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. MDI[0]+/- B1_DA+/- MDI[1]+/- B1_DB+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	Marvell PHY
GBE0_ACT#	Output	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	Marvell PHY
GBE0_LINK#	Output	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 link indicator, active low.	Microcontroller
GBE0_LINK100#	Output	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	Microcontroller

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
GBE0_LINK1000#	Output	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	Microcontroller
GBE0_CTREF	REF			GND min 3.3V max		Marvell PHY: 1,8V	Marvell PHY

2.7.3 Serial ATA

If a flash disk is populated on the module then this will use the second SATA interface (SATA1) otherwise both SATA ports are available.

Signal	Pin Type	Signal Level	Power Rail	Remark	PU/PD	Description	Source / Target
SATA0_TX+ SATA0_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	EG20T
SATA0_RX+ SATA0_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	EG20T
SATA1_TX+ SATA1_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 1 transmit differential pair if no SATA SSD is assembled.	EG20T
SATA1_RX+ SATA1_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 1 receive differential pair if no SATA SSD is assembled.	EG20T
SATA_ACT#	O	CMOS	3.3V	3.3V		SATA activity indicator, active low.	EG20T

2.7.4 PCI Express Lanes

The module has 3 PCIe x1 lanes routed to the carrier board.

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PCIE_TX[0..2]+ PCIE_TX[0..2]-	O	PCIe	Core	AC coupled on module		PCI Express Differential Transmit Pairs 0	EG20T
PCIE_RX[0..2]+ PCIE_RX[0..2]-	I	PCIe	Core	AC coupled off module		PCI Express Differential Receive Pairs 0	EG20T

2.7.5 USB

The USB controller on the module supports USB 2.0 and USB 1.1. Seven ports are provided whereby Port 1 can only be used as a USB client.

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
USB[0,2..6]+ USB[0,2..6]-	I/O	USB	3.3V Sus	3.3V		USB differential pairs, USB Host only, channels 0-2-3-4-5-6	EG20T
USB1+ USB1-	I/O	USB	3.3V Sus	3.3V		USB Client only Port	EG20T
USB_0_1_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	EG20T
USB_2_3_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	EG20T

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
USB_4_5_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	EG20T
USB_6_7_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 6 and 7. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	EG20T
USB_CC	I	CMOS	3.3V Sus	3.3V	10k PD	USB external Host present pin	EG20T
USB_ID	I	CMOS	3.3V Sus	3.3V	100k PD	USB Host control select pin (not used by Design)	EG20T

2.7.6 LVDS Flat Panel

Single Channel 18bpp or 24bpp LVDS interface.

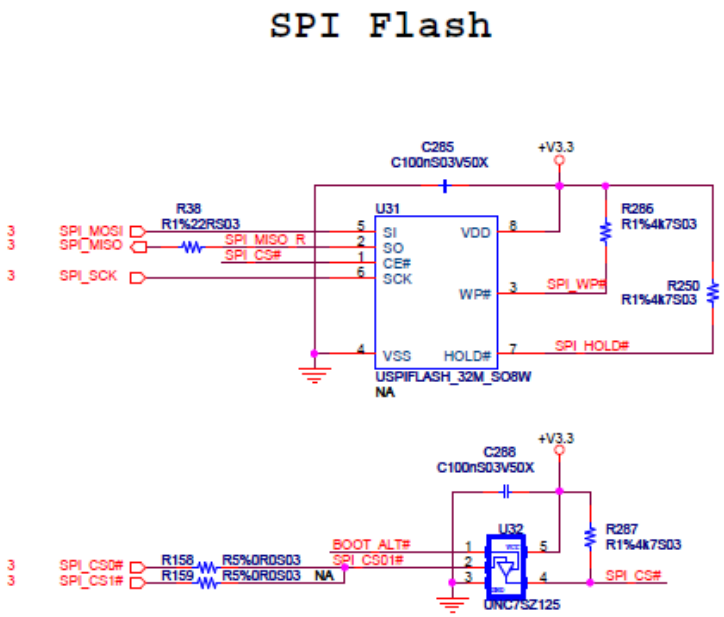
Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LVDS_A[0:3]+ LVDS_A[0:3]-	O	LVDS	Core			LVDS Channel A differential pairs	EG20T
LVDS_A_CK+ LVDS_A_CK-	O	LVDS	Core			LVDS Channel A differential clock	EG20T
LVDS_PPEN	O	CMOS	Core	3.3V		LVDS panel power enable	EG20T
LVDS_BLEN	O	CMOS	Core	3.3V		LVDS panel backlight enable	EG20T
LVDS_BKLT_CTRL	O	CMOS	Core	3.3V		LVDS panel backlight brightness control	EG20T
LVDS_BLC_CLK	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C clock output for external SSC clock chip use	EG20T
LVDS_BLC_DAT	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C data line for external SSC clock chip use	EG20T
LVDS_DID_CLK	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C clock output for LVDS display use	EG20T
LVDS_DID_DAT	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C data line for LVDS display use	EG20T

2.7.7 SPI Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SPI_MOSI	I/O	CMOS	3.3V	3.3V		Master Output Slave Input	E6xx/EG20T
SPI_MISO	I/O	CMOS	3.3V	3.3V		Master Input Slave Output	E6xx/EG20T
SPI_SCK	I/O	CMOS	3.3V	3.3V		Clock	E6xx/EG20T
SPI_CS0#	O	CMOS	3.3V	3.3V		When asserted low, the SPI peripheral is selected	E6xx
SPI_CS1#	I/O	CMOS	3.3V	3.3V		When asserted low, a SPI peripheral is selected	EG20T

2.7.7.1 SPI-Bus from the CPU E6xx

In order to boot the Qseven module the source for the boot device must be selected - either module BIOS or carrier board BIOS. A sample schematic for booting the module from the Qseven carrier board is shown below. BIOS_DISABLE# / BOOT_ALT# is the BIOS boot selection signal available on the Qseven connector. The MSC module uses SPI_CS0# for booting the BIOS.



2.7.7.2 SPI-Bus from the Platform Controller Hub EG20T

This SPI can be used to communicate with peripherals and external micro-controllers. In order to use this SPI interface the Qseven chip select signal SPI_CS1# must be used. For activating this interface the EG20T GPIO 11 must be set to logic "1". The EG20T GPIO11 has a 10k pull down resistor to prevent the signal floating.

BIOS_DISABLE#	EG20T GPIO11	Description / Signals on the Qseven connector	Source / Target
0	0	E6xx SPI at Qseven connector – Boot from carrier board (SPI_CS0# is active)	E6xx
0	1	Invalid configuration	-
1	0	E6xx SPI on Qseven connector – Boot from Module	E6xx
1	1	EG20T SPI on Qseven connector (SPI_CS1# active)	EG20T

2.7.8 LPC Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LPC_AD[0:3]	I/O	CMOS	Core	3.3V	20k PU	LPC multiplexed address, command and data bus	EG20T
LPC_FRAME#	O	CMOS	Core	3.3V		LPC frame indicates the start of an LPC cycle	EG20T
LPC_LDRQ#	I	CMOS	Core	3.3V	10k PU	LPC serial DMA request, not supported	EG20T
SERIRQ	I/O	CMOS	Core	3.3V	10k PU	LPC serial interrupt	EG20T
LPC_CLK	O	CMOS	3.3V	3.3V		LPC clock output - 33MHz nominal	EG20T

2.7.9 SDVO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDVO_RED+ SDVO_RED-	O	PCIe		AC coupled on module		Serial Digital Video red output differential pair	EG20T
SDVO_GREEN+ SDVO_GREEN-	O	PCIe		AC coupled on module		Serial Digital Video green output differential pair	EG20T
SDVO_BLUE+ SDVO_BLUE-	O	PCIe		AC coupled on module		Serial Digital Video blue output differential pair	EG20T
SDVO_BCLK+ SDVO_BCLK-	O	PCIe		AC coupled on module		Serial Digital Video clock output differential pair.	EG20T
SDVO_INT+ SDVO_INT-	I	PCIe		AC coupled off module		Serial Digital Video interrupt input differential pair.	EG20T
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I	PCIe		AC coupled off module		Serial Digital Video TVOUT synchronization clock input differential pair, **not supported**	EG20T

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDVO_FLDSTALL+ SDVO_FLDSTALL-	I	PCIe		AC coupled off module		Serial Digital Video Field Stall input differential pair, **not supported**	EG20T
SDVO_CTRL_CLK	I/O OD	CMOS	Core	3.3V	1M PU	SDVO I2C clock line - to set up SDVO peripherals.	EG20T
SDVO_CTRL_DAT	I/O OD	CMOS	Core	3.3V	1M PU	SDVO I2C data line - to set up SDVO peripherals.	EG20T

2.7.10 SDIO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDIO_DAT[0:7]	I/O	3.3V	Core	3.3V		SDIO Controller Data	EG20T
SDIO_CD#	I	3.3V	Core	3.3V		SDIO Controller Card Detect	EG20T
SDIO_CMD	I/O	3.3V	Core	3.3V	10k PU	SDIO Controller Command	EG20T
SDIO_CLK#	O	3.3V	Core	3.3V		SDIO Controller Clock	EG20T
SDIO_PWR#	I/O	3.3V	Core	3.3V		SDIO Controller Power enable	EG20T
SDIO_LED	O	3.3V	Core	3.3V		SDIO Controller transfer activity LED	EG20T
SDIO_WP	I	3.3V	Core	3.3V		SDIO Controller Write Protect	EG20T

2.7.11 Express card support

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
EXCD0_CPPE#	I	3.3V	Core	3.3V		Express card slot 0 card request	Microcontroller
EXCD0_PERST#	O	3.3V	Core	3.3V		Express card slot 0 reset	Microcontroller
EXCD1_CPPE#	I	3.3V	Core	3.3V		Express card slot 1 card request	Microcontroller
EXCD1_PERST#	O	3.3V	Core	3.3V		Express card slot 1 reset	Microcontroller

2.7.12 Miscellaneous

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
I2C_CLK	I/O	CMOS	3.3V	3.3V	2k PU	General purpose I2C port clock output	EG20T
I2C_DAT	I/O	CMOS	3.3V	3.3V	2k PU	General purpose I2C port data I/O line	EG20T

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SPKR	O	CMOS	3.3V	3.3V		Output for audio buzzer - the "speaker" in PC-AT systems	
BIOS_DISABLE#	I	CMOS	3.3V	3.3V	10k PU	Module BIOS disable input. Pull low to disable module BIOS.	
WDOUT	O	CMOS	3.3V	3.3V		Output indicating that a watchdog time-out event has occurred.	Microcontroller
WDTRIG#	I	CMOS	3.3V	3.3V	10k PU	Watchdog trigger input. This signal restarts the watchdog timer	Microcontroller
FAN_TACHOIN/GP_TIMER_IN	I	CMOS	3.3V		10k PU	Tachometer input	EMC2104 / EG20T
FAN_PWMOUT	O	CMOS	3.3V			Pulse width modulation output for fan speed control	EMC2104
CAN0_TX	O	CMOS	3.3V	3.3V	10k PU	CAN transmit data output	EG20T
CAN0_RX	I	CMOS	3.3V	5V	10k PU	CAN receive data input	EG20T

2.7.12.1 I2C-Bus

The I2C bus interface conforms to the version 2.1 I2C bus specification.

Note:

Please refer to the "Intel Platform Controller Hub EG20T – Integrated Circuit (I2C) Driver for Windows Programmers"

2.7.12.2 CAN-Bus

The EG20T CAN controller supports communication in accordance with BOSCH CAN Protocol Version 2.0B Active (standard format and extended format). The bit rate can be programmed to a maximum of 1MBits/s. To connect the CAN controller to the CAN bus, it is necessary to add a transceiver hardware on the Qseven Mainboard.

Note:

Please refer to the "Intel Platform Controller Hub EG20T – Control Area Network (CAN) Driver for Windows Programmers"

2.7.12.3 FAN_TACHOIN/GP_TIMER_IN

This signal is also connected to the Intel Platform Controller Hub (Topcliff) EG20T GPIO[1:0] and not only to the hardware monitoring chip EMC2104. This means that the signal can be used to make auxiliary snapshots in the IEEE1588 device.

Note:

Please refer to the "Intel Platform Controller Hub EG20T – IEEE1588 Hardware Assist Driver for Windows Programmer's Guide"

2.7.13 Power and System Management

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PWRBTN#	I	CMOS	3.3V Sus	3.3V	10k PU	Power button to bring system into a power state. (Negative pulse)	
RSTBTN#	I	CMOS	3.3V Sus	3.3V	10k PU	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release. (Negative pulse)	
SUS_STAT#	O	CMOS	3.3V Sus	3.3V		Indicates low power suspend operation	
SUS_S3#	O	CMOS	3.3V Sus	3.3V		Indicates system is in Suspend to RAM state. Active low output.	
SUS_S5#	O	CMOS	3.3V Sus	3.3V		Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.	
WAKE#	I	CMOS	3.3V Sus	3.3V	10k PU	External system wake up signal.	
THRM#	NC					Not supported by module.	
THERMTRIP#	O	CMOS	3.3V	3.3V		Active low output indicating that the CPU has entered thermal shutdown.	
SMB_CLK	I/O	CMOS		3.3V	2k PU	System management clock line	
SMB_DAT	I/O	CMOS		3.3V	2k PU	System management data line	
SMB_Alert	I/O	CMOS		3.3V	10k	System management bus alert input	
SLP_BTN#	I	CMOS		3.3V Sus	10k PU	Sleep button. Low active signal to bring the system in sleep state. (Negative pulse)	
LID_BTN#	I	CMOS		3.3V Sus	10k PU	LID button. Low active signal detect a LID switch to bring the system in sleep state or wake up again.(Low signal)	
BATLOW#	I	CMOS		3.3V Sus	10k PU	Battery low input indicates a external battery low state	
PWGIN	I	Low<0.6V High>0.8V		5V	120k PD	Indicates that the external power supply is ready	

2.7.13.1 BATLOW#

This signal is connected to the Intel Platform Controller Hub (Topcliff) EG20T GPIO9. The GPIO can be used as a general purpose I/O.
Features:

- Set as Input (Qseven Spec. conform)
- Set as Output (Qseven Spec. violation)
- capable of generating Interrupts (level/edge, positive logic/negative logic)

Note:
Please refer to the "Intel Platform Controller Hub EG20T – General Purpose Input Output (GPIO) Driver for Windows Programmer's Guide"

2.7.14 Power and GND

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
VCC_5V	Power		5V (±5%)			Primary power input: +5V (±5%)	Voltage Regulators
VCC_5V_SBY	Power		5V (±5%)			Standby power input: +5.0V (±5%) All available VCC_5V_SBY pins on the connector(s) shall be used. Used for microcontroller and standby and suspend functions. If no standby power is available connect to VCC_5V	VCC3.3V SUS regulator
VCC_RTC	Power					Real-time clock circuit-power input : +3.0V (+2.0V to +3.3V)	
GND	Power					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

2.8 Connectors

2.8.1 Module connector

Row A		Row B	
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
KEY		KEY	
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND

41	BIOS_DISABLE#	42	SDIO_CLK#
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5
53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	NC
57	GND	58	GND
59	HDA_SYNC	60	SMB_CLK
61	HDA_RST#	62	SMB_DAT
63	HDA_BITCLK	64	SMB_ALERT#
65	HDA_SDI	66	I2C_CLK
67	HDA_SDO	68	I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	NC	76	USB_P6-
77	NC	78	USB_P6+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5-	82	USB_P4-
83	USB_P5+	84	USB_P4+
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CL_PRES	92	USB_HC_SEL
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	LVDS_A0+	100	NC
101	LVDS_A0-	102	NC
103	LVDS_A1+	104	NC
105	LVDS_A1-	106	NC
107	LVDS_A2+	108	NC
109	LVDS_A2-	110	NC
111	LVDS_PPEN	112	LVDS_BLEN
113	LVDS_A3+	114	NC
115	LVDS_A3-	116	NC
117	GND	118	GND
119	LVDS_A_CLK+	120	NC
121	LVDS_A_CLK-	122	NC
123	LVDS_BLT_CTRL	124	RSVD
125	LVDS_DID_DAT	126	LVDS_BLC_DAT
127	LVDS_DID_CLK	128	LVDS_BLC_CLK

129	CAN0_TX	130	CAN0_RX
131	SDVO_BCLK+	132	SDVO_INT+
133	SDVO_BCLK-	134	SDVO_INT-
135	GND	136	GND
137	SDVO_GREEN+	138	SDVO_FLDSTALL+
139	SDVO_GREEN-	140	SDVO_FLDSTALL-
141	GND	142	GND
143	SDVO_BLUE+	144	SDVO_TVCLKIN+
145	SDVO_BLUE-	146	SDVO_TVCLKIN-
147	GND	148	GND
149	SDVO_RED+	150	SDVO_CTRL_DAT
151	SDVO_RED-	152	SDVO_CTRL_CLK
153	NC	154	NC
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	NC	162	NC
163	NC	164	NC
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	EXCD0_PERST#	172	EXCD1_PERST#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	EXCD0_CPPE#	178	EXCD1_CPPE#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0	186	LPC_AD1
187	LPC_AD2	188	LPC_AD3
189	LPC_CLK	190	LPC_FRAME#
191	SERIRQ	192	LPC_LDRQ#
193	VCC_RTC	194	SPKR
195	FAN_TACHOIN / GP_TIMER_IN	196	FAN_PWMOUT
197	GND	198	GND
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1#
203	SPI_SCK	204	RSVD
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC

215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

3 System resources

3.1 SMB Address Map

Device	A6	A5	A4	A3	A2	A1	A0	R/W̄	Address
DA6011 Power Mangement and Clock Chip	1	1	0	1	0	0	1	x	D2h / D3h *) 69h **)
CMOS backup EEPROM	1	0	1	0	1	0	0	x	A8h / A9h *) 54h **)
External RTC RX-8564LC	1	0	1	0	0	0	1	x	A2h / A3h *) 51h **)
Hardware Monitoring Chip EMC2104	0	1	0	1	1	1	1	x	5Eh / 5Fh *) 2Fh **)
Embedded Controller	1	1	0	0	0	0	0	x	C0h / C1h *) 60h **)

*) 8 bit address (with R/ W̄)
**) 7 bit address (without R/ W̄)

Warning: Please take care when using additional SMBus devices on the Qseven carrier board to ensure that there are no address conflicts.

For example the ATMEL AT24C16B has address conflicts with the external RTC and the CMOS backup EEPROM on the module.

3.2 PCI Express Lanes

Signal /Slot	Source
PCIE_TX[0] PCIE_RX[0]	PCIe-Channel 1 E6xx
PCIE_TX[1] PCIE_RX[1]	PCIe-Channel 2 E6xx
PCIE_TX[2] PCIE_RX[2]	PCIe-Channel 3 E6xx

3.3 USB

Signal	Source / Target	Remark
USB[0]+ USB[0]-	USB0 EG20T	USB1.1/2.0
USB[1]+ USB[1]-	USB EG20T	USB Client 1.1/2.0 supports high-speed und full-speed operations
USB[2]+ USB[2]-	USB1 EG20T	USB1.1/2.0
USB[3]+ USB[3]-	USB2 EG20T	USB1.1/2.0

Signal	Source / Target	Remark
USB[4]+ USB[4]-	USB3 EG20T	USB1.1/2.0
USB[5]+ USB[5]-	USB4 EG20T	USB1.1/2.0
USB[6]+ USB[6]-	USB5 EG20T	USB1.1/2.0
USB[7]+ USB[7]-	-	-

3.4 PCI Interrupt Routing Table

Qseven			Interrupts of Controller (TCTC)							
Slot Number (or Onboard Device)	**IDSEL # or DEV. #**	**Bus #**	**PIRQ 0 (INT A)**	**PIRQ 1 (INT B)**	**PIRQ 2 (INT C)**	**PIRQ 3 (INT D)**	**PIRQ 4 (INT E)**	**PIRQ 5 (INT F)**	**PIRQ 6 (INT G)**	**PIRQ 7 (INT H)**
Internal Graphic Device	Dev 02h	0	A							
HD Audio	Dev 27h Fkt 2	0	A							
PCI Express Root Port 0	Dev 17h Fkt 0	0	A							
PCI Express Root Port 1	Dev 18h Fkt 0	0	A							
PCI Express Root Port 2	Dev 19h Fkt 0	0	A							
PCI Express Root Port 3	Dev 1Ah Fkt 0	0	A							
USB UHCI Host Controller	Dev 2 Fkt 0	2				B				
USB UHCI Host Controller	Dev 2 Fkt 1	2				B				
USB UHCI Host Controller	Dev 2 Fkt 2	2				B				
USB EHCI Controller	Dev 2 Fkt 3	2				B				
USB Client	Dev Fkt 4	2				B				
USB UHCI Host Controller	Dev 8 Fkt 0	2	A							
USB UHCI Host Controller	Dev 8 Fkt 1	2	A							
USB UHCI Host Controller	Dev 8 Fkt 2	2	A							
USB EHCI Host Controller	Dev 8 Fkt 3	2	A							
SDIO1	Dev 4 Fkt 0	2			C					
SDIO2	Dev 4 Fkt 1	2			C					

Qseven			Interrupts of Controller (TCTC)							
Slot Number (or Onboard Device)	**IDSEL # or DEV. #**	**Bus #**	**PIRQ 0 (INT A)**	**PIRQ 1 (INT B)**	**PIRQ 2 (INT C)**	**PIRQ 3 (INT D)**	**PIRQ 4 (INT E)**	**PIRQ 5 (INT F)**	**PIRQ 6 (INT G)**	**PIRQ 7 (INT H)**
SATA	Dev 6 Fkt 0	2		D						
GB Lan Controller	Dev 0 Fkt 1	2	A							
DMA Controller 1	Dev 10 Fkt 0	2				B				
DMA Controller 2	Dev 12 Fkt 0	2			C					
SPI Controller	Dev 12 Fkt 1	2			C					
I2C Controller	Dev 12 Fkt 2	2			C					
CAN BUS Controller	Dev 12 Fkt 3	2			C					
IEEE1588 Controller	Dev 12 Fkt 4	2			C					
GPIO Controller	Dev 0 Fkt 2	2	A							
PCIe Bridge	Dev 0 Fkt 0	1	A							

3.5 IRQ Lines in Legacy IRQ Mode

IRQ#	Available	Typical Interrupt Source
0	No	Counter 0
1	No	Keyboard
2	No	Cascade Interrupt from Slave PIC
3	Yes	
4	Yes	
5	Yes	
6	Yes	
7	Yes	
8	No	RTC
9	Limited	In ACPI mode used for SCI
10	Yes	
11	Yes	
12	Yes	
13	No	Math coprocessor
14	Yes	
15	Yes	

3.6 IRQ Lines in APIC Mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	
1	No	Keyboard	
2	No	Cascade Interrupt from Slave PIC	
3	Yes		
4	Yes		
5	Yes		
6	Yes		
7	Yes		
8	No	RTC	
9	Yes	shared SCI	
10	Yes		
11	Yes		
12	No		
13	No	Math processor	
14	Yes		
15	Yes		
16	Yes		PIRQA
17	Yes		PIRQB
18	Yes		PIRQC
19	Yes		PIRQD
20	No		
21	No		
22	No		
23	No		

3.7 SDIO card support

Intel supports the SDIO with following specification:

• Conforms to SDHC, speed class 6
• Supports the following specifications:
— SD memory card: SD Memory Card Specifications Part 1 Physical Layer Specification Ver2.0
— SDIO card: SDIO Card Specification Ver1.10
— MMC: MMC System Specification Ver4.1
• Supports the following transfer modes:
— SD memory card/SDIO card
— SD bus transfer mode (1-bit/4-bit/high-speed)
— MMC transfer mode (1-bit/4-bit/8-bit/high-speed)
• Supports the SD option functions Stop at block gap, automatic clock stop, and Auto_CMD12
• Supports the SDIO option functions Suspend, resume, wake-up, and read wait
• Supports master interface (DMA) and slave interface
• Note on the ADMA function

4 BIOS

4.1 Introduction

This section describes the AMI Aptio Setup Startup screen and contains information on how to access Aptio setup to modify the settings which control AMI pre-OS (operating system) functions.

4.1.1 Startup Screen Overview

The AMI Aptio Startup screen is a graphical user interface (GUI) that is included in AMI Aptio products. The default bios behavior is to show an informational text screen during bios POST phase, but the graphical boot screen can be enabled in the bios setup. The standard boot screen is a black screen without any logo.

4.1.2 Activity Detection Background

While the Startup screen is displayed, press the Setup Entry key (DEL). The System acknowledges the input, and at the end of POST, the screen clears and setup launches.

4.2 Aptio Setup Utility

With the AMI Aptio Setup program, you can modify Aptio settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter provides an overview of the Setup utility and describes at a high-level how to use it.

4.2.1 Configuring the System BIOS

To start the AMI Aptio Setup utility, press [F2 or DEL] to launch Setup. The Setup main menu appears.

The BIOS Menu Structure

The BIOS Menu is structured as follows:

	Main
	MSC Board Info
	Hardware Monitoring Measurement
	Platform Information
	Advanced
	PCI Subsystem Settings
	ACPI Settings
	Trusted Computing
	CPU Configuration
	USB Configuration
	SDIO Configuration
	WB627 SIO Configuration / SMSC3114 SIO Configuration
	HWM EMC2104 Configuration
	Embedded Controller Features
	Tunnel Creek Watchdog
	Powermanagement Support
	Serial Port Console Redirection
	External RTC RX-8564
	Chipset
	North Bridge Chipset Configuration
	South Bridge Chipset Configuration
	IOH Configuration
	Boot
	Boot Options
	Security
	Save & Exit

The Menu Bar

The Menu Bar at the top of the window provides the following options :

Menu Items	Description
Main	Use this menu for basic system information.
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Chipset	Use this menu to set Chipset Features.
Boot	Use this menu to set the boot order in which the BIOS attempts to boot to OS.
Security	Use this menu to set User and Supervisor Passwords and the Backup and Virus-Check reminders.
Save & Exit	Saves and Exits the Aptio setup utility.

Use the left and right arrow keys on the keyboard to select a menu.

The Legend Bar

Use the keys listed in the legend bar on the right side of the screen to make selections, or to exit the current menu. The following table describes the legend keys and their alternatives:

Key	Function
Esc	Exit submenu / Exit Setup utility without saving..
Left and right arrow keys	Select Screen.
Up and down arrow keys	Select Item.
+/-	Change Option.
F1	General Help window.
F2	Previous Values
F3	Optimized Defaults
F4	Save and Exit

Select an item

To select an item, use the arrow keys to move the cursor to the desired field. Then use the plus-and-minus value keys to select a value for that field. Alternatively the Enter key can be used to select a value from a Pop Up menu. The Save Values commands in the Exit Menu saves the values currently displayed in all the menus.

Display a submenu

To display a submenu, use the arrow keys to move the cursor to the desired sub menu. Then press Enter. A pointer marks all submenus.

4.2.2 The Main Menu

The following selections can be made in the Main Menu. Use the sub menus for other options.

Feature	Options	Description
Bios Vendor	Informative	Shows the Bios Vendor
Core Version	Informative	Shows the Aptio Core Version
Project Version	Informative	Shows the Project Version
Build Date	Informative	Shows the Build Date
MRC Version	Informative	Shows the Memory Reference Code Version
Total Memory	Informative	Shows the total amount of Memory installed
MSC Board Info	Submenu	Shows board specific information
Platform Information	Submenu	Shows platform specific information.
System Language	English	Select the system default language
System Date	Enter Date (DD:MM:YYYY)	Set the system date on the real time clock.
System Time	Enter Time (HH:MM:SS)	Set the system time on the real time clock.
Access Level	Informative	This feature shows which user type has entered the Aptio setup. It depends on the Security Tab if a Adminstrator and/or User password is set.

4.2.2.1 MSC Board Info

Feature	Options	Description
Manufacturer	MSC-Vertriebs GmbH	
Board Name	Informative	Shows the board name
Board Revision	Informative	Shows the board revision
Bios Version	Informative	Shows the bios version
Serial Number	Informative	Shows the board serial number
Boot Counter	Informative	Shows how often board has booted
EC Bootloader Version	Informative	Shows the EC Bootloader version
EC Firmware Version	Informative	Shows the EC Firmware version
Onboard LAN MAC address	Informative	Shows the MAC address
UUID	Informative	Shows the UUID

4.2.2.2 Hardware Monitoring Measurement

Feature	Options	Description
CPU Temperature	Informative	Shows CPU Temperature
Chipset Temperature	Informative	Shows Chipset Temperature
System Temperature	Informative	Shows System Temperature
CPU Fan Speed	Informative	Shows Fan 1 Speed

4.2.2.3 Platform Information

Feature	Options	Description
Platform specific Version	Informative	Shows the platform name and version
PUNIT Build Date	Informative	Shows the PUNIT build date
PUNIT Build time	Informative	Shows the PUNIT build time

4.2.3 The Advanced Menu

Feature	Options	Description
Launch PXE OPROM	Disabled, Enabled	Enable or Disable Boot Option for Legacy Network Devices.
Launch Storage OPROM	Enabled, Disabled	Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.
PCI Subsystem Settings	Submenu	PCI, PCI-X and PCI Express settings
ACPI Settings	Submenu	System ACPI Parameters
Trusted Computing	Submenu	Trusted Computing (TPM) settings
CPU Configuration	Submenu	CPU Configuration Parameters
USB Configuration	Submenu	USB Configuration Parameters
SDIO Configuration	Submenu	SDIO Configuration Parameters
WB627 SIO Configuration	Submenu	WB627 SIO Configuration settings
HWM EMC2104 Configuration	Submenu	HWM EMC2104 settings
Tunnel Creek Watchdog	Submenu	Tunnel Creek Watchdog settings
Serial Port Console Redirection	Submenu	Serial Port Console Redirection settings
External RTC RX-8564	Submenu	External RTC settings

4.2.3.1 PCI Subsystem Settings Submenu

Feature	Options	Description
PCI ROM Priority	Legacy Rom, EFI Compatible ROM	This option allows the user to specify what PCI option ROM to launch in case of multiple options ROMs (Legacy and EFI Compatible) is available. Legacy ROM: Set this value to launch Legacy ROM EFI Compatible ROM: Set this value to launch Legacy ROM
PCI Latency Timer	32, 64, 96, 128, 260, 198, 192, 224, 248 PCI Bus Clocks	Set this value to change the PCI Bus clocks. Default is 32 PCI Bus clocks
VGA Palette Snoop	Disabled, Enabled	Enables or Disables VGA Palette Registers Snooping.
PERR# Generation	Disabled, Enabled	Enables or disables PCI Device generated PERR#.
SERR# Generation	Disabled, Enabled	Enables or disables PCI Device generated SERR#.
PCI Express settings	Submenu	PCI Express settings

4.2.3.2 PCI Express settings

Feature	Options	Description
Relaxed Ordering	Disabled, Enabled	Enables or disables PCI Express Device Relaxed Ordering.
Extended Tag	Disabled, Enabled	If enabled allows device to use 8-bit Tag field as a requester
No Snoop	Disabled, Enabled	Enables or disables PCI Express Device No Snoop option
Maximum Payload	Auto, 128, 256, 512, 1024, 2048. 4096 Bytes	Set maximum payload of PCI Express Device or allow system Bios to select the value
Maximum Read Request	Auto, 128, 256, 512, 1024, 2048. 4096 Bytes	Set read request size of PCI Express Device or allow system Bios to select the value
ASPM Support	Disabled, Auto, Force L0	Automatically enable ASPM based on reported capabilities and known issues **WARNING**: Enabling ASPM may

Feature	Options	Description
		cause some PCIe devices to fail
Extended Synch	Disabled, Enabled	If enabled allows generation of Extended Synchronization patterns.
Link Training Retry	Disabled, 2, 3, 5	Defines the number of retry attempts that software will take to retrain the link if previous training attempt was unsuccessful.
Link Training Timeout	Value	Defines number of microseconds. Software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000us.
Unpopulated Links	Keep Link ON, Disable Link	In order to save power, software will disable unpopulated PCI Express links, if this option is set to 'Disabled Link'.

4.2.3.3 ACPI Settings

Feature	Options	Description
Enable ACPI Auto Conf	Disabled, Enabled	Enables or disables Bios ACPI Auto Configuration.
Enable Hibernation	Disabled, Enabled	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not work with some OS's.
ACPI Sleep State	Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM)	Select the highest ACPI Sleep state the system will enter, when the Suspend button is pressed.
Lock Legacy Resources	Disabled, Enabled	Enables or Disables Lock of Legacy Resources

4.2.3.4 TPM

Feature	Options	Description
TPM Support	Disabled, Enabled	Enables or disables TPM support. OS will not show TPM. Reset of platform is required

4.2.3.5 CPU Configuration

Feature	Options	Description
CPU Feature Information	Informative	Shows information about the CPU (e.g CPU Speed, System BUS Speed)
Intel SpeedStep	Disabled, Enabled	Enable or Disable Intel® Speedstep™
Hyper-Threading	Disabled, Enabled	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).
Execute Disable Bit	Disabled, Enabled	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)
Limit CPUID Maximum	Disabled, Enabled	Disabled for Windows XP

Feature	Options	Description
Intel Virtualization	Disabled, Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Intel Virtualisation Technology
C-States	Disabled, Enabled	Enable or Disable C2 and above
Enhanced C1	Disabled, Enabled	Enable or disable Enhanced C1 State
Enhanced C2	Disabled, Enabled	Enable or disable Enhanced C2 State
Enhanced C3	Disabled, Enabled	Enable or disable Enhanced C3 State
Enhanced C4	Disabled, Enabled	Enable or disable Enhanced C4 State

4.2.3.6 USB Configuration

Feature	Options	Description
Legacy USB Support	Enabled, Disabled, Auto	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
EHCI Hand-off	Disabled, Enabled	This is a workaround for OS's without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.
USB transfer time-out	1, 5, 10, 15, 20 sec.	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10, 20, 30, 40 sec.	USB mass storage device Start Unit command time-out.
Device power-up delay	Auto, manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Device Power-up delay	1…40sec.	Delay range is 1..40 seconds, in one second increments

4.2.3.7 SDIO Configuration

Feature	Options	Description
SDIO Access Mode	Auto, DMA, PIO	Auto Option: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. DMA Option: Access SD device in DMA mode. PIO Option: Access SD device in PIO mode.

4.2.3.8 Winbond WB627 / SMSC3114 SuperIO Configuration (if available on carrier board)

Feature	Options	Description
COM A:	Disabled, Enabled	Enable or disable COM A
COM A Setting:	Auto, I/O 3F8h, IRQ 4 I/O 3F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 3E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12	Resource setting for COM A
COM B:	Disabled, Enabled	Enable or disable COM B

Feature	Options	Description
COM B Setting:	Auto, I/O 2F8h, IRQ 3 I/O 3F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 3E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12	Resource setting for COM B
COM C Setting:	Auto, I/O 3F8h, IRQ 4 I/O 3F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 3E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12	Resource setting for COM C **Note: only available for SMSC3114 SIO**
COM D Setting:	Auto, I/O 3F8h, IRQ 4 I/O 3F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2F8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 3E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12 I/O 2E8h, IRQ 3, 4, 5, 6, 7 ,8 ,10, 11, 12	Resource setting for COM D **Note: only available for SMSC3114 SIO**
LPT:	Disabled, Enabled	Enable or disable LPT on Winbond SIO

Feature	Options	Description
LPT Setting:	Auto, I/O 378h, IRQ 5, 7 I/O 278, IRQ 5, 7	Resource setting for LPT
LPT Mode:	SPP, EPP 1.9, ECP, ECP + EPP 1.9, Printer Mode, EPP 1.7, ECP+EPP 1.7	Mode setting for LPT

4.2.3.9 HWM EMC2104 Configuration

Feature	Options	Description
Fan 1 Settings	Manual, Temperature based	Defines how the fan should be controlled: manually set to a fixed duty cycle, or using a temperature-based control circuit.
Duty Cycle	Off, 40%, 60%, 80%, 100%	Set up the fan duty cycle for manual fan control.
Temperature Source	CPU, Memory, System	Select which channel should be the source temperature for the fan control.
Temperature Threshold1	1…120°C	Temperature Threshold (in degrees Celsius) at which the fan should be set to 40% duty cycle. At temperatures lower than this threshold, the fan will be off. **Note: For proper cooling it is recommended to set Treshold1 < Treshold2 < Treshold3**
Temperature Threshold2	1…120°C	Temperature Threshold (in degrees Celsius) at which the fan should be set to 70% duty cycle. **Note: For proper cooling it is recommended to set Threshold1 < Threshold2 < Threshold3**
Temperature Threshold3	1…120°C	Temperature Threshold (in degrees Celsius) at which the fan should be set to 100% duty cycle. **Note: For proper cooling it is recommended to set Threshold1 < Threshold2 < Threshold3**
Temperature Hysteresis	1…16°C	The hysteresis value (in degrees Celsius) that the temperature has to change before the fan speed is altered.

4.2.3.10 Embedded Controller Feature

Feature	Options	Description
Watchdog Start on Boot	Yes, No	Start the watchdog after Bios Post if enabled
Startup Delay Value	1s, 10s, 30s, 1min, 5min	Select the initial delay value. This is an additional one-time delay before the standard timeout timer is started.
Event Timeout Value	1s, 10s, 30s, 1min, 5min	Select the timeout value after which the watchdog will be executing its event action.
Reset Timeout Value	1s, 10s, 30s, 1min, 5min	Select the timeout value after which the watchdog will be executing its reset action. This timeout will start to countdown after the event timeout expired.
After Power Fail	Power On, Stay Off	Define the behavior of the system after a power failure.

4.2.3.11 Powermanagement Support

Feature	Options	Description
Spread Spectrum	Disabled, Down Spread 0.3%;1.0%;1.5% 2.0% Center Spread 0.3%;1.0%;1.5% 2.0%	Set up the spread spectrum value for the PLL1 output.

4.2.3.12 Serial Port Console Redirection

Feature	Options	Description
Com 0 Console Redirection	Disabled, Enabled	Console Redirection Enable or Disable
Console Redirection settings Com 0	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

Feature	Options	Description
Com1 Console Redirection	Disabled, Enabled	Console Redirection Enable or Disable
Console Redirection Settings Com1	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
Serial Port for Out-of Band Management/Windows Emergency Management Service (EMS) Console Redirection	Disabled, Enabled	Console Redirection Enable or Disable
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

4.2.3.12.1 Console Redirection Settings COM0/COM1 Submenu

Feature	Options	Description
Terminal Type	ANSI, VT100, VT100+, VT-UTF8	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600, 19200, 38400, 57600, 115200	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7, 8	Data Bits
Parity	None, Even, Odd, Mark, Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	1,2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Feature	Options	Description
Flow Control	None, Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Recorder Mode	Disabled, Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Disabled, Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection	80x24, 80x25	On Legacy OS, the number of rows and Columns supported redirection

4.2.3.12.2 Console Redirection EMS

Feature	Options	Description
Out-of-Band Mgmt Port	COM0, COM1	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
Terminal Type	ANSI, VT100, VT100+, VT-UTF8	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600, 19200, 38400, 57600, 115200	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Flow Control	None, Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Data Bits	7, 8	Data Bits
Parity	None, Even, Odd, Mark, Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	1,2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

4.2.3.13 External RTC

Feature	Options	Description
External RTC	Enabled, Disabled	To maintain time and date settings when powered off the external RTC must be enabled. If the system is permanently powered (S0-S5) or for battery-less systems use the internal RTC. **Note: See section on RTC for more details**

4.2.4 Chipset

Feature	Options	Description
North Bridge Chipset Configuration	Submenu	North Bridge Parameters
South Bridge Chipset Configuration	Submenu	South Bridge Parameters
IOH Configuration Options	Submenu	IOH Configuration settings

4.2.4.1 North Bridge chipset Configuration Submenu

Feature	Options	Description
Primary Display	Auto, IGD, PEG	Select which graphics controller to use as the primary boot display. IGD = Internal Graphics Device PEG = PCIe Graphics Device

Feature	Options	Description
Boot Device	LVDS, SDVO, Auto-SDVO DDC, Auto-SDVO Dvice	Use LVDS or SDVO VBIOS as Boot device or select auto detection methode. - Auto SDVO DDC: enables SDVO if DDC/EDID data is detected from CRT or DVI device. (Some devices may not support this eg. DDC-less device). - Auto SDVO Device: enables SDVO if SDVO chip is detected.
Boot Device Type	640x480 18bit, 800x600 18bit, 1024x768 18bit, 640x480 24bit, 800x480 18bit, 1024x600 18bit, 800x480 24bit, 800x600 24bit, 1024x768 24bit, 1280x800 24bit, 1366x768 24bit, Reserved, Reserved, 1280x800 18bit, 1366x768 18bit	Select LVDS Display type
LFP-Backlight Brightness	0-100%	Select the initial backlight brightness for the LVDS panel. **Note**: Graphics driver may change this brightness setting.
TV Standard	VBIOS default, e.g PAL, NTSC (due to size limitations these options are not listed here)	TV Standard
IGD Mode Select	Disabled, Enabled 4MB, Enabled 8MB, Enabled 16MB, Enabled 32MB, Enabled 64MB,	Select the amount of system memory used by the Integrated Graphics Device
MSAC Mode Select	Enabled 128 MB, Enabled 256 MB, Enabled 512 MB	Select the size of the graphics memory aperture and untrusted space. Used by the IGD.
DRAM Refresh Period	3,9us, 7,8us	Select the DRAM Refresh Period

4.2.4.2 South Bridge Chipset Configuration

Feature	Options	Description
Audio Controller	Auto, Disabled, Enabled	Audio Controller Options
Azalia PME Enable	Disabled, Enabled	Enable/Disable Intel HD Audio PME
Azalia Vci Enable	Disabled, Enabled	Enable/Disable Intel HD Audio Vci
SMBUS Controller [Enabled]	Disabled, Enabled	SMBUS Controller options
Serial IRQ Mode	Continuous, Quiet	Set the Serial IRQ Mode
High Precision Timer	Disabled, Enabled	Enable or disable the High Precision Timer (HPET)
PCI Express Ports Configuration	Submenu	Enable or Disable the PCI Express Ports in the Chipset
PPM Config	Submenu	PPM Config

4.2.4.3 PCI Express Ports Configuration

Feature	Options	Description
PCI Express Root Port 0	Enabled, Disabled	PCI Express Root Port 0 settings
PCI Express Root Port 1	Enabled, Disabled	PCI Express Root Port 1 settings
PCI Express Root Port 2	Enabled, Disabled	PCI Express Root Port 2 settings
PCI Express Root Port 3	Enabled, Disabled	PCI Express Root Port 3 settings
PCI-to-PCI Bridge	0..7	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

4.2.4.4 PPM Config

Feature	Options	Description
C-state POPUP	Enabled, Disabled	Enable/Disable C-State POPUP

4.2.4.5 IOH Configuration

Feature	Options	Description
Wake On Lan Configuration	Submenu	Wake On Lan Configuration settings
AHCI-SATA Configuration	Submenu	AHCI SATA Configuration settings

4.2.5 Wake On Lan Configuration

Feature	Options	Description
Wake on Lan	Disabled, Enabled, OS	Enable/Disable WOL
WOL Mode	Wake Up Frame	Select WOL Mode
WOL Speed	10 Mbps, 100Mbps, 1000Mbps	Select WOL Speed

4.2.6 AHCI SATA Configuration

Feature	Options	Description
Port 0	Enabled, Disabled	Enable/Disable Port 0. Set transfer Mode programming
Port 1	Enabled, Disabled	Enable/Disable Port 1. Set transfer Mode programming

4.2.7 Boot

Feature	Options	Description
Quiet Boot	Enabled, Disabled	Enables/Disables Quiet Boot option
Setup Prompt Timeout	0-65535sec	Number of seconds to wait for setup activation key. 65535(0xFFFF) indicates wait indefinitely.
Bootup NumLock State	On, Off	Select the keyboard NumLock state
Option ROM Messages	Force Bios, Keep current	Set display mode for Option ROM
Interrupt 19 Capture	Enabled, Disabled	Enabled: Allows Option ROMs to trap Int 19

Feature	Options	Description
Boot Option #1…	Device x	Set the System boot order Note: The number of available Boot options is dependent on the devices connected. Hard Drives must be set up explicitly in the Hard Drive BBS Priorities Submenu to appear in the Boot order.
Hard Drive BBS Priorities	Submenu	Set the order of the legacy devices in this group

Note: By pressing F10 during the POST, a Boot option Pop Up window will appear where the boot device can be selected from the available connected devices**.**

4.2.7.1 Hard Drive / Network / DVD BBS Priorities

Feature	Options	Description
Boot Option #1…	Device x	Set the Hard Drive / Network / DVD device which should be available in the boot options. Note: The number of available Boot options is dependent on the devices which are connected.

Note: any FAT16 or FAT32 Device will also appear as a UEFI Device. Select the UEFI device if you want to boot an EFI Shell or other EFI OS. For EFI Shell the correct path on the device must be /EFI/BOOT/BOOTIA32.efi.

4.2.8 Security

Feature	Options	Description
Administrator Password	Set Password	Set Setup Administrator Password
User Password	Set Password	Set User Password

4.2.9 The Save & Exit Menu

The following sections describe each of the options on this menu.

Save Changes and Exit

After making changes in the Setup menus, always select "Save changes and Exit/Reset". This procedure stores the selections displayed in the menus in a flash. The next time the computer is booted, the BIOS configures the system according to the Setup selections stored in the flash. Attempting to exit without saving, will cause the BIOS to prompt for confirmation whether you want to save before exiting. During boot-up, the Aptio BIOS attempts to load the values saved in the flash. If these values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can reset to the Default Values using the procedure described below or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Select this option to quit Aptio™ TSE without making any modifications to the system configuration.

Save Changes and Reset

When you have completed the system configuration changes, select this option to save the changes and reboot the system, so the new system configuration parameters can take effect.

Discard Changes and Reset

Select this option to quit Aptio™ TSE without making any modifications to the system configuration

Save Changes

Selecting "Save Changes" saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

Discard Changes

If, during a Setup Session, you change your mind about changes made and have not yet saved the values to CMOS, you can restore the values previously saved to CMOS.
Selecting "Discard Changes" on the Exit menu updates all the selections with their previous values.

Save as User Defaults

Save changes done so far as User defaults.

Restore User Defaults

Restore the User defaults to all the setup options.

Boot Override

Displays all the available boot options from the Boot Option List. User can select any of the options to select a particular device and boot directly from it.

Launch EFI Shell from filesystem device

Attempts to Launch EFI Shell application (Shell.efi) from one of the available file system devices. The shell.efi must be located on the devices root directory and the device must be formatted as FAT16 or FAT32. To exit the EFI Shell type exit to switch back to setup.

4.3 BIOS and Firmware Update

If a System-BIOS update is required please follow these instructions:

- **Bios Update from DOS:**

1.) Create a bootable DOS disk, USB Stick or hard disk.

2.) Copy the files "afudos.exe", "uefi.rom" and "update.bat" to this device.

3.) Boot the system from this device.

4.) Type "update" to update the System Bios.

5.) When the Bios update has finished, reboot the system.

- **Bios Update under Windows:**

1.) Copy the afuwingui.exe, amifldrv32.sys and the bios image uefi.rom to a storage media (e.g USB stick).

2.) Boot Windows XP or Windows 7.

3.) Copy the 3 files from your storage media to your Harddisk

4.) Run afuwingui.exe. Make sure that no other application is running to avoid crashes during the update procedure.

5.) Select "Open" and choose the bios image file uefi.rom.

6.) After it has opened, a new Tab Window will be displayed where you can choose what block options should be updated. To make sure all relevant updates will be updated, select "Program all Blocks". All Blocks should be marked now.

7.) Click the Button "Flash" and Bios update will start.

8.) After update is finished (all blocks are green), restart your system.

Note: The Amiflash tool for windows can be downloaded from www.ami.com

- **Bios Update from EFI Shell**

Create a FAT32 formatted removable device.

1.) Copy an EFI Shell (shell.efi) into the root directory of the device.

2.) Copy the files "Afuefi.efi", "uefi.rom" , "update.nsh" to this device.

3.) Enter System setup and under the menu bar "Save and Exit" choose Launch EFI Shell from filesystem device.

4.) After Shell is loaded, type:

- fs0:

- update.nsh

5.) When the Bios update has finished, reboot the system.

Note: If an EFI Shell is needed for Bios updates, please contact MSC Technical support.

The Embedded Controller Firmware will be updated automatically by the Bios Update. Embedded Controller Firmware will only be updated if the Bootloader is version 1.0 or later.

The actual EC Firmware version and Bootloader version can be checked in setup under Main/MSC Boardinfo.

Note: After the system has been updated, the setup settings will be changed to defaults and therefore it may be necessary to enter Setup to reconfigure the system settings.

4.4 Blind Restoration of Bios default settings (no display available)

- Power up the System
- Repeatedly press DEL for several seconds
- Press F3 for default settings or F2 for previous values.
- Press Enter
- Press F4
- Press Enter
- System will restart

4.5 Restore Bios settings from file

It is possible to save configured Bios settings and copy these settings to other boards which have the same Bios version.

- Configure the setup as required
- Load DOS or EFI Shell with afudos.exe (for DOS) or afuefi.efi (for EFI Shell).
- Run afudos.exe/afuefi.efi with following switch to save current Bios:
  Afudos.exe filename /o
  Afuefi.efi filename /o
- To copy these Bios settings onto another module run afudos.exe or afuefi.efi with following switch:
  Afudos.exe filename /n /R
  Afuefi.efi filename /n /R

  Only the Bios settings will be updated without flashing the complete Bios.

If complete Bios update is also needed, additional switches are needed :
Afudos.exe filename /p /b /n /x
Afuefi.efi filename /p /b /n /x

4.6 Post Codes

For Post Code information please contact MSC Technical Support
Phone: +49 - 8165 906 - 200
Fax: +49 - 8165 906 - 201
Email: support@mscembedded.com