RX630 Group

Reducing Power Consumption

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Abstract

This document describes a method of reducing power consumption for the RX630 Group.

Products

RX630 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Using the Module-Stop Function to Reduce Power Consumption 3
1.1 Peripheral Modules That Support the Module-Stop Function 3
1.2 Peripheral Modules That Do Not Support the Module-Stop Function 3
1.2.1 Settings When Not Using the Realtime Clock 3
1.2.2 When Not Using the Voltage Detection Circuit 3

2. Controlling Clocks to Reduce Power Consumption 4
2.1 Operating and Stopping Clocks 4
2.2 Clock Frequencies 4
2.3 Power Supply for the HOCO 4
2.4 Operating Power Consumption Control Modes 4
2.4.1 High-Speed Operating Mode 4
2.4.2 Low-Speed Operating Mode 1 4
2.4.3 Low-Speed Operating Mode 2 4
2.5 Correspondence Between the Operating Frequency and the Operating Power Consumption Control Modes 4

3. Using Low Power Consumption Modes to Reduce Power Consumption 5
3.1 Low Power Consumption Modes 5
3.1.1 Sleep Mode 5
3.1.2 All-Module Clock Stop Mode 6
3.1.3 Software Standby Mode 7
3.1.4 Deep Software Standby Mode 9
3.2 Correspondence Between the Time for Returning From a Low Power Consumption Mode and Power Consumption 11
3.3 Notes on Using Low Power Consumption Modes 12
3.3.1 DMAC and DTC Status When Transitioning to a Low Power Consumption Mode 12
3.3.2 BCLK Output When Using a Low Power Consumption Mode 12
3.3.3 Transitioning to a Low Power Consumption Mode During D/A Conversion 12
3.3.4 Transitioning to a Low Power Consumption Mode During A/D Conversion (S12AD and AD Modules) 12
3.3.5 Transitioning to a Low Power Consumption Mode During Data Transmission/Reception (SCI) 12

4. Other Processing 13
4.1 Handling of Unused Pins 13

5. Reference Documents 14

1. Using the Module-Stop Function to Reduce Power Consumption

The RX630 Group has a module-stop function that stops the supply of clocks to peripheral modules. Power consumption can be reduced by putting peripheral modules that are not used in the module-stop state.

1.1 Peripheral Modules That Support the Module-Stop Function

The module-stop can be set with module stop control registers (MSTPCRA to MSTPCRC) for each peripheral module. After a reset is canceled, all peripheral modules other than the DMAC, DTC, and RAM are placed in the module-stop state. Transition these modules to the module-stop state as needed.

- DMAC/DTC – Set the MSTPCRA.MSTPA28 bit to toggle the module-stop state.
- RAM0 – Set the MSTPCRC.MSTPC0 bit to toggle the module-stop state.
- RAM1 – Set the MSTPCRC.MSTPC1 bit to toggle the module-stop state.

1.2 Peripheral Modules That Do Not Support the Module-Stop Function

Some peripheral modules do not support the module-stop function. When not using these peripheral modules, their operation should be stopped.

1.2.1 Settings When Not Using the Realtime Clock

As registers in the realtime clock (RTC) are not initialized after a reset, values after a reset may cause unintentional interrupt requests to be generated, or as counters are operating, power consumption may increase.

When not using the RTC, follow the initialization process described in the user's manual to initialize the registers.

1.2.2 When Not Using the Voltage Detection Circuit

When not using the voltage detection circuit (LVD), set bits LVCMPCR.LVD1E and LVD2E to 0 (voltage detection 1 circuit disabled, and voltage detection 2 circuit disabled, respectively).

2. Controlling Clocks to Reduce Power Consumption

2.1 Operating and Stopping Clocks

Power consumption can be reduced by stopping as many of the following as possible – main clock oscillator, sub-clock oscillator, high-speed on-chip oscillator (HOCO), low-speed on-chip oscillator (LOCO), PLL circuit, and IWDT-dedicated on-chip oscillator. Refer to the user's manual for notes on stopping clocks.

2.2 Clock Frequencies

Power consumption can be reduced by lowering the frequencies of the following clocks – system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and the flash interface clock (FCLK). When clocks are not used (e.g. when not using the external bus), power consumption can be reduced by setting the frequency division ratio to 64 (the maximum frequency division ratio).

2.3 Power Supply for the HOCO

Set the HOCOPCR.HOCOPCNT bit to 1 to turn off the power supply of the HOCO.

2.4 Operating Power Consumption Control Modes

Power consumption can be reduced by selecting an appropriate operating power consumption control mode according to the clock, operating frequency, and operating voltage. The three operating power control modes in the RX630 Group are high-speed operating mode, low-speed operating mode 1, and low-speed operating mode 2.

When transitioning to another mode, follow the procedure in the user's manual in section 11.5.1 Setting Operating Power Consumption Control Mode to set the OPCCR register.

2.4.1 High-Speed Operating Mode

This mode allows high-speed operation. After a reset cancellation or recovery from software standby mode, the LSI is activated in this mode. Use the high-speed operating mode when a clock faster than 1 MHz is necessary.

2.4.2 Low-Speed Operating Mode 1

This mode consumes less power than the high-speed operating mode.

In this mode, ICLK, FCLK, PCLKB, and BCLK operate at 1 MHz or less. The PLL and HOCO cannot be used. Set the PLLCR2.PLLEN bit to 1 (PLL is stopped) and set the HOCOCR.HCSTP bit to 1 (HOCO is stopped). Program and erase operations of the flash memory are disabled.

2.4.3 Low-Speed Operating Mode 2

This mode consumes even less power than low-speed operating mode 1.

In low-speed operating mode 2, the ICLK, FCLK, PCLKB, and BCLK operate at 125 kHz or less, and the minimum operating frequency of the ICLK and FCLK is 32 kHz. The PLL and HOCO cannot be used. Set the PLLCR2.PLLEN bit to 1 (PLL is stopped) and set the HOCOCR.HCSTP bit to 1 (HOCO is stopped). Program and erase operations of the flash memory (ROM, E2 DataFlash) are disabled, and the E2 DataFlash cannot be read.

2.5 Correspondence Between the Operating Frequency and the Operating Power Consumption Control Modes

Table 2.1 lists the operating power consumption control modes and their maximum operating frequencies. Select an operating power consumption control mode appropriate to your operating frequency needs.

Table 2.1 Operating Frequency Limitations and Operating Power Consumption Control Modes

Operating Power Consumption Control Mode	Operating Frequency (ICLK)
High-speed operating mode	100 MHz max.
Low-speed operating mode 1	1 MHz max.
Low-speed operating mode 2	32 to 125 kHz

3. Using Low Power Consumption Modes to Reduce Power Consumption

3.1 Low Power Consumption Modes

The RX630 Group has four low power consumption modes to help reduce power consumption. Each mode drastically reduces the amount of power consumed, but as the operating status differs, special consideration should be given to each mode's specifications before creating the user program.

The Low Power Consumption Modes are listed in Table 3.1.

Table 3.1 Low Power Consumption Modes

Low Power Consumption Mode	Power Consumed
Sleep mode	More
All-module clock stop mode	↑
Software standby mode	↓
Deep software standby mode	Less

3.1.1 Sleep Mode

If the WAIT instruction is executed while the SBYCR.SSBY bit is set to 0 and the MSTPCRA.ACSE bit is set to 0, the MCU enters sleep mode.

Table 3.2 lists the Operating Status of Various Functions While the MCU is in Sleep Mode.

Table 3.2 Operating Status of Various Functions While the MCU is in Sleep Mode

Status	Function
Operating	• Main clock oscillator, sub-clock oscillator, HOCO, LOCO, PLL • IWDT-dedicated on-chip oscillator • RAM0, RAM1 • Flash memory • Peripheral modules (except for the CPU and WDT) • Power-on reset circuit • Bus controller • I/O ports
Stopped	• CPU • WDT

Figure 3.1 shows the Procedure to Enter Sleep Mode.

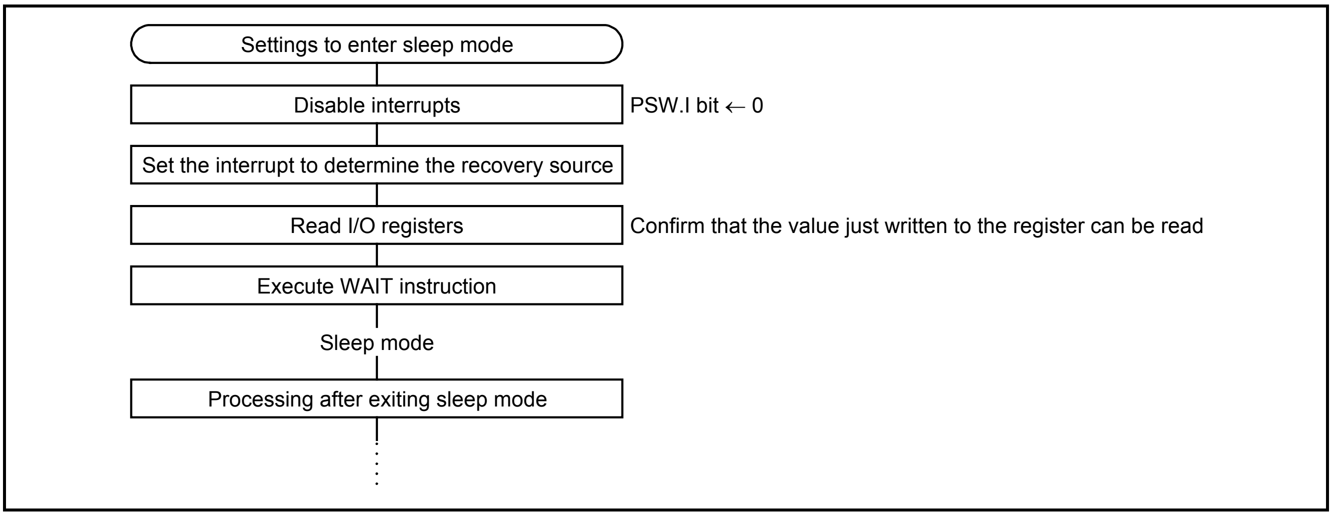


Figure 3.1 Procedure to Enter Sleep Mode

3.1.2 All-Module Clock Stop Mode

To enter all-module clock stop mode, set the MSTPCAR.ACSE bit to 1 and put modules controlled by registers MSTPCRA, MSTPCRB, and MSTPCRC in the module-stop state [1], set the SBYSC.SSBY bit to 0, then execute the WAIT instruction.

Note 1. Set the MSTPCRA register to FFFF FF[C-F]Fh, set the MSTPCRB register to FFFF FFFFh, and set bits MSTPCRC.MSTPC[31:16] to FFFFh.

Table 3.3 lists the Operating Status of Various Functions While the MCU is in All-Module Clock Stop Mode.

Table 3.3 Operating Status of Various Functions While the MCU is in All-Module Clock Stop Mode

Status	Function
Operating	• Main clock oscillator, sub-clock oscillator, HOCO, LOCO, PLL • IWDT-dedicated on-chip oscillator • Power-on reset circuit • LVD • TMR • RTC • IWDT • USB (USB resumption only)
Stopped	• CPU • RAM0 (data retained), RAM1 (data retained) • Flash memory • Peripheral modules (except those listed in the Operating row above) • Bus controller • I/O ports

Figure 3.2 shows the Procedure to Enter All-Module Clock Stop Mode.

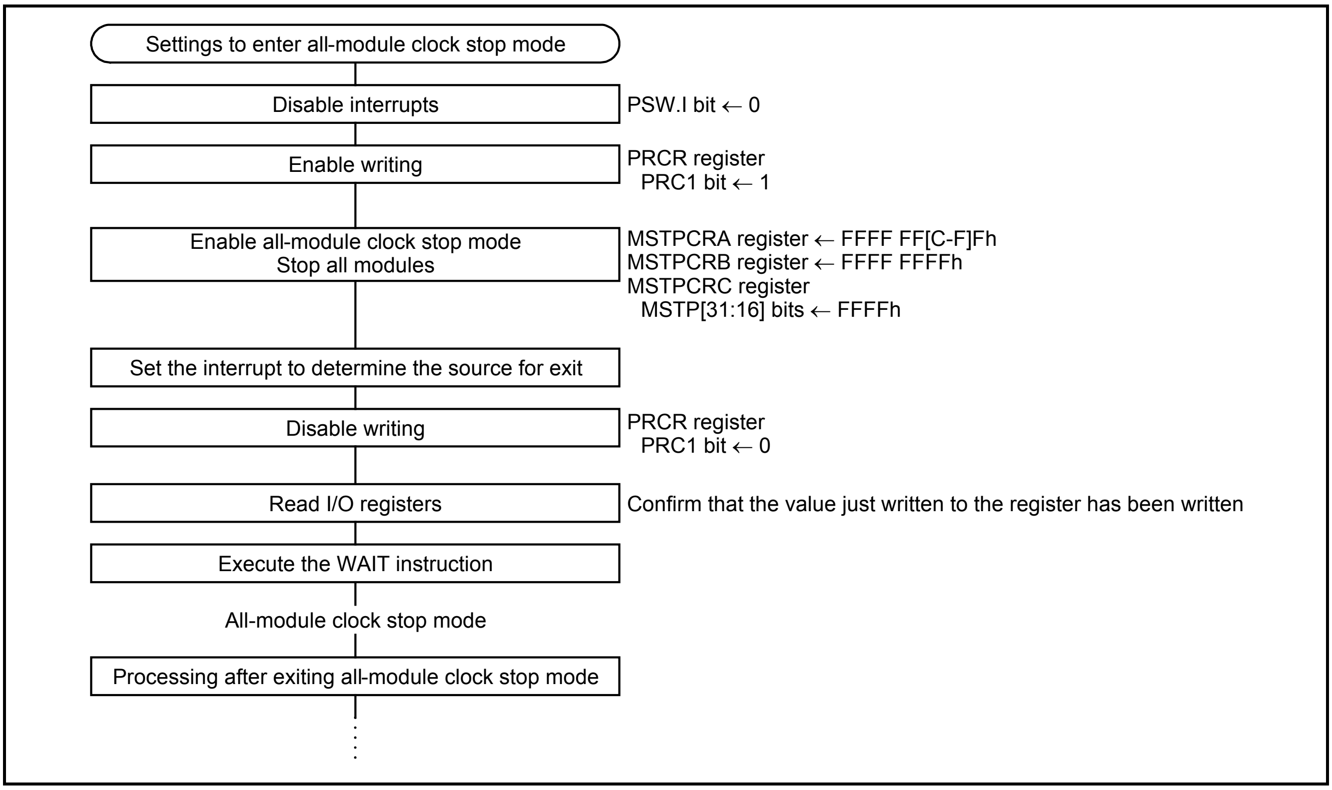


Figure 3.2 Procedure to Enter All-Module Clock Stop Mode

3.1.3 Software Standby Mode

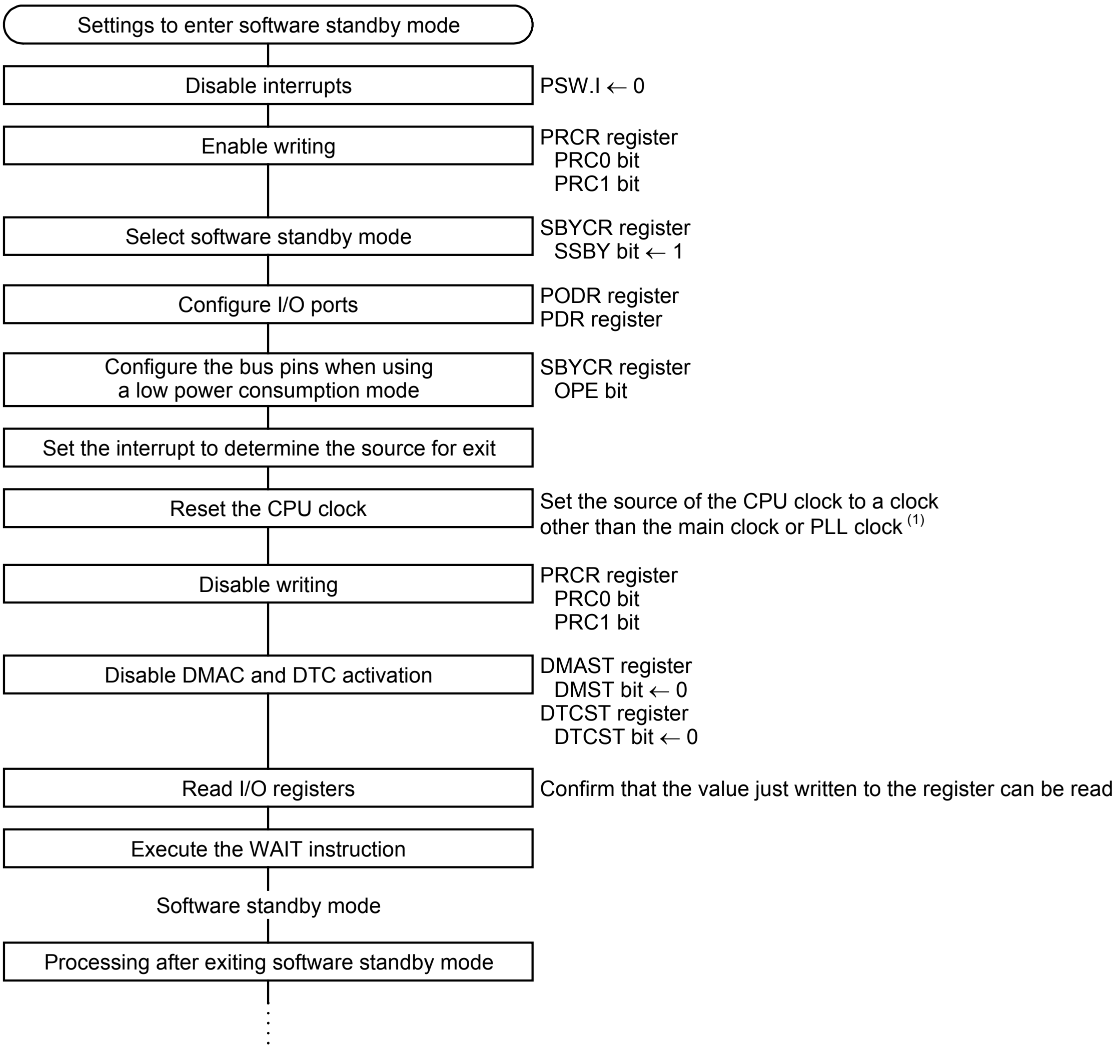
If the WAIT instruction is executed while the SBYCR.SSBY bit is set to 1 and the DPSBYCR.DPSBY bit is set to 0, the MCU enters software standby mode.

Table 3.4 lists the Operating Status of Various Functions While the MCU is in Software Standby Mode.

Table 3.4 Operating Status of Various Functions While the MCU is in Software Standby Mode

Status	Function
Operating	• Main clock oscillator, sub-clock oscillator, IWDT-dedicated on-chip oscillator • IWDT • RTC • LVD • Power-on reset circuit
Stopped	• CPU • HOCO, LOCO, PLL • RAM0 (data retained), RAM1 (data retained) • Flash memory • Peripheral modules (except those listed in the Operating row above) • Bus controller • I/O ports

Figure 3.3 shows the Procedure to Enter Software Standby Mode.



Note 1: For products with ROM capacities of at least 1.5 MB or products with at least 176 pins, when selecting the main clock oscillator or PLL circuit as the clock source for the ICLK, the MCU will not enter software standby mode even if the WAIT instruction is executed. Switch the clock source to the LOCO, HOCO, or sub-clock oscillator and then execute the WAIT instruction.

Figure 3.3 Procedure to Enter Software Standby Mode

3.1.4 Deep Software Standby Mode

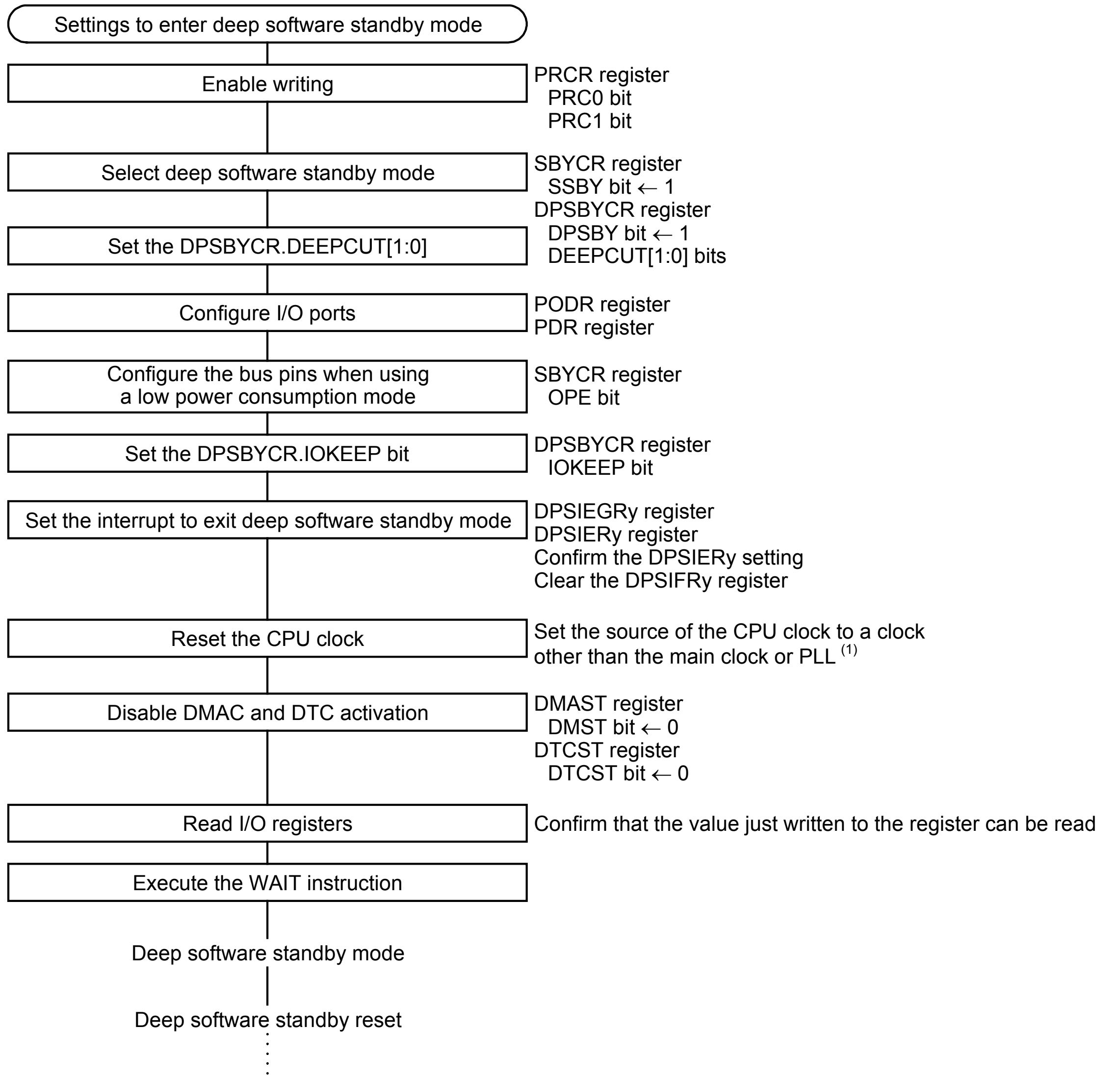
If the WAIT instruction is executed while the SBYCR.SSBY bit is set to 1 and the DSPBYCR.DPSBY bit is set to 1, the MCU enters deep software standby mode.

Table 3.5 lists the Operating Status of Various Functions While the MCU is in Deep Software Standby Mode.

Table 3.5 Operating Status of Various Functions While the MCU is in Deep Software Standby Mode

Status	Function
Operating	• Main clock oscillator, sub-clock oscillator • Power-on reset circuit • LVD • RTC • USB (only the USB suspend/resume detecting unit)
Stopped	• CPU • HOCO, LOCO, IWDT-dedicated on-chip oscillator, PLL • RAM1 (data undefined), RAM0 (data retained) While in deep software standby mode, data retention can be selected by setting the DPSBYCR.DEEPCUT[1:0] bits. • Flash memory • Peripheral modules (except those that are operating) • Bus controller • I/O ports

Figure 3.4 shows the Procedure to Enter Deep Software Standby Mode.



Note 1. For products with ROM capacities of at least 1.5 MB or products with at least 176 pins, when selecting the main clock oscillator or PLL circuit as the clock source for the ICLK, the MCU will not enter software standby mode even if the WAIT instruction is executed. Switch the clock source to the LOCO, HOCO, or sub-clock oscillator and then execute the WAIT instruction.

Figure 3.4 Procedure to Enter Deep Software Standby Mode

3.1.4.1 DEEPCUT[1:0] Bits

When the MCU is in deep software standby mode, the DPSBYCR.DEEPCUT[1:0] bit setting controls the power supply to the RAM and USB resume detecting unit, and also controls the LVD and power-on reset circuit.

Refer to the user's manual for more information on settings these bits.

3.2 Correspondence Between the Time for Returning From a Low Power Consumption Mode and Power Consumption

The time for returning from a low power consumption mode is dependent which low power consumption mode the MCU entered, and the ICLK before the MCU entered the aforementioned low power consumption mode. Use a low power consumption mode appropriate to the specifications of the user program.

Table 3.6 lists the Correspondence Between the Time for Returning From a Low Power Consumption Mode and Power Consumption.

Table 3.6 Correspondence Between the Time for Returning From a Low Power Consumption Mode and Power Consumption

Low Power Consumption Mode	Return Time (1)	Power Consumption
Sleep mode	Short	More
All-module clock stop mode	↑	↑
Software standby mode	↓	↓
Deep software standby mode	Long	Less

Note 1: This column shows a comparison of the ICLK in any mode before entering a low power consumption mode.

3.3 Notes on Using Low Power Consumption Modes

3.3.1 DMAC and DTC Status When Transitioning to a Low Power Consumption Mode

When entering the all-module clock stop mode, software standby mode, or deep software standby mode, set the DMAST.DMST bit to 0 (DMAC activation is disabled) and set the DTCST.DTCST bit to 0 (DTC module-stop).

For more information, refer to section 18.6 Low-Power Consumption Function and section 19.8 Low-Power Consumption Function in the user's manual.

3.3.2 BCLK Output When Using a Low Power Consumption Mode

When the external bus is enabled and the SCKCR.PSTOP1 bit is 0 (BCLK pin output is enabled), BCLK output is stopped in software standby mode and deep software standby mode, and the BCLK pin outputs a high, but BCLK output is not stopped in sleep mode or all-module clock stop mode.

When BCLK is output, power consumption increases, so if BCLK output is not needed while the MCU is in sleep mode or all-module clock stop mode, set the PSTOP1 bit to 1 (BCLK pin output is disabled (always output the high level) before entering sleep mode or all-module clock stop mode.

3.3.3 Transitioning to a Low Power Consumption Mode During D/A Conversion

When the RX630 Group enters the module-stop state or software standby mode with D/A conversion enabled, the analog outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current has to be reduced in the module-stop state or software standby mode, disable analog output by setting bits DACR.DAOE1, DAOE0, and DAE to 0.

When the MCU enters deep software standby mode, the analog output pin is placed in a high-impedance state.

For details, refer to section 40.4.3 Operation of the D/A Converter in Software Standby Mode in the user's manual.

3.3.4 Transitioning to a Low Power Consumption Mode During A/D Conversion (S12AD and AD Modules)

If the MCU enters the module-stop state with A/D conversion enabled, the analog power supply current is the same as during A/D conversion. If the module-stop function must be used to reduce the analog power supply current, stop A/D conversion by setting the ADCSR.ADST bit to 0.

For details, refer to section 38.5.5 Notes on Entering Low Power Consumption States and section 39.6.4 Notes on Entering Power-Down States in the user's manual.

3.3.5 Transitioning to a Low Power Consumption Mode During Data Transmission/Reception (SCI)

Set the SCR.TIE, TE, RE, and TIEI bits to 0 before configuring the module-stop state and before transitioning to software standby mode. Setting the TE bit to 0 resets registers TSR, TDR, and SSR.

When modules are in the module-stop state and when the MCU is in software standby mode, the status of output pins is dependent on the port settings, and the pins output a high when the module-stop states and software standby mode are canceled.

When the MCU enters a low power consumption mode while data is being transmitted, the data being transmitted becomes undetermined. When the MCU enters a low power consumption mode while data is being received, the data being received becomes invalid.

4. Other Processing

4.1 Handling of Unused Pins

Unused pins should be connected as listed in Table 4.1.

Table 4.1 Handling of Unused Pins

Classification	Pin	I/O	Connect To
Battery backup function	VBATT	Input	Connect this pin to VCC.
Analog power supply	AVCC0	Input	Connect this pin to VCC.
	AVSS0	Input	Connect this pin to VSS.
	VREFH0	Input	Connect this pin to VCC.
	VREFL0	Input	Connect this pin to VSS.
	VREFH	Input	Connect this pin to VCC.
	VREFL	Input	Connect this pin to VSS.
USB	USB0_DP	Input	Keep the pin open.
	USB0_DM	Input	Keep the pin open.
	VCC_USB	Input	Connect this pin to VCC.
	VSS_USB	Input	Connect this pin to VSS.
Clock	XCIN	Input	Connect this pin to VSS through a resistor (pull down).
	XCOUT	Output	Keep the pin open.
	EXTAL	Input	Connect this pin to VSS through a resistor (pull down).
	XTAL	Output	Keep the pin open.
Interrupt	NMI	Input	Connect this pin to VCC through a resistor (pull up).
I/O ports	Pxx	I/O	For general I/O port pins, set the input direction, and connect each pin to VCC through a resistor (pull up), or connect each to VSS through a resistor (pull down).

5. Reference Documents

User's Manual: Hardware

RX630 Group User's Manual: Hardware Rev.1.20 (R01UH0040EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RX630 Group Application Note Reducing Power Consumption

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		Page	**Summary**
1.00	Apr. 1, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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